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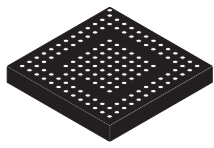
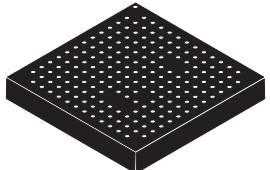


Power Management Integrated Circuit (PMIC) for i.MX35/51

The MC13892 is a Power Management Integrated Circuit (PMIC) designed specifically for use with the Freescale i.MX35 and i.MX51 families. It is also compatible with the i.MX27, i.MX31, and i.MX37 application processors targeting netbooks, ebooks, smart mobile devices, smart phones, personal media players, and portable navigation devices.

Features

- Battery charger system for wall charging and USB charging
- 10-bit ADC for monitoring battery and other inputs, plus a coulomb counter support module
- Four adjustable output buck regulators for direct supply of the processor core and memory
- 12 adjustable output LDOs with internal and external pass devices
- Boost regulator for supplying RGB LEDs
- Serial backlight drivers for displays and keypad, plus RGB LED drivers
- Power control logic with processor interface and event detection
- Real time clock and crystal oscillator circuitry, with coin cell backup and support for external secure real time clock on a companion system processor IC
- Touch screen interface
- SPI/I²C bus interface for control and register access

13892	
POWER MANAGEMENT	
 VK SUFFIX 98ASA10820D 139-PIN 7X7MM BGA	 VL SUFFIX 98ASA10849D 186-PIN 12X12MM BGA
ORDERING INFORMATION	
See Device Variation Table on Page 2.	

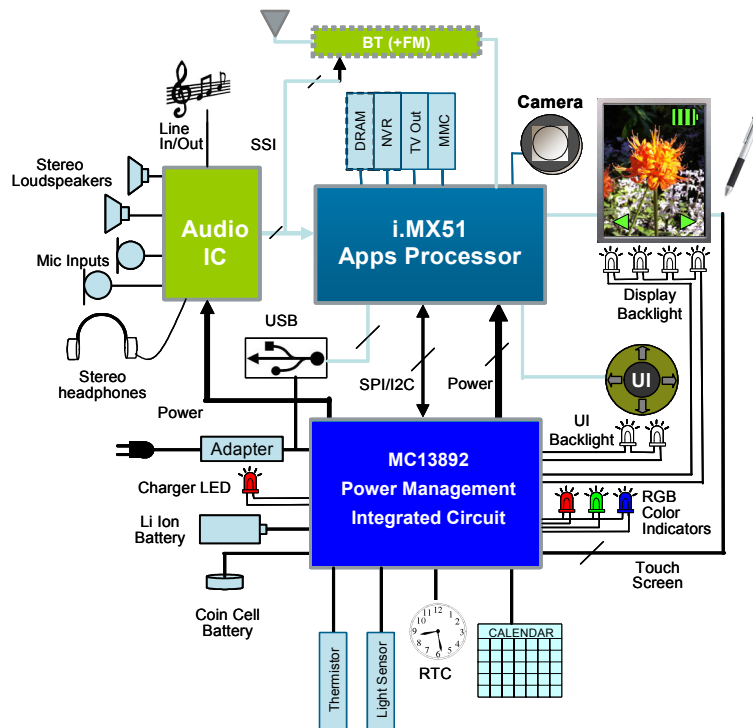


Figure 1. MC13892 Typical Operating Circuit

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DEVICE VARIATIONS

Table 1. MC13892 Device Variations

Part Number ⁽¹⁾	Notes	Package	Temperature Range (T _A)	Pin Map	Description		
MC13892CJVK MC13892AJVK	(2) (3)	139-PIN 7x7 mm BGA	-40 to +85 °C	Figure 3	Global Reset Function Default ON		
MC13892DJVK MC13892BJVK	(2) (4) (3)				Global Reset Function Default OFF		
MC13892VK MC13892JVK	(3) (3)				No Global Reset Function		
MC13892CJVL MC13892AJVL	(2) (3)				186-PIN 12x12 mm BGA	Figure 4	Global Reset Function Default ON
MC13892DJVL MC13892BJVL	(2) (4) (3)						Global Reset Function Default OFF
MC13892VL MC13892JVL	(3) (3)						No Global Reset Function

Notes

1. For Tape and Reel product, add an "R2" suffix to the part number.
2. Recommended for all new designs
3. Not recommended for new designs
4. Backward compatible replacement part for MC13892VK, MC13892JVK, MC13892VL, MC13892JVL, MC13892BJVK, and MC13892BJVL

INTERNAL BLOCK DIAGRAM

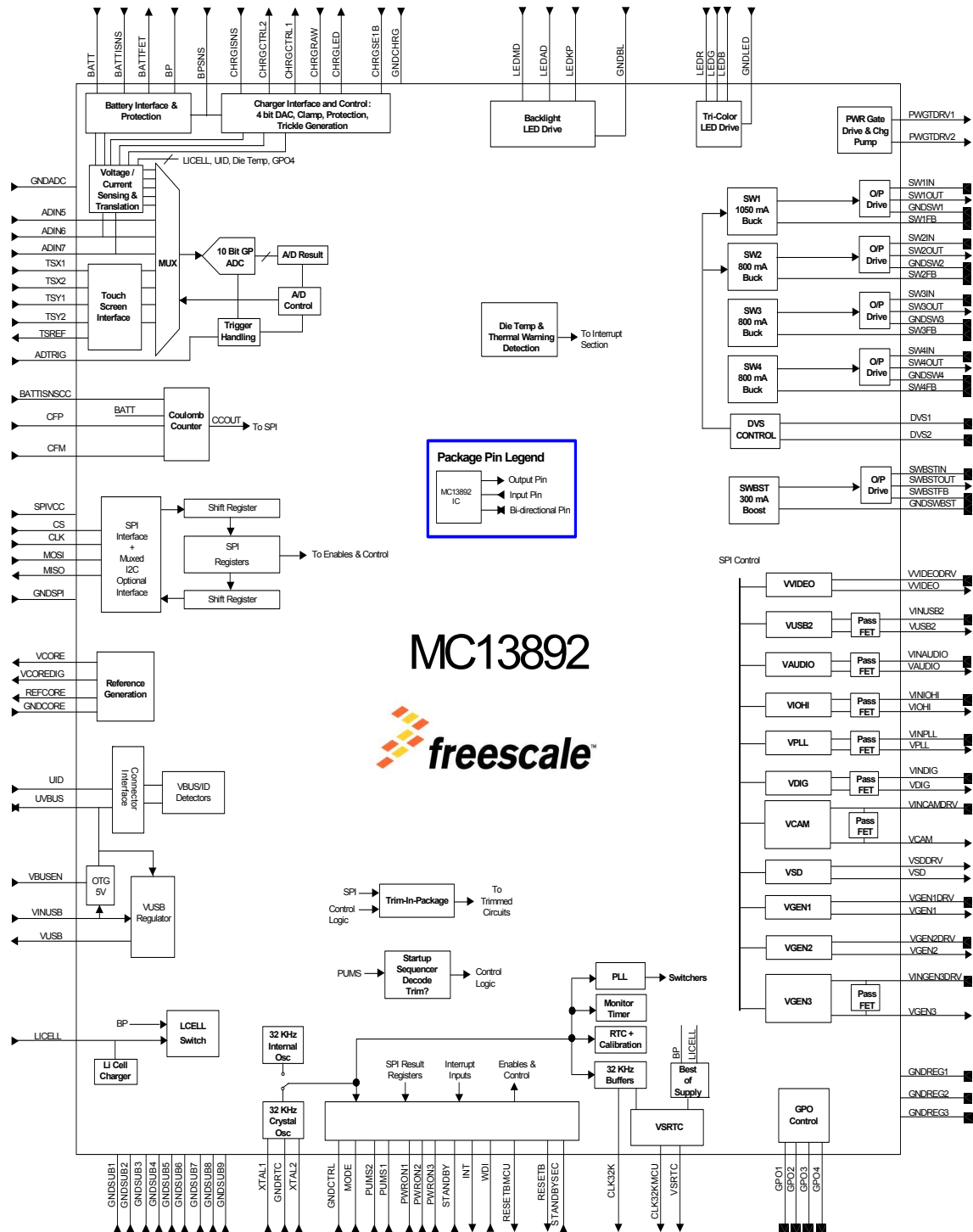


Figure 2. MC13892 Simplified Internal Block Diagram

PIN CONNECTIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	VUSE2	VUSE2	VINUSE2	SWBSTIN	GND5BST	GND6L	NC	MODE	VCORE	BATT	CHRGRAW	CHRGCTRL2	CHRGCTRL2	
B	VUSE2	GPO1	DVS2	SWBSTOUT	LEDB	LEDKP	LEDR	GNDCORE	VOCOREDIG	BP	CHRGCTRL1	BATTIN5CC	CHRGCTRL2	
C	VINFL	VSDDRV										CHRGINS	BATTINS	
D	USB	VSD		SWBSTFB	LEDMD	DVS1	REFCORE	CHRGSEIB	LICELL	BATTIFET		BPNS	PWRON1	
E	UMBUS	VRL		LEDG	GNDLED	UID	PUMS2	GNDCHRG	CHRGLED	PWRON2	ADTRIG	INT	GND5M1	
F	GND5M3	VBLSEN		SW3FB	LEDAD	GND5UB	GND5UB	GND5UB	GPO3	GPO2	RESETBMCU	RESETB	SW1OUT	
G	SW3OUT	VINUSB		SW4FB	GNDREG2	GND5UB	GND5UB	GND5UB	PUMS1	VDI		GPO4	SW1IN	
H	SW3IN	MISO		GND5P1	GNDREG3	GND5UB	GND5UB	GND5UB	GNDCTRL	SW1FB		STANDBYSEC	SW2IN	
J	SW4IN	MOSI		CLK32KMCU	STANDBY	GNDACC	GNDREG1	PWRON3	TSX1	SW2FB		TSX2	SW2OUT	
K	SW4OUT	SPVCC		PWGTDRV1	CLK32K	VQAM	CFP	CFM	ADIN5	ADIN6		WIDEDRV	GND5M2	
L	GND5M4	CS										TSY2	WIDEO	
M	VGEN6	CLK	VGEN2	VSRRTC	GNDRTC	VINCAMDRV	PWGTDRV2	VDIG	VINDIG	VGENIDRV	ADIN7	TSY1	TSREF	
N	VGEN6	VGEN6	VINGENDRV	VGENZDRV	XTAL2	XTAL1	VINVALID	VALIDO	VOH	VINH	VGEN1	TSREF	TSREF	

	Regulators
	Switchers
	Backlights
	Control Logic
	Charger
	RTC
	Grounds
	USB
	ADC
	SPI/I2C
	No Connect

Figure 3. MC13892VK Pin Connections

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A		VUSB2	VINUSB2	SWBSTOUT	SWBSTIN	GNDSUB	NC	MODE	VCORE	BATT	CHRGRW	CHRCTRL2	CHRGISNS		Regulators
B	VSDDRV	GPO1	GNDSUB	GNDSUB	LEDR	UID	DVS1	REFCORE	GNDCORE	CHRGSE1B	BP	GNDCHRG	BATTISNSCC	BATTISNS	Switchers
C	VSD	DVS2	SWBSTFB	LEDB	LEDG	LEDKP	LEDAD	PUMS2	VCOREDIG	LICELL	BATTFET	BPSNS	GPO3	PUMS1	Backlights
D	VUSB	VPLL	GNDSUB	GNDSUB	GNDSWBST	GNDLED	LEDMD	GNDBL	CHRGCTRL1	CHRGLED	PWRON1	PWRON3	ADTRIG	GPO4	Control Logic
E	UVBUS	GNDREG2	VINPLL	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	PWRON2	GPO2	INT	RESETMCU	Charger
F	SW3OUT	VBUSEN	VINUSB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDCTRL	WDI	RESETB	SW1OUT	RTC
G	GNDSW3	GNDSW3	SW3FB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	SW1FB	GNDSW1	GNDSW1	Grounds
H	SW3IN	SW3IN	GNDSUB		GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB		GNDSUB	SW1IN	SW1IN	USB
J	SW4IN	SW4IN	SW4FB		GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB		SW2FB	SW2IN	SW2IN	ADC
K	GNDSW4	GNDSW4	SPIVCC	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB		GNDSUB		VVIDEODRV	GNDSW2	GNDSW2	SPI/I2C
L	SW4OUT	CS	GNDSPI	GNDSUB	GNDSUB	GNDSUB	VCAM	VINAUDIO	VDIG	GNDSUB	TSY2	STANDBYSEC	VVIDEO	SW2OUT	No Connect
M	CLK	VINGEN3DRV	CLK32KMCU	CLK32K	VSRTC	STANDBY	VINCAMDRV	CFP	CFM	VGEN1DRV	VGEN1	TSX1	TSX2	TSY1	
N	VGEN3	MOSI	VGEN2	GNDREG3	XTAL2	XTAL1	VAUDIO	PWGTDRV2	VIOHI	VINIOHI	GNDADC	ADIN5	ADIN7	TSREF	
P		MISO	PWGTDRV1	VGEN2DRV	GNDSUB	GNDRTC	GNDSUB	GNDSUB	GNDSUB	GNDSUB	VINDIG	GNDREG1	ADIN6		

Figure 4. MC13892VL Pin Connections

Table 2. MC13892 Pin Definitions

A functional description of each pin can be found in the [Functional Description](#).

Pin Number on the 13982VK 7x7 mm	Pin Number on the 13982VL 12x12 mm	Pin Name	Rating (V)	Pin Function	Formal Name	Definition
A1, A2, B1	A2	VUSB2	3.6	Output	USB 2 Supply	Output regulator for USB PHY
A3	A3	VINUSB2	5.5	Power	USB 2 Supply Input	Input regulator VUSB2
A4	A5	SWBSTIN	5.5	Power	Switcher Boost Power Input	Switcher BST input
A5	D5	GNDSWBST	–	Ground	Switcher Boost Ground	Ground for switcher BST
A6	D8	GNDBL	–	Ground	Backlight LED Ground	Ground for serial LED drive
A7	A7	NC	–	–	No Connect	Do not connect
A8	A8	MODE	9.0	Input	Mode Configuration	USB LBP mode, normal mode, test mode selection, & anti-fuse bias
A9	A9	VCORE	3.6	Output	Core Supply	Regulated supply output for the IC analog core circuitry
A10	A10	BATT	5.5	Input	Battery Connection	1. Battery positive pin 2. Battery current sensing point 2 3. Battery supply voltage sense
A11	A11	CHRGRAW	20	I/O	Charger Input	1. Charger input 2. Output to battery supplied accessories
A12, A13, B13	A12	CHRGCTRL2	5.5	Output	Charger Control 2	Driver output for charger path FETs M2
B2	B2	GPO1	3.6	Output	General Purpose Output 1	General purpose output 1
B3	C2	DVS2	3.6	Input	Dynamic Voltage Scaling Control 2	Switcher 2 DVS input pin
B4	A4	SWBSTOUT	7.5	Power	Switcher Boost Output	Switcher BST BP supply
B5	C4	LEDB	7.5	Input	LED Driver	General purpose LED current sink driver Blue
B6	C6	LEDKP	28	Input	LED Driver	Keypad lighting LED current sink driver
B7	B5	LEDR	7.5	Input	LED Driver	General purpose LED current sink driver Red
B8	B9	GNDCORE	–	Ground	Core Ground	Ground for the IC core circuitry
B9	C9	VCOREDIG	1.5	Output	Digital Core Supply	Regulated supply output for the IC digital core circuitry
B10	B11	BP	5.5	Power	Battery Plus	1. Application supply point 2. Input supply to the IC core circuitry 3. Application supply voltage sense
B11	D9	CHRGCTRL1	20	Output	Charger Control 1	Driver output for charger path FETs M1
B12	B13	BATTISNSCC	4.8	Input	Battery Current Sense	Accumulated current counter current sensing point
C1	E3	VINPLL	5.5	Power	PLL Supply Input	Input regulator processor PLL
C2	B1	VSDDRV	5.5	Output	VSD Driver	Drive output regulated SD card
C12	A13	CHRGISNS	4.8	Input	Charger Current Sense	Charge current sensing point 1
C13	B14	BATTISNS	4.8	Input	Battery Current Sense	Battery current sensing point 1

Table 2. MC13892 Pin Definitions (continued)

A functional description of each pin can be found in the [Functional Description](#).

Pin Number on the 13982VK 7x7 mm	Pin Number on the 13982VL 12x12 mm	Pin Name	Rating (V)	Pin Function	Formal Name	Definition
D1	D1	VUSB	3.6	Output	USB Supply	USB transceiver regulator output
D2	C1	VSD	3.6	Output	SD Card Supply	Output regulator SD card
D4	C3	SWBSTFB	3.6	Input	Switcher Boost Feedback	Switcher BST feedback
D5	D7	LEDMD	28	Input	LED Driver	Main display backlight LED current sink driver
D6	B7	DVS1	3.6	Input	Dynamic Voltage Scaling Control 1	Switcher 1DVS input pin
D7	B8	REFCORE	3.6	Output	Core Reference	Main bandgap reference
D8	B10	CHRGSE1B	3.6	Input	Charger Select	Charger forced SE1 detection input
D9	C10	LICELL	3.6	I/O	Coin Cell Connection	1. Coin cell supply input 2. Coin cell charger output
D10	C11	BATTFET	4.8	Output	Battery FET Connection	Driver output for battery path FET M3
D12	C12	BPSNS	4.8	Input	Battery Plus Sense	1. BP sense point 2. Charge current sensing point 2
D13	D11	PWRON1	3.6	Input	Power On 1	Power on/off button connection 1
E1	E1	UVBUS	20	I/O	USB Bus	1. USB transceiver cable interface 2. VBUS & OTG supply output
E2	D2	VPLL	3.6	Output	Voltage Supply for PLL	Output regulator processor PLL
E4	C5	LEDG	7.5	Input	PWM Driver for Green LED	General purpose LED current sink driver Green
E5	D6	GNDLED	–	Ground	LED Ground	Ground for LED drivers
E6	B6	UID	5.5	Input	USB ID	USB OTG transceiver cable ID
E7	C8	PUMS2	3.6	Input	Power Up Mode Select 2	Power up mode supply setting 2
E8	B12	GNDCHRG	–	Ground	Charger Ground	Ground for charger interface
E9	D10	CHRGLED	20	Output	Charger LED	Trickle LED driver output 1
E10	E11	PWRON2	3.6	Input	Power On 2	Power on/off button connection 2
E11	D13	ADTRIG	3.6	Input	ADC Trigger	ADC trigger input
E12	E13	INT	3.6	Output	Interrupt Signal	Interrupt to processor
E13	G13, G14	GNDSW1	–	Ground	Switcher 1 Ground	Ground for switcher 1
F1	G1, G2	GNDSW3	–	Ground	Switcher 3 Ground	Ground for switcher 3
F2	F2	VBUSEN	3.6	Input	VBUS Enable	External VBUS enable pin for OTG supply
F4	G3	SW3FB	3.6	Input	Switcher 3 Feedback	Switcher 3 feedback
F5	C7	LEDAD	28	Input	Auxiliary Display LED	Auxiliary display backlight LED sinking current driver
F6	A6, B3, B4, D3, D4, E4, E5, E6	GNDSUB1	–	Ground	Ground 1	Non critical signal ground and thermal heat sink

Table 2. MC13892 Pin Definitions (continued)

A functional description of each pin can be found in the [Functional Description](#).

Pin Number on the 13982VK 7x7 mm	Pin Number on the 13982VL 12x12 mm	Pin Name	Rating (V)	Pin Function	Formal Name	Definition
F7	E7, E8, E9, E10, F4, F5, F6	GNDSUB2	–	Ground	Ground 2	Non critical signal ground and thermal heat sink
F8	F7, F8, F9, F10, G4, G5, G6, G7, G8	GNDSUB3	–	Ground	Ground 3	Non critical signal ground and thermal heat sink
F9	C13	GPO3	–	Output	General Purpose Output 3	General purpose output 3
F10	E12	GPO2	3.6	Output	General Purpose Output 2	General purpose output 2
F11	E14	RESETBMCU	3.6	Output	MCU Reset	Reset output for processor
F12	F13	RESETB	3.6	Output	Peripheral Reset	Reset output for peripherals
F13	F14	SW1OUT	5.5	Output	Switcher 1 Output	Switcher 1 output
G1	F1	SW3OUT	5.5	Output	Switcher 3 Output	Switcher 3 output
G2	F3	VINUSB	7.5	Input	VUSB Supply Input	Input option for UVUSB; tie to SWBST at top level
G4	J3	SW4FB	3.6	Input	Switcher 4 Feedback	Switcher 4 feedback
G5	E2	GNDREG2	–	Ground	Regulator 2 Ground	Ground for regulators 2
G6	G9, G10, G11, H3, H5, H6, H7, H8	GNDSUB4	–	Ground	Ground 4	Non critical signal ground and thermal heat sink
G7	H9, H10, H12, J5, J6, J7	GNDSUB5	–	Ground	Ground 5	Non critical signal ground and thermal heat sink
G8	J8, J9, J10, K4, K5, K6, K7	GNDSUB6	–	Ground	Ground 6	Non critical signal ground and thermal heat sink
G9	C14	PUMS1	3.6	Input	Power Up Mode Select 1	Power up mode supply setting 1
G10	F12	WDI	3.6	Input	Watchdog Input	Watchdog input
G12	D14	GPO4	3.6	Output	General Purpose Output 4	General purpose output 4
G13	H13, H14	SW1IN	5.5	Input	Switcher 1 Input	Input voltage for switcher 1
H1	H1, H2	SW3IN	5.5	Power	Switcher 3 Input	Switcher 3 input
H2	P2	MISO	3.6	I/O	Master In Slave Out	Primary SPI read output
H4	L3	GNDSPI	–	Ground	SPI Ground	Ground for SPI interface
H5	N4	GNDREG3	–	Ground	Regulator 3 Ground	Ground for regulators 3
H6	K8, K10, L4, L5, L6, L10	GNDSUB7	–	Ground	Ground 7	Non critical signal ground and thermal heat sink
H7	P5, P7, P8, P9, P10	GNDSUB8	–	Ground	Ground 8	Non critical signal ground and thermal heat sink
H8	–	GNDSUB9	–	Ground	Ground 9	Non critical signal ground and thermal heat sink
H9	F11	GNDCTRL	–	Ground	Logic Control Ground	Ground for control logic

Table 2. MC13892 Pin Definitions (continued)

A functional description of each pin can be found in the [Functional Description](#).

Pin Number on the 13982VK 7x7 mm	Pin Number on the 13982VL 12x12 mm	Pin Name	Rating (V)	Pin Function	Formal Name	Definition
H10	G12	SW1FB	3.6	Input	Switcher 1 Feedback	Switcher 1 feedback
H12	L12	STANDBYSEC	3.6	Input	Secondary Standby Signal	Standby input signal from peripherals
H13	J13, J14	SW2IN	5.5	Input	Switcher 2 Input	Input voltage for Switcher 2
J1	J1, J2	SW4IN	5.5	Power	Switcher 4 Input	Switcher 4 input
J2	N2	MOSI	3.6	Input	Master Out Slave In	Primary SPI write input
J4	M3	CLK32KMCU	3.6	Output	32 kHz Clock for MCU	32 kHz clock output for processor
J5	M6	STANDBY	3.6	Input	Standby Signal	Standby input signal from processor
J6	N11	GNDADC	–	Ground	ADC Ground	Ground for A to D circuitry
J7	P12	GNDREG1	–	Ground	Regulator 1 Ground	Ground for regulators 1
J8	D12	PWRON3	3.6	Input	Power On 3	Power on/off button connection 3
J9	M12	TSX1	3.6	Input	Touch Screen Interface X1	Touch screen interface X1
J10	J12	SW2FB	3.6	Input	Switcher 2 Feedback	Switcher 2 feedback
J12	M13	TSX2	3.6	Input	Touch Screen Interface X2	Touch screen interface X2
J13	L14	SW2OUT	5.5	Output	Switcher 2 Output	Switcher 2 output
K1	L1	SW4OUT	5.5	Output	Switcher 4 Output	Switcher 4 output
K2	K3	SPIVCC	3.6	Input	Supply Voltage for SPI	Supply for SPI bus and audio bus
K4	P3	PWGTDRV1	4.8	Output	Power Gate Driver 1	Power gate driver 1
K5	M4	CLK32K	3.6	Output	32 kHz Clock	32 kHz clock output for peripherals
K6	L7	VCAM	3.6	Output	Camera Supply	Output regulator camera
K7	M8	CFP	4.8	Passive	Current Filter Positive	Accumulated current filter cap plus pin
K8	M9	CFM	4.8	Passive	Current Filter Negative	Accumulated current filter cap minus pin
K9	N12	ADIN5	4.8	Input	ADC Channel 5 Input	ADC generic input channel 5
K10	P13	ADIN6	4.8	Input	ADC Channel 6 Input	ADC generic input channel 6
K12	K12	VVIDEODRV	5.5	Output	VVIDEO Driver	Drive output regulator VVIDEO
K13	K13, K14	GNDSW2	–	Ground	Switcher 2 Ground	Ground for switcher 2
L1	K1, K2	GNDSW4	–	Ground	Switcher 4 Ground	Ground for switcher 4
L2	L2	CS	3.6	Input	Chip Select	Primary SPI select input
L12	L11	TSY2	3.6	Input	Touch Screen Interface Y2	Touch screen interface Y2
L13	L13	VVIDEO	3.6	Output	Video Supply	Output regulator TV DAC
M1, N1, N2	N1	VGEN3	3.6	Output	General Purpose Regulator 3	Output GEN3 regulator
M2	M1	CLK	3.6	Input	Clock	Primary SPI clock input
M3	N3	VGEN2	3.6	Output	General Purpose Regulator 2	Output GEN2 regulator

Table 2. MC13892 Pin Definitions (continued)

A functional description of each pin can be found in the [Functional Description](#).

Pin Number on the 13982VK 7x7 mm	Pin Number on the 13982VL 12x12 mm	Pin Name	Rating (V)	Pin Function	Formal Name	Definition
M4	M5	VSRTC	3.6	Output	SRTC Supply	Output regulator for SRTC module on processor
M5	P6	GNDRTC	–	Ground	Real Time Clock Ground	Ground for the RTC block
M6	M7	VINCAMDRV	5.5	I/O	Camera Regulator Supply Input and Driver Output	1. Input regulator camera using internal PMOS FET. 2. Drive output regulator for camera voltage using external PNP device.
M7	N8	PWGTDREV2	4.8	Output	Power Gate Driver 2	Power gate driver 2
M8	L9	VDIG	3.6	Output	Digital Supply	Output regulator digital
M9	P11	VINDIG	5.5	Input	VDIG Supply Input	Input regulator digital
M10	M10	VGEN1DRV	5.5	Output	VGEN1 Driver	Drive output GEN1 regulator
M11	N13	ADIN7	4.8	Input	ADC Channel 7 Input	ADC generic input channel 7, group 1
M12	M14	TSY1	3.6	Input	Touch Screen Interface Y1	Touch screen interface Y1
M13, N12, N13	N14	TSREF	3.6	Output	Touch Screen Reference	Touch screen reference
N3	M2	VINGEN3DRV	5.5	Power/Output	VGEN3 Supply Input and Driver Output	1. Input VGEN3 regulator 2. Drive VGEN3 output regulator
N4	P4	VGEN2DRV	5.5	Output	VGEN2 Driver	Drive output GEN2 regulator
N5	N5	XTAL2	2.5	Input	Crystal Connection 2	32.768 kHz oscillator crystal connection 2
N6	N6	XTAL1	2.5	Input	Crystal Connection 1	32.768 kHz oscillator crystal connection 1
N7	L8	VINAUDIO	5.5	Power	Audio Supply Input	Input regulator VAUDIO
N8	N7	VAUDIO	3.6	Output	Audio Supply	Output regulator for audio
N9	N9	VIOHI	3.6	Output	High Voltage IO Supply	Output regulator high voltage IO, efuse
N10	N10	VINIOHI	5.5	Input	High Voltage IO Supply Input	Input regulator high voltage IO
N11	M11	VGEN1	3.6	Output	General Purpose Regulator 1	Input GEN1 regulator

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Charger and USB Input Voltage ⁽⁵⁾	V_{CHRGR}	-0.3 to 20	V
MODE pin Voltage	V_{MODE}	-0.3 to 9.0	V
Main/Aux/Keypad Current Sink Voltage	$V_{\text{LEDMD}},$ $V_{\text{LEDAD}},$ V_{LEDKP}	-0.3 to 28	V
Battery Voltage	V_{BATT}	-0.3 to 4.8	V
Coin Cell Voltage	V_{LICELL}	-0.3 to 3.6	V
ESD Voltage ⁽⁶⁾ Human Body Model - HBM with Mode pin excluded ⁽⁹⁾ Charge Device Model - CDM	V_{ESD}	± 1500 ± 250	V

THERMAL RATINGS

Ambient Operating Temperature Range	T_{A}	-40 to +85	°C
Operating Junction Temperature Range	T_{J}	-40 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

THERMAL RESISTANCE

Peak Package Reflow Temperature During Reflow ^{(7), (8)}	T_{PPRT}	Note 8	°C
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Notes

- USB Input Voltage applies to UVBUS pin only
- ESD testing is performed in accordance with the Human Body Model (HBM) (CZAP = 100 pF, RZAP = 1500 Ω) and the Charge Device Model (CDM), Robotic (CZAP = 4.0 pF).
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxx enter 33xxx)], and review parametrics.
- Mode Pin is not ESD protected.

Table 4. Dissipation Ratings

Rating Parameter	Condition	Symbol	VK Package	VL Package	Unit
Junction to Ambient Natural Convection	Single layer board (1s)	$R_{\theta\text{JA}}$	104	65	°C/W
Junction to Ambient Natural Convection	Four layer board (2s2p)	$R_{\theta\text{JMA}}$	54	42	°C/W
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta\text{JMA}}$	88	55	°C/W
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta\text{JMA}}$	49	38	°C/W
Junction to Board		$R_{\theta\text{JB}}$	32	28	°C/W
Junction to Case		$R_{\theta\text{JC}}$	29	22	°C/W
Junction to Package Top	Natural Convection	θJT	7.0	5.0	°C/W

STATIC ELECTRICAL CHARACTERISTICS

Table 5. Static Electrical Characteristics

Characteristics noted under conditions $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT CONSUMPTION					
RTC Mode All blocks disabled, no main battery attached, coin cell is attached to LICELL ⁽¹⁰⁾ RTC	I_{RTC}	–	3.00	6.00	μA
OFF Mode (All blocks disabled, main battery attached) ⁽¹⁰⁾ MC13892 core and RTC module	I_{OFF}	–	10	30	μA
Power Cut Mode (All blocks disabled, no main battery attached, coin cell is attached and valid) ⁽¹⁰⁾ MC13892 core and RTC module	I_{PCUT}	–	3.0	6.0	μA
ON Standby mode - Low-power mode 4 buck regulators in low-power mode, 3 regulators ⁽¹¹⁾	I_{STBY}	–	230	295	μA
ON Mode - Typical use case 4 buck regulators in PWMPS mode, 5 Regulators ⁽¹²⁾	I_{ON}	–	459	1500	μA
I/O CHARACTERISTICS ⁽¹³⁾					
PWRON1, PWRON2, PWRON3, Pull-up ⁽¹⁴⁾ Input Low, 47 kOhm Input High, 1.0 MOhm		0.0 1.0	– –	0.3 VCOREDIG	V
CHRGSE1B, Pull-up ⁽¹⁵⁾ Input Low Input High		0.0 1.0	– –	0.3 VCORE	V
STANDBY, STANDBYSEC, WDI, ADTRIG, Weak Pull-down ^{(16), (17)} Input Low Input High		0.0 1.0	– –	0.3 3.6	V
CLK32K, CMOS Output Low, -100 μA Output High, 100 μA		0.0 SPIVCC -0.2	– –	0.2 SPIVCC	V
CLK32KMCU, CMOS Output Low, -100 μA Output High, 100 μA		0.0 VSRTC - 0.2	– –	0.2 VSRTC	V
RESETB, RESETBMCU, Open Drain ⁽¹⁸⁾ Output Low, -2.0 mA Output High, Open Drain		0.0 0.0	– –	0.4 3.6	V

Notes

10. Valid at 25 °C only.
11. VPLL, VIOHI, VGEN2
12. VPLL, VIOHI, VGEN2, VAUDIO, VVIDEO
13. SPIVCC is typically connected to the output of buck regulator: SW4 and set to 1.800 V
14. Input has internal pull-up to VCOREDIG equivalent to 200 kOhm
15. Input has internal pull-up to VCORE equivalent to 100 kOhm
16. SPIVCC needs to remain enabled for proper detection of WDI High to avoid involuntary shutdown
17. A weak pull-down represents a nominal internal pull down of 100 nA, unless otherwise noted
18. RESETB & RESETBMCU have open drain outputs, external pull-ups are required

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
I/O CHARACTERISTICS (CONTINUED) ⁽¹⁹⁾					
VSRTC, Voltage Output		1.1	–	1.3	V
DVS1, DVS2, Weak Pull-down ⁽²⁰⁾					V
Input Low		0.0	–	0.3* SPIVCC	
Input High		0.7* SPIVCC	–	3.1	
GPO1, CMOS					V
Output Low, -400 μA		0.0	–	0.2	
Output High, 400 μA		VCORE- 0.2	–	VCORE	
To VCORE		200	–	500	Ohm
GPO2, GPO3, GPO4, CMOS					V
Output Low, -100 μA		0.0	–	0.2	
Output High, 100 μA		VIOHI - 0.2	–	VIOHI	
GPO4, Analog Input		0.0	–	VCORE+0.3	V
CS, CLK, MOSI, VBUSEN, Weak Pull-down on CS and VBUSEN ⁽²⁰⁾					V
Input Low		0.0	–	0.3* SPIVCC	
Input High		0.7* SPIVCC	–	SPIVCC+0.3	
CS, MOSI (at Booting for SPI / I ² C decoding), Weak Pull-down on CS ⁽²¹⁾					V
Input Low		0.0	–	0.3 * VCORE	
Input High		0.7 * VCORE	–	VCORE	
MISO, INT, CMOS ⁽²²⁾					V
Output Low, -100 μA		0.0	–	0.2	
Output High, 100 μA		SPIVCC -0.2	–	SPIVCC	
PUMS1, PUMS2 ⁽²²⁾					V
PUMSxS = 00		0.0	–	0.3	
PUMSxS = 01, Load < 10 pF		Open	–	Open	
PUMSxS = 10		1.3	–	2.0	
PUMSxS = 11		2.5	–	3.1	
MODE ⁽²³⁾					V
Input Low		0.0	–	0.4	
Input Med		1.1	–	1.7	
Input High		VCORE	–	9.0	

Notes

19. SPIVCC is typically connected to the output of buck regulator: SW4 and set to 1.800 V
20. A weak pull-down represents a nominal internal pull down of 100 nA unless otherwise noted
21. The weak pull-down on CS is disabled if a VIH is detected at startup to avoid extra consumption in I²C mode
22. The output drive strength is programmable
23. Input state is latched in first phase of cold start, refer to [Power Control System](#) for description of PUMS configuration
24. Input state is not latched

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
32 KHZ CRYSTAL OSCILLATOR					
Operating Voltage Oscillator and RTC Block from BP	V_{XTAL}	1.2	–	4.65	V
Coincell Disconnect Threshold At LICELL	V_{LCD}	1.8	–	2.0	V
Output Low CLK32K, CLK32KMCU Output sink 100 μA	V_{CLKLO}	0.0	–	0.2	V
Output High CLK32K Output source 100 μA CLK32KMCU Output source 100 μA	V_{CLKHI} $V_{CLKMCUHI}$	$\text{SPIV}_{CC}-0.2$ $\text{VSRTC}-0.2$	– –	SPIV_{CC} VSRTC	V
VSRTC GENERAL					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} Valid Coin Cell range Or valid BP	V_{LICELL} V_{BP}	1.8 UVDET	– –	3.6 4.65	V
Operating Current Load Range I_{LMIN} to I_{LMAX}	I_{SRTC}	0.0	–	50	μA
Bypass Capacitor Value	C_{SRTC}	–	1.0	–	μF
VSRTC ACTIVE MODE – DC					
Output Voltage V_{OUT} $V_{INMIN} < V_{IN} < V_{INMAX}$, $I_{LMIN} < I_L < I_{LMAX}$	V_{SRTC}	1.15	1.20	1.25	V
CLK AND MISO					
Input Low CS, MOSI, CLK	V_{INCSLO} $V_{INMOSILO}$ $V_{INCLKLO}$	0.0	–	$0.3 * \text{SPIV}_{CC}$	V
Input High CS, MOSI, CLK	V_{INCSHI} $V_{INMOSIHI}$ $V_{INCLKHI}$	$0.7 * \text{SPIV}_{CC}$	–	$\text{SPIV}_{CC} + 0.3$	V
Output Low MISO, INT Output sink 100 μA	$V_{OMISOLO}$ V_{OINTLO}	0.0	–	0.2	V
Output High MISO, INT Output source 100 μA	$V_{OMISOHI}$ V_{OINTHI}	$\text{SPIV}_{CC}-0.2$	–	SPIV_{CC}	V
SPIVCC Operating Range	SPIV_{CC}	1.75	–	3.1	V

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BUCK REGULATORS					
Operating Input Voltage PWM operation, $0 < I_L < I_{MAX}$ PFM operation, $0 < I_L < I_{MAX}$ Extended PWM or PFM operation ⁽²⁵⁾	V_{SWIN}	3.0 2.8 UVDET	– – –	4.65 4.65 4.65	V
Output Voltage Range Switcher 1 Switchers 2, 3, and 4	V_{SW1}	0.6 0.6	– –	1.375 1.850	V
Output Accuracy PWM mode including ripple, load regulation, and transients ⁽²⁶⁾ PFM Mode, including ripple, load regulation, and transients	V_{SWLOPP} $V_{SWLIPPI}$	Nom-50 Nom-50	Nom Nom	Nom+50 Nom+50	mV
Maximum Continuous Load Current, I_{MAX} , $V_{INMIN} < BP < 4.65\text{ V}$ SW1 in PWM mode (SWILIMB = 0, no max current limit) SW1 in PWM Mode (SWILIMB = 1, no max current limit) ⁽²⁷⁾ SW2, SW3, SW4 in PWM mode (SWILIMB = 0, no max current limit) SW2, SW3, SW4 in PWM mode (SWILIMB = 1, no max current limit) ⁽²⁷⁾ SW1, SW2, SW3, SW4 in PFM mode	I_{SW1} $I_{SW2,3,4}$ $I_{SW2,3,4}$ $I_{SW1, 2, 3, 4}$	800 1050 800 800 –	– – – – 50	– – – – –	mA
Maximum Peak Load Current, I_{PEAK} , $BP \leq 4.2\text{ V}$, SW1 in PWM Mode (SWILIMB = 1, no max current limit) ⁽²⁷⁾ SW4 in PWM Mode (SWILIMB = 1, no max current limit) ⁽²⁷⁾	I_{SW1} I_{SW4}	1250 1000	– –	– –	mA

Notes

25. In the extended operating range the performance may be degraded
26. Transient loading for load steps of $I_{Lmax}/2$
27. In this mode, current limit protection is disabled for SW1 - SW4 by setting SWILIMB = 1. Therefore, the load on SW1-4 should not exceed the conditions specified in the table above. Application needs to provide current limit protection circuitry either in battery or as pre-regulated supply to BP.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BUCK REGULATORS (CONTINUED)					
Automatic Mode Change Threshold, Switchover between PFM and PWM modes	AMC_{TH}	–	50	–	mA
Efficiency					η
PFM, 0.9 V, 1.0 mA		–	75	–	
PFM, 01.8 V, 1.0 mA		–	85	–	
PWM Pulse Skipping, 1.25 V, 50 mA		–	78	–	
PWM Pulse Skipping, 1.8 V, 50 mA		–	82	–	
PWM, 1.25 V, 500 mA		–	78	–	
PWM, 1.8 V, 500 mA		–	82	–	
External Components, Used as a condition for all other parameters					
Inductor for SW2, SW3, SW4 ⁽²⁸⁾	L_{SW234}	-20%	2.2	+20%	μH
Inductor for SW1 ⁽²⁸⁾	L_{SW1}	-30%	1.5	+30%	μH
Inductor Resistance	R_{SW}	–	–	0.16	Ω
Bypass Capacitor for SW2, SW3, SW4 ⁽²⁹⁾	C_{OSW234}	-35%	10	+35%	μF
Bypass Capacitor for SW1 ⁽³⁰⁾	C_{OSW1}	-35%	2x22	+35%	μF
Bypass Capacitor ESR	ESR_{SW}	5.0	–	50	$\text{m}\Omega$
Input Capacitor ⁽³¹⁾		1.0	4.7	–	μF

SWBST

Average Output Voltage ⁽³²⁾ $3.0\text{ V} < V_{\text{IN}} < 4.65\text{ (1)}, 0 < \text{IL} < \text{IL}_{\text{MAX}}\text{ (33)}$	V_{BST}	Nom-5%	5.0	Nom+5%	V
Output Ripple $3.0\text{ V} < V_{\text{IN}} < 4.65, 0 < \text{IL} < \text{IL}_{\text{MAX}}$, Excluding reverse recovery of Schottky diode	V_{BSTPP}	–	–	120	mVpp
Average Load Regulation $V_{\text{IN}} = 3.6\text{ V}, 0 < \text{IL} < \text{IL}_{\text{MAX}}$	V_{BSTLOR}	–	–	0.5	mV/mA
Average Line Regulation $3.0\text{ V} < V_{\text{IN}} < 4.65\text{ V}, \text{IL} = \text{IL}_{\text{MAX}}$	V_{BSTLIR}	–	–	50	mV

Notes

28. Preferred device TDK VLS252012 series at 2.5x2.0 mm footprint and 1.2 mm max height
29. Preferably 0603 style 6.3 V rated X5R/X7R type at 35% total make tolerance, temperature spread and DC bias derating such as TDK C1608X5R0J106M
30. Preferably 0805 style 6.3 V rated X5R/X7R type at 35% total make tolerance, temperature spread and DC bias derating such as TDK C2012X5R0J226M
31. Preferably 0603 style 6.3 V rated X5R/X7R type at 35% total make tolerance, temperature spread and DC bias derating such as TDK C1608X5R0J475
32. Output voltage when configured to supply VBUS in OTG mode can be as high as 5.75 V
33. V_{in} is the low side of the inductor that is connected to BP.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SWBST (CONTINUED)					
Maximum Continuous Load Current I_{L_MAX} $3.0\text{ V} < V_{IN} < 4.65, V_{OUT} = 5.0\text{ V}$	I_{BST}	300	–	–	mA
Start-up Overshoot $I_L = 0\text{ mA}$	V_{BSTOS}	–	–	500	mV
Efficiency, $I_L = I_{L_MAX}$	$SWBST_{EFF}$	–	80	–	%
External Components - Used as a condition for all other parameters					
Inductor ⁽³⁴⁾	L_{BST}	-20%	2.2	+20%	μH
Inductor Resistance	R_{W_BST}	–	–	0.2	Ω
Inductor saturation current at 30% loss in inductance value	I_{L_SAT}	1.0	–	–	A
Bypass Capacitor ⁽³⁵⁾	C_{O_BST}	-60%	10	+35%	μF
Bypass Capacitor ESR at resonance	ESR_{BST}	1.0	–	10	m Ω
Input Capacitor	C_{BSTD}	1.0	4.7	–	μF
Diode current capability	I_{BSTDPK}	850	–	–	mAdc
Diode current capability	I_{BSTDPK}	1500	–	–	mApk
NMOS Off Leakage, $SWBSTIN = 4.5\text{ V}, SWBSTEN = 0$	I_{BSTIK}	–	1.0	5.0	μA

VVIDEO

Operating Input Voltage Range V_{INMIN} to V_{INMAX}	$V_{INVIDEO}$	$V_{NOM}+0.25$	–	4.65	V
Operating Current Load Range I_{L_MIN} to I_{L_MAX} (Not exceeding PNP max power)	I_{VIDEO}	0.0	–	350	mA
Minimum Bypass Capacitor Value Used as a condition for all other parameters	C_{O_VIDEO}	1.1	2.2	–	μF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{VIDEO}	20	–	100	m Ω

VVIDEO ACTIVE MODE DC

Output Voltage V_{OUT} $V_{INMIN} < V_{IN} < V_{INMAX}, I_{L_MIN} < I_L < I_{L_MAX}$	ΔV_{VIDEO}	$V_{NOM} - 3\%$	V_{NOM}	$V_{NOM} + 3\%$	V
Load Regulation $1.0\text{ mA} < I_L < I_{L_MAX}, \text{ For any } V_{INMIN} < V_{IN} < V_{INMAX}$	$V_{VIDEOLOPP}$	–	–	0.20	mV/mA
Line Regulation $V_{INMIN} < V_{IN} < V_{INMAX}, \text{ For any } I_{L_MIN} < I_L < I_{L_MAX}$	$V_{VIDEOLIPP}$	–	5.0	8.0	mV
Short-circuit Protection Threshold $V_{INMIN} < V_{IN} < V_{INMAX}, \text{ Short-circuit } V_{OUT} \text{ to GND}$	$I_{VIDEOSHT}$	$I_{L_MAX}+20\%$	–	–	mA

Notes

34. Preferred device TDK VLS252012 series at 2.5x2.0 mm footprint and 1.2 mm max height
35. Applications of SWBST should take into account impact of tolerance and voltage derating on the bypass capacitor at the output level.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VVIDEO LOW-POWER MODE DC - VVIDEOMODE = 1					
Output Voltage V_{OUT} $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, $I_{\text{LMINLP}} < I_{\text{L}} < I_{\text{LMAXLP}}$	$\Delta V_{\text{VIDEOLO}}$	$V_{\text{NOM}} - 3\%$	V_{NOM}	$V_{\text{NOM}} + 3\%$	V
Current Load Range I_{Lminlp} to I_{Lmaxlp}	I_{VIDEOLO}	0.0	–	3.0	mA
VAUDIO					
Operating Input Voltage Range V_{INMIN} to V_{INMAX}	V_{AUDIO}	$V_{\text{NOM}} + 0.25$	–	4.65	V
Operating Current Load Range I_{LMIN} to I_{LMAX}	I_{AUDIO}	0.0	–	150	mA
Minimum Bypass Capacitor Value	C_{OAUDIO}	0.65	2.2	–	μF
Bypass Capacitor ESR 10 kHz -1.0 MHz	$\text{ESR}_{\text{AUDIO}}$	0.0	–	0.1	Ω
VAUDIO ACTIVE MODE DC					
Output Voltage V_{OUT} ($V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$)	V_{AUDIO}	$V_{\text{NOM}} - 3\%$	V_{NOM}	$V_{\text{NOM}} + 3\%$	V
Load Regulation (1.0 mA $< I_{\text{L}} < I_{\text{LMAX}}$, For any $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$)	$V_{\text{AUDIO}}_{\text{LOR}}$	–	–	0.25	mV/mA
Line Regulation $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, For any $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$	$V_{\text{AUDIO}}_{\text{LIR}}$	–	5.0	8.0	mV
Short-circuit Protection Threshold $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, Short-circuit V_{OUT} to GND	$I_{\text{AUDIO}}_{\text{SHT}}$	$I_{\text{LMAX}} + 20\%$	–	–	mA
VPLL AND VDIG					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} VDIG, VPLL all settings, BP biased VPLL, VDIG [1:0] = 00,01 VPLL, VDIG [1:0] = 10, 11, External Switcher	V_{INPLL} , V_{INDIG}	UVDET 1.75 2.15	– SW4 = 1.8 2.2	4.65 4.65 4.65	V
Operating Current Load Range I_{LMIN} to I_{LMAX}	I_{PLL} , I_{DIG}	0.0	–	50	mA
Minimum Bypass Capacitor Value Used as a condition for all other parameters	C_{OPLL} , C_{ODIG}	0.65	2.2	–	μF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{PLL} , ESR_{DIG}	0.0	–	0.1	Ω
VPLL AND VDIG ACTIVE MODE DC					
Output Voltage V_{OUT} $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$	V_{PLL} , V_{DIG}	$V_{\text{NOM}} - 0.05$	V_{NOM}	$V_{\text{NOM}} + 0.05$	V
Load Regulation 1.0 mA $< I_{\text{L}} < I_{\text{LMAX}}$ for any $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$	$V_{\text{PLL}}_{\text{LOR}}$, $V_{\text{DIG}}_{\text{LOR}}$	–	–	0.35	mV/mA
Line Regulation $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$ for any $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$	$V_{\text{PLL}}_{\text{LIR}}$, $V_{\text{DIG}}_{\text{LIR}}$	–	5.0	8.0	mV
VIOHI					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} $V_{\text{NOM}} = 2.775\text{ V}$	V_{IOHI}	$V_{\text{NOM}} + 0.25$	–	4.65	V
Operating Current Load Range I_{LMIN} to I_{LMAX}	I_{IOHI}	0.0	–	100	mA
Minimum Bypass Capacitor Value	C_{OIOHI}	0.65	2.2	–	μF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{IOHI}	0.0	–	100	m Ω

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VIOHI ACTIVE MODE DC					
Output Voltage V_{OUT} ($V_{\text{NOM}} = 2.775$) $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$; $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$	V_{IOH}	$V_{\text{NOM}} - 3\%$	V_{NOM}	$V_{\text{NOM}} + 3\%$	V
Load Regulation $1.0\text{ mA} < I_{\text{L}} < I_{\text{LMAX}}$, for any $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$	V_{IOHLOR}	–	–	0.35	mV/mA
Line Regulation $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, for any $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$	V_{IOHLIR}	–	5.0	8.0	mV
VCAM					
Operating Input Voltage Range V_{INMIN} to V_{INMAX}	V_{INCAM}	$V_{\text{NOM}} + 0.25$	–	4.65	V
Operating Current Load Range I_{LMIN} to I_{LMAX} Internal pass FET External PNP	I_{CAM}	0.0 0.0	– –	65 250	mA
Minimum Bypass Capacitor Value Internal pass device External PNP (not exceeding PNP max power)	C_{OCAM}	0.65 1.1	2.2 2.2	– –	μF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{CAM}	20	–	100	$\text{m}\Omega$
VCAM ACTIVE MODE DC					
Output Voltage V_{OUT} ($V_{\text{NOM}} = 2.775$) $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$; $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$	V_{CAM}	$V_{\text{NOM}} - 3\%$	V_{NOM}	$V_{\text{NOM}} + 3\%$	V
Load Regulation $1.0\text{ mA} < I_{\text{L}} < I_{\text{LMAX}}$, for any $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$	V_{CAMLOR}	–	–	0.25	mV/mA
Line Regulation $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, for any $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$	V_{CAMLIR}	–	5.0	8.0	mV
Short-circuit Protection Threshold $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$; Short-circuit V_{OUT} to GND	I_{CAMSHT}	$I_{\text{LMAX}} + 20\%$	–	–	mA
VCAM LOW-POWER MODE DC					
Output Voltage V_{OUT} $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$; $I_{\text{LMINLP}} < I_{\text{L}} < I_{\text{LMAXLP}}$	V_{CAMLO}	$V_{\text{NOM}} - 3\%$	V_{NOM}	$V_{\text{NOM}} + 3\%$	V
Current Load Range I_{LMINLP} to I_{LMAXLP}	I_{CAMLO}	0.0	–	3.0	mA
VSD					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} VSD[2:0] = 010 to 111 VSD[2:0] = 010 to 111, Extended Operation VSD[2:0] = 000, 001 [000] BP Supplied VSD[2:0] = 000 External Switcher Supplied	V_{INSD}	$V_{\text{NOM}} + 0.25$ UVDET UVDET 2.15	– – – 2.20	4.65 4.65 4.65 4.65	V
Operating Current Load Range I_{LMIN} to I_{LMAX} Not exceeding PNP max power	I_{SD}	0.0	–	250	mA
Minimum Bypass Capacitor Value	C_{OSD}	1.1	2.2	–	μF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{SD}	20	–	100	$\text{m}\Omega$

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VSD ACTIVE MODE DC					
Output Voltage V_{OUT} $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$	V_{SD}	$V_{\text{NOM}} - 3\%$	V_{NOM}	$V_{\text{NOM}} + 3\%$	V
Load Regulation $1.0\text{ mA} < I_{\text{L}} < I_{\text{LMAX}}$, for any $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$	V_{SDLOR}	–	–	0.25	mV/mA
Line Regulation $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, for any $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$	V_{SDLIR}	–	5.0	8.0	mV
Short-circuit Protection Threshold $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, Short-circuit V_{OUT} to GND	I_{SDSHT}	$I_{\text{LMAX}} + 20\%$	–	–	mA

VSD LOW-POWER MODE DC - VSDMODE = 1

Output Voltage V_{OUT} $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, $I_{\text{LMINLP}} < I_{\text{L}} < I_{\text{LMAXLP}}$	V_{SDLO}	$V_{\text{NOM}} - 3\%$	V_{NOM}	$V_{\text{NOM}} + 3\%$	V
Current Load Range I_{LMINLP} to I_{LMAXLP}	I_{SDLO}	0.0	–	3.0	mA

VUSB GENERAL

Operating Input Voltage Range V_{INMIN} to V_{INMAX} Supplied by VBUS Supplied by SWBST	V_{INUSB}	4.4 –	5.0 –	5.25 5.75	V
Operating Current Load Range I_{LMIN} to I_{LMAX}	I_{USB}	0.0	–	100	mA
Bypass Capacitor Value Range	C_{OUSB}	0.65	2.2	–	μF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{USB}	0.0	–	0.1	Ω

VUSB ACTIVE MODE DC

Output Voltage V_{OUT} $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$	V_{USB}	$V_{\text{NOM}} - 4\%$	3.3	$V_{\text{NOM}} + 4\%$	V
Load Regulation $0 < I_{\text{L}} < I_{\text{LMAX}}$ from DM/DP for any $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$	V_{USBLOR}	–	–	1.0	mV/mA
Line Regulation $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, for any $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$	V_{USBLIR}	–	–	20	mV
Short-circuit Protection Threshold $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, Short-circuit V_{OUT} to GND	V_{USBSHT}	$I_{\text{LMAX}} + 20\%$	–	–	mA

VUSB2

Operating Input Voltage Range V_{INMIN} to V_{INMAX} Extended operation	V_{INUSB2}	$V_{\text{NOM}} + 0.25$ UVDET	– –	4.65 4.65	V
Operating Current Load Range I_{LMIN} to I_{LMAX}	I_{USB2}	0.0	–	50	mA
Minimum Bypass Capacitor Value Used as a condition for all other parameters	C_{OUSB2}	0.65	2.2	–	μF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{USB2}	0.0	–	0.1	Ω

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
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USB2 ACTIVE MODE DC

Output Voltage V_{OUT} $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$	V_{USB2}	$V_{\text{NOM}} - 3\%$	V_{NOM}	$V_{\text{NOM}} + 3\%$	V
Load Regulation 1.0 mA $< I_{\text{L}} < I_{\text{LMAX}}$, for any $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$	V_{USB2LOR}	–	–	0.35	mV/mA
Line Regulation $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, for any $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$	V_{USB2LIR}	–	5.0	8.0	mV

UVBUS

Operating Input Voltage Range V_{INMIN} to V_{INMAX} V_{INUSB} supplied by SWBST	V_{INUVBUS}	4.75	5.0	5.25	V
Operating Current Load Range I_{LMIN} to I_{LMAX}	I_{UVBUS}	0.0	–	100	mA
Minimum Bypass Capacitor Value	C_{OUVBUS}	(36)	(36)	6.5 (37)	μF
Bypass Capacitor ESR 10 kHz -1.0 MHz	V_{INUVBUS}	(36)	(36)	(37)	Ω

UVBUS ACTIVE MODE DC

Output Voltage V_{out} $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$	V_{UVBUS}	4.4	5.0	5.25	V
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VGEN1

Operating Input Voltage Range V_{INMIN} to V_{INMAX} All settings, BP biased VGEN1=00,01, External switcher supplied	V_{INGEN1}	$UVDET < V_{\text{NOM}} + 0.25$ 2.15	– 2.2	4.65 4.65	V
Operating Current Load Range I_{LMIN} to I_{LMAX} (not exceeding PNP max power)	I_{GEN1}	0.0	–	200	mA
Extended input voltage range (BP biased, performance may be out of specification for output levels VGEN1[1:0] = 10 to 11)		UVDET	–	4.65	V
Minimum Bypass Capacitor Value	C_{OGEN1}	1.1	2.2	+35%	μF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{GEN1}	20	–	100	m Ω

VGEN1 ACTIVE MODE DC

Output Voltage V_{OUT} VGEN1 = 00, 01, $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$ VGEN1 = 10, 11, $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$	V_{GEN1}	$V_{\text{NOM}} - 0.05$ $V_{\text{NOM}} - 3\%$	V_{NOM} V_{NOM}	$V_{\text{NOM}} + 0.05$ $V_{\text{NOM}} + 3\%$	V
Load Regulation 1.0 mA $< I_{\text{L}} < I_{\text{LMAX}}$, for any $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$	V_{GEN1LOR}	–	–	0.25	mV/mA
Line Regulation $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, for any $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$	V_{GEN1LIR}	–	5.0	8.0	mV
Short-circuit Protection Threshold $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, Short-circuit V_{OUT} to GND	V_{GEN1SHT}	$I_{\text{LMAX}} + 20\%$	–	–	mA

Notes

36. Filtering is shared with CHRGRAY (shorted at board level). 2.2 μF is typically included at the CHRGRAY pin.
37. 6.5 μF is the maximum allowable capacitance on VBUS including all tolerances of filtering capacitance on VBUS and CHRGRAY (which are shorted at the board level).

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VGEN1 LOW-POWER MODE DC - VGEN1MODE = 1					
Output Voltage V_{OUT} - $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, $I_{\text{LMINLP}} < I_{\text{L}} < I_{\text{LMAXLP}}$ VGEN1 = 00, 01 VGEN1 = 10, 11	V_{GEN1LO}	$V_{\text{NOM}} - 0.05$ $V_{\text{NOM}} - 3\%$	V_{NOM} V_{NOM}	$V_{\text{NOM}} + 0.05$ $V_{\text{NOM}} + 3\%$	V
Current Load Range I_{LMINLP} to I_{LMAXLP}	I_{GEN1LO}	0.0	–	3.0	mA
VGEN2 GENERAL					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} All settings, BP biased VGEN2=000,001, External switcher supplied	V_{INGEN2}	UVDET < $V_{\text{NOM}} + 0.25$ 2.15	– 2.2	4.65 4.65	V
Operating Current Load Range I_{LMIN} to I_{LMAX} (Not exceeding PNP max power)	I_{GEN2}	0.0	–	350	mA
Minimum Bypass Capacitor Value	C_{OGEN2}	1.1	2.2	+35%	μF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{GEN2}	20	–	100	$\text{m}\Omega$
VGEN2 ACTIVE MODE DC					
Output Voltage V_{OUT} VGEN2 = 000, 001, 010, $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$ VGEN2 = 011, 100, 101, 110, 111, $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$	V_{GEN2}	$V_{\text{NOM}} - 0.05$ $V_{\text{NOM}} - 3\%$	V_{NOM} V_{NOM}	$V_{\text{NOM}} + 0.05$ $V_{\text{NOM}} + 3\%$	V
Load Regulation 1.0 mA < $I_{\text{L}} < I_{\text{LMAX}}$, For any $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$	V_{GEN2LOR}	–	–	0.20	mV/mA
Line Regulation $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, For any $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$	V_{GEN2LIR}	–	5.0	8.0	mV
Short-circuit Protection Threshold $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, Short-circuit V_{OUT} to GND	V_{GEN2SHT}	$I_{\text{LMAX}} + 20\%$	–	–	mA
VGEN2 LOW-POWER MODE DC - VGEN2MODE=1					
Output Voltage V_{OUT} - $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, $I_{\text{LMINLP}} < I_{\text{L}} < I_{\text{LMAXLP}}$ VGEN2 = 000 to 010 VGEN2 = 011 to 111	V_{GEN2LO}	$V_{\text{NOM}} - 0.05$ $V_{\text{NOM}} - 3\%$	V_{NOM} V_{NOM}	$V_{\text{NOM}} + 0.05$ $V_{\text{NOM}} + 3\%$	V
Current Load Range I_{LMINLP} to I_{LMAXLP}	I_{GEN2LO}	0.0	–	3.0	mA
VGEN3 GENERAL					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} VGEN3CONFIG, VGEN3 = 01, 11 VGEN3CONFIG, VGEN3 = 00, 10	V_{INGEN3}	$V_{\text{NOM}} + 0.2$ UVDET	– –	4.65 4.65	V
Operating Current Load Range I_{LMIN} to I_{LMAX} Internal Pass FET External PNP (Not exceeding PNP max power)	I_{GEN3}	0.0 0.0	– –	50 200	mA
Minimum Bypass Capacitor Value Internal pass device External pass device	C_{OGEN3}	0.65 1.1	2.2 2.2	– –	μF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{GEN3}	20	–	100	$\text{m}\Omega$

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VGEN3 ACTIVE MODE DC					
Output Voltage V_{OUT} $V_{\text{GEN2}} = 000, 001, 010, V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}, I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$	V_{GEN3}	$V_{\text{NOM}} - 3\%$	V_{NOM}	$V_{\text{NOM}} + 3\%$	V
Load Regulation $1.0\text{ mA} < I_{\text{L}} < I_{\text{LMAX}}, \text{For any } V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$	V_{GEN3LOR}	–	–	0.40	mV/mA
Line Regulation $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}, \text{For any } I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$	V_{GEN3SHT}	–	5.0	9.0	mV
Short-circuit Protection Threshold $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}, \text{Short circuit } V_{\text{OUT}} \text{ to GND}$	V_{GEN3SHT}	$I_{\text{LMAX}} + 20\%$	–	–	mA
VGEN3 LOW-POWER MODE DC					
Output Voltage V_{OUT} - (Accuracy) $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}, I_{\text{LMINLP}} < I_{\text{L}} < I_{\text{LMAXLP}}$	V_{GEN3LO}	$V_{\text{NOM}} - 3\%$	V_{NOM}	$V_{\text{NOM}} + 3\%$	V
Current Load Range I_{LMINLP} to I_{LMAXLP}	I_{GEN3LO}	0.0	1.0	3.0	mA
CHARGE PATH REGULATOR					
Input Operating Voltage - CHRGRW	V_{INCHRG}	BATT_{MIN}	–	5.6	V
Output Voltage Spread - $V_{\text{CHRG}[2:0]} = 011, 1XX$ Charge current 1.0 mA to 100 mA Charge current 100 mA and above	BP_{SP}	-1.5 -3.0	– –	1.5 1.5	%
Current Limit Tolerance ⁽³⁸⁾ $I_{\text{CHRG}[3:0]} = 0001$ $I_{\text{CHRG}[3:0]} = 0100$ $I_{\text{CHRG}[3:0]} = 0110$ All other settings	ΔI_{LIM}	68 360 500 –	80 400 560 –	92 440 620 15	mA mA mA %
Start-up Overshoot - Unloaded	$\text{BP}_{\text{OS-START}}$	v	–	2.0	%
Configuration Input Capacitance - CHRGRW ⁽³⁹⁾ Load Capacitor - BPSNS ⁽³⁹⁾ Cable length	C_{INCHRG} C_{BP} L_{C}	– 10 –	2.2 – –	– 47 3.0	μF μF m
THERMAL					
Thermal Warning Lower Threshold	T_{WL}	–	100	–	$^{\circ}\text{C}$
Thermal Warning Higher Threshold	T_{WH}	–	120	–	$^{\circ}\text{C}$
Thermal Warning Hysteresis	T_{WHYS}	–	3.0	–	$^{\circ}\text{C}$
Thermal Protection Threshold	T_{PT}	–	140	–	$^{\circ}\text{C}$
BACKLIGHT LED DRIVERS					
Absolute Accuracy - All current settings		–	–	15	%
Matching - At 400 mV, 21 mA		–	–	3.0	%
Leakage - $\text{LEDxDC}[5:0] = 000000$		–	–	1.0	μA
SIGNALING LED DRIVERS					
Absolute Accuracy - All current settings		–	–	15	%
Matching - At 400 mV, 21 mA		–	–	10	%
Leakage - $\text{LEDxDC}[5:0] = 000000$		–	–	1.0	μA

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
ACTIVE MODE DC					
Output Voltage V_{OUT} - ($V_{\text{NOM}} = 2.775$), $V_{\text{INMIN}} < V_{\text{IN}} < V_{\text{INMAX}}$, $I_{\text{LMIN}} < I_{\text{L}} < I_{\text{LMAX}}$		4.4	5.0	5.25	V
ADC					
Converter Core Input Range Single ended voltage readings Differential readings		0.0 -1.2	- -	2.4 1.2	V
Maximum Input Voltage ⁽⁴⁰⁾ Channels ADIN5, ADIN6 and ADIN7		-	-	BP	V
Integral Nonlinearity		-	-	3	LSB
Differential Nonlinearity		-	-	1	LSB
Zero Scale Error (Offset) after auto calibration		-	-	1	LSB
Full Scale Error (Gain) after auto calibration		-	-	5	LSB
Drift Over-temperature - Including scaling		-	-	1	LSB
Source Impedance No bypass capacitor at input Bypass capacitor at input 10 nF		- -	- -	5.0 30	K Ω
TOUCH SCREEN					
Plate Maximum Voltage X, Y ⁽⁴¹⁾		-	-	VCORE	V
Plate Resistance X, Y		100	-	1000	Ω
Resistance Between Plates Settling Time - Contact Position measurement		180 3.0	- -	1200 5.5	Ω μs
TOUCH SCREEN IN STAND ALONE MODE⁽⁴²⁾					
Max Load Current - Active Mode		-	-	20	mA
Output Voltage - $0.0 < I_{\text{L}} < 20\text{ mA}$		-3%	1.20	+3%	V
PSRR - $I_{\text{L}} = 15\text{ mA}$		50	-	-	dB
Bypass Capacitor ESR		0.0	-	0.1	Ω
Bypass Capacitance		0.65	2.2	+35%	μF

Notes

38. Excludes spread and tolerance due to board and 100 mOhm sense resistor tolerances.
39. An additional derating of 35% is allowed.
40. ADIN5, 6 and 7 inputs must not exceed BP voltage.
41. TS[xy][1,2] inputs must not exceed BP or VCORE
42. All characteristics in this table are applicable only for non touch screen operation. This applies to Touch Screen in Standalone mode and below.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 6. Dynamic Electrical Characteristics

Characteristics noted under conditions $3.1\text{ V} \leq \text{BATT} \leq 4.65\text{ V}$, $-40 \leq T_A \leq 85\text{ }^\circ\text{C}$, $\text{GND} = 0\text{ V}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^\circ\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
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32 KHZ CRYSTAL OSCILLATOR

RTC oscillator start-up time Upon application of power	t_{RTCST}	–	–	1.0	Sec
CLK32K Rise and Fall Time - CL = 50 pF CLK32KDRV[1:0] = 00 (default) CLK32KDRV[1:0] = 01 CLK32KDRV[1:0] = 10 CLK32KDRV[1:0] = 11	t_{CLK32KET}	–	22 11 High Z 44	–	ns
CLK32KMCU Rise and Fall Time CL = 12 pF	$t_{\text{CLK32KMCUET}}$	–	22	–	ns
CLK32K and CLK32KMCU Output Duty Cycle Crystal on XTAL1, XTAL2 pins	t_{CLK32KDC} , $t_{\text{CLK32KMCUDC}}$	45	–	55	%

CLK AND MISO

MISO Rise and Fall Time, CL = 50 pF, SPIVCC = 1.8 V SPIDRV [1:0] = 00 (default) SPIDRV [1:0] = 01 SPIDRV [1:0] = 10 SPIDRV [1:0] = 11	t_{MISOET}	–	11 6.0 High Z 22	–	ns
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BUCK REGULATORS

Turn-on Time, Enable to 90% of end value, IL = 0	t_{ONPWM}	–	–	500	μs
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SWBST

Turn-on Time Enable to 90% of V_{OUT} , IL = 0	t_{ONBST}	–	–	2.0	ms
Transient Load Response, IL from 1.0 mA to 100 mA in 1.0 μs steps Maximum transient Amplitude Time to settle 80% of transient	A_{TMAX}	–	–	300 500	mV μs
Transient Load Response, IL from 100 mA to 1.0 mA Maximum transient Amplitude Time to settle 80% of transient	A_{TMAX}	–	–	300 20	mV μs

VVIDEO ACTIVE MODE - AC

PSRR - IL = 75% of I_{LMAX} , 20 Hz to 20 kHz $V_{\text{IN}} = V_{\text{INMIN}} + 100\text{ mV}$ $V_{\text{IN}} = V_{\text{NOM}} + 1.0\text{ V}$	$V_{\text{VIDEO PSSR}}$	35 50	40 60	–	dB
Max Output Noise - $V_{\text{IN}} = V_{\text{INMIN}}$, IL = 75% of I_{LMAX} 100 Hz – 1.0 kHz >1.0 kHz – 10 kHz >10 kHz – 1.0 MHz	$V_{\text{VIDEO ON}}$	–	-114 -124 -129	–	dBV/ $\sqrt{\text{Hz}}$
Turn-on Time Enable to 90% of end value, $V_{\text{IN}} = V_{\text{INMIN}}$, V_{INMAX} , IL = 0	$V_{\text{VIDEO}}t_{\text{ON}}$	–	–	1.0	ms

VVIDEO ACTIVE MODE - AC (CONTINUED)

Turn-off Time Disable to 10% of initial value, $V_{\text{IN}} = V_{\text{INMIN}}$, V_{INMAX} , IL = 0	$V_{\text{VIDEO}}t_{\text{OFF}}$	0.1	–	10	ms
Transient Load Response $V_{\text{IN}} = V_{\text{INMIN}}$, V_{INMAX}	$V_{\text{VIDEO TLOR}}$	–	1.0	2.0	%