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Decade Counter

The MC14017B is a five-stage Johnson decade counter with built-in code converter. High speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

Features

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- Divide-by-N Counting
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4017B
- Triple Diode Protection on All Inputs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P _D	Power Dissipation, per Package (Note 1)	500	mW
T _A	Ambient Temperature Range	-55 to +125	°C
T _{stg}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}.$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



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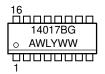


SOIC-16 D SUFFIX CASE 751B

PIN ASSIGNMENT

Q5 [1●	16] V _{DD}
Q1 [2	15	RESET
Q0 [3	14	CLOCK
Q2 [4		CE
Q6 [5	12] C _{out}
Q7 [6	11] Q9
Q3 [7	10] Q4
V _{SS} [8	9] Q8

MARKING DIAGRAM



A = Assembly Location WL, L = Wafer Lot

YY, Y = Year WW, W = Work Week G = Pb-Free Indicator

ORDERING INFORMATION

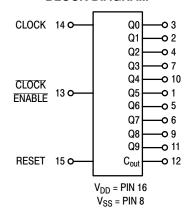
See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

FUNCTIONAL TRUTH TABLE (Positive Logic)

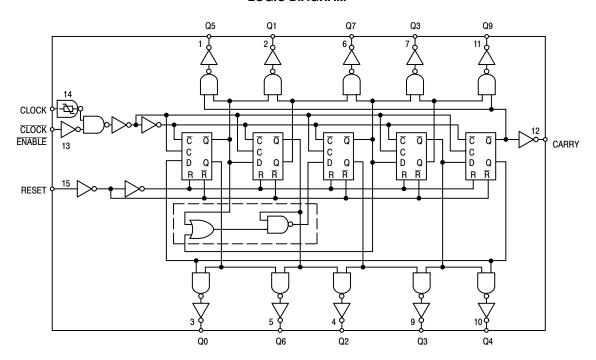
Clock	Clock Enable	Reset	Decode Output=n
0	Х	0	n
X	1	0	n
X	Χ	1	Q0
	0	0	n+1
\	Χ	0	n
X		0	n
1	~	0	n+1

X = Don't Care. If n < 5 Carry = "1", Otherwise = "0".

BLOCK DIAGRAM



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

				-55	5° C		25°C		125	5° C	
Characteristic		Symbol	V _{DD} Vdc	Min	Max	Min	Typ (Note 2)	Max	Min	Max	Unit
Output Voltage "0 V _{in} = V _{DD} or 0	" Level	V _{OL}	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
V _{in} = 0 or V _{DD}	" Level	V _{OH}	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.0 10 15	- - -	4.95 9.95 14.95	- - -	Vdc
Input Voltage "0 $(V_O = 4.5 \text{ or } 0.5 \text{ Vdc})$ $(V_O = 9.0 \text{ or } 1.0 \text{ Vdc})$ $(V_O = 13.5 \text{ or } 1.5 \text{ Vdc})$	" Level	V _{IL}	5.0 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.50 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	Vdc
$(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$ $(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$	" Level	V _{IH}	5.0 10 15	3.5 7.0 11	- - -	3.5 7.0 11	2.75 5.50 8.25	- - -	3.5 7.0 11	- - -	Vdc
Output Drive Current $ (V_{OH} = 2.5 \text{ Vdc}) $ $ (V_{OH} = 4.6 \text{ Vdc}) $ $ (V_{OH} = 9.5 \text{ Vdc}) $ $ (V_{OH} = 13.5 \text{ Vdc}) $	Source	Гон	5.0 5.0 10 15	-3.0 -0.64 -1.6 -4.2	- - -	-2.4 -0.51 -1.3 -3.4	-4.2 -0.88 -2.25 -8.8	- - -	-1.7 -0.36 -0.9 -2.4	- - -	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	Sink	I _{OL}	5.0 10 15	0.64 1.6 4.2	- - -	0.51 1.3 3.4	0.88 2.25 8.8	- - -	0.36 0.9 2.4	- - -	mAdc
Input Current		I _{in}	15	-	±0.1	_	±0.00001	±0.1	_	±1.0	μAdc
Input Capacitance (V _{in} = 0)		C _{in}	-	-	_	-	5.0	7.5	-	-	pF
Quiescent Current (Per Package)		I _{DD}	5.0 10 15		5.0 10 20	- - -	0.005 0.010 0.015	5.0 10 20	- - -	150 300 600	μAdc
Total Supply Current (Notes 3 (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, buffers switching)	,	Ι _Τ	5.0 10 15			$I_T = (0)$.27 μA/kHz) 1 .55 μA/kHz) 1 .83 μA/kHz) 1	f + I _{DD}			μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

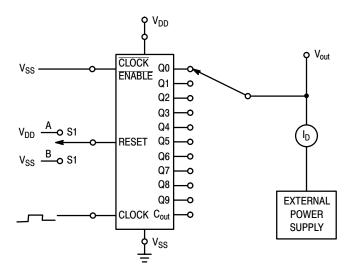
where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.0011.

^{4.} To calculate total supply current at loads other than 50 pF:

SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}, T_A = 25^{\circ}\text{C}$)

Characteristic	Symbol	V _{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) \text{ C}_L + 25 \text{ ns}$ t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) \text{ C}_L + 12.5 \text{ ns}$ t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) \text{ C}_L + 9.5 \text{ ns}$	t _{TLH} , t _{THL}	5.0 10 15	- - -	100 50 40	200 100 80	ns
Propagation Delay Time Reset to Decode Output tplh, tphl = (1.7 ns/pF) C _L + 415 ns tplh, tphl = (0.66 ns/PF) C _L + 197 ns tplh, tphl = (0.5 ns/pF) C _L + 150 ns	t _{PLH} , t _{PHL}	5.0 10 15	- - -	500 230 175	1000 460 350	ns
Propagation Delay Time Clock to C_{out} t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 142 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 100 \text{ ns}$	t _{PLH} , t _{PHL}	5.0 10 15	- - -	400 175 125	800 350 250	ns
Propagation Delay Time Clock to Decode Output tplh, tphl = (1.7 ns/pF) C _L + 415 ns tplh, tphl = (0.66 ns/pF) C _L + 197 ns tplh, tphl = (0.5 ns/pF) C _L + 150 ns	t _{PLH} , t _{PHL}	5.0 10 15	- - -	500 230 175	1000 460 350	ns
Turn–Off Delay Time Reset to C_{out} $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 142 \text{ ns}$ $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 100 \text{ ns}$	t _{PLH}	5.0 10 15	- - -	400 175 125	800 350 250	ns
Clock Pulse Width	t _{w(H)}	5.0 10 15	250 100 75	125 50 35	- - -	ns
Clock Frequency	f _{cl}	5.0 10 15	- - -	5.0 12 16	2.0 5.0 6.7	MHz
Reset Pulse Width	t _{w(H)}	5.0 10 15	500 250 190	250 125 95	- - -	ns
Reset Removal Time	t _{rem}	5.0 10 15	750 275 210	375 135 105	- - -	ns
Clock Input Rise and Fall Time	t _{TLH} , t _{THL}	5.0 10 15		No Limit		-
Clock Enable Setup Time	t _{su}	5.0 10 15	350 150 115	175 75 52	- - -	ns
Clock Enable Removal Time	t _{rem}	5.0 10 15	420 200 140	260 100 70	- - -	ns

^{5.} The formulas given are for the typical characteristics only at 25°C.6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



	Output Sink Drive	Output Source Drive
Decode Outputs	(S1 to A)	Clock to desired outputs (S1 to B)
Carry	Clock to 5 thru 9 (S1 to B)	S1 to A
V _{GS} =	V_{DD}	– V _{DD}
V _{DS} =	V _{out}	$V_{out} - V_{DD}$

Figure 1. Typical Output Source and Output Sink Characteristics Test Circuit

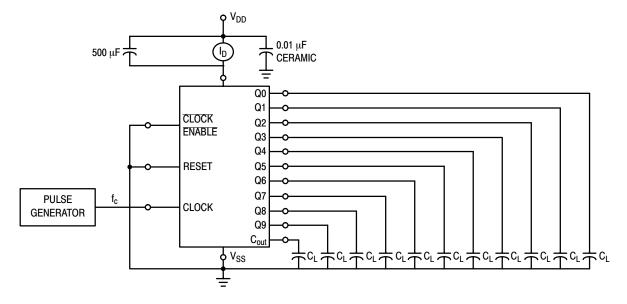


Figure 2. Typical Power Dissipation Test Circuit

APPLICATIONS INFORMATION

Figure 3 shows a technique for extending the number of decoded output states for the MC14017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

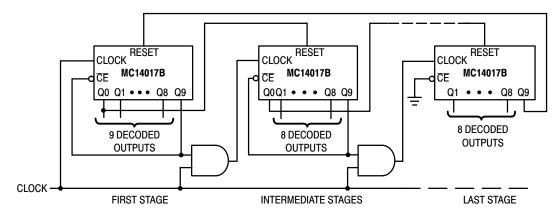


Figure 3. Counter Expansion

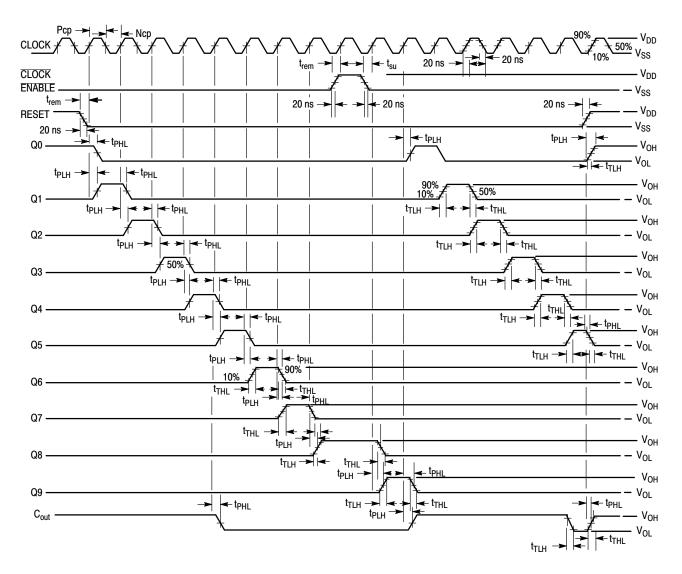


Figure 4. AC Measurement Definition and Functional Waveforms

ORDERING INFORMATION

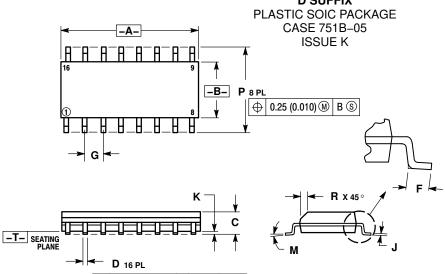
Device	Package	Shipping [†]
MC14017BDG	SOIC-16 (Pb-Free)	48 Units / Rail
NLV14017BDG*	SOIC-16 (Pb-Free)	48 Units / Rail
MC14017BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14017BDR2G*	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP

Capable.

PACKAGE DIMENSIONS

SOIC-16 **D SUFFIX**



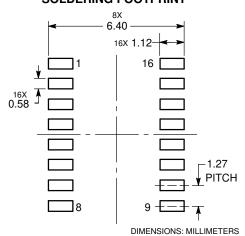
⊕ 0.25 (0.010) M T B S A S

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
 DIMENSIONS A AND B DO NOT INCLUDE MOLD
- PROTRUSION.

 MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	9.80	10.00	0.386	0.393	
В	3.80	4.00	0.150	0.157	
C	1.35	1.75	0.054	0.068	
ם	0.35	0.49	0.014	0.019	
F	0.40	1.25	0.016	0.049	
G	1.27	BSC	0.050) BSC	
7	0.19	0.25	0.008	0.009	
K	0.10	0.25	0.004	0.009	
M	0°	7°	0°	7°	
Р	5.80	6.20	0.229	0.244	
R	0.25	0.50	0.010	0.019	

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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