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## MC14028B

## BCD-To-Decimal Decoder Binary-To-Octal Decoder

The MC14028B decoder is constructed so that an 8421 BCD code on the four inputs provides a decimal (one-of-ten) decoded output, while a 3-bit binary input provides a decoded octal (one-of-eight) code output with D forced to a logic " 0 ". Expanded decoding such as binary-to-hexadecimal (one-of-sixteen), etc., can be achieved by using other MC14028B devices. The part is useful for code conversion, address decoding, memory selection control, demultiplexing, or readout decoding.

## Features

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Positive Logic Design
- Low Outputs on All Illegal Input Combinations
- Similar to CD4028B
- NLV Prefix for Automotive and Other Applications Requiring

Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

- This Device is $\mathrm{Pb}-$ Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to $\mathrm{V}_{\mathrm{SS}}$ )

| Parameter | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| DC Supply Voltage Range | $\mathrm{V}_{\mathrm{DD}}$ | -0.5 to +18.0 | V |
| Input or Output Voltage Range <br> (DC or Transient) | $\mathrm{V}_{\text {in }}, \mathrm{V}_{\text {out }}$ | -0.5 to $\mathrm{V}_{\mathrm{DD}}$ <br> +0.5 | V |
| Input or Output Current (DC or Transient) <br> per Pin | $\mathrm{I}_{\text {in }}, \mathrm{I}_{\text {out }}$ | $\pm 10$ | mA |
| Power Dissipation per Package (Note 1) | $\mathrm{P}_{\mathrm{D}}$ | 500 | mW |
| Ambient Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature (8-Second Soldering) | $\mathrm{T}_{\mathrm{L}}$ | 260 | ${ }^{\circ} \mathrm{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: $-7.0 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ From $65^{\circ} \mathrm{C}$ To $125^{\circ} \mathrm{C}$ This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $\mathrm{V}_{\text {in }}$ and $\mathrm{V}_{\text {out }}$ should be constrained to the range $\mathrm{V}_{\mathrm{SS}} \leq\left(\mathrm{V}_{\text {in }}\right.$ or $\left.\mathrm{V}_{\text {out }}\right) \leq \mathrm{V}_{\mathrm{DD}}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $\mathrm{V}_{\mathrm{SS}}$ or $\mathrm{V}_{\mathrm{DD}}$ ). Unused outputs must be left open.

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http://onsemi.com

SOIC-16
D SUFFIX
CASE 751B

## PIN ASSIGNMENT

| Q4 1 - | 16 | $\mathrm{V}_{\mathrm{DD}}$ |
| :---: | :---: | :---: |
| Q2 2 | 15 | Q3 |
| Q0 3 | 14 | Q1 |
| Q7 [ 4 | 13 | B |
| Q9 [5 | 12 | ] |
| Q5 6 | 11 | ] |
| Q6 7 | 10 | 1 A |
| $\mathrm{V}_{\text {SS }} 8$ | 9 | Q8 |

## MARKING DIAGRAM



$$
\begin{array}{ll}
\text { A } & =\text { Assembly Location } \\
\text { WL } & =\text { Wafer Lot } \\
\text { YY, Y } & =\text { Year } \\
\text { WW } & =\text { Work Week } \\
\text { G } & =\text { Pb-Free Package }
\end{array}
$$

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet

## BLOCK DIAGRAM



TRUTH TABLE

| $\mathbf{D}$ | $\mathbf{C}$ | $\mathbf{B}$ | $\mathbf{A}$ | Q9 | Q8 | $\mathbf{Q} 7$ | $\mathbf{Q} 6$ | $\mathbf{Q}$ | Q4 | Q3 | Q2 | Q1 | Q0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

ORDERING INFORMATION

| Device | Package | Shipping ${ }^{\dagger}$ |
| :--- | :--- | :---: |
| MC14028BDG | SOIC-16 <br> (Pb-Free) | 48 Units / Rail |
| MC14028BDR2G | SOIC-16 <br> (Pb-Free) | $2500 /$ Tape \& Reel |
| NLV14028BDR2G* | SOIC-16 <br> (Pb-Free) | $2500 /$ Tape \& Reel |

$\dagger$ For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to $\mathrm{V}_{\mathrm{SS}}$ )

| Characteristic | Symbol | $\begin{aligned} & \mathrm{V}_{\mathrm{DD}} \\ & \mathrm{Vdc} \end{aligned}$ | $-55^{\circ} \mathrm{C}$ |  | $25^{\circ} \mathrm{C}$ |  |  | $125^{\circ} \mathrm{C}$ |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Max | Min | $\begin{gathered} \text { Typ } \\ \text { (Note 2) } \end{gathered}$ | Max | Min | Max |  |
| Output Voltage $\quad$ "0" Level $V_{\text {in }}=V_{D D}$ or 0 | $\mathrm{V}_{\text {OL }}$ | $\begin{aligned} & \hline 5.0 \\ & 10 \\ & 15 \end{aligned}$ | - | $\begin{aligned} & \hline 0.05 \\ & 0.05 \\ & 0.05 \end{aligned}$ | - | $\begin{aligned} & 0 \\ & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & \hline 0.05 \\ & 0.05 \\ & 0.05 \end{aligned}$ | - | $\begin{aligned} & \hline 0.05 \\ & 0.05 \\ & 0.05 \end{aligned}$ | Vdc |
| $V_{\text {in }}=0$ or $V_{\text {DD }}$ | $\mathrm{V}_{\mathrm{OH}}$ | $\begin{aligned} & 5.0 \\ & 10 \\ & 15 \end{aligned}$ | $\begin{gathered} \hline 4.95 \\ 9.95 \\ 14.95 \end{gathered}$ | - | $\begin{gathered} \hline 4.95 \\ 9.95 \\ 14.95 \end{gathered}$ | $\begin{aligned} & \hline 5.0 \\ & 10 \\ & 15 \end{aligned}$ | - | $\begin{gathered} \hline 4.95 \\ 9.95 \\ 14.95 \end{gathered}$ | - | Vdc |
| $\begin{aligned} & \text { Input Voltage } \\ & \left(\mathrm{V}_{\mathrm{O}}=4.5 \text { or } 0.5 \mathrm{Vdc}\right) \\ & \left(\mathrm{V}_{\mathrm{O}}=9.0 \text { or } 1.0 \mathrm{Vdc}\right) \\ & \left(\mathrm{V}_{\mathrm{O}}=13.5 \text { or } 1.5 \mathrm{Vdc}\right) \\ & \\ & \left(\mathrm{V}_{\mathrm{O}}=0.5 \text { or } 4.5 \mathrm{Vdc}\right) \\ & \left(\mathrm{V}_{\mathrm{O}}=1.0 \text { or } 9.0 \mathrm{Vdc}\right) \\ & \left(\mathrm{V}_{\mathrm{O}}=1.5 \text { or } 13.5 \mathrm{Vdc}\right) \end{aligned}$ | VIL | $\begin{aligned} & 5.0 \\ & 10 \\ & 15 \end{aligned}$ | - | $\begin{aligned} & 1.5 \\ & 3.0 \\ & 4.0 \end{aligned}$ | - | $\begin{aligned} & 2.25 \\ & 4.50 \\ & 6.75 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 3.0 \\ & 4.0 \end{aligned}$ | - | $\begin{aligned} & 1.5 \\ & 3.0 \\ & 4.0 \end{aligned}$ | Vdc |
|  | $\mathrm{V}_{\mathrm{IH}}$ | $\begin{aligned} & 5.0 \\ & 10 \\ & 15 \end{aligned}$ | $\begin{gathered} 3.5 \\ 7.0 \\ 11 \end{gathered}$ | - | $\begin{aligned} & 3.5 \\ & 7.0 \\ & 11 \end{aligned}$ | $\begin{aligned} & 2.75 \\ & 5.50 \\ & 8.25 \end{aligned}$ | - | 3.5 7.0 11 | - | Vdc |
| Output Drive Current  <br> $\left(\mathrm{VOH}_{\mathrm{OH}}=2.5 \mathrm{Vdc}\right)$ Source <br> $(\mathrm{VOH}=4.6 \mathrm{Vdc})$  <br> $\left(\mathrm{V}_{\mathrm{OH}}=9.5 \mathrm{Vdc}\right)$  <br> $\left(\mathrm{V}_{\mathrm{OH}}=13.5 \mathrm{Vdc}\right)$  | IOH | $\begin{aligned} & 5.0 \\ & 5.0 \\ & 10 \\ & 15 \\ & \hline \end{aligned}$ | $\begin{gathered} -3.0 \\ -0.64 \\ -1.6 \\ -4.2 \\ \hline \end{gathered}$ | - - - | $\begin{array}{r} -2.4 \\ -0.51 \\ -1.3 \\ -3.4 \\ \hline \end{array}$ | $\begin{aligned} & -4.2 \\ & -0.88 \\ & -2.25 \\ & -8.8 \\ & \hline \end{aligned}$ | - | $\begin{gathered} -1.7 \\ -0.36 \\ -0.9 \\ -2.4 \\ \hline \end{gathered}$ | - | mAdc |
| $\begin{array}{lll} \left(\mathrm{V}_{\mathrm{OL}}=0.4 \mathrm{Vdc}\right) & \text { Sink } \\ \left(\mathrm{V}_{\mathrm{OL}}=0.5 \mathrm{Vdc}\right) & \\ \left(\mathrm{V}_{\mathrm{OL}}=1.5 \mathrm{Vdc}\right) & \end{array}$ | loL | $\begin{aligned} & 5.0 \\ & 10 \\ & 15 \end{aligned}$ | $\begin{gathered} 0.64 \\ 1.6 \\ 4.2 \end{gathered}$ | - | $\begin{gathered} \hline 0.51 \\ 1.3 \\ 3.4 \end{gathered}$ | $\begin{gathered} 0.88 \\ 2.25 \\ 8.8 \end{gathered}$ | - | $\begin{gathered} \hline 0.36 \\ 0.9 \\ 2.4 \end{gathered}$ | - | mAdc |
| Input Current | $\mathrm{l}_{\text {in }}$ | 15 | - | $\pm 0.1$ | - | $\pm 0.00001$ | $\pm 0.1$ | - | $\pm 1.0$ | $\mu \mathrm{Adc}$ |
| Input Capacitance ( $\mathrm{V}_{\text {in }}=0$ ) | $\mathrm{C}_{\text {in }}$ | - | - | - | - | 5.0 | 7.5 | - | - | pF |
| Quiescent Current (Per Package) | IDD | $\begin{aligned} & 5.0 \\ & 10 \\ & 15 \end{aligned}$ | - | $\begin{aligned} & 5.0 \\ & 10 \\ & 20 \end{aligned}$ | - | $\begin{aligned} & 0.005 \\ & 0.010 \\ & 0.015 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 10 \\ & 20 \end{aligned}$ | - | $\begin{aligned} & 150 \\ & 300 \\ & 600 \end{aligned}$ | $\mu \mathrm{Adc}$ |
| Total Supply Current (Note 3, 4) (Dynamic plus Quiescent, Per Package) ( $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ on all outputs, all buffers switching) | ${ }^{\text {T }}$ | $\begin{aligned} & 5.0 \\ & 10 \\ & 15 \end{aligned}$ | $\begin{aligned} & \mathrm{I}_{\mathrm{T}}=(0.3 \mu \mathrm{~A} / \mathrm{kHz}) \mathrm{f}+\mathrm{I}_{\mathrm{DD}} \\ & \mathrm{I}_{\mathrm{T}}=(0.6 \mu \mathrm{~A} / \mathrm{kHz}) \mathrm{f}+\mathrm{I}_{\mathrm{DD}} \\ & \mathrm{I}_{\mathrm{T}}=(0.9 \mu \mathrm{kHz}) \mathrm{f}+\mathrm{I}_{\mathrm{DD}} \end{aligned}$ |  |  |  |  |  |  | $\mu \mathrm{Adc}$ |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at $25^{\circ} \mathrm{C}$.
4. To calculate total supply current at loads other than 50 pF : $\mathrm{I}_{\mathrm{T}}\left(\mathrm{C}_{\mathrm{L}}\right)=\mathrm{I}_{T}(50 \mathrm{pF})+\left(\mathrm{C}_{\mathrm{L}}-50\right)$ Vfk where: $\mathrm{I}_{\mathrm{T}}$ is in $\mu \mathrm{A}$ (per package), $\mathrm{C}_{\mathrm{L}}$ in pF , $V=\left(V_{D D}-V_{S S}\right)$ in volts, $f$ in $k H z$ is input frequency, and $k=0.001$.

SWITCHING CHARACTERISTICS (Note 5) ( $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ )

| Characteristic | Symbol | $\mathrm{V}_{\mathrm{DD}}$ | Min | Typ <br> (Note 6) | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Rise and Fall Time <br> $\mathrm{t}_{\text {TLH }}, \mathrm{t}_{\text {THL }}=(1.5 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}}+25 \mathrm{~ns}$ <br> $\mathrm{t}_{\mathrm{TL}}, \mathrm{t}_{\mathrm{THL}}=(0.75 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}}+12.5 \mathrm{~ns}$ <br> $\mathrm{t}_{\mathrm{T} L \mathrm{H}}, \mathrm{t}_{\mathrm{THL}}=(0.55 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}}+9.5 \mathrm{~ns}$ | $\begin{aligned} & \mathrm{t}_{\mathrm{TLLH}}, \\ & \mathrm{t}_{\mathrm{TH}} \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 10 \\ & 15 \end{aligned}$ | - | $\begin{aligned} & 100 \\ & 50 \\ & 40 \end{aligned}$ | $\begin{gathered} 200 \\ 100 \\ 80 \end{gathered}$ | ns |
| Propagation Delay Time <br> $\mathrm{t}_{\mathrm{PLH}}, \mathrm{t}_{\mathrm{PHL}}=(1.7 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}}+215 \mathrm{~ns}$ <br> $t_{\text {PLH }}, t_{\text {PHL }}=(0.66 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}}+97 \mathrm{~ns}$ <br> $t_{\text {PLH }}, \mathrm{t}_{\text {PHL }}=(0.5 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}}+65 \mathrm{~ns}$ | $\begin{aligned} & \text { tpLH, } \\ & t_{\text {PHLL }} \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 10 \\ & 15 \end{aligned}$ | - | $\begin{gathered} 300 \\ 130 \\ 90 \end{gathered}$ | $\begin{aligned} & 600 \\ & 260 \\ & 180 \end{aligned}$ | ns |

5. The formulas given are for the typical characteristics only at $25^{\circ} \mathrm{C}$.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

Inputs $\mathrm{B}, \mathrm{C}$, and D switching in respect to a BCD code.


All outputs connected to respective $\mathrm{C}_{\mathrm{L}}$ loads. f in respect to a system clock.

Inputs $A, B$, and $D$ low.


Figure 1. Dynamic Signal Waveforms


LOGIC DIAGRAM

## APPLICATIONS INFORMATION

Expanded decoding can be performed by using the MC14028B and other CMOS Integrated Circuits. The circuit in Figure 2 converts any 4-bit code to a decimal or hexadecimal code. The accompanying table shows the input binary combinations, the associated "output numbers" that go "high" when selected, and the "redefined output numbers" needed for the proper code. For example: For the combination DCBA $=0111$ the output number 7 is redefined for the 4-bit binary, 4-bit gray, excess-3, or excess-3 gray codes as $7,5,4$, or 2 , respectively. Figure 3 shows a 6 -bit binary $1-$ of -64 decoder using nine MC14028B circuits and two MC14069UB inverters.

The MC14028B can be used in decimal digit displays, such as, neon readouts or incandescent projection indicators as shown in Figure 4.


Figure 2. Code Conversion Circuit and Truth Table

| Inputs |  |  |  | Output Numbers |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Code and Redefined Output Numbers |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Hexadecimal | Decimal |  |  |
|  |  |  |  |  |  | $\begin{aligned} & 0 \\ & ⿹ 勹 䶹 \\ & \ddot{0} \\ & \dot{0} \\ & \underset{\sim}{x} \end{aligned}$ |  |  | $\overline{\underset{\sim}{N}}$ |
| D | C | B | A |  |  |  |  |  |  | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |  |  | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |  |  | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 2 | 3 |  | 0 | 2 | 2 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 3 | 2 | 0 | 3 | 3 |  |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 4 | 7 | 1 | 4 | 4 |  |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 5 | 6 | 2 |  |  | 3 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 6 | 4 | 3 | 1 |  | 4 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 7 | 5 | 4 | 2 |  |  |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 15 | 5 |  |  |  |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 9 | 14 | 6 |  |  | 5 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 10 | 12 | 7 | 9 |  | 6 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 11 | 13 | 8 |  | 5 |  |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 12 | 8 | 9 | 5 | 6 |  |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 13 | 9 |  | 6 | 7 | 7 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 14 | 11 |  | 8 | 8 | 8 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 15 | 10 |  | 7 | 9 | 9 |



Figure 3．Six－Bit Binary 1－of－64 Decoder


Figure 4．Decimal Digit Display Application

## PACKAGE DIMENSIONS



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 ( 0.006 ) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR

PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |  | INCHES |  |
| :---: | :---: | ---: | :---: | ---: |
|  | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC |  | 0.050 |  |
| BSC |  |  |  |  |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | $0^{\circ}$ | $7^{\circ}$ | $0^{\circ}$ | $7^{\circ}$ |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

SOLDERING FOOTPRINT*


DIMENSIONS: MILLIMETERS
*For additional information on our $\mathrm{Pb}-$ Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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