
Chipsmall
深圳市津利帝科技有限公司
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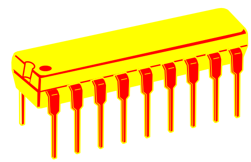
采购部

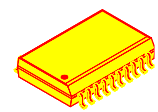
MC144110 and MC144111

Digital-to-Analog Converters with Serial Interface

CMOS LSI

MC144110

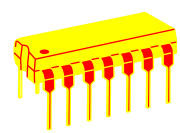


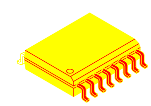


Package Information
P Suffix
Plastic DIP
Case 707

Package Information
DW Suffix
SOG Package
Case 751D

MC144111





Package Information
P Suffix
Plastic DIP
Case 646

Package Information
DW Suffix
SOG Package
Case 751G

Ordering Information

Device	Package
MC144110P	Plastic DIP
MC144110DW	SOG
MC144111P	Plastic DIP
MC144111DW	SOG

Contents

1 Introduction

The MC144110 and MC144111 are low-cost 6-bit D/A converters with serial interface ports to provide communication with CMOS microprocessors and microcomputers. The MC144110 contains six static D/A converters; the MC144111 contains four converters.

Due to a unique feature of these DACs, the user is permitted easy scaling of the analog outputs of a system. Over a 5 to 15 V supply range, these DACs may be directly interfaced to CMOS MPUs operating at 5 V.

- Direct R-2R Network Outputs
- Buffered Emitter-Follower Outputs
- Serial Data Input
- Digital Data Output Facilitates Cascading
- Direct Interface to CMOS µP
- Wide Operating Voltage Range: 4.5 to 15 V
- Wide Operating Temperature Range: 0 to 85°C
- Software Information is Contained in Document M68HC11RM/AD

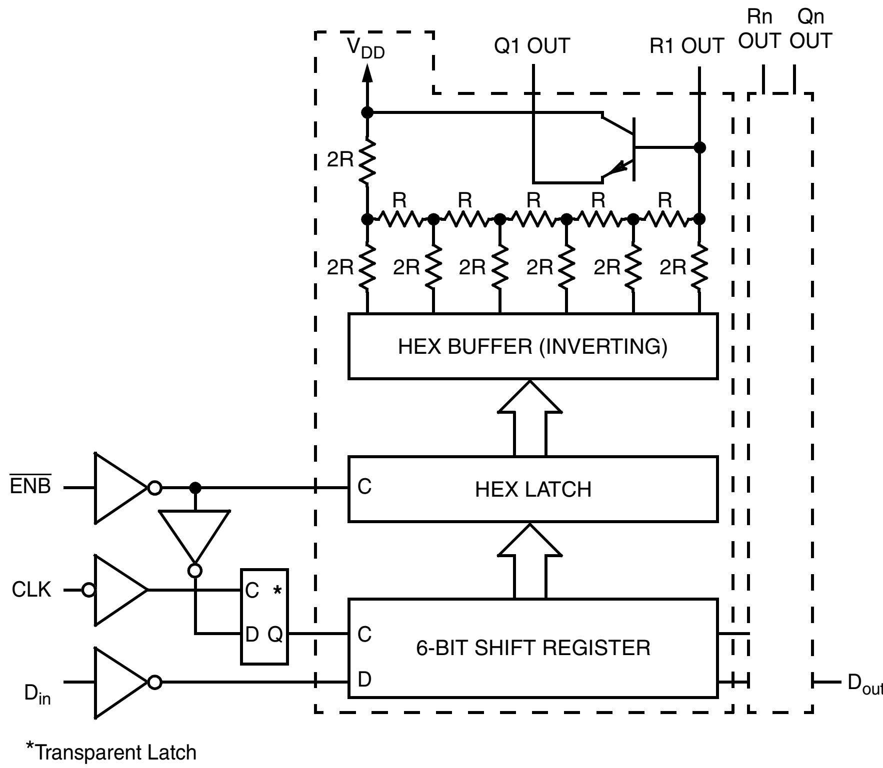
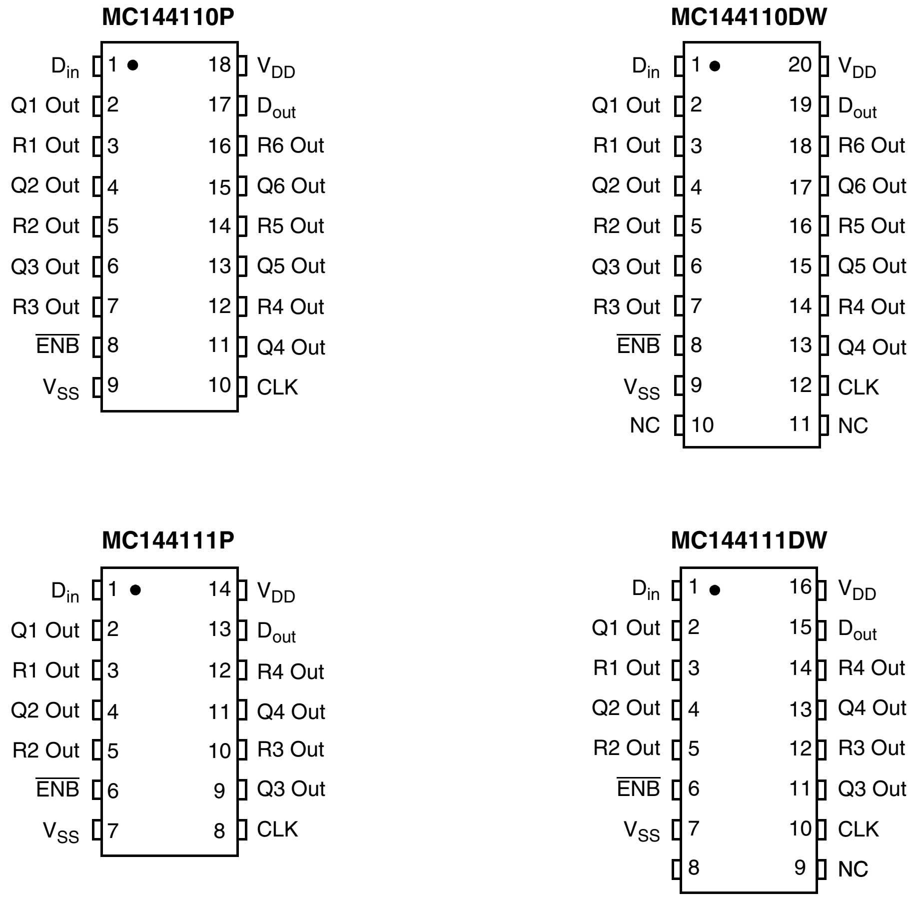


Figure 1. Block Diagram



NC = No Connection

Figure 2. Pin Assignments

2 Electrical Specifications

Table 1. Maximum Ratings
(Voltages referenced to V_{SS})

Ratings	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	- 0.5 to + 18	V
Input Voltage, All Inputs	V_{in}	- 0.5 to V_{DD} + 0.5	V
DC Input Current, per Pin	I	± 10	mA
Power Dissipation (Per Output) T_A = 70°C MC144110 MC144111 T_A = 85°C MC144110 MC144111	P_{OH}	 30 50 10 20	mW
Power Dissipation (Per Package) T_A = 70°C MC144110 MC144111 T_A = 85°C MC144110 MC144111	P_D	 100 150 25 50	mW
Storage Temperature Range	T_{stg}	- 65 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields; however, it is advised that precautions be taken to avoid application of voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Table 2. Electrical Characteristics
(Voltages referenced to V_{SS}, T_A = 0 to 85°C unless otherwise indicated)

Symbol	Parameter	Test Conditions	V_{DD}	Min	Max	Unit
V_{IH}	High-Level Input Voltage (D_{in}, $\overline{ENB}$, CLK)		5 10 15	3.0 3.5 4	- - -	V
V_{IL}	Low-Level Input Voltage (D_{in}, $\overline{ENB}$, CLK)		5 10 15	- - -	0.8 0.8 0.8	V
I_{OH}	High-Level Output Current (D_{out})	$V_{out} = V_{DD}$ - 0.5 V	5	- 200	-	µA
I_{OL}	Low-Level Output Current (D_{out})	V_{out} = 0.5 V	5	200	-	µA
I_{DD}	Quiescent Supply Current MC144110 MC144111	I_{out} = 0 µA	15 15	- -	12 8	mA
I_{in}	Input Leakage Current (D_{in}, $\overline{ENB}$, CLK)	$V_{in} = V_{DD}$ or 0 V	15	-	± 1	µA
V_{nonl}	Nonlinearity Voltage (Rn Out)	See Figure 3	5 10 15	- - -	100 200 300	mV

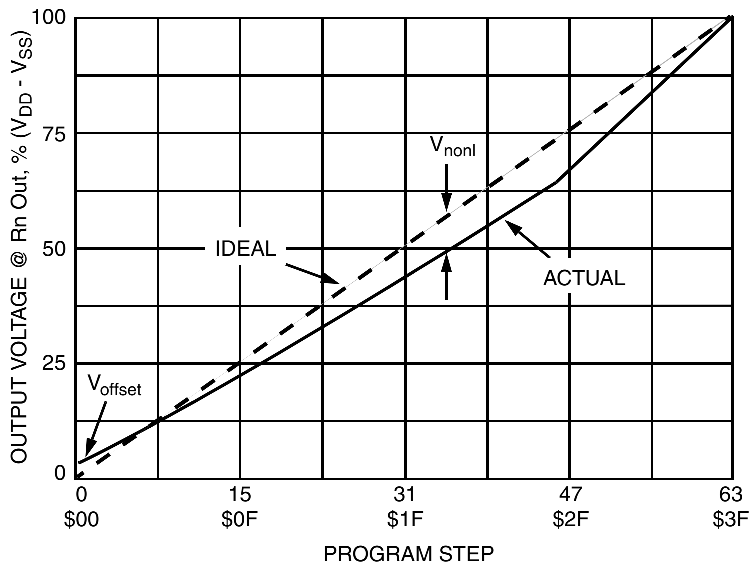
Table 2. Electrical Characteristics (continued)
(Voltages referenced to V_{SS}, T_A = 0 to 85°C unless otherwise indicated)

Symbol	Parameter	Test Conditions	V_{DD}	Min	Max	Unit
V_{step}	Step Size (Rn Out)	See Figure 4	5 10 15	19 39 58	137 274 411	mV
V_{offset}	Offset Voltage from V_{SS}	D_{in} = $00, See Figure 3	-	-	1	LSB
I_E	Emitter Leakage Current	$V_{Rn\ Out}$ = 0 V	15	-	10	µA
h_{FE}	DC Current Gain	I_E = 0.1 to 10.0 mA T_A = 25°C	-	40	-	-
V_{BE}	Base-to-Emitter Voltage Drop	I_E = 1.0 mA	-	0.4	0.7	V

3 Switching Characteristics

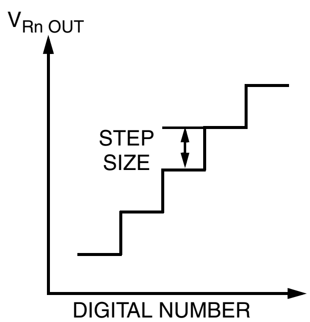
Table 3. Switching Characteristics
(Voltages referenced to V_{SS}, T_A = 0 to 85°C, C_L = 50 pF, Input t_r = t_f = 20 ns unless otherwise indicated)

Symbol	Parameter	V_{DD}	Min	Max	Unit
t_{wH}	Positive Pulse Width, CLK (Figures 5 and 6)	5 10 15	2 1.5 1	- - -	µs
t_{wL}	Negative Pulse Width, CLK (Figure 5 and 6)	5 10 15	5 3.5 2	- - -	µs
t_{su}	Setup Time, $\overline{ENB}$ to CLK (Figures 5 and 6)	5 10 15	5 3.5 2	- - -	µs
t_{su}	Setup Time, D_{in} to CLK (Figures 5 and 6)	5 10 15	1000 750 500	- - -	ns
t_h	Hold Time, CLK to $\overline{ENB}$ (Figures 5 and 6)	5 10 15	5 3.5 2	- - -	µs
t_h	Hold Time, CLK to D_{in} (Figures 5 and 6)	5 10 15	5 3.5 2	- - -	µs
t_r, t_f	Input Rise and Fall Times	5 - 15	-	2	µs
C_{in}	Input Capacitance	5 - 15	-	7.5	pF



LINEARITY ERROR (integral linearity). A measure of how straight a device's transfer function is, it indicates the worst-case deviation of linearity of the actual transfer function from the best-fit straight line. It is normally specified in parts of an LSB.

Figure 3. D/A Transfer Function



$$\text{Step Size} = \frac{V_{DD}}{64} \pm 0.75\frac{V_{DD}}{64}$$

(For any adjacent pair of digital numbers)

Figure 4. Definition of Step Size

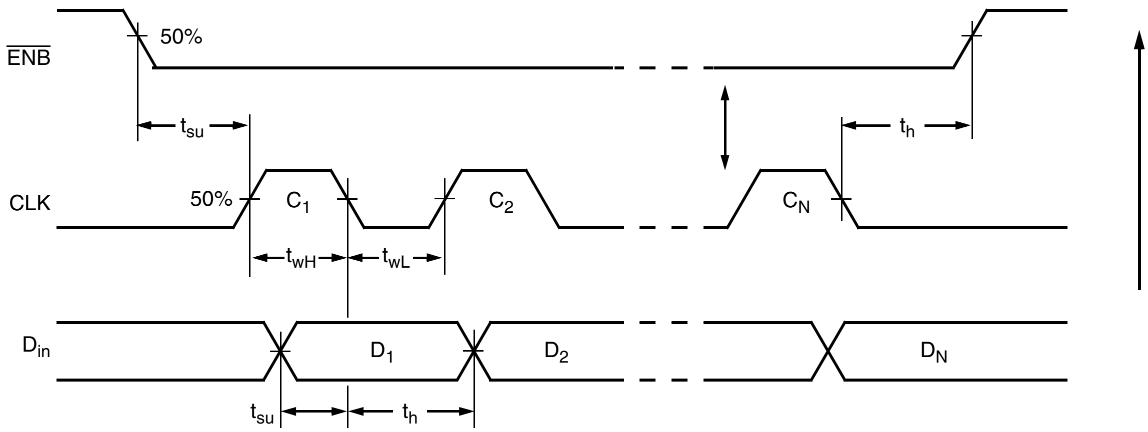


Figure 5. Serial Input, Positive Clock

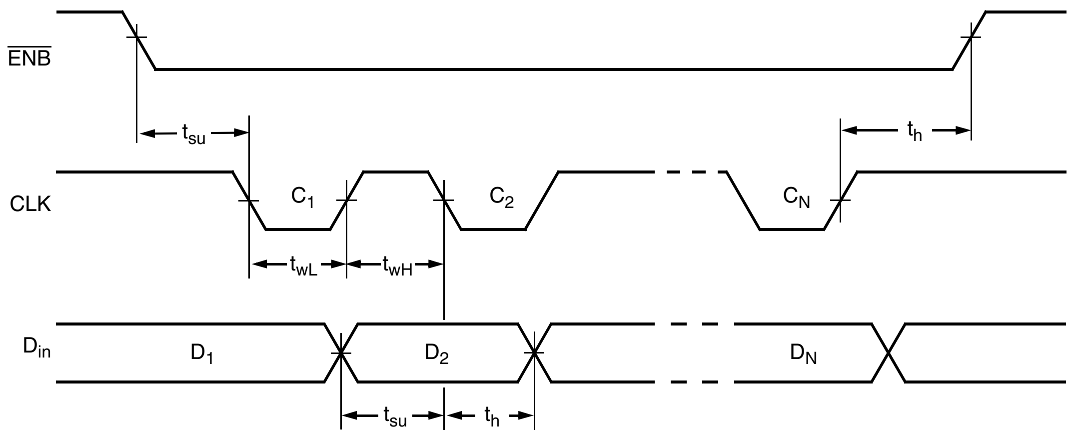


Figure 6. Serial Input, Negative Clock

Table 4. Number of Channels vs Clocks Required

Number of Channels Required	Number of Clock Cycles	Outputs Used on MC144110	Outputs Used on MC144111
1	6	Q1/R1	Q1/R1
2	12	Q1/R1, Q2/R2	Q1/R1, Q2/R2
3	18	Q1/R1, Q2/R2, Q3/R3	Q1/R1, Q2/R2, Q3/R3
4	24	Q1/R1, Q2/R2, Q3/R3, Q4/R4	Q1/R1, Q2/R2, Q3/R3, Q4/R4
5	30	Q1/R1, Q2/R2, Q3/R3, Q4/R4, Q5/R5	Not Applicable
6	36	Q1/R1, Q2/R2, Q3/R3, Q4/R4, Q5/R5, Q6/R6	Not Applicable

4 Pin Descriptions

4.1 INPUTS

D_{in}
Data Input

Six-bit words are entered serially, MSB first, into digital data input, D_{in}. Six words are loaded into the MC144110 during each D/A cycle; four words are loaded into the MC144111.

The last 6-bit word shifted in determines the output level of pins Q1 Out and R1 Out. The next-to-last 6-bit word affects pins Q2 Out and R2 Out, etc.

$\overline{\text{ENB}}$
Negative Logic Enable

The $\overline{\text{ENB}}$ pin must be low (active) during the serial load. On the low-to-high transition of $\overline{\text{ENB}}$, data contained in the shift register is loaded into the latch.

CLK
Shift Register Clock

Data is shifted into the register on the high-to-low transition of CLK. CLK is fed into the D-input of a transparent latch, which is used for inhibiting the clocking of the shift register when $\overline{\text{ENB}}$ is high.

The number of clock cycles required for the MC144110 is usually 36. The MC144111 usually uses 24 cycles. See Table 4 for additional information.

4.2 OUTPUTS

D_{out}
Data Output

The digital data output is primarily used for cascading the DACs and may be fed into D_{in} of the next stage.

R1 Out through Rn Out
Resistor Network Outputs

These are the R-2R resistor network outputs. These outputs may be fed to high-impedance input FET op amps to bypass the on-chip bipolar transistors. The R value of the resistor network ranges from 7 to 15 kΩ.

Q1 Out through Qn Out
NPN Transistor Outputs

Buffered DAC outputs utilize an emitter-follower configuration for current-gain, thereby allowing interface to low-impedance circuits.

4.3 SUPPLY PINS

V_{SS}
Negative Supply Voltage

This pin is usually ground.

V_{DD}
Positive Supply Voltage

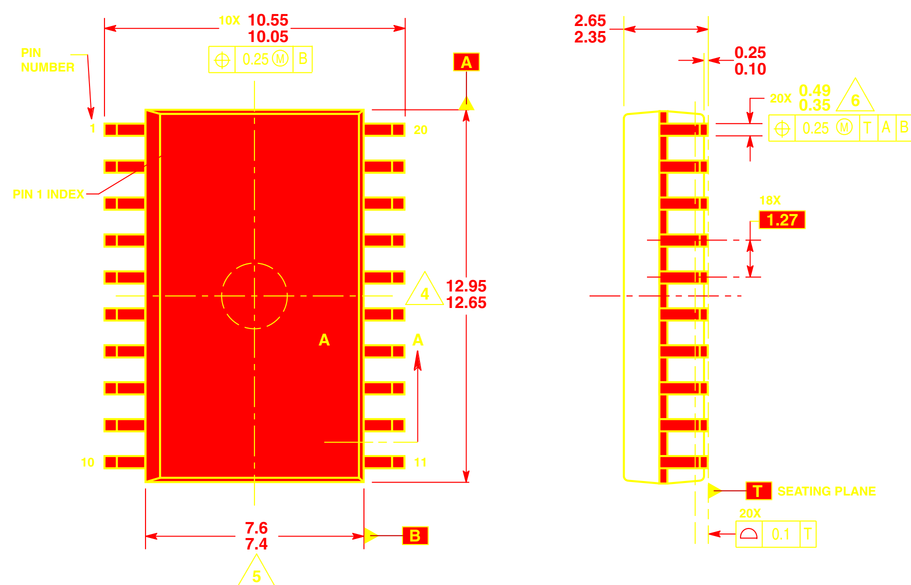
The voltage applied to this pin is used to scale the analog output swing from 4.5 to 15 V p-p.

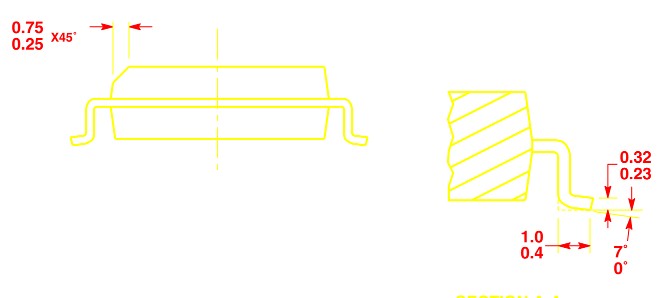
5 Packaging

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D). SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.875	0.915	22.22	23.24
B	0.240	0.260	6.10	6.60
C	0.140	0.180	3.56	4.57
D	0.014	0.022	0.36	0.56
F	0.050	0.070	1.27	1.78
G	0.100 BSC		2.54 BSC	
H	0.040	0.060	1.02	1.52
J	0.008	0.012	0.20	0.30
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

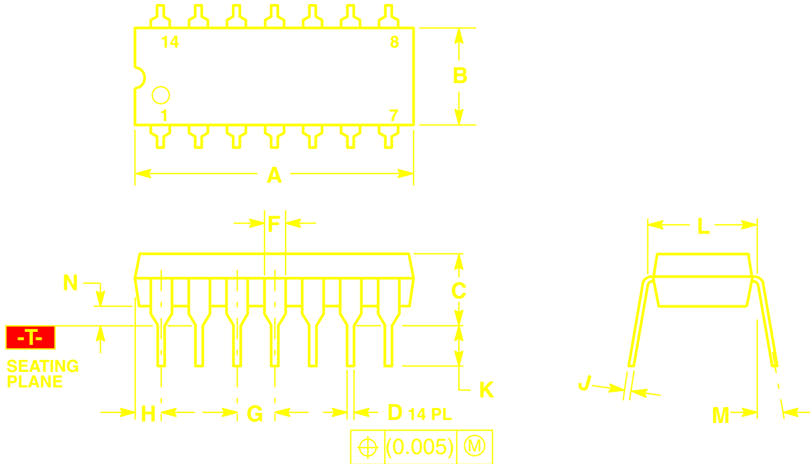
Figure 7. Outline Dimensions for P SUFFIX, PLASTIC DIP (CASE 707-02, Issue C)





NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE WIDTH TO EXCEED 0.62mm.

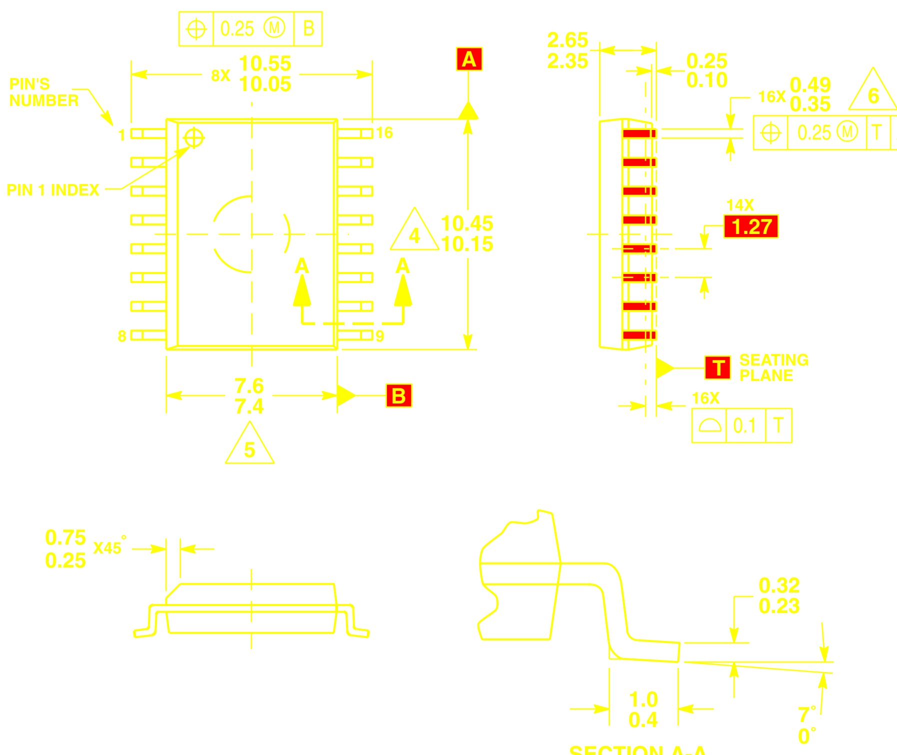
Figure 8. Outline Dimensions for DW SUFFIX, SOG (CASE 751D-06, Issue H)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.
6. 646-06 OBSOLETE, NEW STANDARD 646-07.

	INCHES	
DIM	MIN	MAX
A	0.715	0.770
B	0.240	0.260
C	0.145	0.185
D	0.015	0.021
F	0.040	0.070
G	0.100 BSC	
H	0.052	0.095
J	0.008	0.015
K	0.115	0.135
L	0.290	0.310
M	---	10°
N	0.015	0.040

Figure 9. Outline Dimensions for P SUFFIX, PLASTIC DIP (CASE 646-07, Issue P)



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62mm.

Figure 10. Outline Dimensions for DW SUFFIX, SOG (CASE 751G-04, Issue D)

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