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MC145574/D
REV 6

MC145574

ISDN S/T-Interface Transceiver

Coming through loud and clear.

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MC145574

ISDN S/T-Interface Transceiver

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1
INTRODUCTION

1.1 INTRODUCTION

The MC145574 is Motorola's second generation S/T transceiver and is a follow–up to the MC145474/75 transceiver.

The MC145574 provides the improved interfacing capabilities and reduced power consumption required by today's ISDN applications, while maintaining the functionality and extended range performance of the MC145474/75.

The MC145574 provides an economical VLSI layer 1 interface for the transportation of two 64 kbps B channels and one 16 kbps D channel between the network termination (NT) and terminal equipment applications (TEs). The MC145574 conforms to CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specifications.

The MC145574 provides the modulation/line drive and demodulation/line receive functions required of the interface. In addition, the MC145574 provides the activation/deactivation, error monitoring, framing, bit, and octet timing. The MC145574 provides the control signals for the interface to the layer 2 devices. Complete multiframe capability is provided.

The MC145574 features the interchip digital link (IDL2) for the exchange of the 2B+D channel information between ISDN components and systems. The MC145574 provides an industry standard serial control port (SCP) to program the operation of the transceiver. As an alternative to the IDL2+SCP combination, a general circuit interface (GCI) is provided.

The MC145574 is not pin compatible with the MC145474/75, but it does have a compatible register set. However, to make full use of the additional MC145574 features, software enhancements are required.

1.2 ORGANIZATION OF DATA SHEET

This data sheet is comprised of 20 sections. Section 1 is an introduction, serving to outline the features, package types, and pin assignments of the MC145574. Section 2 describes the various wiring configurations which are applicable to the MC145574, and the operational distances as recommended by CCITT I.430, ETSI ETS 300012, and ANSI T1.605. Section 3 addresses the activation and deactivation procedures of the MC145574.

The MC145574 incorporates the IDL2. This is a four–wire interface used for full–duplex communication between ICs on the board level. Two 64 kbps B channels and one 16 kbps D channel are transmitted and received over this interface. Section 4 is a detailed description of the IDL2.

The MC145574 incorporates an SCP interface. The SCP is a four–wire interface conforming to an industry standard multi–drop serial link. The SCP is compatible with Motorola's serial peripheral interface (SPI). The SCP makes use of seven nibble registers, 16 byte registers and 10 overlay registers. Section 5 is a description of the SCP. A per bit description of the nibble, byte, and overlay registers is provided in Sections 8, 9, and 10, respectively. When the MC145574 is configured as a TE, it is equipped with five interrupt modes. When configured as an NT, it is equipped with four interrupt modes. Section 15 describes these interrupts.

The MC145574 also features a GCI interface. This is a standard four–wire interface which allows full–duplex transmission of two 64 kbps B channels and one 16 kbps D channel, multiplexed with control and maintenance information channels. Section 6 is a description of the GCI.

Section 7 contains pin descriptions of the MC145574. The pin descriptions differentiate between the device configured for NT mode or TE mode of operation, and GCI and IDL2+SCP.

As mentioned previously, the MC145574 is used for the transmission of two 64 kbps B channels and one 16 kbps D channel. Access to the B channels is determined by the network. The TEs gain access to the D channel in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605 recommendations. A description of the D channel operation is contained in Section 11.

In addition to the 2B+D channels, the S/T transceiver has a multiframing capability. Multiframing is a layer 1 signalling channel for use between the NT and the TE(s). The multiframing operation is described in Section 12.

The MC145574 can be configured in several different operating modes depending on the application. Section 13 describes all the possible configurations, whether in the NT or TE mode.

Section 16 describes how to interface the MC145574 to the S/T bus. Section 17 describes the various power modes of operation. Section 18 contains electrical specifications, and Section 19 contains mechanical data relevant to the MC145574. Section 20 describes the differences between this data book and the F57J4 mask version of the MC145574.

1.3 FEATURES

The features of the MC145574 are described below.

- Conforms to CCITT I.430, ETSI ETS 300012, and ANSI T1.605 Specifications
- Register Compatible With the First Generation MC145474/75
- Exceeds Q.502 Jitter Requirements for TE Slave Applications
- Pin Selectable NT or TE Modes of Operation
- Incorporates the IDL2, With Timeslot Assigner
- Industry Standard Microprocessor SCP
- GCI Interface
- Uses 2.5:1 Transformers for Transmit and Receive
- Exceeds the Recommended Range of Operation in All Configurations
- Complete Multiframing Capability Supported (SC1 – SC5 and Q Channel)
- Optional B Channel Idle, Invert, or Exchange
- Supports Full Range of S/T and IDL2 Loopbacks
- Supports Transmit Power–Down, Listening, and Absolute Minimum Power Modes
- Supports Crystal or External Clock Input Mode
- NT Star and NT Terminal Modes Supported
- Low Power Consumption
- Compatible with 3 V Devices

1.4 BLOCK DIAGRAM

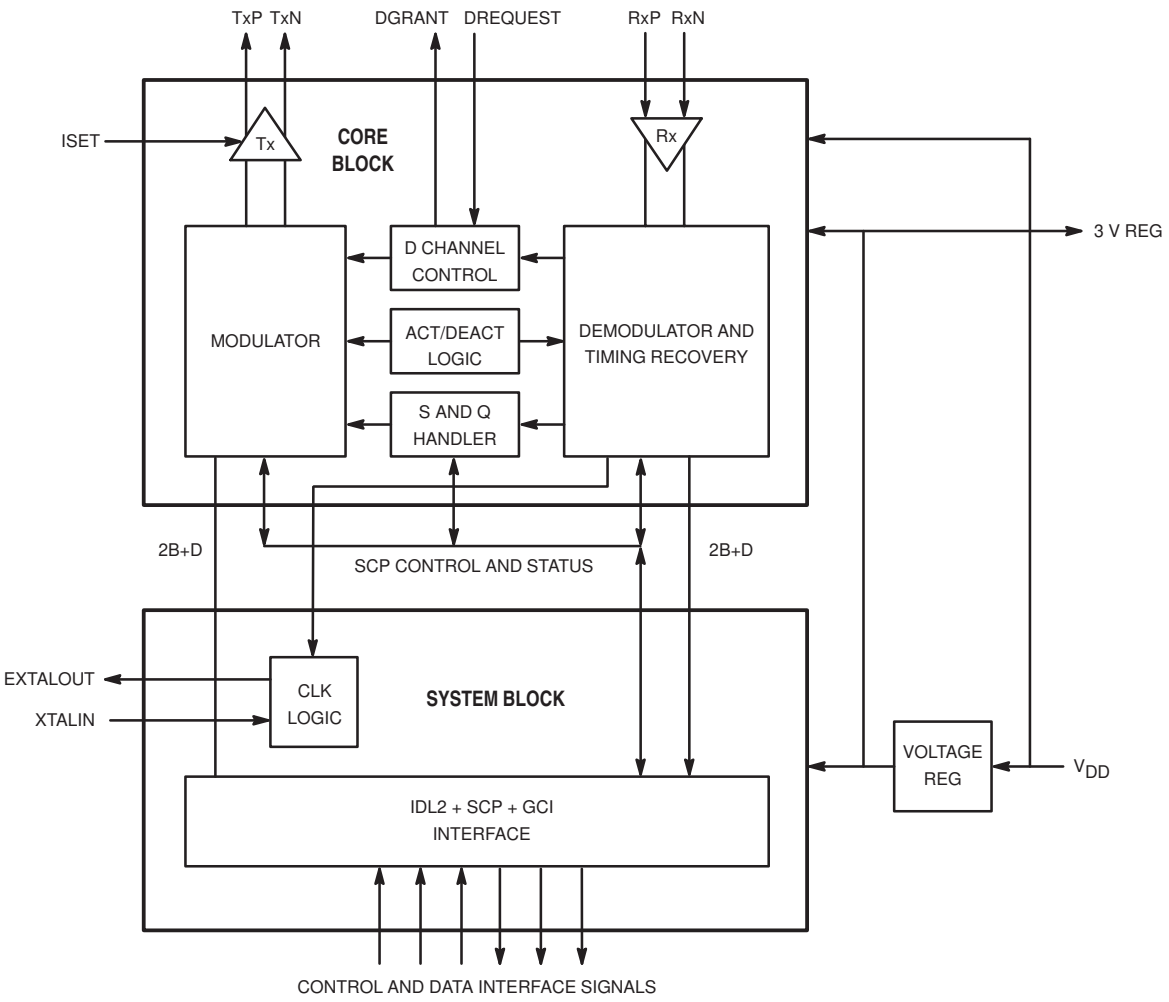

Figure 1–1. Block Diagram

1.5 PACKAGING

The MC145574 comes in the following packages:

28–Pin, 600 mil Wide, Plastic SOIC
32–Pin, 700 mil Square, TQFP

The pin assignments for the MC145574 are described in Section 7. Package dimensions are in Section 19.

2
WIRING CONFIGURATIONS

2.1 INTRODUCTION

The MC145574 ISDN S/T transceiver conforms to CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specifications. It is a layer 1 transceiver designed for use at the ISDN S and T reference points. It is designed for both point–to–point and multipoint operation. The S/T transceiver is designed for use in either the network terminating (NT) mode or in the terminal endpoint (TE) applications. Two 64 kpbs B channels and one 16 kbps D channel are transmitted in a full–duplex fashion across the interface.

Sections 2.2 through 2.6 contain suggested wiring configurations for use. These configurations are deemed to be the most common but by no means the only wiring configurations. Section 16 specifies the recommended circuitry for interfacing the MC145574 to the S/T bus. Note that when operating in the TE mode, only one TE has the 100 Ω termination resistors in the transmit and receive paths. Figures 2–1 through 2–4 illustrate where to connect the termination resistors for the described loop configurations.

A description of the most commonly used loop configurations is as described below.

2.2 POINT-TO-POINT OPERATION

In the point–to–point mode of operation, one NT communicates with one TE. As such, 100 Ω termination resistors must be connected across the transmit and receive paths of both the NT and TE transceivers. Figure 2–1 illustrates this wiring configuration.

When using the MC145574 in this configuration, the NT must be in adaptive timing. This is accomplished by holding the FIX pin low; i.e., connecting it to V_{SS}. Refer to Section 6 for a more detailed description of this pin function. CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specify that the S/T transceiver must be able to operate up to a distance of 1 km in the point–to–point mode. This is the distance D1 as shown in Figure 2–1.

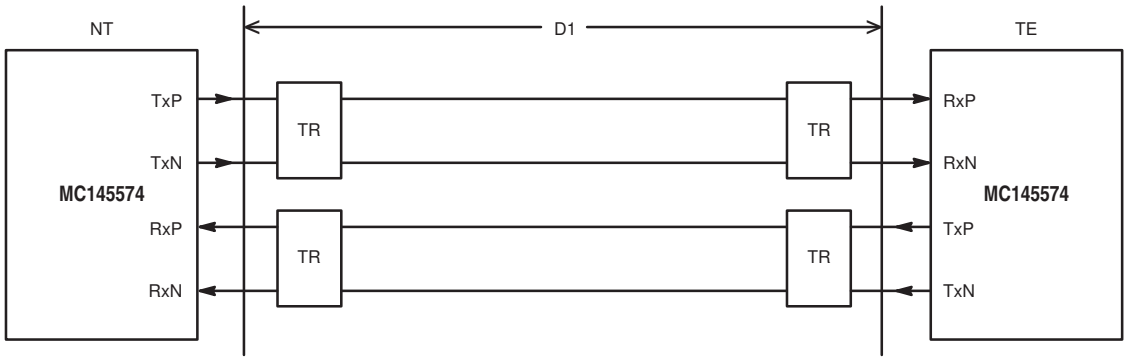

Figure 2–1. Point–to–Point

2.3 SHORT PASSIVE BUS OPERATION

The short passive bus is intended for use when up to eight TEs are required to communicate with one NT. The TEs can be distributed at any point along the passive bus, the only requirement being that the termination resistors be located at the end of the passive bus. Figure 2–2 illustrates this wiring configuration. CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specify a maximum operational distance from the NT of 200 meters. This corresponds to the distance D2 as shown in Figure 2–2.

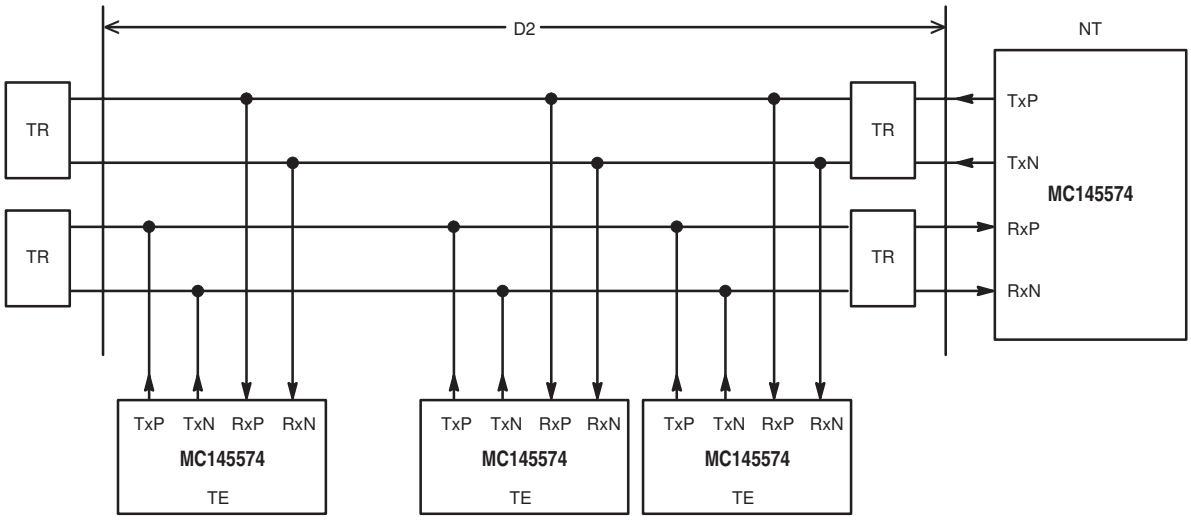

Figure 2–2. Short Passive Bus

2.4 EXTENDED PASSIVE BUS OPERATION

A wiring configuration whereby the TEs are restricted to a grouping at the far end of the cable, distant from the NT, is shown as the “Extended Passive Bus.” This configuration is shown in Figure 2–3. The termination resistors are to be positioned as shown in Figure 2–3.

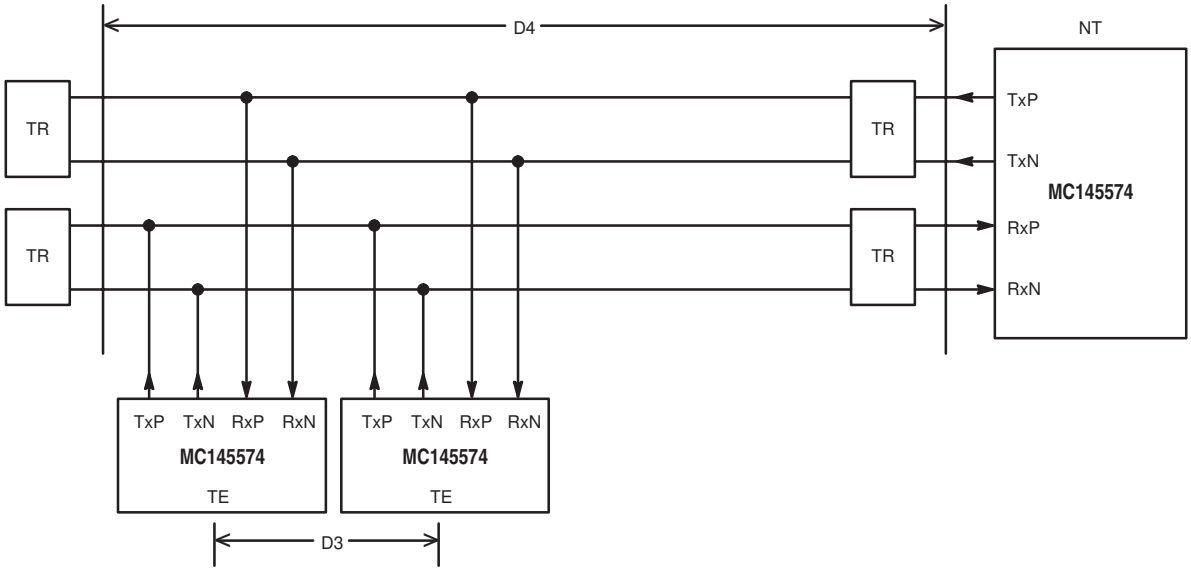

Figure 2–3. Extended Passive Bus

The essence of this configuration is that a restriction is placed on the distance between the TEs. The distance, D3 (as shown in Figure 2–3), corresponds to the maximum distance between the grouping of TEs. CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specify a distance of 25 – 50 meters for the separation between the TEs, and a distance of 500 meters for the total length. These distances correspond to the distances D3 and D4 as shown in Figure 2–3.

Note that the “NT configured” MC145574 should be placed in the adaptive timing mode for this configuration. This is achieved by holding the FIX pin low.

2.5 BRANCHED PASSIVE BUS OPERATION

A wiring configuration which has somewhat similar characteristics to those of the “extended passive bus” is known as the “branched passive bus” and is shown in Figure 2–4. In this configuration the branching occurs at the end of the bus. The branching occurs after a distance D1 from the NT. The distance D5 corresponds to the maximum separation between the TEs.

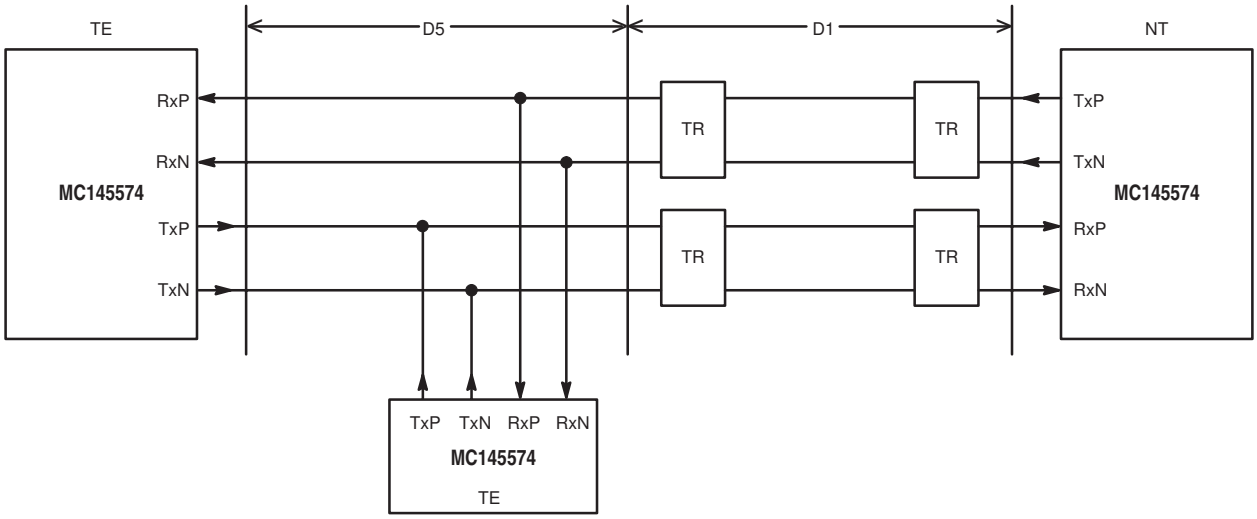

Figure 2–4. Branched Passive Bus

2.6 NT1 STAR MODE OF OPERATION

A wiring configuration which may be used to support multiple T interfaces is known as the “NT1 Star mode of operation.” This mode of operation is supported by the MC145574. This mode is described in Section 11. Note that the NT1 Star mode contains multiple NTs. Each of these NTs can be connected to either a passive bus (short, extended, or branched) or to a single TE.

3

ACTIVATION/DEACTIVATION OF S/T TRANSCEIVER

3.1 INTRODUCTION

CCITT I.430, ETSI ETS 300012, and ANSI T1.605 define five information states for the S/T transceiver. When the NT is in the fully operational state, it transmits INFO 4. When the TE is in the fully operational state, it transmits INFO 3. INFO 1 is transmitted by the TE when it wants to wake up the NT. INFO 2 is transmitted by the NT when it wants to wake up the TE, or in response to the TE's transmitted INFO 1. These states cause unique patterns of symbols to be transmitted over the S/T–interface. Only when the S/T loop is in the fully activated state are the 2B+D channels of data transmitted over the interface.

3.2 TRANSMISSION STATES FOR NT MODE S/T TRANSCEIVER

When configured as an NT, an S/T transceiver can be in any of the following transmission states shown in Table 3–1.

Table 3–1. NT Mode Transmission States

Information State	Description
INFO 0	The NT transmits 1s in every bit position. This corresponds to no signal being transmitted.
INFO 2	The NT sets its B1, B2, D, and E channels to 0. The A bit is set to 0. (See Sections 3.12.1 and 3.12.2.)
INFO 4	INFO 4 corresponds to frames containing operational data on the B1, B2, D, and E channels. The A bit is set to 1.

3.3 TRANSMISSION STATES FOR TE MODE S/T TRANSCEIVER

When configured as a TE, an S/T transceiver can be in any of the following transmission states shown in Table 3–2.

Table 3–2. TE Mode Transmission States

Information State	Description
INFO 0	The TE transmits 1s in every bit position. This corresponds to no signal being transmitted.
INFO 1	The TE transmits a continuous signal with the following pattern: positive 0, negative 0, six 1s. This signal is asynchronous to the NT.
INFO 3	INFO 3 corresponds to frames containing operational data on the B1, B2, and D channels. If INFO 4 or INFO 2 is being received, INFO 3 will be synchronized to it.

3.4 ACTIVATION OF S/T LOOP BY NT

The NT activates the loop by transmitting INFO 2 to the TE(s). This is accomplished in the MC145574 by setting NR2(3) to a 1 (see Section 3.12.3). Note that this bit is internally reset to 0 after the internal activation state machine has recognized its active transition.

The TE on receiving INFO 2 synchronizes to it and transmits back INFO 3 to the NT. The NT, on receiving INFO 3 from the TE, responds with INFO 4, thus activating the loop.

3.5 ACTIVATION OF S/T LOOP BY TE

The TE activates an inactive loop by transmitting INFO 1 to the NT. This is accomplished in the MC145574 by setting NR2(3) to a 1. Note that this bit is internally reset to 0 after the internal activation state machine has recognized its active transition.

The NT, upon detecting INFO 1 from the TE, responds with INFO 2. The TE, upon receiving a signal from the NT, ceases transmission of INFO 1, reverting to transmitting INFO 0. After synchronizing to the received signal and having fully verified that it is INFO 2, the TE responds with INFO 3, thus activating the loop.

3.6 ACTIVATION PROCEDURES IGNORED

The MC145574 has the capability of being forced into the highest transmission state. This is accomplished by setting BR7(7) to a 1. Thus when this bit is set in the NT, it forces the NT to transmit INFO 4. Correspondingly, in the TE, setting this bit to 1 forces the TE to transmit INFO 3.

Note that CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specifications allow a TE to be activated by reception of INFO 4, without having to go through the intermediate handshaking. This is to allow for the situation where a TE is connected to an already active loop.

However, an NT can not be activated by a TE sending it INFO 3, without going through the intermediate INFO 1, INFO 2, INFO 3, and INFO 4 states.

This “Activation Procedures Ignored” feature is provided for test purposes, allowing the NT to forcibly activate the TE(s). In the TE, the forced transmission of INFO 3 enables verification of the TEs operation.

3.7 FRAME SYNC

3.7.1 NT Mode

When the S/T transceiver in the NT mode is receiving INFO 3 from the TE(s) and has achieved frame synchronization, it sets the FSYNC status bit NR1(0) high.

3.7.2 TE Mode

When the TE is receiving either INFO 2 or INFO 4 from the NT, and has achieved frame synchronization, the MC145574 internally sets the SCP nibble bit, NR1(0). NR1(0) performs this function in both the NT and TE modes, for the MC145574.

3.8 ACTIVATION INDICATION

NR1(3), the activation indication bit, is used to signify that the loop is fully active. When the MC145574 is configured as an NT, this corresponds to the NT transmitting INFO 4 and receiving INFO 3. When the MC145574 is configured as a TE, this corresponds to it transmitting INFO 3 and receiving INFO 4. When the loop is in the fully active state, NR1(3) is internally set high.

3.9 NR1(2) — ERROR INDICATION (EI)

NR1(2) is set by the MC145574 S/T transceiver to indicate an error condition has been detected by the activation state machine of the transceiver, as outlined in CCITT I.430, ETSI ETS 300012, and ANSI T1.605. The low–to–high level transition of the EI bit corresponds to the EI1 error indication reporting, while the high–to–low level transition of the EI bit corresponds to the EI2 error indication reporting recovery. Note that NR1(2) is a read only bit.

3.10 DEACTIVATION PROCEDURES

CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specifications dictate that only an NT can deactivate the S/T loop. Intuitively, this has to be the case because in a passive bus if one TE sends INFO 0, seeking to deactivate the loop, the other TE's INFO 3 simply overrides it.

An NT transmits INFO 0 to the TE(s) when it wishes to deactivate the S/T loop. This is done by setting NR2(2) (Deactivation Request) to a 1. Note that this bit is internally reset to 0 after the internal activation state machine has recognized its active transition.

3.11 INITIAL STATE OF B1 AND B2 CHANNELS

3.11.1 NT

When the MC145574 is configured as an NT, NR5(3:2) corresponds to "IDLE B1 channel on S/T loop", and "IDLE B2 channel on S/T loop", respectively. The device comes out of a hardware or software reset with these two bits reset to 0. Thus, the NT comes out of reset with the B1 and B2 channels enabled. When the NT is transmitting INFO 4, data on the B1 and B2 IDL2 timeslots will be modulated onto the S/T loop. Setting either of these nibble bits in the NT mode will idle the corresponding B channel on the S/T loop. Note that putting a B channel in the idle mode affects only the transmitted B channel. The demodulated B data is still transmitted out on IDL2 Tx, in accordance with the IDL2 specification.

3.11.2 TE

When the MC145574 is configured as a TE, NR5(3:2) corresponds to "ENABLE B1 channel on S/T loop," and "ENABLE B2 channel on S/T loop," respectively. The device comes out of a hardware or software reset with these two bits reset to 0. Thus, the TE comes out of reset with the B1 and B2 channels disabled. When the TE is transmitting INFO 3, data on the B1 and B2 IDL2 timeslots is not modulated onto the S/T loop. Setting either of these bits enables the modulation of the corresponding B channel onto the S/T loop.

Note that although the TE comes out of reset with both B channels in the idle mode, this only affects the modulation path. Demodulated data is still transmitted on D_{out}.

3.12 ADDITIONAL NOTES

3.12.1 M and N Parameters

For conformance qualification procedures, it is often necessary to state the values of M and N, where:

M is the number of successive good S0 frames for frame synchronization, and
N is the number of successive bad S0 frames for frame loss.

For the MC145574, M = 5 and N = 3.

3.12.2 Echo Channel

The NT demodulates the 2B+D data received from the TE(s). In addition to passing this data onto the network, the NT echoes the D channel data back to the TE(s) using the echo channel. This echo channel is monitored by the TEs and used in the D channel contention algorithm. For a detailed description, refer to Section 11.