Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Power management integrated circuit (PMIC) for i.MX 7 & i.MX 6SL/SX/UL

PF3000

POWER MANAGEMENT

EP SUFFIX
98ASA00719D
48 QFN 7.0 X 7.0

ES SUFFIX
98ASA00933D
48 QFN 7.0 X 7.0

The PF3000 is a power management integrated circuit (PMIC) designed specifically for use with the NXP i.MX 7 and i.MX 6SL/SX/UL application processors. With up to four buck converters, six linear regulators, RTC supply, and coin-cell charger, the PF3000 can provide power for a complete system, including applications processors, memory, and system peripherals. This device is powered by SMARTMOS technology.

Features:

- Four adjustable high efficiency buck regulators: 1.75 A, 1.5 A, 1.25 A, 1.0 A
  - Selectable modes: PWM, PFM, APS
- 5.0 V, 600 mA boost regulator with PFM or auto mode
- Six adjustable general purpose linear regulators
- Input voltage range: 2.8 V to 4.5 V or 3.7 V to 5.5 V
- OTP (One Time Programmable) memory for device configuration
  - Programmable start-up sequence and timing
  - Selectable output voltage, frequency, soft start
- I^2C control
- Coin cell charger and always ON RTC supply
- DDR reference voltage
- -40 °C to +125 °C operating junction temperature

Applications:

- Tablets
- eReaders
- Wearables
- POS terminals
- Industrial control
- Medical monitoring
- Home automation
- Home security/energy management

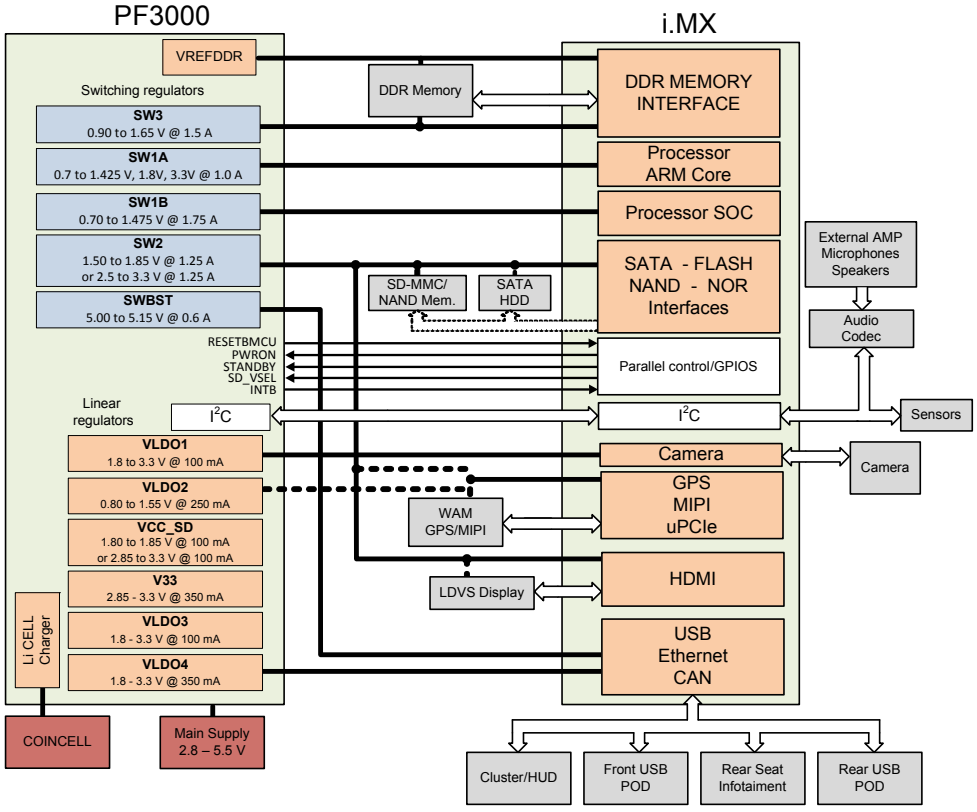

Figure 1. PF3000 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table of Contents

1 Orderable parts

The PF3000 is available with pre-programmed OTP memory configurations. The devices are identified using the program codes from Table 1. Details of the OTP programming for each device can be found in Table 42.

Table 1. Orderable part variations

Part number	Temperature (T_A)	Package	Programming options	Notes
MC32PF3000A0EP	-40 °C to 85 °C (For use in Consumer applications)	98ASA00719D, 48 QFN 7.0 mm x 7.0 mm with exposed pad	0 - Not programmed	(1), (2)
MC32PF3000A1EP			1 (i.MX 7 with DDR3L)	
MC32PF3000A2EP			2 (i.MX 7 with LPDDR3)	
MC32PF3000A3EP			3 (i.MX 6SX with DDR3L)	
MC32PF3000A4EP			4 (i.MX 6SX with DDR3)	
MC32PF3000A5EP			5 (i.MX 6SL with LPDDR2)	
MC32PF3000A6EP			6 (i.MX 6UL with LPDDR2)	
MC32PF3000A7EP			7 (i.MX 6UL with DDR3L)	
MC32PF3000A8EP			8 (i.MX 6UL with DDR3)	
MC33PF3000A0ES	-40 °C to 105 °C (For use in Automotive applications)	98ASA00933D, 48 QFN 7.0 mm x 7.0 mm WF-type (wettable flank)	0 - Not programmed	(1), (2)
MC33PF3000A3ES			3 (i.MX 6SX with DDR3L)	
MC33PF3000A4ES			4 (i.MX 6SX with DDR3)	
MC33PF3000A5ES			5 (i.MX 6SL with LPDDR2)	
MC33PF3000A6ES			6 (i.MX 6UL with LPDDR2)	
MC33PF3000A7ES			7 (i.MX 6UL with DDR3L)	
MC34PF3000A0EP	-40 °C to 105 °C (For use in Industrial applications)	98ASA00719D, 48 QFN 7.0 mm x 7.0 mm with exposed pad	0 - Not programmed	(1), (2)
MC34PF3000A1EP			1 (i.MX 7 with DDR3L)	
MC34PF3000A2EP			2 (i.MX 7 with LPDDR3)	
MC34PF3000A3EP			3 (i.MX 6SX with DDR3L)	
MC34PF3000A4EP			4 (i.MX 6SX with DDR3)	
MC34PF3000A5EP			5 (i.MX 6SL with LPDDR2)	
MC34PF3000A6EP			6 (i.MX 6UL with LPDDR2)	
MC34PF3000A7EP			7 (i.MX 6UL with DDR3L)	
MC34PF3000A8EP			8 (i.MX 6UL with DDR3)	

Notes
1. For tape and reel, add an R2 suffix to the part number.
2. The programming options specified in this table are reference for customer application. The part number selection should match the board power tree design. Table 42 provides details of the OTP programming for each device.

2 General description

The PF3000 is the power management integrated circuit (PMIC) designed primarily for use with NXP's i.MX 7 series of multi-media application processors. It is also capable of providing full power solution to i.MX 6SL/SX/UL processors.

2.1 Features

This section summarizes the PF3000 features.

- Input voltage range to PMIC: 2.8 V to 4.5 V, or 3.7 V to 5.5 V [(3)]
  - Buck regulators
    - Configurable three to four channels
    - SW1A/B, 2.75 A (single); 0.7 V to 1.425 V, 1.8 V, 3.3 V
    - SW1A, 1.0 A (independent); 0.7 V to 1.425 V, 1.8 V, 3.3 V
    - SW1B 1.75 A (independent); 0.7 V to 1.475 V
    - SW2, 1.25 A; 1.50 V to 1.85 V or 2.50 V to 3.30 V
    - SW3, 1.5 A; 0.90 V to 1.65 V
    - Dynamic voltage scaling
    - Modes: PWM, PFM, APS
    - Programmable output voltage
    - Programmable current limit
    - Programmable soft start sequence
    - Programmable PWM switching frequency
  - Boost regulator
    - SWBST, 5.0 to 5.15 V, 0.6 A, OTG support
    - Modes: PFM and Auto
    - OCP fault interrupt
  - LDOs
    - VCC_SD, 1.8 V to 1.85 V or 2.85 V to 3.30 V, 100 mA based on SD_VSEL
    - V33, 2.85 V to 3.30 V, 350 mA
    - VLDO1, 1.8 V to 3.3 V, 100 mA
    - VLDO2, 0.80 V to 1.55 V, 250 mA
    - VLDO3, 1.8 V to 3.3 V, 100 mA
    - VLDO4, 1.8 V to 3.3 V, 350 mA
- Always ON RTC Regulator/Switch VSNVS 3.0 V, 1.0 mA
- DDR memory reference voltage, VREFDDR, 0.5 V to 0.9 V, 10 mA
- OTP (One time programmable) memory for device configuration, user-programmable start-up sequence and timing
- Battery backed memory including coin cell charger
- I^2C interface
- User programmable standby, sleep/LPSR, and Off modes

Notes

3. 2.8 V to 4.5 V when VIN is used at input. 3.7 V to 5.5 V when VPWR is used as input.

2.2 Functional block diagram

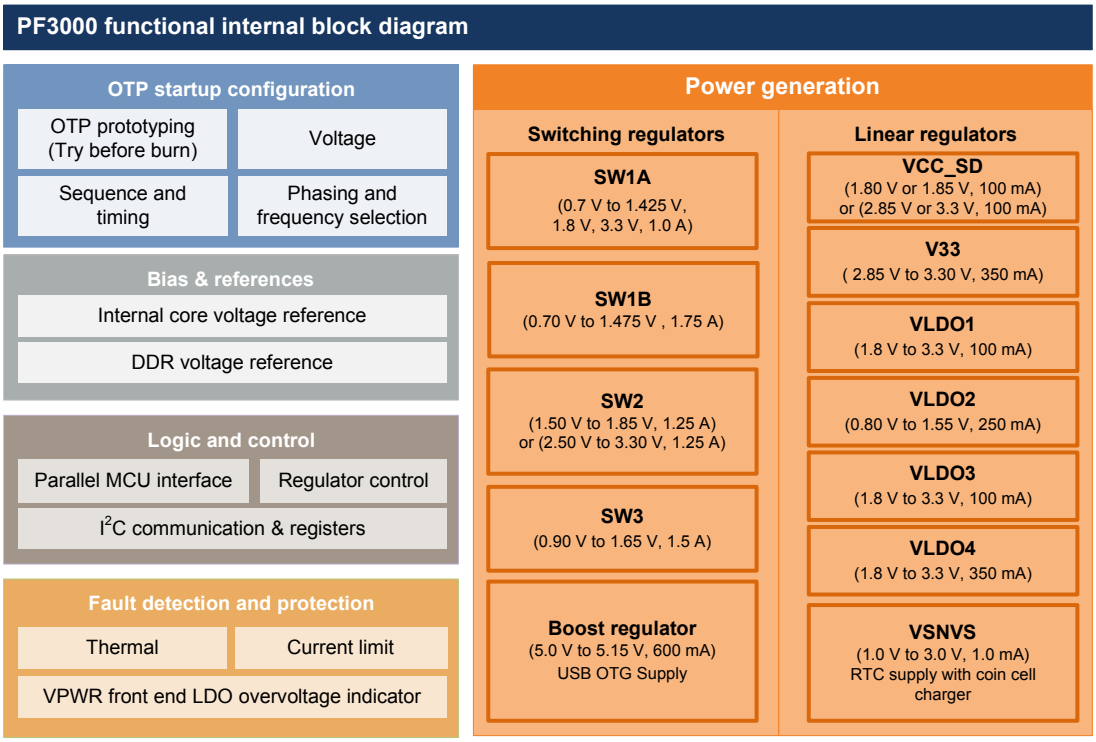

Figure 2. Functional block diagram

3 Internal block diagram

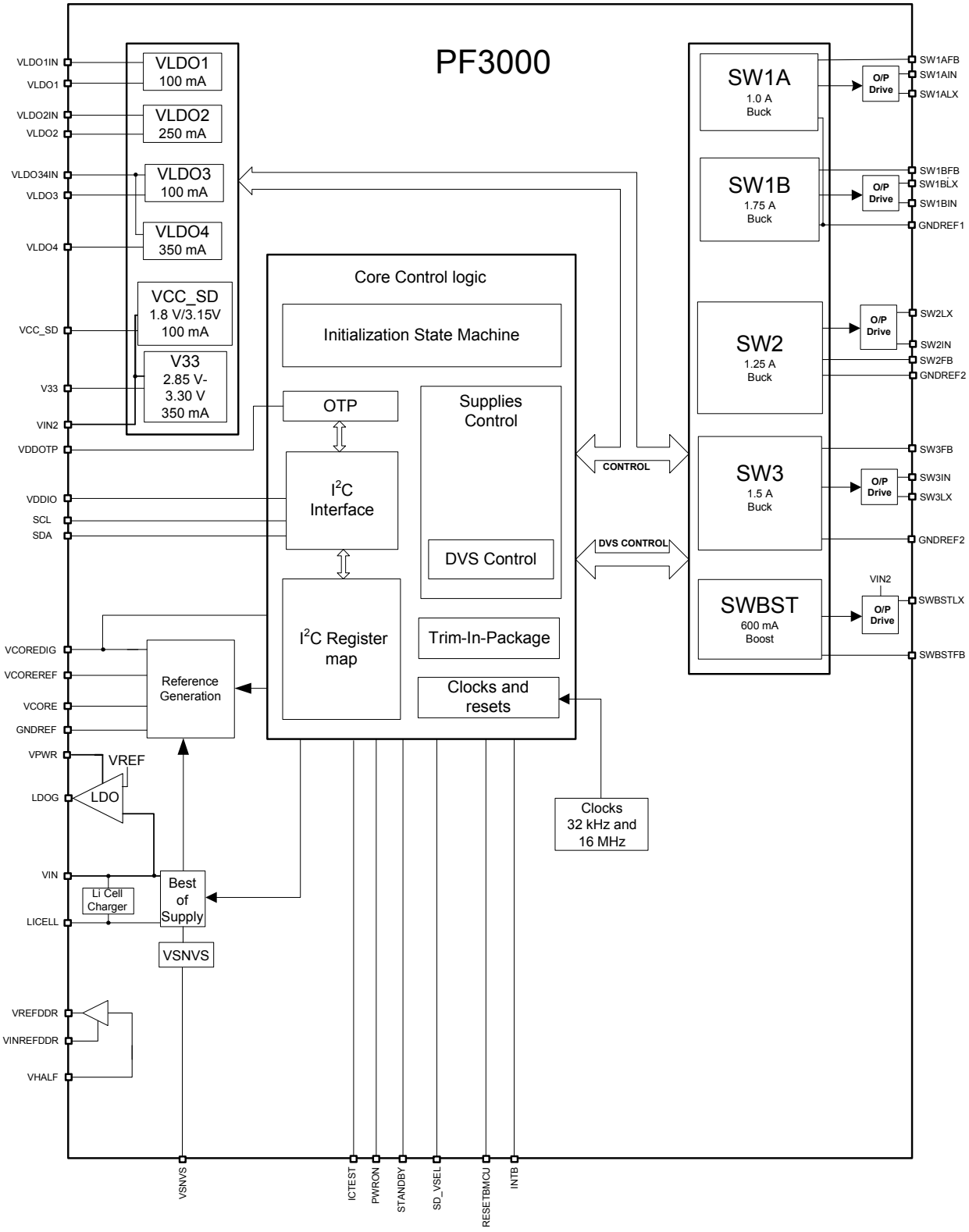

Figure 3. PF3000 simplified internal block diagram

4 Pin connections

4.1 Pinout diagram

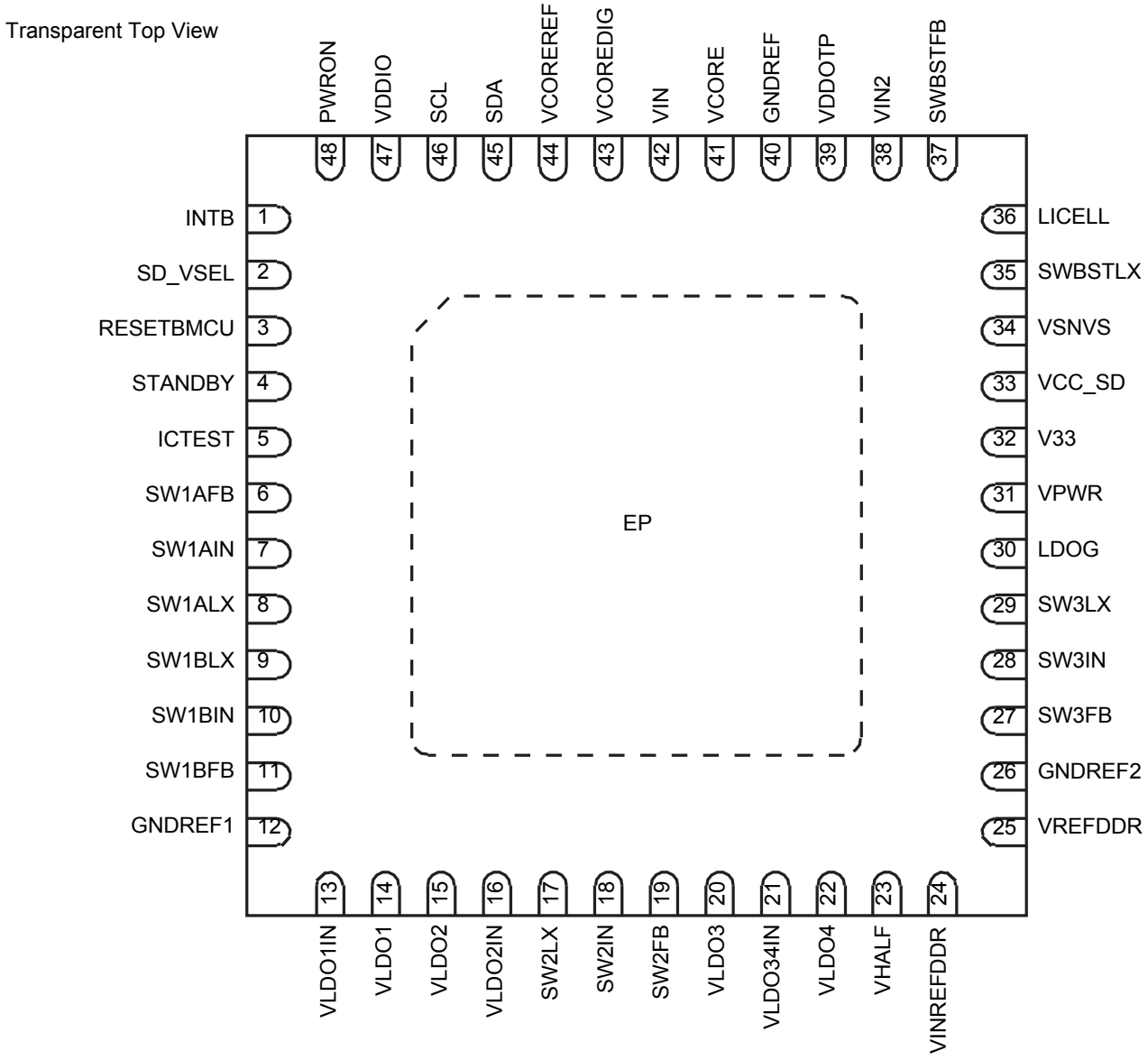

Figure 4. Pinout diagram

4.2 Pin definitions

Table 2. Pin definitions

Pin number	Pin name	Pin function	Type	Definition
1	INTB	O	Digital	Open drain interrupt signal to processor
2	SD_VSEL	I/O	Digital	Input from i.MX processor to select VCC_SD regulator voltage • SD_VSEL=0, VCC_SD = 2.85 V to 3.3 V • SD_VSEL= 1, VCC_SD = 1.8 V to 1.85 V
3	RESETBMCU	O	Digital	Open drain reset output to processor
4	STANDBY	I	Digital	Standby input signal from processor
5	ICTEST	I	Digital and Analog	Reserved pin. Connect to GND in application
6	SW1AFB (4)	I	Analog	SW1A output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitance or near the load, if possible for best regulation
7	SW1AIN (4)	I	Analog	Input to SW1A regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible
8	SW1ALX (4)	O	Analog	Switcher 1A switch node connection. Connect to SW1A inductor when used in SW1A independent mode. Connect to SW1BLX and connect to SW1AB inductor when using SW1A/B as a single regulator
9	SW1BLX (4)	O	Analog	Switcher 1B switch node connection. Connect to SW1B inductor when used in SW1B independent mode. Connect to SW1ALX and connect to SW1AB inductor when using SW1A/B as a single regulator
10	SW1BIN (4)	I	Analog	Input to SW1B regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible
11	SW1BFB (4)	I	Analog	SW1B output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitor or near the load, if possible for best regulation
12	GNDREF1	GND	GND	Ground reference for SW1A/B. Connect to GND. Keep away from high current ground return paths
13	VLDO1IN	I	Analog	VLDO1 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible
14	VLDO1	O	Analog	VLDO1 regulator output. Bypass with a 2.2 µF ceramic output capacitor
15	VLDO2	O	Analog	VLDO2 regulator output. Bypass with a 4.7 µF ceramic output capacitor
16	VLDO2IN	I	Analog	VLDO2 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible
17	SW2LX (4)	O	Analog	Switcher 2 switch node connection.Connect to SW2 inductor
18	SW2IN (4)	I	Analog	Input to SW2 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible
19	SW2FB (4)	I	Analog	SW2 output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitor or near the load, if possible for best regulation
20	VLDO3	O	Analog	VLDO3 regulator output. Bypass with a 2.2 µF ceramic output capacitor
21	VLDO34IN	I	Analog	VLDO3 and VLDO4 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible
22	VLDO4	O	Analog	VLDO4 regulator output. Bypass with a 2.2 µF ceramic output capacitor
23	VHALF	I	Analog	Half supply reference for VREFDDR. Bypass with 0.1 µF to ground.
24	VINREFDDR	I	Analog	VREFDDR regulator input. Connect a 0.1 µF capacitor between VINREFDDR and VHALF pin. Ensure there is at least 1.0 µF net capacitance from VINREFDDR to ground
25	VREFDDR	O	Analog	VREFDDR regulator output.Bypass with 1.0 µF to ground

Table 2. Pin definitions (continued)

26	GNDREF2	GND	GND	Reference ground for SW2 and SW3 regulators. Connect to GND. Keep away from high current ground return paths
27	SW3FB (4)	I	Analog	SW3 output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitor or near the load, if possible for best regulation
28	SW3IN (4)	I	Analog	Input to SW3 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible
29	SW3LX (4)	O	Analog	Switcher 3 switch node connection. Connect the SW3 inductor
30	LDOG	O	Analog	Connect to gate of front-end LDO external pass P-MOSFET. Leave floating if VPWR LDO is not used
31	VPWR	I	Analog	Input to optional front-end VPWR LDO for systems with input voltage > 4.5 V
32	V33	O	Analog	V33 regulator output. Bypass with a 4.7 µF ceramic output capacitor
33	VCC_SD	O	Analog	Output of VCC_SD regulator. Bypass with a 2.2 µF ceramic output capacitor.
34	VSNVS	O	Analog	VSNVS regulator/switch output. Bypass with 0.47 µF capacitor to ground.
35	SWBSTLX (4)	I/O	Analog	SWBST switch node connection. Connect to SWBST inductor and anode of Schottky diode
36	LICELL	I/O	Analog	Coin cell supply input/output. Bypass with 0.1 µF capacitor. Connect to optional coin cell.
37	SWBSTFB (4)	I	Analog	SWBST output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitor
38	VIN2	I	Analog	Input to VCC_SD, V33 regulators and SWBST control circuitry. Connect to VIN rail and bypass with 10 µF capacitor
39	VDDOTP	I	Digital & Analog	Supply to program OTP fuses. Connect VDDOTP to GND during normal application
40	GNDREF	GND	GND	Ground reference for IC core circuitry. Connect to ground. Keep away from high current ground return paths
41	VCORE	O	Analog	Internal analog core supply. Bypass with 1 µF capacitor to ground
42	VIN	I	Analog	Main IC supply. Bypass with 1.0 µF capacitor to ground. Connect to system input supply if voltage ≤ 4.5 V. Connect to drain of external PFET when VPWR LDO is used for systems with input voltage > 4.5 V
43	VCOREDIG	O	Analog	Internal digital core supply. Bypass with 1.0 µF capacitor to ground
44	VCOREREF	O	Analog	Main band gap reference. Bypass with 220 nF capacitor to ground
45	SDA	I/O	Digital	I^2C data line (open drain). Pull up to VDDIO with a 4.7 kΩ resistor
46	SCL	I	Digital	I^2C clock. Pull up to VDDIO with a 4.7 kΩ resistor
47	VDDIO	I	Analog	Supply for I^2C bus. Bypass with 0.1 µF ceramic capacitor. Connect to 1.7 to 3.6 V supply. Ensure that VDDIO is always lesser than or equal to VIN
48	PWRON	I	Digital	Power ON/OFF input from processor
-	EP	GND	GND	Expose pad. Functions as ground return for buck and boost regulators. Tie this pad to the inner and external ground planes through vias to allow effective thermal dissipation

Notes

4. Unused switching regulators should be connected as follows: Pins SWxLX and SWxFB should be unconnected and Pin SWxIN should be connected to VIN with a 0.1 µF bypass capacitor.

5 General product characteristics

5.1 Absolute maximum ratings

Table 3. Absolute maximum voltage ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause malfunction or permanent damage to the device. The detailed maximum voltage rating per pin can be found in the pin list section.

Symbol	Description	Value	Unit	Notes
Electrical ratings				
VPWR, ICTEST, LDOG, SWBSTLX	–	-0.3 to 7.5	V	
VIN, VIN2, VLDO1IN, SW1AIN, SW1BIN, SW2IN, SW3IN, SW1ALX, SW1BLX, SW2LX, SW3LX	–	-0.3 to 4.8	V	
VDDOTP	OTP programming input supply voltage	-0.3 to 10.0	V	(5)
SWBSTFB	Boost switcher feedback	-0.3 to 5.5	V	
INTB, SD_VSEL, RESETBMCU, STANDBY, SW1AFB, SW1BFB, SW2FB, SW3FB, VLDO1, VLDO2IN, VLDO3, VLDO34IN, VLDO4, VHALF, VINREFDDR, VREFDDR, V33, VCC_SD, VSNVS, LICELL, VCORE, SDA, SCL, VDDIO, PWRON	–	-0.3 to 3.6	V	
VLDO2	VLDO2 linear regulator output	-0.3 to 2.5	V	
VCOREDIG	Digital core supply voltage output	-0.3 to 1.65	V	
VCOREREF	Bandgap reference voltage output	-0.3 to 1.5	V	
V_{ESD}	ESD ratings • Human body model • Charge device model	 ±2000 ±500	V	(6)

Notes

5. 10 V maximum voltage rating during OTP fuse programming. 7.5 V maximum DC voltage rated otherwise.
6. ESD testing is performed in accordance with the human body model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the charge device model (CDM), robotic (C_{ZAP} = 4.0 pF).

5.2 Thermal Characteristics

Table 4. Thermal ratings

Symbol	Description (rating)	Min.	Max.	Unit	Notes
Thermal Ratings					
T_A	Ambient operating temperature range • Industrial version • Consumer version	 -40 -40	 105 85	°C	
T_J	Operating junction temperature range	-40	125	°C	(7)
T_{ST}	Storage temperature range	-65	150	°C	
T_{PPRT}	Peak package reflow temperature	–	(9)	°C	(8) (9)
QFN48 thermal resistance and package dissipation ratings					
$R_{\theta JA}$	Junction to ambient, natural convection • Four layer board (2s2p) • Eight layer board (2s6p)	 – –	 24 15	°C/W	(10) (11) (12)
$R_{\theta JB}$	Junction to board	–	11	°C/W	(13)
$R_{\Theta JCBOTTOM}$	Junction to case bottom	–	1.4	°C/W	(14)
ΨJT	Junction to package top • Natural convection	–	1.3	°C/W	(15)

Notes

7. Do not operate beyond 125 °C for extended periods of time. Operation above 150 °C may cause permanent damage to the IC. See Thermal Protection Thresholds for thermal protection features.
8. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
9. NXP's package reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For peak package reflow temperature and moisture sensitivity levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts, and review parametrics.
10. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
11. The Board uses the JEDEC specifications for thermal testing (and simulation) JESD51-7 and JESD51-5.
12. Per JEDEC JESD51-6 with the board horizontal.
13. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
14. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
15. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters (Ψ) are not available, the thermal characterization parameter is written as Psi-JT.

5.3 Current consumption

The current consumption of the individual blocks is described in detail in the following table.

Table 5. Current consumption summary

T_A= -40 °C to 105 °C, V_{PWR}= 0 V (External pass FET is not populated), V_{IN} = 3.6 V, V_{DDIO} = 1.7 V to 3.6 V, L_{ICELL} = 1.8 V to 3.3 V, V_{SNVS} = 3.0 V, typical external component values, unless otherwise noted. Typical values are characterized at VIN = 3.6 V, V_{PWR} = 0 V, V_{DDIO} = 3.3 V, L_{ICELL} = 3.0 V, V_{SNVS} = 3.0 V and 25 °C, unless otherwise noted.

Mode	PF3000 conditions	System conditions	Typ.	Max.	Unit	Notes
Coin cell	VSNVS from LICELL, All other blocks off, V_{IN} = 0.0 V	No load on VSNVS	4.0	7.0	µA	(16) (17)
Off	VSNVS from VIN or LICELL Wake-up from PWRON active 32 kHz RC on All other blocks off VIN ≥ UVDET	No load on VSNVS, PMIC able to wake-up	16	25	µA	(16) (17)
Sleep LPSR	VSNVS from VIN Wake-up from PWRON active Trimmed reference active SW3 PFM. All other regulators off. Trimmed 16 MHz RC off 32 kHz RC on VREFDDR disabled	No load on any of the regulators.	130 (16) 200 (19)	220 (16)	µA	(18)
	LDO1 & LDO3 activated in addition to SW3	No load on any of the regulators.	170 (16) 260 (19)	248 (16)	µA	(18)
Standby	VSNVS from either VIN or LICELL SW1A in PFM SW1B in PFM SW2 in PFM SW3 in PFM SWBST off Trimmed 16 MHz RC enabled Trimmed reference active VLDO1-4 enabled V33 enabled VCC_SD enabled VREFDDR enabled	No load on any of the regulators.	297	450	µA	(18)
ON	VSNVS from VIN SW1A in APS SW1B in APS SW2 in APS SW3 in APS SWBST off Trimmed 16 MHz RC enabled Trimmed reference active VLDO1-4 enabled V33 enabled VCC_SD enabled VREFDDR enabled	No load on any of the regulators.	1.2		mA	

Notes

16. At 25 °C only.
17. When V_{IN} is below the UVDET threshold, in the range of 1.8 V ≤ V_{IN} < 2.65 V, the quiescent current increases by 50 µA, typically.
18. For PFM operation, headroom should be 300 mV or greater.
19. At 105 °C only.

5.4 Electrical characteristics

Table 6. Electrical characteristics – front-end input LDO

All parameters are specified at T_A = -40 °C to 105 °C, V_{PWR} = 5.0 V, V_{IN} = 4.4 V, I_{VIN} = 300 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{PWR} = 5.0 V, V_{IN} = 4.4 V, I_{VIN} = 300 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Front end input LDO (VPWR LDO)						
V_{PWR}	Operating input voltage • In regulation • In dropout operation	 4.6 3.7	 – –	 5.5 4.6	V	(20)
V_{IN}	On mode output voltage, 4.6 V < V_{PWR} < 5.5 V, 0.0 mA < I_{VIN} < 3000 mA	4.3	4.4	4.55	V	
I_{VIN}	Operating load current at VIN, 3.7 V < V_{PWR} < 5.5 V	0.0	–	3.0	A	
I_{LDOGQ}	ON mode quiescent current, no load,	–	5.0	10	mA	
V_{IN}	Low-power mode output voltage, 4.6 V < V_{PWR} < 5.5 V 0.0 mA < I_{VIN} < 1.0 mA	3.7		4.5	V	
V_{IN_OFF}	Off mode output voltage, (CL = 100 µF) 4.6 V < V_{PWR} < 5.5 V, 0.0 mA < I_{VIN} < 35 µA	3.2		4.8	V	
I_{LDOQLP}	Low-power mode quiescent current, no load (Standby/Sleep/LPSR states)	–	150	300	µA	
V_{PWRUV}	VPWR undervoltage threshold (upon undervoltage condition the external pass FET is turned off)	3.1	–	3.7	V	
V_{PWROV}	VPWR overvoltage threshold (upon overvoltage condition interrupt is asserted at INTB)	5.5	–	6.5	V	
$I_{VINUVILIMIT}$	VPWR LDO current limit under VIN short-circuit (V_{IN} < UVDET)	–	–	300	mA	
$I_{VINLEAKAGE}$	Reverse leakage current from VIN to VPWR, No external pass FET, VPWR is grounded, device is in OFF state	–	–	1.0	µA	
$I_{VPWROFF}$	VPWR LDO Off mode quiescent current	–	–	75	µA	(21)

Notes

20. While the front end LDO can handle spikes up to 7.5 V at VPWR for as long as 200 µs, the circuit is not expected to be continuously operated when VPWR is above 5.5 V.
21. This specification gives the leakage current in the VPWR LDO block. Total OFF mode current includes the quiescent current from the other blocks as specified in Table 5.

Table 7. Static electrical characteristics – SW1

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW1xIN} = 3.6 V, V_{SW1x} = 1.2 V, I_{SW1x} = 100 mA, typical external component values, f_{SW1x} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW1xIN} = 3.6 V, V_{SW1x} = 1.2 V, I_{SW1x} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW1A/B (single phase)						
V_{SW1AIN} V_{SW1BIN}	Operating input voltage	2.8	–	4.5	V	(22), (23)
V_{SW1AB}	Nominal output voltage	–	Table 53	–	V	
$V_{SW1ABACC}$	Output voltage accuracy • PWM, APS, 2.8 V < V_{SW1xIN} < 4.5 V, 0 < I_{SW1AB} < 2.75 A 0.7 V ≤ V_{SW1AB} ≤ 1.2 V • PFM, APS, 2.8 V < V_{SW1xIN} < 4.5 V, 0 < I_{SW1AB} < 2.75A 1.225 V < V_{SW1AB} < 1.425 V • PFM, steady state, 2.8 V < V_{SW1xIN} < 4.5 V, 0 < I_{SW1AB} < 150 mA 1.8 V ≤ V_{SW1AB} ≤ 1.425 V • PWM, APS, 2.8 V < V_{SW1xIN} < 4.5 V, 0 < I_{SW1AB} < 2.75A 1.8 V < V_{SW1AB} < 3.3 V • PFM, steady state, 2.8 V < V_{SW1xIN} < 4.5 V, 0 < I_{SW1AB} < 150 mA 1.8 V ≤ V_{SW1AB} ≤ 3.3 V	 -25 -25 -45 -6.0 -6.0	 – 	 25 35 45 6.0 6.0	 mV mV mV % %	
I_{SW1AB}	Rated output load current, • 2.8 V ≤ V_{SW1xIN} ≤ 4.5 V, 0.7 V < V_{SW1AB} < 1.425 V, 1.8V, 3.3V	2750	–	–	mA	
I_{SW1ABQ}	Quiescent current • PFM mode • APS mode	 – –	 22 300	 – –	 µA	
$I_{SW1ABLIM}$	Current limiter peak current detection , current through inductor • SW1xILIM = 0 • SW1xILIM = 1	 3.5 2.6	 5.5 4.0	 7.5 5.4	 A	
ΔV_{SW1AB}	Output ripple	–	5.0	–	mV	
$R_{SW1ABDIS}$	Discharge resistance	–	600	–	Ω	
Switch mode supply SW1A (independent)						
V_{SW1AIN}	Operating input voltage	2.8	–	4.5	V	(22), (23)
V_{SW1A}	Nominal output voltage	–	Table 53	–	V	
$V_{SW1AACC}$	Output voltage accuracy • PWM, APS, 2.8 V < V_{SW1AIN} < 4.5 V, 0 < I_{SW1A} < 1.0 A 0.7 V ≤ V_{SW1A} ≤ 1.2 V • APS, 3.0 V ≤ V_{SW1AIN} ≤ 3.6 V, 0.01 A < I_{SW1A} < 0.75 A V_{SW1A} = 1.225 V, T_A = 0 °C to 85 °C • PWM, APS, 2.8 V < V_{SW1AIN} < 4.5 V, 0 < I_{SW1A} < 1.0 A 1.225 V < V_{SW1A} ≤ 1.425 V • PFM, steady state, 2.8 V < V_{SW1AIN} < 4.5 V, 0 < I_{SW1A} < 50 mA 0.7 V ≤ V_{SW1A} ≤ 1.425V • PWM, APS, 2.8 V < V_{SW1AIN} < 4.5 V, 0 < I_{SW1A} < 1.0 A 1.8 V ≤ V_{SW1A} ≤ 3.3 V • PFM, steady state, 2.8 V < V_{SW1AIN} < 4.5 V, 0 < I_{SW1A} < 50 mA 1.8 V ≤ V_{SW1A} ≤ 3.3 V	 -25 -25 -25 -45 -6.0 -6.0	 – 	 25 25 35 45 6.0 6.0	 mV mV mV % %	
I_{SW1A}	Rated output load current 2.8 V < V_{SW1AIN} < 4.5 V, 0.7 V < V_{SW1A} < 1.425 V, 1.8V, 3.3V	1000	–	–	mA	
Switch mode supply SW1a (independent) (Continued)						
I_{SW1AQ}	Quiescent current • PFM mode • APS mode	 – –	 50 250	 – –	 µA	

Table 7. Static electrical characteristics – SW1 (continued)

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW1xIN} = 3.6 V, V_{SW1x} = 1.2 V, I_{SW1x} = 100 mA, typical external component values, f_{SW1x} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW1xIN} = 3.6 V, V_{SW1x} = 1.2 V, I_{SW1x} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
$I_{SW1ALIM}$	Current limiter peak current detection, current through inductor • SW1AILIM = 0 • SW1AILIM = 1	 1.78 1.3	 2.75 2.0	 3.7 2.7	A	
ΔV_{SW1A}	Output Ripple	–	5.0	–	mV	
$R_{ONSW1AP}$	SW1A P-MOSFET R_{DSON}, at V_{SW1AIN} = 3.3 V	–	265	295	mΩ	
$R_{ONSW1AN}$	SW1A N-MOSFET R_{DSON}, at V_{SW1AIN} = 3.3 V	–	300	370	mΩ	
I_{SW1APQ}	SW1A P-MOSFET leakage current, V_{SW1AIN} = 4.5 V	–	–	10.5	µA	
I_{SW1ANQ}	SW1A N-MOSFET leakage current, V_{SW1AIN} = 4.5 V	–	–	3.5	µA	
$R_{SW1ADIS}$	Discharge resistance	–	600	–	Ω	
Switch mode supply SW1B (independent)						
V_{SW1BIN}	Operating input voltage	2.8	–	4.5	V	(24), (25)
V_{SW1B}	Nominal output voltage	–	Table 53	–	V	
$V_{SW1BACC}$	Output voltage accuracy • PWM, APS, 2.8 V < V_{SW1BIN} < 4.5 V, 0 < I_{SW1B} < 1.75 A 0.7 V < V_{SW1B} < 1.2 V • PWM, APS, 2.8 V < V_{SW1BIN} < 4.5 V, 0 < I_{SW1B} < 1.75 A 1.225 V < V_{SW1B} < 1.475 V • PFM, steady state 2.8 V < V_{SW1BIN} < 4.5 V, 0 < I_{SW1B} < 50 mA 0.7 V < V_{SW1B} < 1.475 V	 -25 -25 -45	 – 	 25 35 45	mV	
I_{SW1B}	Rated output load current 2.8 V < V_{SW1BIN} < 4.5 V, 0.7 V < V_{SW1B} < 1.475 V	1750	–	–	mA	
I_{SW1BQ}	Quiescent current • PFM mode • APS mode	 – –	 50 150	 – –	µA	
$I_{SW1BLIM}$	Current limiter peak current detection, current through inductor • SW1BILIM = 0 • SW1BILIM = 1	 2.4 1.725	 3.50 2.65	 4.725 3.575	A	
ΔV_{SW1B}	Output ripple	–	5.0	–	mV	
$R_{ONSW1BP}$	SW1B P-MOSFET R_{DSON}, at V_{SW1BIN} = 3.3 V	–	195	225	mΩ	
$R_{ONSW1BN}$	SW1B N-MOSFET R_{DSON}, at V_{SW1BIN} = 3.3 V	–	228	295	mΩ	
I_{SW1BPQ}	SW1B P-MOSFET leakage current, V_{SW1BIN} = 4.5 V	–	–	12	µA	
I_{SW1BNQ}	SW1B N-MOSFET leakage current, V_{SW1BIN} = 4.5 V	–	–	4.0	µA	
$R_{SW1BDIS}$	Discharge resistance during OFF mode	–	600	–	Ω	

Notes

22. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
23. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3000 regulator, or external system supply.
24. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
25. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3000 regulator, or external system supply.

Table 8. Dynamic electrical characteristics - SW1

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW1xIN} = 3.6 V, V_{SW1x} = 1.2 V, I_{SW1x} = 100 mA, typical external component values, f_{SW1x} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW1xIN} = 3.6 V, V_{SW1x} = 1.2 V, I_{SW1x} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW1A/B (single phase)						
$V_{SW1ABOSH}$	Start-up overshoot, I_{SW1AB} = 0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{SW1xIN} = 4.5 V, V_{SW1AB} = 1.425 V	–	–	66	mV	
$t_{ONSW1AB}$	Turn-on time, enable to 90% of end value, I_{SW1AB} = 0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{SW1xIN} = 4.5 V, V_{SW1AB} = 1.425 V	–	–	500	µs	
Switch mode supply SW1A (independent)						
$V_{SW1AOSH}$	Start-up overshoot, ISW1A = 0 mA, DVS clk = 25 mV/4.0 µs, V_{IN} = V_{SW1AIN} = 4.5 V, V_{SW1A} = 1.425 V	–	–	66	mV	
t_{ONSW1A}	Turn-on time, enable to 90% of end value, I_{SW1A} = 0 mA, DVS clk = 25 mV/4.0 µs, V_{IN} = V_{SW1AIN} = 4.5 V, V_{SW1A} = 1.425 V	–	–	500	µs	
Switch mode supply SW1B (independent)						
$V_{SW1BOSH}$	Start-up overshoot, I_{SW1B} = 0 mA, DVS clk = 25 mV/4.0 µs, V_{IN} = V_{SW1BIN} = 4.5 V, V_{SW1B} = 1.475 V	–	–	66	mV	
t_{ONSW1B}	Turn-on time, enable to 90% of end value, I_{SW1B} = 0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{SW1BIN} = 4.5 V, V_{SW1B} = 1.475 V	–	–	500	µs	

Table 9. Static electrical characteristics – SW2

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, typical external component values, f_{SW2} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW2						
V_{SW2IN}	Operating input voltage	2.8	–	4.5	V	(26), (27)
V_{SW2}	Nominal output voltage	–	Table 55	–	V	
V_{SW2ACC}	Output voltage accuracy • PWM, APS, 2.8 V ≤ V_{SW2IN} ≤ 4.5 V, 0 ≤ I_{SW2} ≤ 1.25 A • 1.50 V ≤ V_{SW2} ≤ 1.85 V • 2.5 V ≤ V_{SW2} ≤ 3.3 V • PFM, 2.8 V ≤ V_{SW2IN} ≤ 4.5 V, 0 ≤ I_{SW2} ≤ 50 mA • 1.50 V ≤ V_{SW2} ≤ 1.85 V • 2.5 V ≤ V_{SW2} ≤ 3.3 V	 -3.0% -6.0% -6.0% -6.0%	 – – – –	 3.0% 6.0% 6.0% 6.0%	%	
I_{SW2}	Rated output load current, 2.8 V < V_{SW2IN} < 4.5 V, 1.50 V < V_{SW2} < 1.85 V, 2.5 V < V_{SW2} < 3.3 V	1250	–	–	mA	(28)
I_{SW2Q}	Quiescent current • PFM mode • APS mode (low output voltage settings) • APS mode (high output voltage settings, SW2_HI=1)	 – – –	 23 145 305	 – – –	µA	

Notes

26. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
27. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3000 regulator, or external system supply.
28. The higher output voltages available depend on the voltage drop in the conduction path as given by the following equation: (V_{SW2IN} - V_{SW2}) = I_{SW2}* (DCR of Inductor +R_{ONSW2P} + PCB trace resistance).

Table 9. Static electrical characteristics – SW2 (continued)

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, typical external component values, f_{SW2} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW2 (continued)						
I_{SW2LIM}	Current limiter peak current detection, current through inductor • SW2ILIM = 0 • SW2ILIM = 1	 1.625 1.235	 2.5 1.9	 3.375 2.565	A	
ΔV_{SW2}	Output ripple	–	5.0	–	mV	
R_{ONSW2P}	SW2 P-MOSFET R_{DSON} at V_{IN} = V_{SW2IN} = 3.3 V	–	215	245	mΩ	
R_{ONSW2N}	SW2 N-MOSFET R_{DSON} at V_{SW2IN} = V_{SW2IN} = 3.3 V	–	258	326	mΩ	
I_{SW2PQ}	SW2 P-MOSFET leakage current, V_{IN} = V_{SW2IN} = 4.5 V	–	–	10.5	µA	
I_{SW2NQ}	SW2 N-MOSFET leakage current, V_{IN} = V_{SW2IN} = 4.5 V	–	–	3.0	µA	
R_{SW2DIS}	Discharge resistance during OFF mode	–	600	–	Ω	

Table 10. Dynamic electrical characteristics - SW2

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, ISW2 = 100 mA, typical external component values, f_{SW2} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW2						
V_{SW2OSH}	Start-up overshoot, I_{SW2} = 0.0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{SW2IN} = 4.5 V	–	–	66	mV	
t_{ONSW2}	Turn-on time, enable to 90% of end value, I_{SW2} = 0.0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{SW2IN} = 4.5 V	–	–	500	µs	

Table 11. Static electrical characteristics – SW3

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW3IN} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, typical external component values, f_{SW3} = 2.0 MHz. Typical values are characterized at V_{IN} = V_{SW3IN} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW3						
V_{SW3IN}	Operating input voltage	2.8	–	4.5	V	(29), (30)
V_{SW3}	Nominal output voltage	–	Table 57	–	V	
V_{SW3ACC}	Output voltage accuracy • PWM, APS, 2.8 V < V_{SW3IN} < 4.5 V, 0 < I_{SW3} < 1.5 A, 0.9 V < V_{SW3} < 1.65 V • PFM, steady state (2.8 V < V_{SW3IN} < 4.5 V, 0 < I_{SW3} < 50 mA), 0.9 V < V_{SW3} < 1.65 V	 -3.0% -6.0%	 – –	 3.0% 6.0%	%	
I_{SW3}	Rated output load current, 2.8 V < V_{SW3IN} < 4.5 V, 0.9 V < V_{SW3} < 1.65 V, PWM, APS mode	1500	–	–	mA	(31)

Notes

29. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
30. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3000 regulator, or external system supply.
31. The higher output voltages available depend on the voltage drop in the conduction path as given by the following equation: (V_{SW3IN} - V_{SW3}) = I_{SW3}* (DCR of Inductor +R_{ONSW3P} + PCB trace resistance).

Table 11. Static electrical characteristics – SW3 (continued)

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW3IN} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, typical external component values, f_{SW3} = 2.0 MHz. Typical values are characterized at V_{IN} = V_{SW3IN} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW3 (continued)						
I_{SW3Q}	Quiescent current • PFM mode • APS mode	 – –	 50 150	 – –	µA	
I_{SW3LIM}	Current limiter peak current detection, current through inductor • SW3ILIM = 0 • SW3ILIM = 1	 1.95 1.45	 3.0 2.25	 4.05 3.05	A	
ΔV_{SW3}	Output ripple	–	5.0	–	mV	
R_{ONSW3P}	SW3 P-MOSFET R_{DSON} at V_{IN} = V_{SW3IN} = 3.3 V	–	205	235	mΩ	
R_{ONSW3N}	SW3 N-MOSFET R_{DSON} at V_{IN} = V_{SW3IN} = 3.3 V	–	250	315	mΩ	
I_{SW3PQ}	SW3 P-MOSFET leakage current, V_{IN} = V_{SW3IN} = 4.5 V	–	–	12	µA	
I_{SW3NQ}	SW3 N-MOSFET leakage current, V_{IN} = V_{SW3IN} = 4.5 V	–	–	4.0	µA	
R_{SW3DIS}	Discharge resistance during Off mode	–	600	–	Ω	

Table 12. Dynamic electrical characteristics - SW3

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW3IN} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, typical external component values, f_{SW3} = 2.0 MHz. Typical values are characterized at V_{IN} = V_{SW3IN} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{SW3OSH}	Start-up overshoot, I_{SW3} = 0.0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{SW3IN} = 4.5 V	–	–	66	mV	
t_{ONSW3}	Turn-on time, enable to 90% of end value, I_{SW3} = 0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{SW3IN} = 4.5 V	–	–	500	µs	

Table 13. Static electrical characteristics - SWBST

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = $V_{SWBSTIN}$ = 3.6 V, V_{SWBST} = 5.0 V, I_{SWBST} = 100 mA, typical external component values, f_{SWBST} = 2.0 MHz, otherwise noted. Typical values are characterized at V_{IN} = $V_{SWBSTIN}$ = 3.6 V, V_{SWBST} = 5.0 V, I_{SWBST} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameters	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SWBST						
$V_{SWBSTIN}$	Input voltage range	2.8	–	4.5	V	(32), (33)
V_{SWBST}	Nominal output voltage	–	Table 59	–	V	
I_{SWBST}	Continuous load current • 2.8 V ≤ V_{IN} ≤ 3.0 V • 3.0 V ≤ V_{IN} ≤ 4.5 V	 500 600	 – –	 – –	mA	
$V_{SWBSTACC}$	Output voltage accuracy, 2.8 V ≤ V_{IN} ≤ 4.5 V, 0 < I_{SWBST} < $I_{SWBSTMAX}$	-4.0	–	3.0	%	
I_{SWBSTQ}	Quiescent current (auto mode)	–	222	289	µA	

Notes

32. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
33. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3000 regulator, or external system supply.

Table 13. Static electrical characteristics - SWBST (continued)

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = $V_{SWBSTIN}$ = 3.6 V, V_{SWBST} = 5.0 V, I_{SWBST} = 100 mA, typical external component values, f_{SWBST} = 2.0 MHz, otherwise noted. Typical values are characterized at V_{IN} = $V_{SWBSTIN}$ = 3.6 V, V_{SWBST} = 5.0 V, I_{SWBST} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameters	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SWBST (continued)						
ΔV_{SWBST}	Output ripple, 2.8 V ≤ V_{IN} ≤ 4.5 V, 0 < I_{SWBST} < $I_{SWBSTMAX}$, excluding reverse recovery of Schottky diode	–	–	120	mVp-p	
$I_{SWBSTLIM}$	Peak Current Limit	1400	2200	3200	mA	(34)
$R_{DS(on)BST}$	MOSFET on resistance	–	206	306	mΩ	
$I_{SWBSTHSQ}$	NMOS Off leakage, V_{SWBST} = 4.5 V, SWBSTMODE [1:0] = 00	–	1.0	5.0	µA	

Notes

34. Only in Auto and APS modes.

Table 14. Dynamic electrical characteristics - SWBST

All parameters are specified at T_A = -40 °C to 105 °C, VIN = $V_{SWBSTIN}$ = 3.6 V, V_{SWBST} = 5.0 V, I_{SWBST} = 100 mA, typical external component values, f_{SWBST} = 2.0 MHz, otherwise noted. Typical values are characterized at V_{IN} = $V_{SWBSTIN}$ = 3.6 V, V_{SWBST} = 5.0 V, I_{SWBST} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SWBST						
$V_{SWBSTOSH}$	Start-up overshoot, I_{SWBST} = 0.0 mA	–	–	500	mV	
$t_{ONSWBST}$	Turn-on time, enable to 90% of VSWBST, ISWBST = 0.0 mA	–	–	2.0	ms	

Table 15. Static electrical characteristics - VSNVS

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VSNVS						
V_{IN}	Operating input voltage • Valid coin cell range • Valid V_{IN}	 1.8 2.25	 – –	 3.3 4.5	V	(35)
I_{SNVS}	Operating load current, V_{INMIN} < V_{IN} < V_{INMAX}	1.0	–	1000	µA	
V_{SNVS}	Output voltage • 5.0 µA < I_{SNVS} < 1000 µA (OFF), 3.20 V < V_{IN} < 4.5 V • 5.0 µA < I_{SNVS} < 1000 µA (ON), 3.20 V < V_{IN} < 4.5 V • 5.0 µA < I_{SNVS} < 1000µA (Coin cell mode), 2.84 V < V_{COIN} < 3.3 V	 -5.0% -5.0% V_{COIN}-0.10	 3.0 3.0 –	 7.0% 5.0% V_{COIN}	V	
$V_{SNVSDROP}$	Dropout voltage, 2.85 V < V_{IN} < 2.9 V, 1.0 µA < I_{SNVS} < 1000 µA	–	–	110	mV	
$I_{SNVSLIM}$	Current limit, V_{IN} > V_{TH1}	1100	–	6750	µA	
VSNVS DC, SWITCH						
V_{LiCell}	Operating input voltage, valid coin cell range	1.8	–	3.3	V	
I_{SNVS}	Operating load current	1.0	–	1000	µA	
$R_{DS(on)SNVS}$	Internal switch $R_{DS(on)}$, V_{COIN} = 2.6 V	–	–	100	Ω	

Notes

35. The maximum operating input voltage is 4.55 V when VPWR LDO is used

Table 16. Dynamic electrical characteristics - VSNVS

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VSNVS						
$V_{SNVSTON}$	Turn-on time (load capacitor, 0.47 µF), from V_{IN} = V_{TH1} to 90% of V_{SNVS}, V_{COIN} = 0.0 V, I_{SNVS} = 5.0 µA	–	–	24	ms	(36),(37)
$V_{SNVSOSH}$	Start-up overshoot, I_{SNVS} = 5.0 µA	–	40	70	mV	
$V_{SNVSLOTR}$	Transient load response, 3.2 < V_{IN} ≤ 4.5 V, I_{SNVS} = 100 to 1000 µA	2.8	–	–	V	
V_{TL1}	V_{IN} falling threshold (V_{IN} powered to coin cell powered)	2.45	2.70	3.05	V	
V_{TH1}	V_{IN} rising threshold (coin cell powered to V_{IN} powered)	2.50	2.75	3.10	V	
V_{HYST1}	V_{IN} threshold hysteresis for V_{TH1}-V_{TL1}	5.0	–	–	mV	
$V_{SNVSCROSS}$	Output voltage during crossover, V_{COIN} > 2.9 V, Switch to LDO: V_{IN} > V_{TH1}, I_{SNVS} = 100 µA, LDO to Switch: V_{IN} < V_{TL1}, I_{SNVS} = 100 µA	2.45	–	–	V	

Notes

36. The start-up of V_{SNVS} is not monotonic. It first rises to 1.0 V and then settles to 3.0 V.
37. From coin cell insertion to V_{SNVS} = 1.0 V, the delay time is typically 400 ms.

Table 17. Static electrical characteristics - VLDO1

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{LDO1IN} = 3.6 V, V_{LDO1} = 3.3 V, I_{LDO1} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDO1IN} = 3.6 V, V_{LDO1} = 3.3 V, I_{LDO1} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO1 linear regulator						
V_{LDO1IN}	Operating input voltage • 1.8 V ≤ $V_{LDO1NOM}$ ≤ 2.5 V • 2.6 V ≤ $V_{LDO1NOM}$ ≤ 3.3 V	2.8 $V_{LDO1NOM}$ +0.250	– –	4.5 4.5	V	(38), (39)
$V_{LDO1NOM}$	Nominal output voltage	–	Table 62	–	V	
I_{LDO1}	Rated output load current	100	–	–	mA	
$V_{LDO1TOL}$	Output voltage tolerance, $V_{LDO1INMIN}$ < V_{LDO1IN} < 4.5 V, 0.0 mA < I_{LDO1} < 100 mA, VLDO1 = 1.8 V to 3.3 V	-3.0	–	3.0	%	
I_{LDO1Q}	Quiescent current, no load, change in $I_{VIN,}$ when VLDO1 enabled	–	13	–	µA	
$I_{LDO1LIM}$	Current limit, I_{LDO1} when V_{LDO1} is forced to $V_{LDO1NOM}$/2	122	167	280	mA	

Notes

38. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
39. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3000 regulator, or external system supply.

Table 18. Dynamic electrical characteristics - VLDO1

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{LDO1IN} = 3.6 V, V_{LDO1} = 3.3 V, I_{LDO1} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDO1IN} = 3.6 V, V_{LDO1} = 3.3 V, I_{LDO1} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO1 linear regulator						
$PSRR_{VLDO1}$	PSRR, I_{LDO1} = 75 mA, 20 Hz to 20 kHz • VLDO1 = 1.8 V to 3.3 V, V_{LDO1IN} = $V_{LDO1INMIN}$ + 100 mV • VLDO1 = 1.8 V to 3.3 V, V_{LDO1IN} = $V_{LDO1NOM}$ + 1.0 V	 35 52	 40 60	 – –	dB	
$NOISE_{VLDO1}$	Output noise density, V_{LDO1IN} = $V_{LDO1INMIN}$, I_{LDO1} = 75 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/ √Hz	
t_{ONLDO1}	Turn-on time, enable to 90% of end value, V_{LDO1IN} = $V_{LDO1INMIN}$ to 4.5 V, I_{LDO1} = 0.0 mA, all output voltage settings	60	–	500	µs	
$t_{OFFLDO1}$	Turn-off time, disable to 10% of initial value, V_{LDO1IN} = $V_{LDO1INMIN}$, I_{LDO1} = 0.0 mA	–	–	10	ms	
$LDO1_{OSHT}$	Start-up overshoot, V_{LDO1IN} = $V_{LDO1INMIN}$ to 4.5 V, I_{LDO1} = 0.0 mA	–	1.0	2.0	%	

Table 19. Static electrical characteristics - VLDO2

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{LDO2IN} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDO2IN} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO2 linear regulator						
V_{LDO2IN}	Operating input voltage	1.75	–	3.40	V	
$V_{LDO2NOM}$	Nominal output voltage	–	Table 63	–	V	
I_{LDO2}	Rated output load current	250	–	–	mA	
$V_{LDO2TOL}$	Output voltage tolerance, 1.75 V < V_{LDOIN1} < 3.40 V, 0.0 mA < I_{LDO2} < 250 mA, VLDO2 = 0.8 V to 1.55 V	-3.0	–	3.0	%	
I_{LDO2Q}	Quiescent current, no load, change in I_{VIN} and $I_{VLDO2IN}$, when V_{LDO2} enabled	–	16	–	µA	
$I_{LDO2LIM}$	Current limit, I_{LDO2} when V_{LDO2} is forced to $V_{LDO2NOM}$/2	333	417	612	mA	

Table 20. Dynamic electrical characteristics - VLDO2

All parameters are specified at TA = -40 °C to 105 °C, VIN = 3.6 V, V_{LDO2IN} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDO2IN} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO2 linear regulator						
$PSRR_{VLDO2}$	PSRR, I_{LDO2} = 187.5 mA, 20 Hz to 20 kHz • VLDO2 = 0.8 V to 1.55 V • VLDO2 = 1.1 V to 1.55 V	 50 37	 60 45	 – –	dB	
$NOISE_{VLDO2}$	Output noise density, V_{LDO2IN} = 1.75 V, I_{LDO2} = 187.5 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	 – – –	 -108 -118 -124	 -100 -108 -112	dBV/√Hz	

Table 20. Dynamic electrical characteristics - VLDO2 (continued)

All parameters are specified at TA = -40 °C to 105 °C, VIN = 3.6 V, V_{LDO2IN} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDO2IN} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO2 linear regulator (continue)						
t_{ONLDO2}	Turn-on time, enable to 90% of end value, V_{LDO2IN} = 1.75 V to 3.4 V, I_{LDO2} = 0.0 mA	60	–	500	µs	
$t_{OFFLDO2}$	Turn-off time, disable to 10% of initial value, V_{LDO2IN} = 1.75 V, I_{LDO2} = 0.0 mA	–	–	10	ms	
$LDO2_{OSHT}$	Start-up overshoot, V_{LDO2IN} = 1.75 V to 3.4 V, I_{LDO2} = 0.0 mA	–	1.0	2.0	%	

Table 21. Static electrical characteristics – VCC_SD

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, VCC_SD = 1.85 V, I_{VCC_SD} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, VCC_SD = 1.85 V, I_{VCC_SD} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VCC_SD linear regulator						
V_{IN}	Operating input voltage	2.8	–	4.5	V	(40), (41), (41)
V_{CC_SDNOM}	Nominal output voltage	–	Table 65	–	V	
I_{VCC_SD}	Rated output load current	100	–	–	mA	
V_{CC_SDTOL}	Output voltage accuracy, 2.8 V < V_{IN} < 4.5 V, 0.0 mA < I_{VCC_SD} < 100 mA, VCC_SD[1:0] = 00 to 11	-3.0	–	3.0	%	
I_{VCC_SDQ}	Quiescent current, no load, change in I_{VIN} and I_{VIN2}, when V_{CC_SD} enabled	–	13	–	µA	
I_{VCC_SDLIM}	Current limit, I_{VCC_SD} when V_{CC_SD} is forced to V_{CC_SDNOM}/2	122	167	280	mA	

Notes

40. When the LDO output voltage is set above 2.6 V, the minimum allowed input voltage needs to be at least the output voltage plus 0.25 V.
41. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
42. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3000 regulator, or external system supply.

Table 22. Dynamic electrical characteristics - VCC_SD

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, VCC_SD = 1.85 V, IVCC_SD = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, VCC_SD = 1.85 V, IVCC_SD = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VCC_SD linear regulator						
$PSRR_{VCC\_SD}$	PSRR, I_{VCC_SD} = 75 mA, 20 Hz to 20 kHz • VCC_SD[1:0] = 00 - 10, V_{IN} = 2.8 V + 100 mV • VCC_SD[1:0] = 10 - 11, V_{IN} = V_{CC_SDNOM} + 1.0 V	 35 52	 40 60	 – –	dB	
$NOISE_{VCC\_SD}$	Output noise density, V_{IN} = 2.8V, I_{VCC_SD} = 75 mA • 100 Hz – <1.0 kHz • 1.0 kHz – <10 kHz • 10 kHz – 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/√Hz	
t_{ONVCC_SD}	Turn-on time, enable to 90% of end value, V_{IN} = 2.8 V to 4.5 V, I_{VCC_SD} = 0.0 mA	60	–	500	µs	

Table 22. Dynamic electrical characteristics - VCC_SD (continued)

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, VCC_SD = 1.85 V, IVCC_SD = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, VCC_SD = 1.85 V, IVCC_SD = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VCC_SD linear regulator (continued)						
t_{OFFVCC_SD}	Turn-off time, disable to 10% of initial value, V_{IN} = 2.8 V, I_{VCC_SD} = 0.0 mA	–	–	10	ms	
VCC_SD_{OSHT}	Start-up overshoot, V_{IN} = 2.8 V to 4.5 V, I_{VCC_SD} = 0.0 mA	–	1.0	2.0	%	

Table 23. Static electrical characteristics – V33

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V33 linear regulator						
V_{IN}	Operating input voltage, 2.9 V ≤ V_{33NOM} ≤ 3.6 V	2.8	–	4.5	V	(43), (44), (45)
V_{33NOM}	Nominal output voltage	–	Table 64	–	V	
I_{V33}	Rated output load current	350	–	–	mA	
V_{33TOL}	Output voltage tolerance, 2.8 V < V_{IN} < 4.5 V, 0.0 mA < I_{V33} < 350 mA, V_{33}[1:0] = 00 to 11	-3.0	–	3.0	%	
I_{V33Q}	Quiescent current, no load, change in I_{VIN}, when V_{33} enabled	–	13	–	µA	
I_{V33LIM}	Current limit, I_{V33} when V_{33} is forced to V_{33NOM}/2	435	584.5	950	mA	

Notes

43. When the LDO output voltage is set above 2.6 V the minimum allowed input voltage need to be at least the output voltage plus 0.25 V for proper regulation due to the dropout voltage generated through the internal LDO transistor.
44. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
45. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3000 regulator, or external system supply.

Table 24. Dynamic electrical characteristics – V33

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V33 linear regulator						
$PSRR_{V33}$	PSRR, I_{V33} = 262.5 mA, 20 Hz to 20 kHz, V_{33}[1:0] = 00 - 11, V_{IN} = V_{33NOM} + 1.0 V	52	60	–	dB	(46)
$NOISE_{V33}$	Output noise density, V_{IN} = 2.8 V, I_{V33} = 262.5 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/√Hz	
t_{ONV33}	Turn-on time, enable to 90% of end value, V_{IN} = 2.8 V, to 4.5 V, I_{V33} = 0.0 mA	60	–	500	µs	

Table 24. Dynamic electrical characteristics – V33 (continued)

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V33 linear regulator (continued)						
t_{OFFV33}	Turn-off time, disable to 10% of initial value, V_{IN} = 2.8 V, I_{V33} = 0.0 mA	–	–	10	ms	
V_{33OSHT}	Start-up overshoot, V_{IN} = 2.8 V to 4.5 V, I_{V33} = 0.0 mA	–	1.0	2.0	%	

Notes

46. When the LDO Output voltage is set above 2.6 V the minimum allowed input voltage need to be at least the output voltage plus 0.25 V for proper regulation due to the dropout voltage generated through the internal LDO transistor.

Table 25. Static electrical characteristics – VLDO3

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO3 linear regulator						
$V_{LDO34IN}$	Operating input voltage • 1.8 V ≤ $V_{LDO3NOM}$ ≤ 2.5 V • 2.6 V ≤ $V_{LDO3NOM}$ ≤ 3.3 V	2.8 $V_{LDO3NOM}$ +0.250	– –	3.6 3.6	V	(47), (48)
$V_{LDO3NOM}$	Nominal output voltage	–	Table 63	–	V	
I_{LDO3}	Rated output load current	100	–	–	mA	
$V_{LDO3TOL}$	Output voltage tolerance, $V_{LDO34INMIN}$ < $V_{LDO34IN}$ < 4.5 V, 0.0 mA < I_{LDO3} < 100 mA, VLDO3 = 1.8 V to 3.3 V	-3.0	–	3.0	%	
I_{LDO3Q}	Quiescent current, no load, change in I_{VIN} and $I_{VLDO34IN}$, when V_{LDO3} enabled	–	13	–	µA	
$I_{LDO3LIM}$	Current limit, I_{LDO3} when V_{LDO3} is forced to $V_{LDO3NOM}$/2	122	167	280	mA	

Notes

47. Beyond VLDO34IN rating, the ESD protection can be sensitive to voltage transients.
48. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3000 regulator, or external system supply.

Table 26. Dynamic electrical characteristics – VLDO3

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO3 linear regulator						
$PSRR_{VLDO3}$	PSRR, I_{LDO3} = 75 mA, 20 Hz to 20 kHz • VLDO3 = 1.8 V to 3.3 V, $V_{LDO34IN}$ = $V_{LDO34INMIN}$ + 100 mV • VLDO3 = 1.8 V to 3.3 V, $V_{LDO34IN}$ = $V_{LDO3NOM}$ + 1.0 V	35 52	40 60	– –	dB	
$NOISE_{VLDO3}$	Output noise density, $V_{LDO34IN}$ = $V_{LDO34INMIN}$, I_{LDO3} = 75 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	– – –	-114 -129 -135	-102 -123 -130	dBV/√Hz	

Table 26. Dynamic electrical characteristics – VLDO3 (continued)

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO3 linear regulator (continued)						
t_{ONLDO3}	Turn-on time, enable to 90% of end value, $V_{LDO34IN}$ = $V_{LDO34INMIN}$ to 4.5 V, I_{LDO3} = 0.0 mA	60	–	500	µs	
$t_{OFFLDO3}$	Turn-off time, disable to 10% of initial value, $V_{LDO34IN}$ = $V_{LDO34INMIN}$, I_{LDO3} = 0.0 mA	–	–	10	ms	
$LDO3_{OSHT}$	Start-up overshoot, $V_{LDO34IN}$ = $V_{LDO34IN2MIN}$ to 4.5 V, I_{LDO3} = 0.0 mA	–	1.0	2.0	%	

Table 27. Static electrical characteristics - VLDO4

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO4} = 3.3 V, I_{LDO4} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, VLDO4 = 3.3 V, I_{LDO4} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO4 linear regulator						
$V_{LDO34IN}$	Operating input voltage • 1.8 V ≤ $V_{LDO4NOM}$ ≤ 2.5 V • 2.6 V ≤ $V_{LDO4NOM}$ ≤ 3.3 V	2.8 $V_{LDO4NOM}$ +0.250	– –	3.6 3.6	V	(49), (50)
$V_{LDO4NOM}$	Nominal output voltage	–	Table 63	–	V	
I_{LDO4}	Rated output load current	350	–	–	mA	
$V_{LDO4TOL}$	Output voltage tolerance, $V_{LDO34INMIN}$ < $V_{LDO34IN}$ < 4.5 V, 0.0 mA < I_{LDO3} < 100 mA, V_{LDO4} = 1.9 V to 3.3 V	-3.0	–	3.0	%	
I_{LDO4Q}	Quiescent current, no load, change in I_{VIN} and $I_{VLDO34IN}$, when V_{LDO4} enabled	–	13	–	µA	
$I_{LDO4LIM}$	Current limit, I_{LDO4} when V_{LDO4} is forced to $V_{LDO4NOM}$/2	435	584.5	950	mA	
$PSRR_{VLDO4}$	PSRR, I_{LDO4} = 262.5 mA, 20 Hz to 20 kHz • VLDO4 = 1.9 V to 3.3 V, $V_{LDO34IN}$ = $V_{LDO34INMIN}$ + 100 mV • VLDO4 = 1.9 V to 3.3 V, $V_{LDO34IN}$ = $V_{LDO4NOM}$ + 1.0 V	 35 52	 40 60	 – –	dB	

Notes

49. Beyond VLDO34IN rating, the ESD protection can be sensitive to voltage transients.
50. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3000 regulator, or external system supply.