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# PF4210

## 14-channel Power Management Integrated Circuit (PMIC) for audio/video applications

Rev. 1.0 — 14 February 2018 Data sheet: technical data

## 1 General description

The PF4210 high performance power management integrated circuit (PMIC) provides a highly programmable/configurable architecture with fully integrated power devices and minimal external components. With up to six buck converters, six linear regulators, an RTC supply, and a coin cell charger, the PF4210 can provide power for a complete system, including applications processors, memory, and system peripherals, in a wide range of applications.

With on-chip one-time programmable (OTP) memory, the PF4210 is available in preprogrammed standard version or nonprogrammed to support custom programming. The PF4210 is defined to power low-cost audio/video applications using the i.MX 8M family of applications processors.

## 2 Features and benefits

- Four to six buck converters, depending on configuration
  - Single/dual phase/parallel options
  - DDR termination tracking mode option
- Boost regulator to 5.0 V output
- Six general purpose linear regulators
- Programmable output voltage, sequence, and timing
- OTP (one-time programmable) memory for device configuration
- Coin cell charger and RTC supply
- DDR termination reference voltage
- Power control logic with processor interface and event detection
- $I^2C$ control
- Individually programmable on, off, and standby modes

# 3 Simplified application diagram

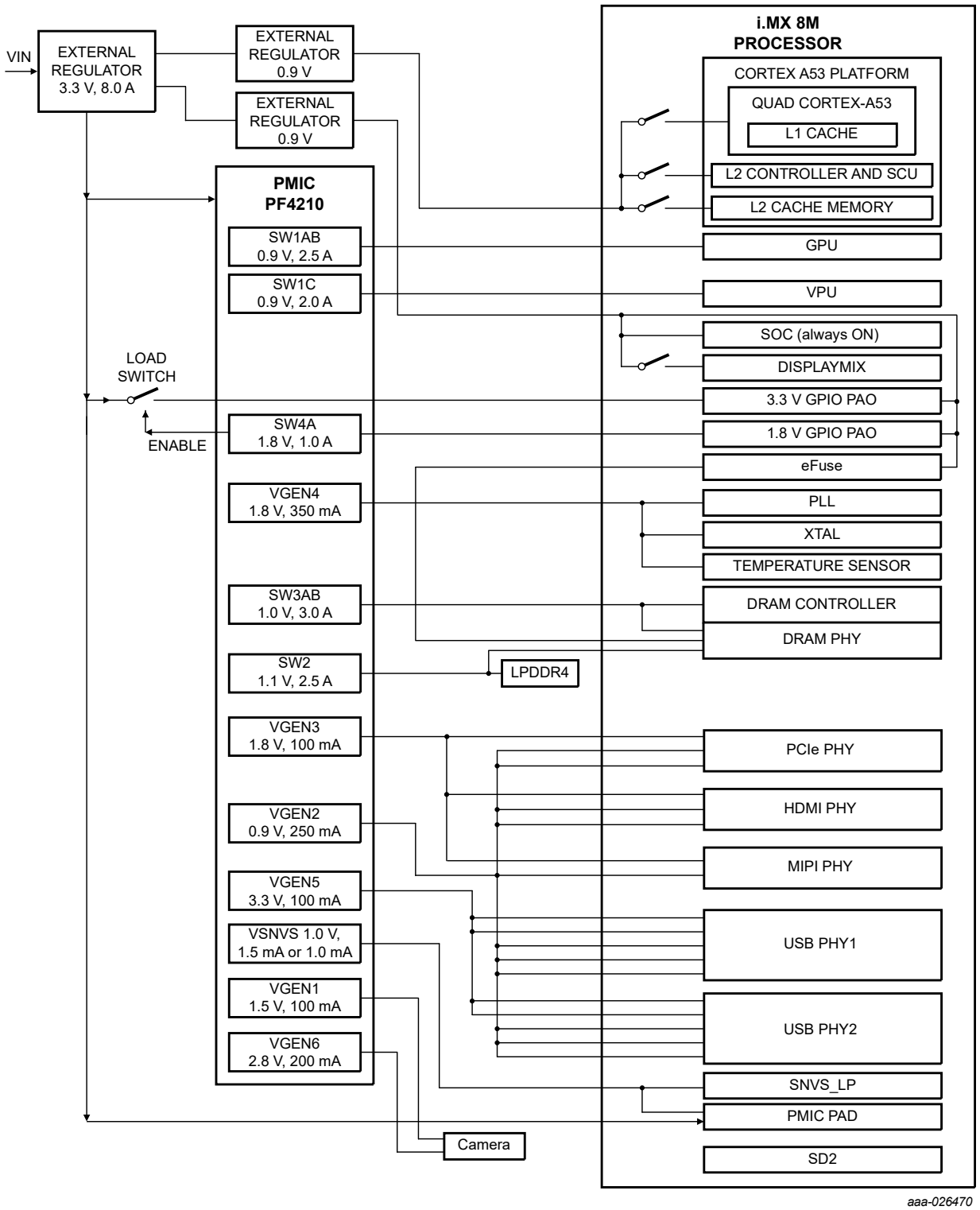


**Figure 1. Simplified application diagram**

# 4 Applications

- OTT STB
- Wireless audio
- Voice recognition assistant
- A/V receivers
- Sound bars
- General embedded

# 5 Orderable parts

The PF4210 is available with both preprogrammed and nonprogrammed OTP memory configurations. The nonprogrammed device uses A0 as the programming code. The preprogrammed devices are identified using the program codes from Table 1, which also list the associated NXP reference designs where applicable.

Details of the OTP programming for each device can be found in Table 8.

**Table 1. Orderable part variations**

| Part number[1] | Temperature ($T_A$) | Package | Programming[2] | Reference designs |
|---|---|---|---|---|
| MC32PF4210A0ES | 0 °C to 85 °C (for use in consumer applications) | 56 QFN 8x8 mm - 0.5 mm pitch WF-type QFN (wettable flank) | A0 (Nonprogrammed) | N/A |
| MC32PF4210A1ES | | | A1 | MCIMX8M-EVK |
| MC32PF4210A2ES | | | A2 | N/A |
| MC32PF4210A3ES | | | A3 | N/A |
| MC34PF4210A0ES | −40 °C to 105 °C (for use in industrial applications) | | A0 (Nonprogrammed) | N/A |
| MC34PF4210A1ES | | | A1 | MCIMX8M-EVK |
| MC34PF4210A2ES | | | A2 | N/A |
| MC34PF4210A3ES | | | A3 | N/A |

[1] For tape and reel, add an R2 suffix to the part number.
[2] For programming details see Table 8. The available OTP options are not restricted to the listed reference designs. They can be used in any application where the listed voltage and sequence details are acceptable.

# 6 Internal block diagram

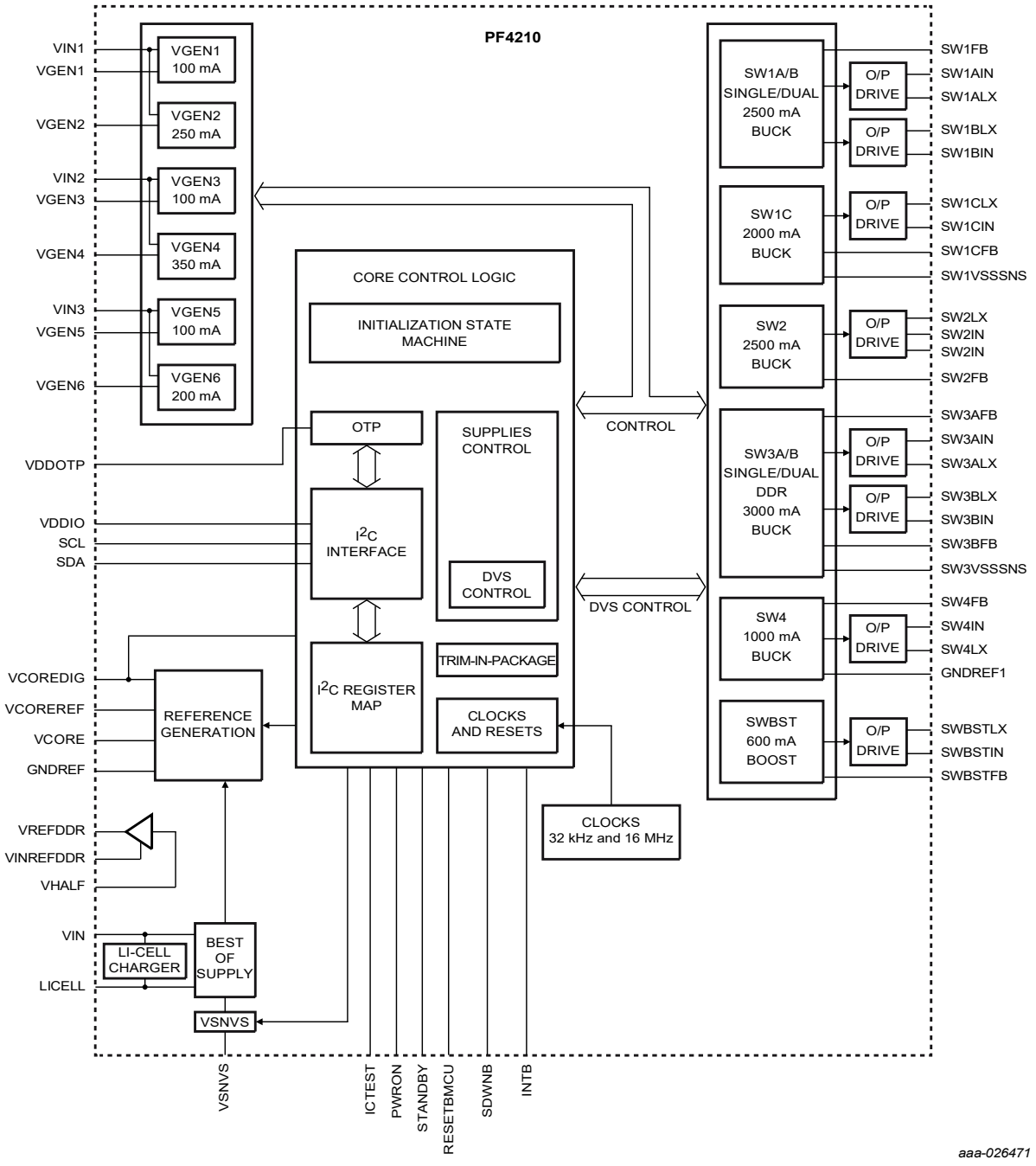


**Figure 2. Simplified internal block diagram**

# 7 Pinning information

## 7.1 Pinning

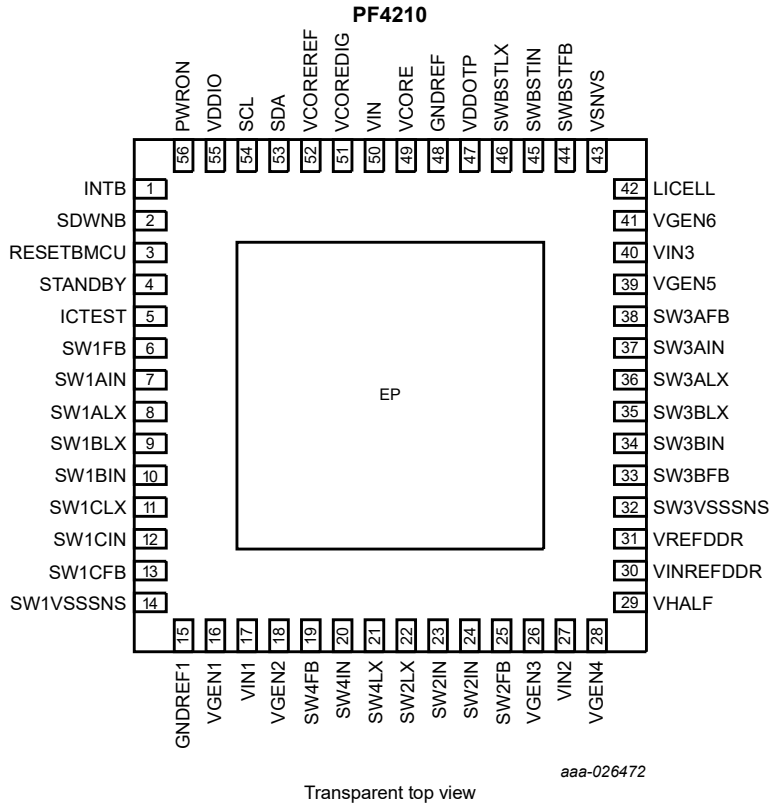


**Figure 3. Pinout diagram**

## 7.2 Pin definitions

**Table 2. Pin definitions**

| Number | Name | Function | Max rating | Type | Definition |
|---|---|---|---|---|---|
| 1 | INTB | Output | 3.6 V | Digital | Open drain interrupt signal to processor |
| 2 | SDWNB | Output | 3.6 V | Digital | Open drain signal to indicate an imminent system shutdown |
| 3 | RESETBMCU | Output | 3.6 V | Digital | Open drain reset output to processor. Alternatively can be used as a power output. |
| 4 | STANDBY | Input | 3.6 V | Digital | Standby input signal from processor |
| 5 | ICTEST | Input | 7.5 V | Digital/ Analog | Reserved pin. Connect to GND in application. |
| 6 | SW1FB [1] | Input | 3.6 V | Analog | Output voltage feedback for SW1A/B. Route this trace separately from the high current path and terminate at the output capacitance. |

| Number | Name | Function | Max rating | Type | Definition |
|---|---|---|---|---|---|
| 7 | SW1AIN [1] | Input | 4.8 V | Analog | Input to SW1A regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible. |
| 8 | SW1ALX [1] | Output | 4.8 V | Analog | Regulator 1A switch node connection |
| 9 | SW1BLX [1] | Output | 4.8 V | Analog | Regulator 1B switch node connection |
| 10 | SW1BIN [1] | Input | 4.8 V | Analog | Input to SW1B regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible. |
| 11 | SW1CLX [1] | Output | 4.8 V | Analog | Regulator 1C switch node connection |
| 12 | SW1CIN [1] | Input | 4.8 V | Analog | Input to SW1C regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible. |
| 13 | SW1CFB [1] | Input | 3.6 V | Analog | Output voltage feedback for SW1C. Route this trace separately from the high current path and terminate at the output capacitance. |
| 14 | SW1VSSSNS | GND | — | GND | Ground reference for regulators SW1ABC. It is connected externally to GNDREF through a board ground plane. |
| 15 | GNDREF1 | GND | — | GND | Ground reference for regulators SW2 and SW4. It is connected externally to GNDREF, via board ground plane. |
| 16 | VGEN1 | Output | 2.5 V | Analog | VGEN1 regulator output. Bypass with a 2.2 µF ceramic output capacitor. |
| 17 | VIN1 | Input | 3.6 V | Analog | VGEN1, 2 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible. |
| 18 | VGEN2 | Output | 2.5 V | Analog | VGEN2 regulator output. Bypass with a 4.7 µF ceramic output capacitor. |
| 19 | SW4FB [1] | Input | 3.6 V | Analog | Output voltage feedback for SW4. Route this trace separately from the high current path and terminate at the output capacitance. |
| 20 | SW4IN [1] | Input | 4.8 V | Analog | Input to SW4 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible. |
| 21 | SW4LX [1] | Output | 4.8 V | Analog | Regulator 4 switch node connection |
| 22 | SW2LX [1] | Output | 4.8 V | Analog | Regulator 2 switch node connection |
| 23 | SW2IN [1] | Input | 4.8 V | Analog | Input to SW2 regulator. Connect pin 23 together with pin 24 and bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to these pins as possible. |
| 24 | SW2IN [1] | Input | 4.8 V | Analog | |
| 25 | SW2FB [1] | Input | 3.6 V | Analog | Output voltage feedback for SW2. Route this trace separately from the high current path and terminate at the output capacitance. |
| 26 | VGEN3 | Output | 3.6 V | Analog | VGEN3 regulator output. Bypass with a 2.2 µF ceramic output capacitor. |
| 27 | VIN2 | Input | 3.6 V | Analog | VGEN3, 4 input. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible. |

| Number | Name | Function | Max rating | Type | Definition |
|---|---|---|---|---|---|
| 28 | VGEN4 | Output | 3.6 V | Analog | VGEN4 regulator output. Bypass with a 4.7 µF ceramic output capacitor. |
| 29 | VHALF | Input | 3.6 V | Analog | Half supply reference for VREFDDR |
| 30 | VINREFDDR | Input | 3.6 V | Analog | VREFDDR regulator input. Bypass with at least 1.0 µF decoupling capacitor as close to the pin as possible. |
| 31 | VREFDDR | Output | 3.6 V | Analog | VREFDDR regulator output |
| 32 | SW3VSSSNS | GND | — | GND | Ground reference for the SW3 regulator. Connect to GNDREF externally via the board ground plane. |
| 33 | SW3BFB [1] | Input | 3.6 V | Analog | Output voltage feedback for SW3B. Route this trace separately from the high current path and terminate at the output capacitance. |
| 34 | SW3BIN [1] | Input | 4.8 V | Analog | Input to SW3B regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible. |
| 35 | SW3BLX [1] | Output | 4.8 V | Analog | Regulator 3B switch node connection |
| 36 | SW3ALX [1] | Output | 4.8 V | Analog | Regulator 3A switch node connection |
| 37 | SW3AIN [1] | Input | 4.8 V | Analog | Input to SW3A regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible. |
| 38 | SW3AFB [1] | Input | 3.6 V | Analog | Output voltage feedback for SW3A. Route this trace separately from the high current path and terminate at the output capacitance. |
| 39 | VGEN5 | Output | 3.6 V | Analog | VGEN5 regulator output. Bypass with a 2.2 µF ceramic output capacitor. |
| 40 | VIN3 | Input | 4.8 V | Analog | VGEN5, 6 input. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible. |
| 41 | VGEN6 | Output | 3.6 V | Analog | VGEN6 regulator output. Bypass with a 2.2 µF ceramic output capacitor. |
| 42 | LICELL | Input/Output | 3.6 V | Analog | Coin cell supply input/output |
| 43 | VSNVS | Output | 3.6 V | Analog | LDO or coin cell output to processor |
| 44 | SWBSTFB [1] | Input | 5.5 V | Analog | Boost regulator feedback. Connect this pin to the output rail close to the load. Keep this trace away from other noisy traces and planes. |
| 45 | SWBSTIN [1] | Input | 4.8 V | Analog | Input to SWBST regulator. Bypass with at least a 2.2 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible. |
| 46 | SWBSTLX [1] | Output | 7.5 V | Analog | SWBST switch node connection |
| 47 | VDDOTP | Input | 10 V [2] | Digital/ Analog | Supply to program OTP fuses |
| 48 | GNDREF | GND | — | GND | Ground reference for the main band gap regulator |
| 49 | VCORE | Output | 3.6 V | Analog | Analog core supply |
| 50 | VIN | Input | 4.8 V | Analog | Main chip supply |
| 51 | VCOREDIG | Output | 1.5 V | Analog | Digital core supply |

| Number | Name | Function | Max rating | Type | Definition |
|---|---|---|---|---|---|
| 52 | VCOREREF | Output | 1.5 V | Analog | Main band gap reference |
| 53 | SDA | Input/Output | 3.6 V | Digital | $I^2C$ data line (open drain) |
| 54 | SCL | Input | 3.6 V | Digital | $I^2C$ clock |
| 55 | VDDIO | Input | 3.6 V | Analog | Supply for $I^2C$ bus. Bypass with 0.1 µF ceramic capacitor |
| 56 | PWRON | Input | 3.6 V | Digital | Power on/off from processor |
| — | EP | GND | — | GND | Expose pad. Functions as ground return for buck regulators. Tie this pad to the inner and external ground planes through vias to allow effective thermal dissipation. |

[1] Unused switching regulators should be connected as follow: Pins SWxLX and SWxFB should be unconnected and pin SWxIN should be connected to VIN with a 0.1 µF bypass capacitor.
[2] 10 V maximum voltage rating during OTP fuse programming. 7.5 V maximum DC voltage rated otherwise.

# 8 General product characteristics

## 8.1 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

*All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause malfunction or permanent damage to the device. For maximum voltage rating for each pin see Section 7.2 "Pin definitions".*

| Symbol | Description | Value | Unit |
|---|---|---|---|
| **Electrical ratings** | | | |
| $V_{IN}$ | Main input supply voltage | −0.3 to 4.8 | V |
| $V_{DDOTP}$ | OTP programming input supply voltage | −0.3 to 10 | V |
| $V_{LICELL}$ | Coin cell voltage | −0.3 to 3.6 | V |
| $V_{ESD}$ | ESD ratings [1]<br>Human body model<br>Charge device model | <br>±2000<br>±500 | V |

[1] ESD testing is performed in accordance with the human body model (HBM) ($C_{ZAP}$ = 100 pF, $R_{ZAP}$ = 1500 Ω), and the charge device model (CDM), robotic ($C_{ZAP}$ = 4.0 pF).

## 8.2 Thermal characteristics

**Table 4. Thermal ratings**

| Symbol | Description (rating) | Min | Max | Unit |
|---|---|---|---|---|
| **Thermal ratings** | | | | |
| $T_A$ | Ambient operating temperature range<br>MC32PF4210<br>MC34PF4210 | <br>0<br>−40 | <br>85<br>105 | °C |
| $T_J$ | Operating junction temperature range [1] | −40 | 125 | °C |
| $T_{ST}$ | Storage temperature range | −65 | 150 | °C |
| $T_{PPRT}$ | Peak package reflow temperature [2] | — | [3] | °C |

| Symbol | Description (rating) | | Min | Max | Unit |
|---|---|---|---|---|---|
| **QFN56 thermal resistance and package dissipation ratings** | | | | | |
| $R_{\Theta JA}$ | Junction to ambient | [4] [5] [6] | | | °C/W |
| | Natural convection | | | | |
| | Four layer board (2s2p) | | — | 28 | |
| | Eight layer board (2s6p) | | — | 15 | |
| $R_{\Theta JMA}$ | Junction to ambient (@200 ft/min) | [4] [6] | | | °C/W |
| | Four layer board (2s2p) | | — | 22 | |
| $R_{\Theta JB}$ | Junction to board | [7] | — | 10 | °C/W |
| $R_{\Theta JCBOTTOM}$ | Junction to case bottom | [8] | — | 1.2 | °C/W |
| ΨJT | Junction to package top | [9] | | | °C/W |
| | Natural convection | | — | 2.0 | |

[1] Do not operate beyond 125 °C for extended period of time. Operation above 150 °C may cause permanent damage to the IC. See Table 5 for thermal protection features.
[2] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
[3] NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts (MC33xxxD enter 33xxx), and review parametrics.
[4] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
[5] The board uses the JEDEC specifications for thermal testing (and simulation) JESD51-7 and JESD51-5.
[6] Per JEDEC JESD51-6 with the board horizontal
[7] Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
[8] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
[9] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letter (Ψ) is not available, the thermal characterization parameter is written as Psi-JT.

## 8.3 Power dissipation

During operation, the temperature of the die should not exceed the operating junction temperature noted in Table 4. To optimize the thermal management and to avoid overheating, the PF4210 provides thermal protection.

An internal comparator monitors the die temperature. Interrupts THERM110I, THERM120I, THERM125I, and THERM130I are generated when the respective thresholds specified in Table 5 are crossed in either direction. The temperature range can be determined by reading the THERMxxxS bits in register INTSENSE0.

In the event of excessive power dissipation, thermal protection circuitry shuts down the PF4210. This thermal protection acts above the thermal protection threshold listed in Table 5. To avoid any unwanted power-down resulting from internal noise, the protection is debounced for 8.0 ms. This protection should be considered as a fail-safe mechanism and therefore the system should be configured so protection is not tripped under normal conditions.

**Table 5. Thermal protection thresholds**

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Thermal 110 °C threshold (THERM110) | 100 | 110 | 120 | °C |
| Thermal 120 °C threshold (THERM120) | 110 | 120 | 130 | °C |

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Thermal 125 °C threshold (THERM125) | 115 | 125 | 135 | °C |
| Thermal 130 °C threshold (THERM130) | 120 | 130 | 140 | °C |
| Thermal warning hysteresis | 2.0 | — | 4.0 | °C |
| Thermal protection threshold | 130 | 140 | 150 | °C |

## 8.4 Electrical characteristics

### 8.4.1 General specifications

**Table 6. General PMIC static characteristics**

*$T_{MIN}$ to $T_{MAX}$ (see Table 4), VIN = 2.8 to 4.5 V, VDDIO = 1.7 to 3.6 V, typical external component values and full load current range, unless otherwise noted.*

| Pin name | Parameter | Load condition | Min | Max | Unit |
|---|---|---|---|---|---|
| PWRON | $V_{IL}$ | — | 0 | 0.2 * VSNVS | V |
| | $V_{IH}$ | — | 0.8 * VSNVS | 3.6 | V |
| RESETBMCU | $V_{OL}$ | −2.0 mA | 0.0 | 0.4 | V |
| | $V_{OH}$ | Open drain | 0.7* VIN | VIN | V |
| SCL | $V_{IL}$ | — | 0.0 | 0.2 * VDDIO | V |
| | $V_{IH}$ | — | 0.8 * VDDIO | 3.6 | V |
| SDA | $V_{IL}$ | — | 0 | 0.2 * VDDIO | V |
| | $V_{IH}$ | — | 0.8 * VDDIO | 3.6 | V |
| | $V_{OL}$ | −2.0 mA | 0.0 | 0.4 | V |
| | $V_{OH}$ | Open drain | 0.7 * VDDIO | VDDIO | V |
| INTB | $V_{OL}$ | −2.0 mA | 0.0 | 0.4 | V |
| | $V_{OH}$ | Open drain | 0.7 * VIN | VIN | V |
| SDWNB | $V_{OL}$ | −2.0 mA | 0.0 | 0.4 | V |
| | $V_{OH}$ | Open drain | 0.7 * VIN | VIN | V |
| STANDBY | $V_{IL}$ | — | 0 | 0.2 * VSNVS | V |
| | $V_{IH}$ | — | 0.8 * VSNVS | 3.6 | V |
| VDDOTP | $V_{IL}$ | — | 0 | 0.3 | V |
| | $V_{IH}$ | — | 1.1 | 1.7 | V |

### 8.4.2 Current consumption

**Table 7. Current consumption summary**

*$T_{MIN}$ to $T_{MAX}$ (see Table 4), VIN = 3.6 V, VDDIO = 1.7 V to 3.6 V, LICELL = 1.8 V to 3.3 V, VSNVS = 3.0 V, typical external component values, unless otherwise noted. Typical values are characterized at VIN = 3.6 V, VDDIO = 3.3 V, LICELL = 3.0 V, VSNVS = 3.0 V and 25 °C, unless otherwise noted.*

| Mode | PF4210 conditions | System conditions | Typ | Max | Unit |
|---|---|---|---|---|---|
| Coin cell | VSNVS from LICELL<br>All other blocks off<br>VIN = 0.0 V<br>VSNVSVOLT[2:0] = 110 | No load on VSNVS [1] [2] | 4.0 | 7.0 | µA |
| Off | VSNVS from VIN or LICELL<br>Wake-up from PWRON active<br>32 kHz RC on<br>All other blocks off<br>VIN ≥ UVDET | No load on VSNVS, PMIC able to wake-up [1] [3] | 17 | 25 | µA |
| Sleep | VSNVS from VIN<br>Wake-up from PWRON active<br>Trimmed reference active<br>SW3A/B PFM<br>Trimmed 16 MHz RC off<br>32 kHz RC on<br>VREFDDR disabled | No load on VSNVS. DDR memories in self refresh [1] | 122<br>122 | 220 [4]<br>250 [5] | µA |
| Standby | VSNVS from either VIN or LICELL<br>SW1A/B combined in PFM<br>SW1C in PFM<br>SW2 in PFM<br>SW3A/B combined in PFM<br>SW4 in PFM<br>SWBST off<br>Trimmed 16 MHz RC enabled<br>Trimmed reference active<br>VGEN1 to 6 enabled<br>VREFDDR enabled | No load on VSNVS. Processor enabled in lowpower mode. All rails powered on except boost (load = 0 mA) [1] | 297<br>297 | 450 [4]<br>550 [5] | µA |

[1] For PFM operation, headroom should be 300 mV or greater.
[2] Additional current may be drawn in the coin cell mode when RESETBMCU is pulled up to VSNVS due to an internal path from RESETBMCU to $V_{IN}$. The additional current is < 30 µA with a pullup resistor of 100 kΩ.
[3] When VIN is below the UVDET threshold, in the range of 1.8 V ≤ $V_{IN}$ < 2.65 V, the quiescent current increases by 50 µA, typically.
[4] From −40 °C to 85 °C
[5] From −40 °C to 105 °C

# 9 Detailed description

The PF4210 is the power management integrated circuit (PMIC) designed primarily for use with NXP's i.MX 8M family of applications processors.

## 9.1 Features

This section summarizes the PF4210 features.

- Input voltage range to PMIC: 2.8 V to 4.5 V
- Buck regulators
  - Four to six channel configurable
    - SW1A/B/C, 4.5 A (single); 0.3 V to 1.875 V
    - SW1A/B, 2.5 A (single/dual); SW1C 2.0 A (independent); 0.3 V to 1.875 V
    - SW2, 2.5 A; 0.4 V to 3.3 V
    - SW3A/B, 3.0 A (single/dual); 0.4 V to 3.3 V
    - SW3A, 1.5 A (independent); SW3B, 1.5 A (independent); 0.4 V to 3.3 V
    - SW4, 1.0 A; 0.4 V to 3.3 V
    - SW4, VTT mode provide DDR termination at 50 % of SW3A
  - Dynamic voltage scaling
  - Modes: PWM, PFM, APS
  - Programmable output voltage
  - Programmable current limit
  - Programmable soft start
  - Programmable PWM switching frequency
  - Programmable OCP with fault interrupt
- Boost regulator
  - SWBST, 5.0 V to 5.15 V, 0.6 A, OTG support
  - Modes: PFM and auto
  - OCP fault interrupt
- LDOs
  - Six user-programmable LDOs
    - VGEN1, 0.80 V to 1.55 V, 100 mA
    - VGEN2, 0.80 V to 1.55 V, 250 mA
    - VGEN3, 1.8 V to 3.3 V, 100 mA
    - VGEN4, 1.8 V to 3.3 V, 350 mA
    - VGEN5, 1.8 V to 3.3 V, 100 mA
    - VGEN6, 1.8 V to 3.3 V, 200 mA
- Soft start
- LDO/switch supply
  - VSNVS (1.0/1.1/1.2/1.3/1.5/1.8/3.0 V), 1.5 mA (consumer version), 1.0 mA (industrial version)
- DDR memory reference voltage
  - VREFDDR, 0.6 V to 0.9 V, 10 mA
- 16 MHz internal master clock
- OTP (one time programmable) memory for device configuration
  - User programmable start-up sequence and timing
- Battery backed memory including coin cell charger
- $I^2C$ interface
- User programmable standby, sleep, and off modes

## 9.2 Functional block diagram

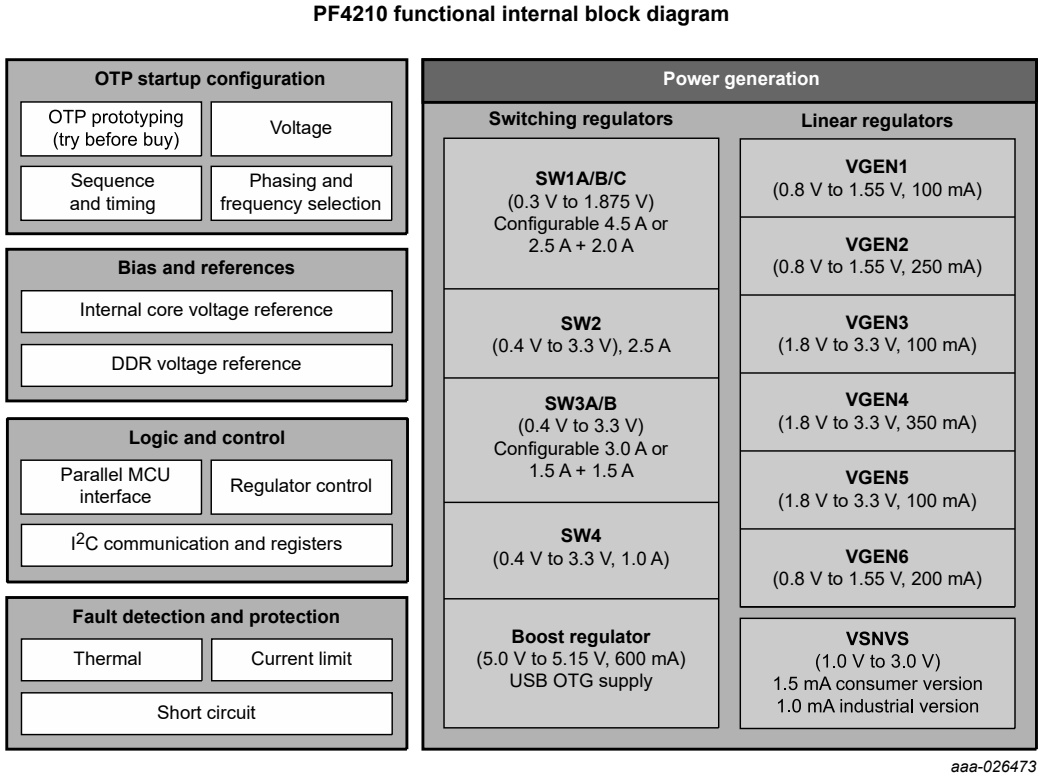


**Figure 4. Functional block diagram**

## 9.3 Functional description

### 9.3.1 Power generation

The PF4210 PMIC features four buck regulators (up to six independent outputs), one boost regulator, six general purpose LDOs, one switch/LDO combination and a DDR voltage reference to supply voltage for the application processor and peripheral devices.

The number of independent buck regulator outputs can be configured from four to six, thereby providing flexibility to operate with higher current capability, or to operate as independent outputs for applications requiring more voltage rails with lower current demands. SW1 and SW3 regulators can be configured as single/dual phase and/or independent converters. One of the buck regulators, SW4, can also operate as a tracking regulator when used for memory termination.

The buck regulators provide supply to processor cores and to other low voltage circuits such as IO and memory. Dynamic voltage scaling is provided to allow controlled supply rail adjustments for the processor cores and/or other circuitry.

Depending on the system power path configuration, the six general purpose LDO regulators can be directly supplied from the main input supply or from the switching regulators to power peripherals, such as audio, camera, bluetooth, and wireless LAN. A specific VREFDDR voltage reference is included to provide an accurate reference voltage for DDR memories operating with or without VTT termination. The VSNVS block

behaves as an LDO, or as a bypass switch to supply the SNVS/SRTC circuitry in the i.MX processors; VSNVS may be powered from VIN, or from a coin cell.

### 9.3.2 Control logic

The PF4210 PMIC is fully programmable via the $I^2C$ interface. Additional communication is provided by direct logic interfacing including interrupt and reset. Startup sequence of the device is selected based on the initial OTP configuration explained in the Section 10.1 "Startup", or by configuring the Try Before Buy feature to test different power up sequences before choosing the final OTP configuration.

The PF4210 PMIC has interfaces for the power buttons and a dedicated signaling interface with the processor. It also ensures supply of critical internal logic and other circuits from the coin cell, in case of brief interruptions from the main battery. A charger for the coin cell is included as well.

#### 9.3.2.1 Interface signals

##### 9.3.2.1.1 PWRON

PWRON is an input signal to the IC generating a turn on event. It can be configured to detect a level, or an edge using the PWRON_CFG bit. See Section 10.4.2.1 "Turn on events" for more details.

##### 9.3.2.1.2 STANDBY

STANDBY is an input signal to the IC. When it is asserted, the part enters standby mode and when deasserted, the part exits standby mode. STANDBY can be configured as active high or active low using the STANDBYINV bit. See Section 10.4.1.3 "Standby mode" for more details.

***Note:*** *When operating the PMIC at VIN ≤ 2.85 V and VSNVS is programmed for a 3.0 V output, a coin cell must be present to provide VSNVS, or the PMIC does not reliably enter and exit the standby mode.*

##### 9.3.2.1.3 RESETBMCU

RESETBMCU is an open drain, active low output configurable for two modes of operation. In default mode, it is deasserted 2.0 ms to 4.0 ms after the last regulator if the startup sequence is enabled (see Figure 5). In this mode, the signal can be used to bring the processor out of reset, or as an indicator that all supplies have been enabled; it is only asserted for a turn off event.

When configured for fault mode, RESETBMCU is deasserted after the startup sequence is completed only if no faults occurred during startup. At anytime, if a fault occurs and persists for 1.8 ms typically, RESETBMCU is asserted, LOW. The PF4210 is turned off if the fault persists for more than 100 ms typically.

The PWRON signal restarts the part, though if the fault persists, the sequence described above is repeated. To enter the fault mode, set bit OTP_PG_EN of register OTP PWRGD EN to 1. This register, 0xE8, is located in Table 135 of the register map. To test the fault mode, the bit may be set during TBB prototyping, or the mode may be permanently chosen by programming OTP fuses.

#### 9.3.2.1.4 SDWNB

SDWNB is an open drain, active low output notifying the processor of an imminent PMIC shut down. It is asserted low for one 32 kHz clock cycle before powering down and is then deasserted in the OFF state.

#### 9.3.2.1.5 INTB

INTB is an open drain, active low output. It is asserted when any fault occurs, provided the fault interrupt is unmasked. INTB is deasserted after the fault interrupt is cleared by software, which requires writing a 1 to the fault interrupt bit.

# 10 Functional block requirements and behaviors

## 10.1 Startup

The PF4210 can be configured to start up from either the internal OTP configuration, or with a hard coded configuration built into the device. The internal hard coded configuration is enabled by connecting the VDDOTP pin to VCOREDIG through a 100 kΩ resistor. The OTP configuration is enabled by connecting VDDOTP to GND.

For NP (nonprogrammed) devices, selecting the OTP configuration causes the PF4210 to not start up. However, the PF4210 can be controlled through the $I^2C$ port for prototyping and programming. Once programmed, the NP device starts up with the customer programmed configuration.

### 10.1.1 Device startup configuration

Table 8 shows the default configuration for all devices and the preprogrammed OTP configurations.

**Table 8. Startup configuration**

| Registers | Default configuration | Preprogrammed OTP configuration | | |
|---|---|---|---|---|
| | A0 | A1 | A2 | A3 |
| Default I2C addr | 0x08 | | | |
| VSNVS_VOLT | 3.0 V | 1.0 V | 1.0 V | 1.0 V |
| SW1AB_VOLT | 1.375 V | 0.9 V | 0.9 V | 0.9 V |
| SW1AB_SEQ | 1 | 4 | 4 | 4 |
| SW1C_VOLT | 1.375 V | 0.9 V | 0.9 V | 0.9 V |
| SW1C_SEQ | 1 | 4 | 4 | 4 |
| SW2_VOLT | 3.0 V | 1.1 V | 1.2 V | 1.35 V |
| SW2_SEQ | 2 | 6 | 6 | 6 |
| SW3A_VOLT | 1.5 V | 1.0 V | 1.0 V | 1.0 V |
| SW3A_SEQ | 3 | 4 | 4 | 4 |
| SW3B_VOLT | 1.5 V | 1.0 V | 1.0 V | 1.0 V |
| SW3B_SEQ | 3 | 4 | 4 | 4 |

| Registers | Default configuration | Preprogrammed OTP configuration | | |
|---|---|---|---|---|
| | A0 | A1 | A2 | A3 |
| SW4_VOLT | 1.8 V | 1.8 V | 1.8 V | 1.8 V |
| SW4_SEQ | 3 | 6 | 6 | 6 |
| SWBST_VOLT | — | — | — | — |
| SWBST_SEQ | — | — | — | — |
| VREFDDR_SEQ | 3 | 6 | 6 | 6 |
| VGEN1_VOLT | — | 1.5 V | 1.5 V | 1.5 V |
| VGEN1_SEQ | — | 31 | 31 | 31 |
| VGEN2_VOLT | 1.5 V | 0.9 V | 0.9 V | 0.9 V |
| VGEN2_SEQ | 2 | 7 | 7 | 7 |
| VGEN3_VOLT | — | 1.8 V | 1.8 V | 1.8 V |
| VGEN3_SEQ | — | 7 | 7 | 7 |
| VGEN4_VOLT | 1.8 V | 1.8 V | 1.8 V | 1.8 V |
| VGEN4_SEQ | 3 | 5 | 5 | 5 |
| VGEN5_VOLT | 2.5 V | 3.3 V | 3.3 V | 3.3 V |
| VGEN5_SEQ | 3 | 7 | 7 | 7 |
| VGEN6_VOLT | 2.8 V | 2.8 V | 2.8 V | 2.8 V |
| VGEN6_SEQ | 3 | 31 | 31 | 31 |
| PU CONFIG, SEQ_CLK_SPEED | 1.0 ms | 2.0 ms | 2.0 ms | 2.0 ms |
| PU CONFIG, SWDVS_CLK | 6.25 mV/ms | 1.5625 mV/ms | 1.5625 mV/ms | 1.5625 mV/ms |
| PU CONFIG, PWRON | Level sensitive | | | |
| SW1AB CONFIG | SW1AB single phase, SW1C independent mode, 2.0 MHz | | | |
| SW1C CONFIG | 2.0 MHz | | | |
| SW2 CONFIG | | | | |
| SW3A CONFIG | SW3AB single phase mode, 2.0 MHz | | | |
| SW3B CONFIG | 2.0 MHz | | | |
| SW4 CONFIG | | | | |
| PG EN | RESETBMCU in default mode | | | |

***Notes:***

- *Keep bit SW2ILIM = 0 for A1, A2, and A3 for max. rated output load current.*
- *Keep bit SW3xILIM = 0 for A1, A2, and A3 for max. rated output load current.*

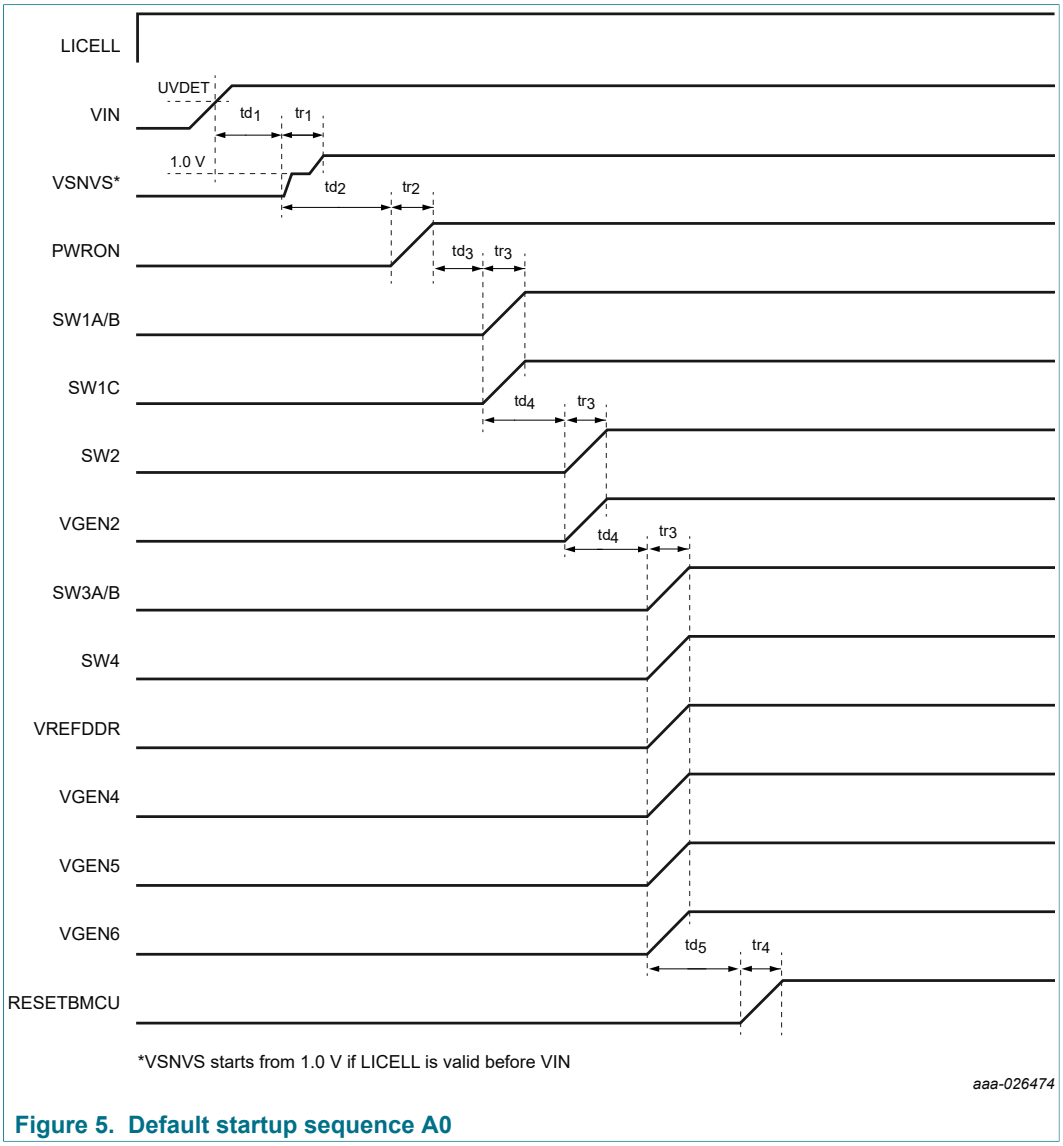


**Figure 5. Default startup sequence A0**

**Table 9. Default startup sequence timing**

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{D1}$ | Turn-on delay of VSNVS [1] | — | 5.0 | — | ms |
| $t_{R1}$ | Rise time of VSNVS | — | 3.0 | — | ms |
| $t_{D2}$ | User determined delay | — | 1.0 | — | ms |
| $t_{R2}$ | Rise time of PWRON | — | [2] | — | ms |
| $t_{D3}$ | Turn-on delay of first regulator | | | | ms |
| | SEQ_CLK_SPEED[1:0] = 00 | — | 2.0 | — | |
| | SEQ_CLK_SPEED[1:0] = 01 [3] | — | 2.5 | — | |
| | SEQ_CLK_SPEED[1:0] = 10 | — | 4.0 | — | |
| | SEQ_CLK_SPEED[1:0] = 11 | — | 7.0 | — | |
| $t_{R3}$ | Rise time of regulators [4] | — | 0.2 | — | ms |

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{D4}$ | Delay between regulators | | | | ms |
| | SEQ_CLK_SPEED[1:0] = 00 | — | 0.5 | — | |
| | SEQ_CLK_SPEED[1:0] = 01 | — | 1.0 | — | |
| | SEQ_CLK_SPEED[1:0] = 10 | — | 2.0 | — | |
| | SEQ_CLK_SPEED[1:0] = 11 | — | 4.0 | — | |
| $t_{R4}$ | Rise time of RESETBMCU | — | 0.2 | — | ms |
| $t_{D5}$ | Turn-on delay of RESETBMCU | — | 2.0 | — | ms |

[1] Assume LICELL voltage is valid before VIN is applied. If LICELL is not valid before VIN is applied, then VSNVS turn on delay may extend to a maximum of 24 ms.
[2] Depends on the external signal driving PWRON.
[3] Default configuration
[4] Rise time is a function of slew rate of regulators and nominal voltage selected.

### 10.1.2 One time programmability (OTP)

OTP allows the programming of startup configurations for a variety of applications. Before permanently programming the IC by programming fuses, a configuration may be prototyped by using the Try Before Buy (TBB) feature. An error correction code (ECC) algorithm is available to correct a single bit error and to detect multiple bit errors when fuses are programmed.

The parameters which can be configured by OTP are listed below.

- General: $I^2C$ slave address, PWRON pin configuration, startup sequence and timing
- Output voltage, dual/single phase or independent mode configuration, switching frequency, and soft start ramp rate
- Boost regulator and LDOs: output voltage

***Note:*** *When prototyping or programming fuses, ensure register settings are consistent with the hardware configuration. This is important for the buck regulators, where the quantity, size, and value of the inductors depend on the configuration (single/ dual phase or independent mode) and the switching frequency. Additionally, if an LDO is powered by a buck regulator, it is gated by the buck regulator in the startup sequence.*

#### 10.1.2.1 Startup sequence and timing

Each regulator has 5-bit allocated to program its startup time slot from a turn on event; therefore, each can be placed from position one to thirty-one in the startup sequence.

The all zeros code indicates a regulator is not part of the startup sequence and remains off (see Table 10). The delay between each position is equal; however, four delay options are available (see Table 11). The startup sequence terminates at the last programmed regulator.

**Table 10. Startup sequence**

| SWxx_SEQ[4:0]/ VGENx_SEQ[4:0]/ VREFDDR_SEQ[4:0] | Sequence |
|---|---|
| 00000 | Off |
| 00001 | SEQ_CLK_SPEED[1:0] * 1 |
| 00010 | SEQ_CLK_SPEED[1:0] * 2 |

| SWxx_SEQ[4:0]/ VGENx_SEQ[4:0]/ VREFDDR_SEQ[4:0] | Sequence |
|---|---|
| * | * |
| * | * |
| * | * |
| * | * |
| 11111 | SEQ_CLK_SPEED[1:0] * 31 |

**Table 11. Startup sequence clock speed**

| SEQ_CLK_SPEED[1:0] | Time (µs) |
|---|---|
| 00 | 500 |
| 01 | 1000 |
| 10 | 2000 |
| 11 | 4000 |

#### 10.1.2.2 PWRON pin configuration

The PWRON pin can be configured as either a level sensitive input (PWRON_CFG = 0), or as an edge sensitive input (PWRON_CFG = 1). As a level sensitive input, an active high signal turns on the part and an active low signal turns off the part, or puts it into sleep mode.

As an edge sensitive input, such as when connected to a mechanical switch, a falling edge turns on the part and if the switch is held low for greater than or equal to 4.0 seconds, the part turns off or enters sleep mode.

**Table 12. PWRON configuration**

| PWRON_CFG | Mode |
|---|---|
| 0 | PWRON pin HIGH = ON<br>PWRON pin LOW = OFF or sleep mode |
| 1 | PWRON pin pulled LOW momentarily = ON<br>PWRON pin LOW for 4.0 seconds = OFF or sleep mode |

#### 10.1.2.3 $I^2C$ address configuration

The $I^2C$ device address can be programmed from 0x08 to 0x0F. This allows flexibility to change the $I^2C$ address to avoid bus conflicts.

Address bit, I2C_SLV_ADDR[3] in OTP_I2C_ADDR register is hard coded to 1 while the lower three LSBs of the $I^2C$ address (I2C_SLV_ADDR[2:0]) are programmable as shown in Table 13.

**Table 13. $I^2C$ address configuration**

| I2C_SLV_ADDR[3] hard coded | I2C_SLV_ADDR[2:0] | $I^2C$ device address (Hex) |
|---|---|---|
| 1 | 000 | 0x08 |

| I2C_SLV_ADDR[3] hard coded | I2C_SLV_ADDR[2:0] | $I^2C$ device address (Hex) |
|---|---|---|
| 1 | 001 | 0x09 |
| 1 | 010 | 0x0A |
| 1 | 011 | 0x0B |
| 1 | 100 | 0x0C |
| 1 | 101 | 0x0D |
| 1 | 110 | 0x0E |
| 1 | 111 | 0x0F |

#### 10.1.2.4 Soft start ramp rate

The startup ramp rate or soft start ramp rate can be selected from the options shown in Section 10.4.4.2.1 "Dynamic voltage scaling".

### 10.1.3 OTP prototyping

Before permanently programming fuses, it is possible to test the desired configuration by using the Try Before Buy feature. With this feature, the configuration is loaded from the OTP registers. These registers serve as temporary storage for the values to be written to the fuses, for the values read from the fuses, or for the values read from the default configuration. To avoid confusion, these registers are referred to as the TBBOTP registers. The portion of the register map concerned with OTP is shown in Table 135 and Table 136.

The contents of the TBBOTP registers are initialized to zero when a valid $V_{IN}$ is first applied. The values loaded into the TBBOTP registers depend on the setting of the VDDOTP pin and on the value of the TBB_POR and FUSE_POR_XOR bits (see Table 14).

- If VDDOTP = VCOREDIG (1.5 V), the values are loaded from the default configuration.
- If VDDOTP = 0.0 V, TBB_POR = 0 and FUSE_POR_XOR = 1, the values are loaded from the fuses. In the PF4210, FUSE_POR1, FUSE_POR2, and FUSE_POR3 are XOR'ed into the FUSE_POR_XOR bit. The FUSE_POR_XOR has to be 1 for fuses to be loaded. This can be achieved by setting any one or all of the FUSE_PORx bits. It is required to set all of the FUSE_PORx bits to be able to load the fuses.
- If VDDOTP = 0.0 V, TBB_POR = 0 and FUSE_POR_XOR = 0, the TBBOTP registers remain initialized at zero.

The initial value of TBB_POR is always 0; only when VDDOTP = 0.0 V and TBB_POR is set to 1 and the values from the TBBOTP registers maintained and not loaded from a different source.

The contents of the TBBOTP registers are modified by $I^2C$. To communicate with $I^2C$, VIN must be valid and VDDIO to which SDA and SCL are pulled up, must be powered by a 1.7 V to 3.6 V supply. VIN or the coin cell voltage must be valid to maintain the contents of the registers. To power on with the contents of the TBBOTP registers, the following conditions must exist:

- VIN is valid
- VDDOTP = 0.0 V

- TBB_POR = 1
- Valid turn on event

### 10.1.4 Reading OTP fuses

As described in the previous section, the contents of the fuses are loaded to the TBBOTP registers when the following conditions are met:

- VIN is valid
- VDDOTP = 0.0 V
- TBB_POR = 0
- FUSE_POR_XOR = 1

If ECC were enabled at the time the fuses were programmed, the error corrected values can be loaded into the TBBOTP registers if desired. Once the fuses are loaded and a turn on event occurs, the PMIC powers on with the configuration programmed in the fuses.

### 10.1.5 Programming OTP fuses

The parameters which can be programmed are shown in the TBBOTP registers in Table 135 of the register map. The PF4210 offers ECC, the control registers for which functions are located in Table 136 of the register map.

There are ten banks of twenty-six fuses each that can be programmed. Programming the fuses requires an 8.25 V, 100 mA supply powering the VDDOTP pin, bypassed with 10 to 20 µF of capacitance.

**Table 14. Source of startup sequence**

| VDDOTP (V) | TBB_POR | FUSE_POR_XOR | Startup sequence |
|---|---|---|---|
| 0 | 0 | 0 | None |
| 0 | 0 | 1 | OTP fuses |
| 0 | 1 | x | TBBOTP registers |
| 1.5 | x | x | Default configuration |

## 10.2 16 MHz and 32 kHz clocks

There are two clocks: a trimmed 16 MHz, RC oscillator, and an untrimmed 32 kHz, RC oscillator. The 16 MHz oscillator is specified within −8.0/+8.0 %.

The 32 kHz untrimmed clock is only used in the following conditions:

- VIN < UVDET
- All regulators are in sleep mode
- All regulators are in PFM switching mode

A 32 kHz clock, derived from the 16 MHz trimmed clock, is used when accurate timing is needed under the following conditions:

- During start up, VIN > UVDET
- PWRON_CFG = 1, for power button debounce timing

In addition, when the 16 MHz is active in the ON mode, the debounce time in Table 25 are referenced to the 32 kHz derived from the 16 MHz clock. The exceptions are the LOWVINI and PWRONI interrupts, which are referenced to the 32 kHz untrimmed clock.

**Table 15. 16 MHz clock specifications**

*$T_{MIN}$ to $T_{MAX}$ (see Table 4), $V_{IN}$ = 2.8 V to 4.5 V, LICELL = 1.8 V to 3.3 V and typical external component values. Typical values are characterized at $V_{IN}$ = 3.6 V, LICELL = 3.0 V, and 25 °C, unless otherwise noted.*

| Symbol | Parameters | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{IN16MHz}$ | Operating voltage from VIN | 2.8 | — | 4.5 | V |
| $f_{16MHZ}$ | 16 MHz clock frequency | 14.7 | 16 | 17.2 | MHz |
| $f_{2MHZ}$ | 2.0 MHz clock frequency [1] | 1.84 | — | 2.15 | MHz |

[1] 2.0 MHz clock is derived from the 16 MHz clock.

### 10.2.1 Clock adjustment

The 16 MHz clock and hence the switching frequency of the regulators, can be adjusted to improve the noise integrity of the system. By changing the factory trim values of the 16 MHz clock, the user may add an offset as small as ±3.0 % of the nominal frequency. Contact your NXP representative for detailed information on this feature.

## 10.3 Bias and references block description

### 10.3.1 Internal core voltage references

All regulators use the main band gap as the reference. The main band gap is bypassed with a capacitor at VCOREREF. The band gap and the rest of the core circuitry are supplied from VCORE.

The performance of the regulator is directly dependent on the performance of the band gap. No external DC loading is allowed on VCORE, VCOREDIG, or VCOREREF. VCOREDIG is powered as long as there is a valid supply and/or valid coin cell. Table 16 shows the main characteristics of the core circuitry.

**Table 16. Core voltages electrical specifications**

*$T_{MIN}$ to $T_{MAX}$ (see Table 4), $V_{IN}$ = 2.8 V to 4.5 V, LICELL = 1.8 V to 3.3 V, and typical external component values. Typical values are characterized at $V_{IN}$ = 3.6 V, LICELL = 3.0 V, and 25 °C, unless otherwise noted.[1]*

| Symbol | Parameters | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **VCOREDIG (digital core supply)** | | | | | |
| $V_{COREDIG}$ | Output voltage [2] | | | | V |
| | ON mode | — | 1.5 | — | |
| | Coin cell mode and OFF | — | 1.3 | — | |
| **VCORE (analog core supply)** | | | | | |
| $V_{CORE}$ | Output voltage | | | | V |
| | ON mode and charging | — | 2.775 | — | |
| | OFF and coin cell mode | — | 0.0 | — | |
| **VCOREREF (band gap / regulator reference)** | | | | | |

| Symbol | Parameters | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{COREREF}$ | Output voltage | — | 1.2 | — | V |
| $V_{COREREFACC}$ | Absolute accuracy | — | 0.5 | — | % |
| $V_{COREREFTACC}$ | Temperature drift | — | 0.25 | — | % |

[1] For information only
[2] 3.0 V < $V_{IN}$ < 4.5 V, no external loading on VCOREDIG, VCORE, or VCOREREF. Extended operation down to UVDET, but no system malfunction.

#### 10.3.1.1 External components

**Table 17. External components for core voltage**

| Regulator | Capacitor value (µF) |
|---|---|
| VCOREDIG | 1.0 |
| VCORE | 1.0 |
| VCOREREF | 0.22 |

### 10.3.2 VREFDDR voltage reference

VREFDDR is an internal PMOS half supply voltage follower capable of supplying up to 10 mA. The output voltage is at one half the input voltage. It is typically used as the reference voltage for DDR memories.

A filtered resistor divider is utilized to create a low frequency pole. This divider then utilizes a voltage follower to drive the load.

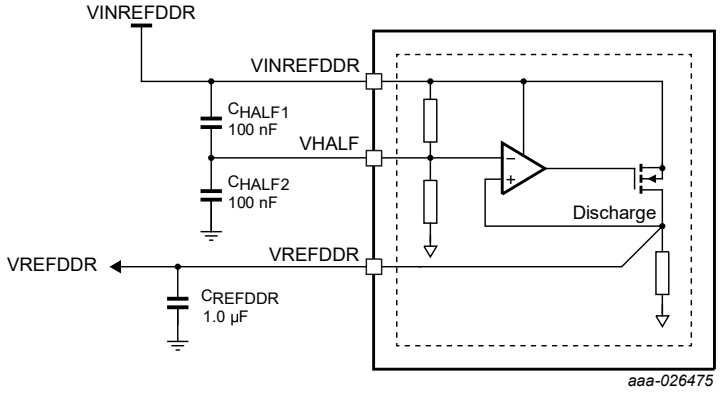


**Figure 6. VREFDDR block diagram**

#### 10.3.2.1 VREFDDR control register

The VREFDDR voltage reference is controlled by a single bit in VREFDDCRTL register in Table 18.

**Table 18. Register VREFDDCRTL – ADDR 0x6A**

| Name | Bit number | R/W | Default | Description |
|---|---|---|---|---|
| UNUSED | 3:0 | — | 0x00 | unused |

| Name | Bit number | R/W | Default | Description |
|---|---|---|---|---|
| VREFDDREN | 4 | R/W | 0x00 | Enables or disables VREFDDR output voltage<br>• 0 = VREFDDR disabled<br>• 1 = VREFDDR enabled |
| UNUSED | 7:5 | — | 0x00 | unused |

#### 10.3.2.1.1 External components

**Table 19. VREFDDR external components**

| Capacitor [1] | Capacitance (µF) |
|---|---|
| VINREFDDR to VHALF [2] | 0.1 |
| VHALF to GND | 0.1 |
| VREFDDR | 1.0 |

[1] Use X5R or X7R capacitors.
[2] VINREFDDR to GND, 1.0 µF minimum capacitance is provided by buck regulator output.

#### 10.3.2.1.2 VREFDDR specifications

**Table 20. VREFDDR electrical characteristics**

*$T_{MIN}$ to $T_{MAX}$ (see Table 4), $V_{IN}$ = 3.6 V, $I_{REFDDR}$ = 0.0 mA, $V_{INREFDDR}$ = 1.5 V and typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN}$ = 3.6 V, $I_{REFDDR}$ = 0.0 mA, $V_{INREFDDR}$ = 1.5 V, and 25 °C, unless otherwise noted.*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **VREFDDR** | | | | | |
| $V_{INREFDDR}$ | Operating input voltage range | 1.1 | — | 1.8 | V |
| $I_{REFDDR}$ | Operating load current range | 0.0 | — | 10 | mA |
| $I_{REFDDRLIM}$ | Current limit<br>$I_{REFDDR}$ when $V_{REFDDR}$ is forced to $V_{INREFDDR}/4$ | 10.5 | 15 | 25 | mA |
| $I_{REFDDRQ}$ | Quiescent current [1] | — | 8.0 | — | µA |
| **Active mode – DC** | | | | | |
| $V_{REFDDR}$ | Output voltage<br>1.2 V < $V_{INREFDDR}$ < 1.8 V<br>0.0 mA < $I_{REFDDR}$ < 10 mA | — | $V_{INREFDDR}/2$ | — | V |
| | 1.1 V ≤ $V_{INREFDDR}$ ≤ 1.2 V<br>0.0 mA < $I_{REFDDR}$ ≤ 1.0 mA | — | $V_{INREFDDR}/2$ | — | |
| $V_{REFDDRTOL}$ | Output voltage tolerance ($T_A$ = 0 °C to 85 °C)<br>1.2 V < $V_{INREFDDR}$ < 1.8 V<br>0.6 mA ≤ $I_{REFDDR}$ ≤ 10 mA | −1.0 | — | 1.0 | % |
| | 1.1 V ≤ $V_{INREFDDR}$ ≤ 1.2 V<br>0.0 mA < $I_{REFDDR}$ ≤ 1.0 mA | −1.0 | — | 1.0 | |

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{REFDDRTOL}$ | Output voltage tolerance ($T_A$ = −40 °C to 105 °C), applicable to the industrial version | | | | % |
| | 1.2 V < $V_{INREFDDR}$ < 1.8 V<br>0.6 mA ≤ $I_{REFDDR}$ ≤ 10 mA | –1.2 | — | 1.2 | |
| | 1.1 V ≤ $V_{INREFDDR}$ ≤ 1.2 V<br>0.0 mA < $I_{REFDDR}$ ≤ 1.0 mA | –1.2 | — | 1.2 | |
| $V_{REFDDRLOR}$ | Load regulation | | | | mV/mA |
| | 1.0 mA < $I_{REFDDR}$ < 10 mA<br>1.2 V < $V_{INREFDDR}$ < 1.8 V | — | 0.40 | — | |
| | 0.1 mA < $I_{REFDDR}$ < 1.0 mA<br>1.1 V ≤ $V_{INREFDDR}$ ≤ 1.2 V | — | 1.15 | — | |
| **Active mode – AC** | | | | | |
| $t_{ONREFDDR}$ | Turn on time<br>Enable to 90 % of end value<br>$V_{INREFDDR}$ = 1.1 V, 1.2 V, 1.8 V<br>$I_{REFDDR}$ = 0.0 mA | — | — | 100 | µs |
| $t_{OFFREFDDR}$ | Turn off time<br>Disable to 10 % of initial value<br>$V_{INREFDDR}$ = 1.1 V, 1.2 V, 1.8 V<br>$I_{REFDDR}$ = 0.0 mA | — | — | 10 | ms |
| $V_{REFDDROSH}$ | Startup overshoot<br>$V_{INREFDDR}$ = 1.1 V, 1.2 V, 1.8 V<br>$I_{REFDDR}$ = 0.0 mA | — | 1.0 | 6.0 | % |
| $V_{REFDDRTLR}$ | Transient load response<br>$V_{INREFDDR}$ = 1.1 V, 1.2 V, 1.8 V | — | 5.0 | — | mV |

[1] When VREFDDR is off there is a quiescent current of 1.5 µA typical.

## 10.4 Power generation

### 10.4.1 Modes of operation

The operation of the PF4210 can be reduced to five states or modes: on, off, sleep, standby, and coin cell.

Figure 7 shows the state diagram of the PF4210, along with the conditions to enter and exit from each state.