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Order Number: MC33388/D
Rev. 2.3, 2001

Fault Tolerant CAN Interface

MC33388

AUTOMOTIVE FAULT TOLERANT CAN PHYSICAL LAYER

SEMICONDUCTOR TECHNICAL DATA

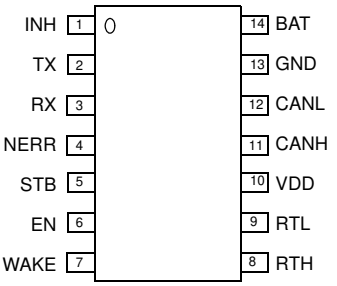
D SUFFIX
PLASTIC PACKAGE
CASE 751A-03
SO-14

The MC33388 is a CAN physical interface device, dedicated to automotive body electronic multiplexing applications. It operates in differential mode, allowing ground shifts up to 1.5V, reducing RFI disturbances. It offers very low standby current in sleep and standby mode operation and supports communication speeds up to 125kBauds.

It is fully protected against harsh automotive environments and the driver is able to detect fault conditions and automatically switches into appropriate default mode. Under fault condition, it continuously monitors bus failures in order to switch back to normal bus operation as soon as faults disappeared.

- Very low sleep/standby current (15uA typical)
- Baud rate from 10kBaud up to 125kBauds
- Automatic switching to single wire mode in case of bus failures and return to differential mode if bus failures disappear
- Supports one wire transmission modes with ground offset up to 1.5V
- Internal bus driver slope control function to minimize RFI
- Bus line short-circuit protected to battery, VDD and ground
- Bus line protected against automotive transients
- Thermal protection of bus line drivers
- Supports unshielded twisted pair bus
- An unpowered node does not disturb the bus lines
- Wake-up capability triggered from bus message and wake-up input pin
- Wake up pin with dual edges sensitivity
- Battery fail flag reported on NERR output
- Ambient temperature range from -40°C to 125°C

PIN CONNECTIONS

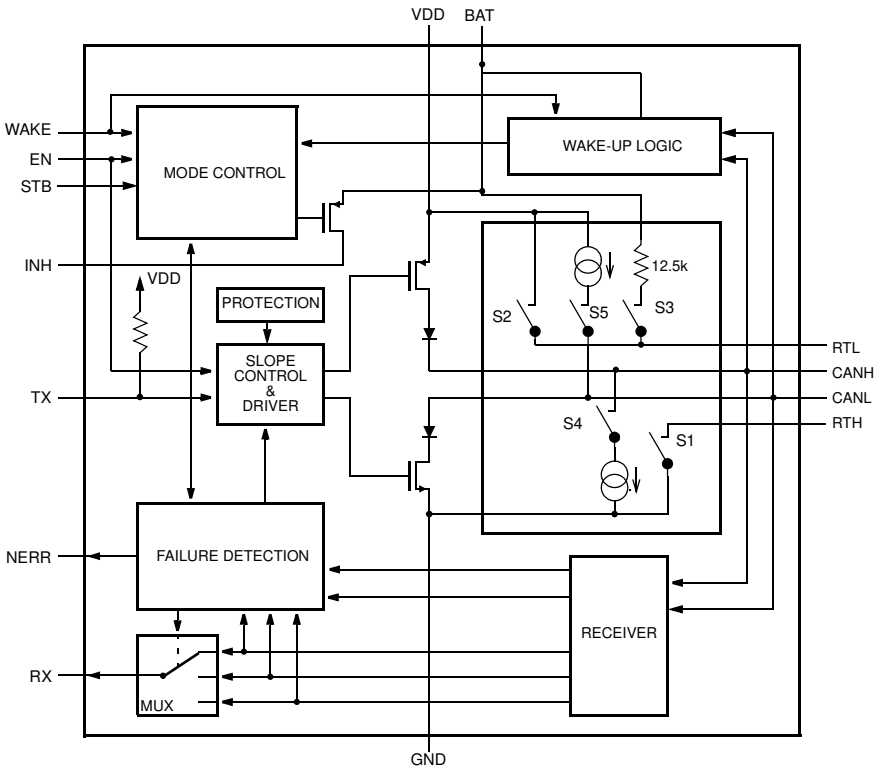


(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33388D	T_A = -40 to 125°C	SO-14

Simplified Block Diagram



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MAXIMUM RATING

Ratings	Symbol	Min	Typ	Max	Unit
DC Supply Voltage Pin 10	V_{DD}	-0.3		6	V
DC Voltage On Pins 2, 3, 4, 5, 6 and 7	V_{DD}	-0.3		V_{DD} + 0.3	V
DC Voltage On Pins 11, 12	V_{BUS}	-20		+27	V
Transient Voltage At Pins 11, 12 $0 < V_{DD} < 5.5V$; $V_{BAT} \geq 0$; $T < 500ms$	V_{CANH}/V_{CANL}	-40		40	V
Transient Voltage On Pins 11, 12 (Coupled Through 1nF Capacitor)	V_{tr}	-150		100	V
DC Voltage On Pin 7	V_{wake}			V_{BAT} +0.3	V
Current In Pin 7	I_{wake}	-15		3	mA
DC Voltage On Pins 1	V_{inh}	-0.3		V_{BAT} + 0.3	V
DC Voltage On Pins 8, 9	V_{rtl}, V_{rth}	-0.3		40	V
DC Voltage On Pins 14	V_{BAT}	-0.3		27	V
Voltage On Pins 14 (Load Dump, 500ms)	V_{BAT}			40	V
ESD Voltage On Any Pins (HBM.100pF ; 1.5kΩ)	V_{ESD}	-3.0		3.0	kV
ESD Voltage On Any Pins (MM.200pF ; 0Ω)	V_{ESD}	-200		200	V
Junction Temperature	T_j	-40		150	°C
Storage Temperature	T_{stg}	-55		150	°C
RTH, RTL Termination Resistance	R_t	500		16000	Ω

THERMAL RATINGS

Ratings	Symbol	Value	Unit
Thermal Resistance From Junction To Ambient	$R_{th\ j/a}$	120	°C/W

ELECTRICAL CHARACTERISTICS V_{DD} = 4,75 to 5,25; V_{BAT}=6 to 27V; T_{amb} = -40 to 125°C unless otherwise specified

Conditions	Symbol	Min	Typ	Max	Unit
SUPPLY					
Vdd Supply Current (Normal Mode) TX= VDD, Recessive State	I_{VDD}		2.3	3	mA
Vdd Supply Current (Normal Mode) TX = 0V, No Load, Dominant State	I_{VDD}		3.3	5	mA
Vbat Supply Current (Normal Mode) TX = VDD	I_{BAT}		150	300	µA
Total Supply Current (Receive Only Mode) VDD = 5V; V_{BAT} = 12V	$I_{VDD} + I_{BAT}$		0.85	1.2	mA
Total Supply Current (Vbat Standby Mode) VDD = 5V; V_{BAT} = 12V	$I_{VDD} + I_{BAT}$		20	40	µA
Vbat Supply Current (Sleep Mode) VDD = 0V; V_{BAT} = 12V	I_{BAT}		15	25	µA

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ELECTRICAL CHARACTERISTICS V_{DD} = 4,75 to 5,25; V_{BAT}=6 to 27V; T_{amb} = -40 to 125°C unless otherwise specified

Conditions	Symbol	Min	Typ	Max	Unit
STB, EN, TX Pins					
High Level Input Voltage	V_{ih}	0.7*V_{DD}		V_{DD}+0.3V	V
Low Level Input Voltage	V_{il}	-0.3		0.3 * V_{DD}	V
High Level Input Current (STB, EN) (V_i = 4V)	I_{ih}		20	40	µA
Low Level Input Current (STB, EN) (V_i = 1V)	I_{il}	10	20		µA
TX High Level Input Current (V_i = 4V)	I_{TX}	-25	-80	-200	µA
TX Low Level Input Current (V_i = 1V)	I_{TX}	-100	-320	-800	µA
Forced V_{BAT} Standby Mode (Fail Safe) Threshold	V_{DD}	3	4	4.7	V
Battery Voltage For Setting Power On Flag	V_{BAT}	1.5	3	4	V
RX, NERR Pins					
High Level Output Voltage NERR (I_0 = -100µA)	V_{oh}	V_{DD} - 0.9		V_{DD}	V
High Level Output Voltage RX (I_0 = -250µA)	V_{oh}	V_{DD} - 0.9		V_{DD}	V
Low Level Output Voltage (I_0 = 1.5mA)	V_{ol}	0		0.9	V
WAKE Pin (must be connected to gnd or BAT if not used)					
Typical Wake Up Threshold (V_{STB} = 0V), High to Low Transition, V_{BAT}=6V to 18V. NOTE1.	$Wu_{threshl}$		0.44 V_{BAT}		V
Typical Wake Up Threshold (V_{STB} = 0V), Low To High Transition, V_{BAT}=6V to 18V. NOTE1.	$Wu_{threslh}$		0.57 V_{BAT}		V
Wake Up Threshold Hysteresis	Wu_{hyst}	500			mV
Wake Up Threshold, High to Low Transition at V_{BAT}=12V	Wu_{hl}	3.6		6.5	V
Wake Up Threshold, Low To High Transition at V_{BAT}=12V	Wu_{lh}	6.2		7.5	V
INH Pin					
High Level Voltage Drop (I_{INH} = -0.2mA, INH High)	V_{drop}	0		0.8	V
Leakage Current (Sleep Mode; V_{INH} = 0V)	$I_{l\ inh}$	0		5	µA
CANH, CANL Pins					
Differential Receiver, Recessive To Dominant Threshold (By Definition, V_{diff}=V_{CANH}-V_{CANL})	V_{diff1}	-3.2		-2.5	V
Differential Receiver, Dominant To Recessive Threshold (Bus Failures 1, 2, 5)	V_{diff2}	-3.2		-2.5	V
CANH Recessive Output Voltage TX = VDD ; $R_{(RTH)}$ < 4k	V_{CANH}			0.2	V
CANL Recessive Output Voltage TX = VDD ; $R_{(RTL)}$ < 4k	V_{CANL}	V_{DD} - 0.2			V
CANH Output Voltage, Dominant TX = 0V; I_{CANH} = -40mA; Normal Operating Mode	V_{CANH}	V_{DD} - 1.4			V

Archive Information

ELECTRICAL CHARACTERISTICS V_{DD} = 4,75 to 5,25; V_{BAT}=6 to 27V; T_{amb} = -40 to 125°C unless otherwise specified

Conditions	Symbol	Min	Typ	Max	Unit
CANL Output Voltage, Dominant TX = 0V; I_{CANL} = 40mA; Normal Operating Mode	V_{CANL}			1.4	V
CANH Output Current (V_{CANH} = 0 ; TX = 0)	I_{CANH}	50	75	100	mA
CANL Output Current (V_{CANL} = 14V; TX = 0)	I_{CANL}	50	90	130	mA
Detection Threshold For Short-circuit To Battery Voltage (Normal Mode)	V_{CANH}, V_{CANL}	7.3	7.9	8.9	V
Detection Threshold For Short-circuit To Battery Voltage (Standby/Sleep Mode)	V_{CANH}	V_{BAT}/2 +3		V_{BAT} /2+5	V
CANH Output Current (Sleep Mode; V_{CANH} = 12V, Failure3)			5	10	µA
CANL Output Current (Sleep Mode ; V_{CANL} = 0V ; V_{BAT} = 12V, Failure 4)	I_{CANL}		0	2	µA
CANL Wake Up Voltage Threshold	$V_{wake,L}$	2.5	3.3	3.9	V
CANH Wake Up Voltage Threshold	$V_{wake,H}$	1.2	2	2.7	V
Wake Up Threshold Difference (Hysteresis)	V_{wakeL}-V_{wakeH}	0.2			V
CANH Single Ended Receiver Threshold (Failures 4, 6, 7)	$V_{SE, CANH}$	1.5	1.85	2.15	V
CANL Single Ended Receiver Threshold (Failures 3, 8)	$V_{SE, CANL}$	2.8	3.05	3.4	V
CANL Pull Up Current (Normal Mode, Failures 4, 6 and 7)	$I_{CANL,pu}$	45	75	90	µA
CANH Pull Down Current (Normal Mode, Failure 3)	$I_{CANH,pd}$	45	75	90	µA
Receiver Differential Input Impedance CANH / CANL	R_{diff}	100		180	kΩ
Differential Receiver Common Mode Voltage Range	V_{com}	-10		10	V
CANH To Ground Capacitance	C_{CANH}			50	pF
CANL To Ground Capacitance	C_{CANL}			50	pF
C_{CANL} to C_{CANH} Capacitor Difference (Absolute Value)	DC_{can}			10	pF

RTH, RTL Pins

RTL to VDD Switch On Resistance (I_{out} < -10mA; Normal Operating Mode)	R_{rtl}	10	30	50	Ω
RTL to BAT Switch Series Resistance (VBAT Standby Mode Or Sleep Mode)	R_{rtl}	8	12.5	20	kΩ
RTH To Ground Switch On Resistance (I_{out} <10mA; Normal Operating Mode)	R_{rth}	10	25	50	Ω

Thermal Shutdown

Shutdown Temperature	T_{sd}		165		°C

CHARACTERISTICS V_{DD} = 4,75 to 5,25; V_{BAT}=6 to 27V; T_{amb} = -40 to 125°C unless otherwise specified

CANL and CANH Slew Rates (10% to 90%). Rising or Falling Edges. NOTE2.	T_{sl}	3.5	5	10	V/µs
Propagation Delay TX to RX Low. NOTE2.	T_{pdlow}		1	2	µs
Propagation Delay TX to RX High. NOTE2.	T_{pdhigh}		1	2	µs
Min. Dominant Time For Wake-up On CANL or CANH (Vbat Standby And Sleep Modes; V_{BAT} = 12V)	T_{wake}	8	16	30	µs
Min. WAKE Time For Wake-up (Vbat Standby And Sleep Modes; V_{BAT}= 12V)	T_{wake}	6	15	30	µs
Failure 3 Detection Time (Normal Mode)	T_{df3}	10		60	µs
Failure 6 Detection Time (Normal Mode)	T_{df6}	50		400	µs
Failure 3 Recovery Time (Normal Mode)	T_{dr3}	10		60	µs
Failure 6 Recovery Time (Normal Mode)	T_{dr6}	150		1000	µs
Failure 4, 7, 8 Detection Time (Normal Mode)	T_{df478}	0.75		4	ms
Failure 4, 7, 8 Recovery Time (Normal Mode)	T_{dr478}	10		60	µs
Failure 3, 4, 7,8 Detection Time (Vbat Standby And Sleep Modes; V_{BAT} = 12V)	T_{dr347}	0.8		8	ms
Failure 3, 4, 7,8 Recovery Time (Vbat Standby And Sleep Modes; V_{BAT} = 12V)	T_{dr347}		2.5		ms
Minimum Hold Time For “Go To Sleep” Command	T_{gts}	4		38	µs
Edge Count Difference Between CANH and CANL for Failures 1, 2, 5 Detection (NERR Becomes Low), (Normal Mode)	E_{cdf}		3		
Edge Count Difference Between CANH And CANL For Failures 1, 2, 5 Recovery (Normal Mode)	E_{cdr}		3		
TX Permanent Dominant Timer Disable Time (Normal Mode And Failure Mode)	$t_{TX,d}$	0.75		4	ms
TX Permanent Dominant Timer Enable Time (Normal Mode And Failure Mode)	$t_{TX,e}$	10		60	µs

NOTE:
1. When VBAT is greater than 18V, the wake up thresholds remain identical to the wake up thresholds at 18V.
2. AC Characteristics measured according to schematic figure 2.

Figure 1. Device Signal Waveforms

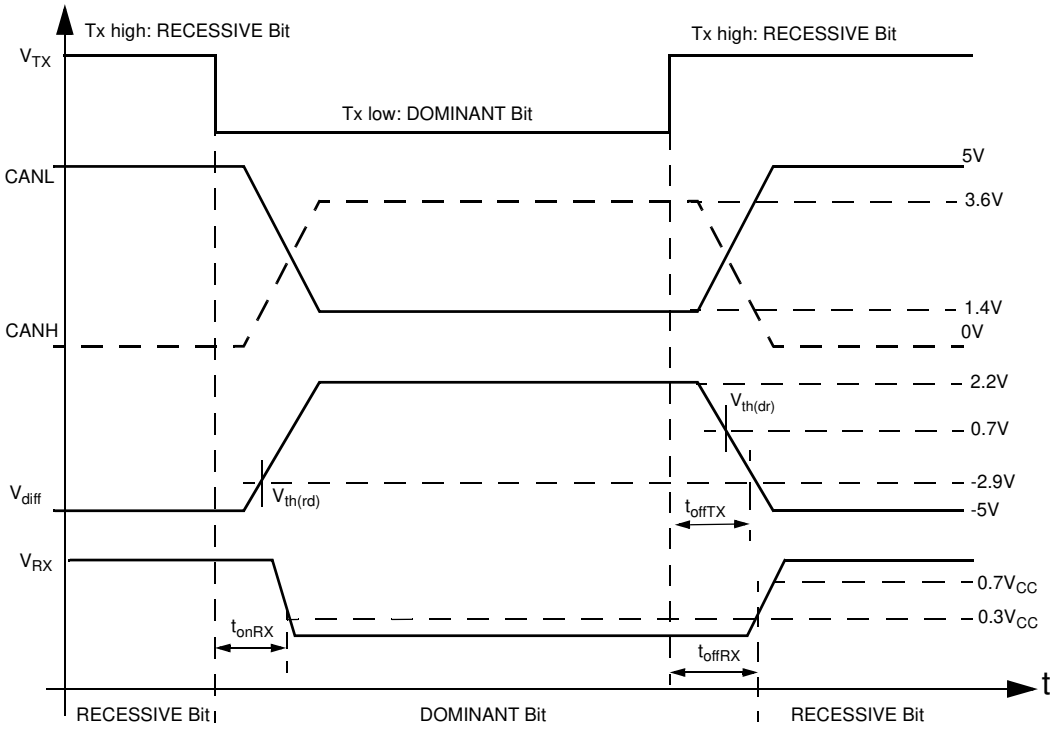
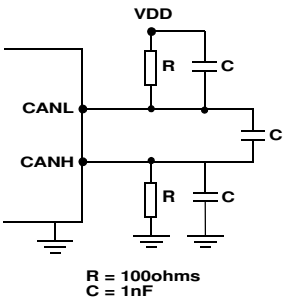


Figure 2. Test Circuit For AC Characteristics



Introduction

The MC33388 is a low speed CAN fault tolerant physical interface designed for automotive multiplexed electronic systems. The MC33388 addresses the low speed body electronics application, in which the speed of communications is between 10 and 125kBauds, on two wires bus configurations. It is designed to operate in the harsh automotive environment.

The MC33388 can control the external voltage regulator of the system through the dedicated INH pin. It allows the application to be switched into low power mode. Wake up can be done either from bus activity or local wake up switch. The MC33388 is tolerant to faults occurring at the CAN bus in normal operating mode and low power mode.

Packaging

The device is assembled in a SO14 narrow body package. Thermal performances allow the device to operate in the automotive ambient temperature range, from –40°C to 125°C.

Transmitter Function

CAN bus levels are called Dominant and Recessive, and correspond respectively to Low and High state of TX input pin. The Recessive state is a weak state, where bus line are driven through pull up and pull down resistors. Recessive state can be over written by any other node forcing a Dominant state, in which bus line are driven through active switches.

The bus is terminated by pull up and pull down resistors, which are connected to GND, VDD or VBAT through dedicated Rtl and Rth pins and internal circuitry.

The bus line slew rates are controlled in order to minimize the RFI and this allows use of unshielded cables for the bus.

Receiver Function

In normal operation (no bus failures), RX is the image of the differential bus voltage. The differential receiver inputs are connected to CANH and CANL through integrated filters. The filtered input signals are also used for the single wire receivers.

The device incorporates comparators connected to CANH and CANL in order to monitor and report the bus state to the microcontroller as well as detect bus failures. Failures are reported back to the microcontroller through NERR pin.

In normal operation when no failure is present the differential comparator is active. Under fault condition, one of the two CANH or CANL pin can be non operational then the single ended comparator of either CANH or CANL is activated and continue to report bus state to the microcontroller. The MC33388 permanently monitors bus failure and recovery, and as soon as fault disappears, it automatically switches back to differential operation.

Noise Filtering

The device is optimized for dual wires operations. During all single wire transmissions, the EMC performances in both immunity and emission are worse than in differential mode. Integrated receiver filters suppress any HF noise induced into the bus wires. The cut-off frequency of these filters is a compromise between propagation delay and HF suppression. In single wire mode, low frequency noise can not be distinguished from the active signal at the bus line.

Device Operation Mode

The device has four operation modes: Normal, Receive Only, Standby VBAT and Sleep. Each of these modes is controlled by the state of EN and STB pins.

The state machine figure 3 and the truth table 1 indicate how to configure the device into each mode and the pins functions in each operation mode.

Operation Mode

Normal mode: In this mode, all functions are available and NERR pin reports bus failure

Receive Only mode: In this mode, the transmitter path is disabled, so the device does not drive the bus. It maintains CANL and CANH in recessive state. The receiver function operates normally. As the device can not drive the bus, an incoming CAN message could not be acknowledge by the node. NERR output signals the VBAT power-on flag and RX reports bus state. Failure detection and management are the same as in normal mode.

Sleep mode: In this mode, the transmitter and receiver functions are disabled. CANL pin is connected to VBAT through Rtl resistor and internal pull up resistor of 12.5kOhms. INH pin is switched in high impedance state. The external voltage regulator connected to INH will be switched off and no VDD is supplied to MC33388. In this mode the device is still supplied by the VBAT. Supply current from VBAT is 15uA typical. The MC33388 monitors the bus activity and the state of WAKE pin and VBAT level. If wake up conditions are encountered, the device wakes up to Standby VBAT mode and INH is switched on.

Standby VBAT mode: This mode is similar to Sleep mode, but the INH pin is in high state in order to maintain the external 5V regulator activated. Wake up events are directly reported to NERR and RX thanks to the 5V available at VDD. CANL is in the same configuration as in Sleep mode.

Standby and Sleep modes are active when STB and EN are low. Selection of Standby or Sleep is done through the sequence of activation of EN and STB pins. Sleep mode is entered through an intermediate steps (go to sleep) where STB, EN are 0, 1. (Refer to truth table 1).

System Power On

When the supply is first applied to the system, VBAT and VDD rise from zero up to their nominal value and the device automatically enters into VBAT standby mode. At this time, INH is switched in high state in order to activate the external voltage regulator and an internal flag is set (batt fail flag). EN and STB pins are internally forced in low state to maintain the device into VBAT standby mode.

The VDD “forced Vbat standby mode (fail safe)” circuit will maintain the device in VBAT standby mode until VDD is higher that 3V, whatever the external state of EN and STB.

As soon as VDD reaches the “forced VBAT standby mode (fail safe)” threshold, the device can enter into other mode, depending upon EN and STB state.

VDD Reset Function

If during operation VDD drops below “forced VBAT standby mode (fail safe)” threshold, the device is automatically switched into VBAT standby mode to provide fail safe functionality.

Archive Information

Battery Fail Flag

When the VBAT supply drops below “battery voltage for setting power on flag” threshold, this information is internally latched. This means that the system power supply has been lost (disconnected and reconnected for instance).

This flag can be read by the microcontroller by switching the device into receive only mode, where NERR pin reports the VBAT power on flag. This flag is reset by entering into the Normal mode.

Bus Failure Detection

The device permanently monitors the bus lines and detects faults in normal and receive only modes. Below is the list of failures detected at the bus level:

1- CANH wire interruption
2- CANL wire interruption
3- CANH short-circuit to battery
4- CANL short-circuit to ground
5- CANH short-circuit to ground
6- CANL short-circuit to battery
7- CANL and CAN H mutually shorted
8- CANH short-circuit to Vdd

TX Permanent Dominant Detection

In addition to the above list, the MC33388 detects a permanent low state at TX input which results of a permanent dominant bus state. The MC33388 detects if TX is Low for more than 2ms typical and then disables the bus output driver in order to switch into recessive state. This avoid to block communication between other nodes of the network.

Behaviour Under Faults Condition

When a fault is detected, the device automatically takes appropriate action to minimize the system current consumption and to allow communication on the network. Depending on the type of fault, the mode of operation and the fault detected, the device automatically switches off one or more of the following functions: CANL or CANH line driver, Rtl or Rth pull up or down resistors or internal switches. These actions are detailed in table 2.

The device permanently monitors the faults and in case of fault recovery, it automatically switches back to normal operation and reconnects the open functions. Faults detection and recovery circuitry have internal filters and delays timing detailed in the AC characteristics parameters section.

Detailed Description of Error Detections

The differential receiver threshold is set at -2,8V. This assures a proper reception in the normal operating modes and in case of failures 1, 2 and 5 noise margin as high as possible. These failures or their recovery do not destroy ongoing transmissions.

Failures 3 and 6 are detected by comparators respectively connected to CANH and CANL. If the comparator threshold is exceeded for a certain time, the device is switched to single wire mode. This time is needed to avoid false triggering by external RF fields. Recovery from these failures is detected automatically after a certain time-out (filtering) and no transmission is lost.

Failures 4, 7 and 8 initially result in a permanent dominant level at the internal comparator outputs. If failure 4 and 7 appear, the CANL driver and the RTL pin are switched off after a time out, only a weak pull up at RTL remains. Reception continues by switching to single wire mode through CANH. When the failures 4 or 7 are removed, the recessive bus levels are restored. If the receiver voltages remain in the recessive state for a certain time, reception and transmission switch back to the differential mode.

If failure 8 is recognized, the CANH driver is switched off after a time out and the reception is switched to single wire mode through CANL. If the receiver voltages remain in the recessive state for a certain time, reception and transmission switch back automatically to the differential mode.

If any of the 8 wiring failure occurs, the output NERR will be switched low. When the error recovers, NERR will be switched back to high state.

Wake Up Events

Wake-up requests are recognized by the MC33388 in Sleep or VBAT Stanby modes, either when a dominant state is detected on CANL or CANH bus lines (remote wake-up) or if the WAKE pin changes state (local wake-up).

Under power-up conditions when VBAT is higher than 5V, the state voltage on the WAKE pin is considered to be the reference state for the wake-up function. On leaving normal mode, the current WAKE pin state becomes the new reference state.

In sleep mode, on a wake-up request the transceiver sets the INH output high, to activate the external voltage regulator, used for VDD supplied. In VBAT standby INH is already set high. When VDD is set, the wake-up request can be read on the NERR or RX outputs by the microcontroller.

To prevent false wake-up due to transients or RF fields, wake-up threshold levels have to be maintained for a certain time. In the low power modes, failure detection circuit remains partly active to prevent increased power consumption in cases of error 3, 4, 7 and 8.

Fault Operation Table

Table 2 shows the device operation in normal and low power modes and the internal actions happening under fault condition. Please refer to simplified block diagram page 1 for device internal switch reference.

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Figure 3. State Machine And Operation Modes

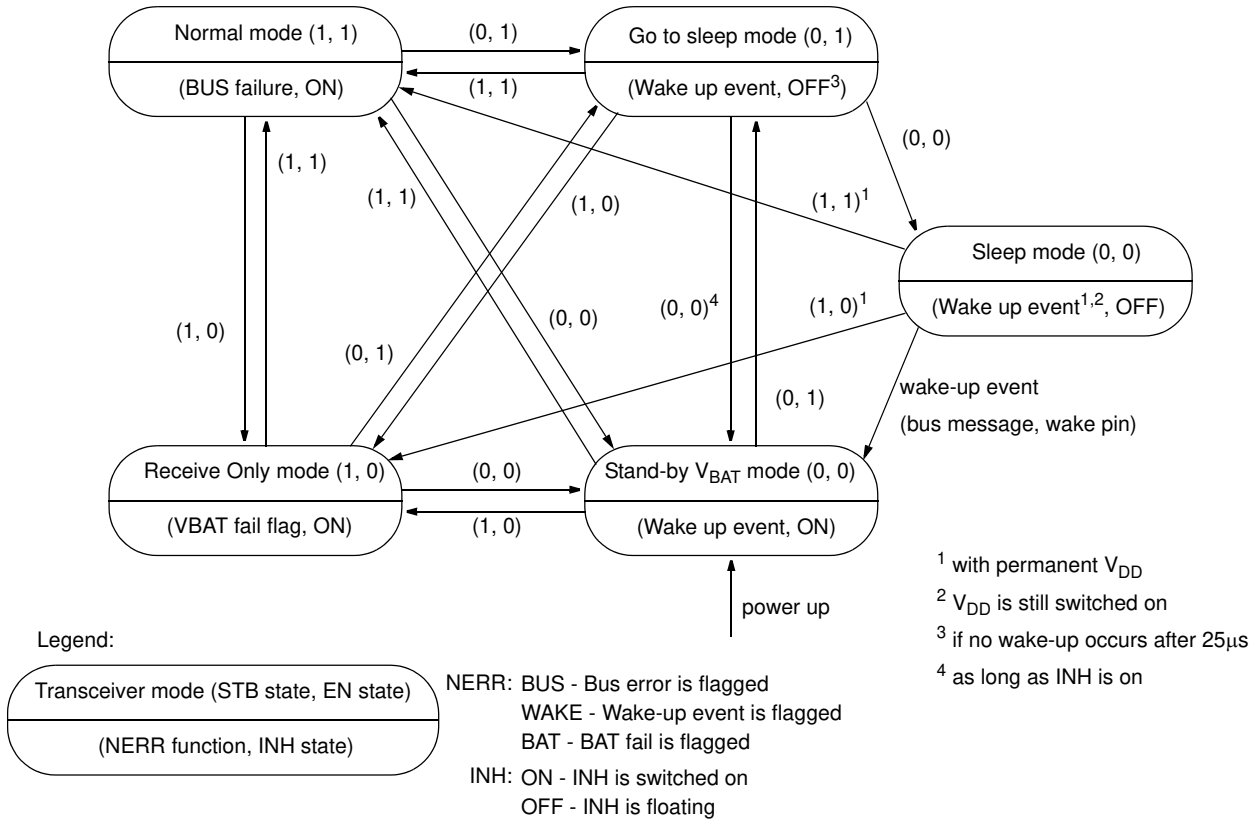

Table 1 • Truth Table

STB	EN	Mode	INH	NERR	RX	RTL	I_{DD} (4)	I_{BAT} (4)
0	0	VBAT Standby[1]	High	Active LOW: wake-up interrupt signal (if V_{DD} is present)		Switched to V_{BAT}	5µA	typ. 15µA
0	0	Sleep[2]	Floating			Switched to V_{BAT}	Not applicable	typ. 15µA
0	1	Go to sleep command	Floating			Switched to V_{BAT}		
1	0	Receive Only[3]	High	Active LOW: V_{BAT} power-on flag	High: recessive state Low: dominant state	Switched to V_{DD}	800µA	
1	1	Normal	High	Active LOW: error flag		Switched to V_{DD}	2.3mA (5) 3.3mA (6)	typ. 150µA

NOTES:
1. Wake-up interrupts are released when entering normal operating mode.
2. If go to sleep command was used before (EN may turn LOW as VDD drops, without affecting internal functions because of fail safe functionality.
3. VBAT power-on flag will be reset when entering normal operation mode.
4. Value are typical, without bus load current.
5. In recessive state.
6. In Dominant State, value with no load at bus.

Table 2 • Detail Fault Operation Table

Failure #	Description	Mode	State of S1, S2, S3 Internal Switches and CANL CANH Output Drivers (Ref to Normal Mode)
No failure		Normal and receive only	S1, S2 closed, CANL, CANH drivers enabled
No failure		VBAT standby	S3 closed, CANL, CANH drivers disabled
No failure		Sleep mode	S3 closed, CANL, CANH drivers disabled
1	CANH wire interrupted	Normal and receive only	CANL, CANH drivers enabled, S1, S2 closed
2	CANL wire interrupted	Normal and receive only	CANL, CANH drivers enabled S1, S2 closed
3	CANH short to BAT	All	S1 open, CANH driver disabled
4	CANL short to GND	All	S2, S3 open & CANL driver disabled
5	CANH short to GND	Normal and receive only	CANL, CANH drivers enabled S1, S2 closed
6	CANL short to BAT	Normal and receive only	S2, S3 open & CANL driver disabled
7	CANL short to CANH	All	S2, S3 open & CANL driver disabled
8	CANH short to VDD	All	S1 open, CANH driver disabled

NOTE: S4 and S5 behaviours are only dependant upon the device operating mode.
S4 and S5 switches are closed in normal and receive only modes and are open in sleep and standby modes.

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PIN FUNCTION DESCRIPTION

VBAT (input): This is the supply line of the device. It can be directly connected to the battery line, can operate up to 27VDC and sustains up to 40V during load dump condition. The supply current is dependant upon the device operation mode. In low power mode, it is as low as 12uA typical. A battery fail flag circuitry is associated to this pin.

The Vbat pin must be protected by external component against reverse battery and negative transient voltages.

VDD (input): 5V input supply voltage for the device. In normal mode, the current is up to 5mA typical and do not exceed few uA in Vbat standby mode. An under voltage function is associated to Vdd and resets the device to Vbat standby mode when Vdd falls below 3V.

CANH: Bus output driver pin. CANH is a high side switch structure connected to VDD supply. In recessive state, the high side switch is off and bus CANH line is biassed through the Rth pin circuitry and external Rth resistor. In dominant state, high side switch is on and CANH line is switched to VDD. Output voltage is above 3.6V. CANH output is protected against short-circuit to ground, by internal current limitation. A thermal shutdown with hysteresis switches off CANH driver if temperature rises above 150°C. CANH is also protected against short-circuit to higher voltage, such as VBAT by an internal serial diode in series with the switching component. CANH has a pull down current source, typically 75uA, which can be activated under some fault condition.

Rth: Connection to the CANH bus terminal resistors. Rth output structure is a low side switch, turned on under normal condition and automatically desactivated under some fault condition. In the application, an external resistor is connected between Rth and CANH pins. In recessive state when CANH driver is off, CANH line is tied to ground through the external Rth resistor.

CANL: Bus output driver pin. CANL is a low side switch structure to the ground. In recessive state, the low side switch is off, and bus CANL line is biassed through the Rtl circuitry and external Rtl resistor. In dominant state, low side switch is on and CANL line is switched to ground. Output voltage is below 1.4V. CANL output is protected against short-circuit to VBAT, by internal current limitation. A thermal shutdown with hysteresis is integrated and switches off CANL driver if temperature rises above 150°C. CANL is protected against negative voltage, by an internal serial diode in series with the switching component. CANL has a pull up current source, typically 75uA, activated under some fault condition.

Rtl: Connection to the CANL bus terminal resistors. Rtl output structure is a low side switch, turned on under normal condition and automatically desactivated under some fault condition. In the application, an external resistor is connected between Rtl and CANL pins. In recessive state when CANL driver is off, CANL line is tied to VDD through external Rtl resistor.

In VBAT Standby and Sleep modes, Rtl pin is connected to the VBAT line through an internal switch and a 12.5kΩ resistor. This means that in these modes CANL bus line is biassed to VBAT. Wake up from these modes are detected by CANL line going from VBAT level to CANL wake up threshold level.

STB and EN: Input pins used to configure the device into desired mode. These pins are CMOS compatible and are connected to the microcontroller of the application.

INH: This is an output of the MC33388 used to control an external voltage regulator having an inhibit input. INH is a high side switch structure, active when the MC33388 is in normal, Receive only or Standby VBAT modes. INH is switched off in Sleep mode to switch off the voltage regulator of the application. INH has no pull down structure.

WAKE: This is a high voltage input used to wake up the device from Sleep and VBAT Standby modes. Wake is usually connected to an external switch in the application. The typical wake thresholds are Vbat/2.

Wake pin has special design structure and allows wake up from both high to low or low to high transitions. When entering into the Sleep or VBAT Standby mode, the MC33388 monitors the state of the wake pin and stores it as reference state. The opposite state of this reference state will be the wake up event used by the device to enter again into normal mode.

An internal filter is implemented, with 8 to 38 μs filtering time delay. Wake pin input structure exhibits a high impedance, with extremely low input current. A serial resistor should be inserted in order to limit the input current mainly during transient pulses.

CAUTION: The Wake pin should not be left open. If wake up function is not used, wake should be connected to GND to avoid false wake up.

TX: Transmitter input pin to control bus state. It is CMOS compatible and usually directly connected to the TX output of a microcontroller. When TX is at high state, CANH and CANL are in recessive state. When TX is low, CANL and CANH are in dominant state. Special fault handling is provided to this input, in order to detect permanent dominant state (TX low) which would result of CAN bus permanently lock in dominant state and do not allow communication. In case where TX is low for more than 2ms typical, the device automatically switches the bus lines to recessive. TX has an internal pull up resistor to VDD.

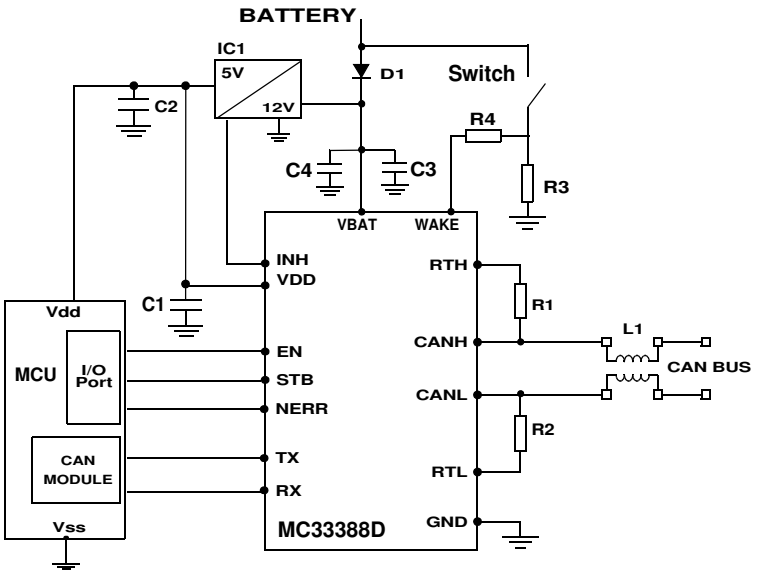
RX: Output receiver connection to the microcontroller. It reports the bus state to the RX input pin of the microcontroller. RX is high when bus is recessive and low in dominant state. In sleep and standby Vbat modes, RX reports wake up events.

NERR: Error output pin which reports errors encountered by the device. When NERR is high, no error is reported, when NERR is low an error has been detected. In Standby VBAT mode NERR reports a wake up event. In receive only mode, NERR reports VBAT power on flag.

Table 3 • Truth Table of RX, TX CAN Bus States

TX	RX	Bus States	Comment
Low	Low	Dominant	
High	High	Recessive	
High	Low	Dominant	Bus Driven By Other Node

Table 4 • Typical Application Schematic



Component information:
R3: 10kΩ
R4: >= 33kΩ
C1>= 47nF
C2>= 4.7uF
C3>= 47nF
C4>= 10uF
L1: optional common mode choke
D1: 1N4148
IC1: LM2935
R1=R2=R (500Ω<R<16kΩ)
R/number of nodes>100Ω

Figure 4 above is the typical application schematic. All MC33388 capabilities are utilized: CAN interface, normal and low power modes, wake up source from CAN bus or wake up switch.

The MC33388 VDD is supplied through an external voltage regulator having an inhibit input pin. In addition to TX and RX connections to the microcontroller CAN module, the MC33388 requires 3 additional connections to a standard microcontroller I/O port for EN, STB and NERR pins.

MC33388 wake pin is connected to an external signal switch. MC33388 allows the signal switch configuration to be either connected to Vbat or to ground through pull up or pull down resistor. Solution with switch to GND is indicated as option in the application schematic. A resistor must be inserted in series with wake pin in order to limit the input current during positive and negative transient pulses.

De-coupling capacitors are recommended on the MC33388 VBAT and VDD lines. Those capacitors might be shared with other devices from the same printed circuit board, depending on its configuration.

R1 and R2 are the network termination resistors. For proper operation, they must have identical value (R1 equals to R2). Their value is determined by the total network termination resistor and the number of nodes.

The total network termination resistor value must be higher than 100Ω. If a 500Ω termination resistor is chosen, with a system composed of 32 nodes, each R1 or R2 will be 16kΩ. In addition, R1 and R2 values should be chosen between 500Ω and 16kΩ at each node.

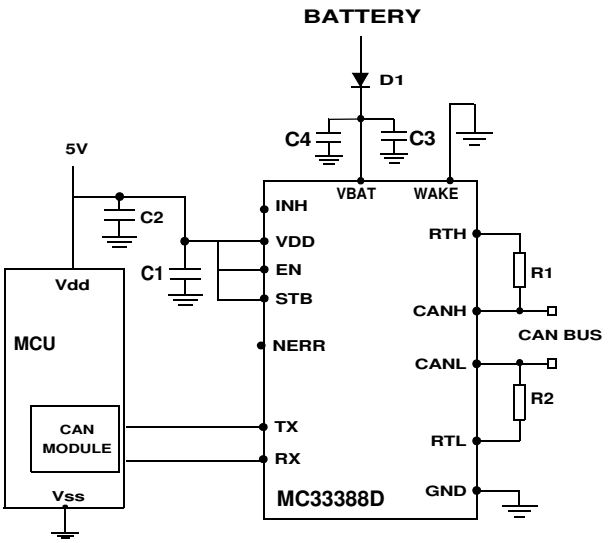
The CANH and CANL pin can be directly connected to the CAN bus. A serial common mode inductance can be inserted in order to improve electromagnetic compatibility performances both in emission and susceptibility.

Minimum Application Configuration

The minimum device configuration is described in minimum application schematic figure 5 below. The device is used as CAN transceiver only and other features are not used. The device EN and STB input pins must be connected to 5V in order to set the device in normal mode. INH and NERR can be left open.

CAUTION: WAKE should not be left open and must be connected to a known state, i.e GND.

Figure 4. Minimum Application Schematic



Component information:
C1>= 47nF
C2>= 4.7uF
C3>= 47nF
C4>= 10uF
D1: 1N4148
R1=R2=R (500Ω<R<16kΩ)
R / number of nodes>100Ω

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Introduction

The device is designed for optimized noise emission (EMI) and high susceptibility performances (EMC). The source for both disturbance and susceptibility is primarily coming form the bus line wires. They are by far the longest connections compared to the printed circuit board of the application receiving the MC333388, the microcontroller and the other components.

EMI Noise

In order to minimize the HF noise generated by the complete application, the MC33388 minimizes the common mode voltage and current glitches occurring at each bus transition: from dominant to recessive and from recessive to dominant. This is achieves by excellent matching in signal transition between CANL and CANH. The common mode voltage and current glitches are defined as follow:

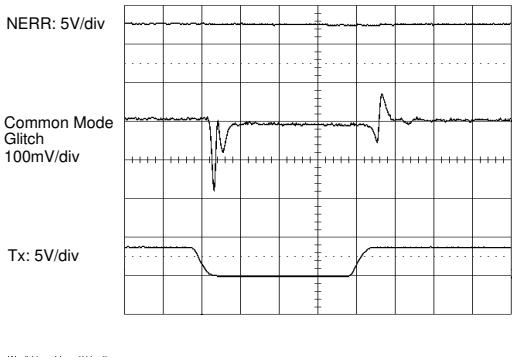
CmV = (Vcanh+Vcanl)/2,

CmI = (Icanh+Icanl)/2.

The device is optimized for dual wires operations. Under a fault condition, for instance one CAN bus connection shorted to fixed voltage, e.g GND, the common mode will be considerably degraded.

Figure below shows the typical signals for common mode voltage measured at CANL and CANH pins.

Figure 5. Typical Common Mode Glitch Measured at CANL CANH



CAUTION: The common mode voltage characteristics are dependant upon immediate device environment, such as bus capacitor loading, bus wire length and type, etc.... In addition, the symmetry of the CANL and CANH bus lines is key parameter to optimize common mode glitches. For instance un-symmetry could result in different parasitic capacitors value between CANL to GND and CANH to GND and will increase common mode glitches and degrade overall system performances.

EMC Susceptibility Performances

The MC33388 is optimized for high immunity from external field disturbances. The bus lines are by far the primary antenna for external field coupling to the CANL, CANH, Rtl and Rth connections. The device performances are characterized using the Bulk Current Injection (BCI) test method, derivated from specification ISO 11452-4.

Susceptibility evaluation with BCI:

The component is configured according to the electrical schematic very close to the typical application schematic, figure 4. Main difference is that the microcontroller is replaced by an external generator and analyzer connected to RX, TX and NERR through optical link. A network composed of two nodes equipped with MC33388, one in emitter and one in receiver is evaluated. The disturbance is applied to both CANL and CANH twisted pair bus line lines with appropriate coupling clamp.

During test sequences, received bits are compared to transmit bits. When received bits are different from transmit bits the device is considered as fail for the particular frequency.

Results

Figures 7 and 8 below describe the device susceptibility performances in the frequency range of 1 to 400MHz with target of injected current of 200mA and 316mA.

When the target current is reached and when no susceptibility is observed, the next frequency point is analyzed, until reaching the max frequency, 400Mhz. If a susceptibility is observed for a particular frequency, the free point is marked.

Figure 7 below shows results with a target susceptibility level of 316mA or 49dBmA with a 1KHz 80% modulation added to the injected current. Figure 8 shows the susceptibility levels with a target susceptibility level of 200mA or 46dBmA without modulation added to the injected current.

Figure 6. Min. Susceptibility Level With Modulation

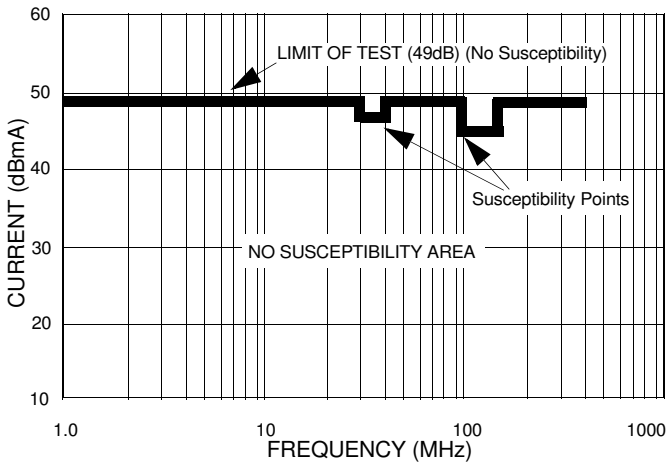
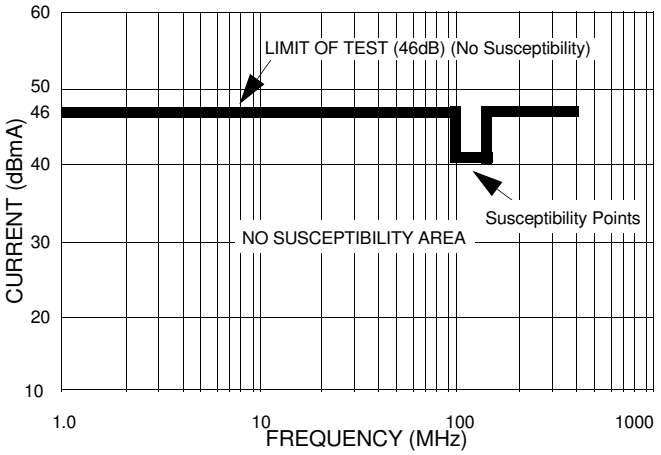


Figure 7. Min. Susceptibility Level Without Modulation



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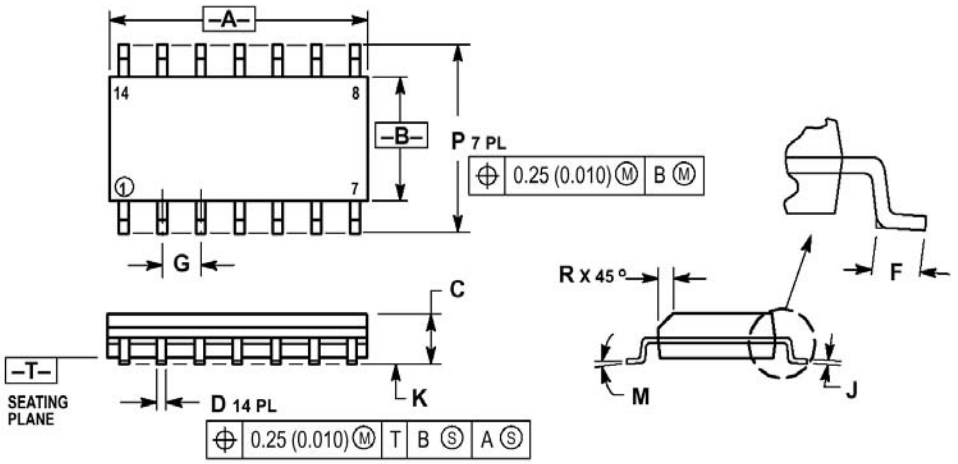
OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

CASE 751A-03
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