Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

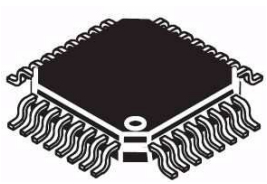
Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MC33696

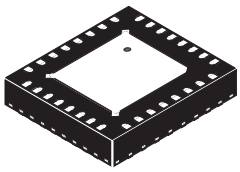
PLL Tuned UHF Transceiver for Data Transfer Applications

1 Overview

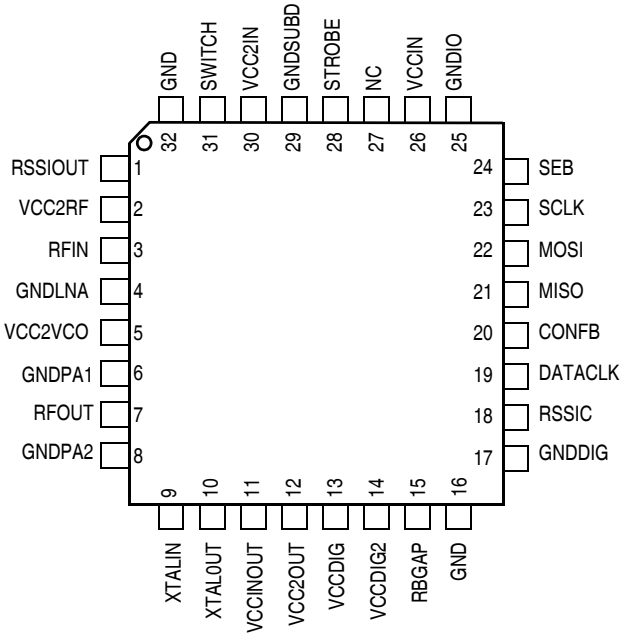
The MC33696 is a highly integrated transceiver designed for low-voltage applications. It includes a programmable PLL for multi-channel applications, an RSSI circuit, a strobe oscillator that periodically wakes up the receiver while a data manager checks the content of incoming messages. A configuration switching feature allows automatic changing of the configuration between two programmable settings without the need of an MCU.



LQFP32



QFN32



2 Features

General:

- 304 MHz, 315 MHz, 426 MHz, 434 MHz, 868 MHz, and 915 MHz ISM bands
- Choice of temperature ranges:
  - –40°C to +85°C
  - –20°C to +85°C
- OOK and FSK transmission and reception
- 20 kbps maximum data rate using Manchester coding
- 2.1 V to 3.6 V or 5 V supply voltage
- Programmable via SPI
- 6 kHz PLL frequency step

- Frequency hopping capability with PLL toggle time below 30 µs
- Current consumption:
  - 13.5 mA in TX mode
  - 10.3 mA in RX mode
  - Less then 1 mA in RX mode with strobe ratio = 1/10
  - 260 nA standby and 24 µA off currents
- Configuration switching — allows fast switching of two register banks

Receiver:

- –106.5 dBm sensitivity, up to –108 dBm in FSK 2.4 kbps
- Digital and analog RSSI (received signal strength indicator)
- Automatic wakeup function (strobe oscillator)
- Embedded data processor with programmable word recognition
- Image cancelling mixer
- 380 kHz IF filter bandwidth
- Fast wakeup time

Transmitter:

- Up to 7.25 dBm output power
- Programmable output power
- FSK done by PLL programming

Ordering information

Temperature Range	QFN Package	LQFP Package
–40°C to +85°C	MC33696FCE/R2	MC33696FJE/R2
–20°C to +85°C	MC33696FCAE/R2	MC33696FJAE/R2

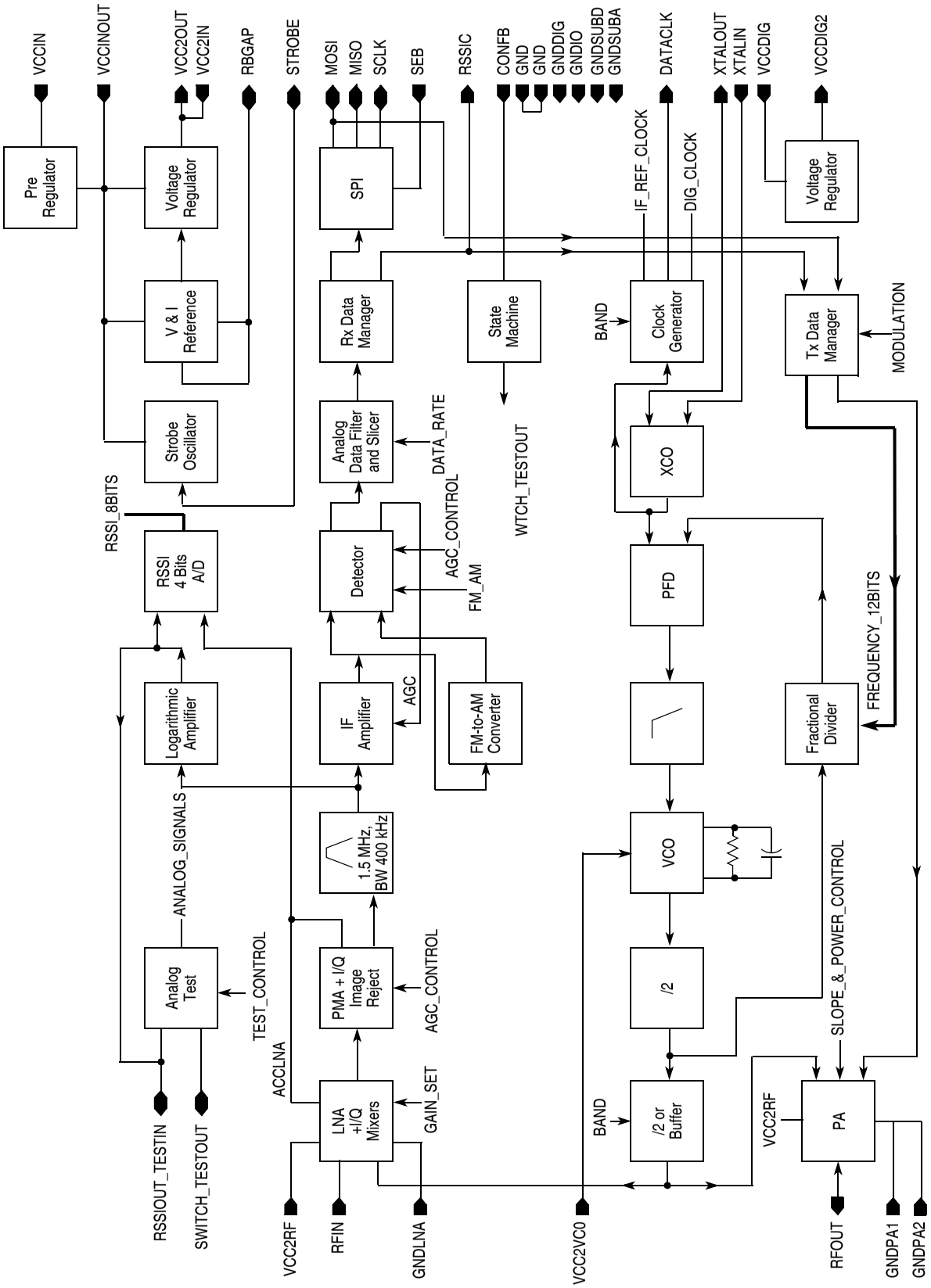

VCCIN
VCCINOUT
VCC2OUT
VCC2IN
RBGAP
STROBE
MOSI
MISO
SCLK
SEB
RSSIC
CONFB
GND
GND
GNDDIG
GNDIO
GNDSUBD
GNDSUBA
DATACLK
XTALOUT
XTALIN
VCCDIG
VCCDIG2
Pre Regulator
Voltage Regulator
SPI
IF_REF_CLOCK
DIG_CLOCK
Voltage Regulator
V & I Reference
Rx Data Manager
State Machine
BAND
Clock Generator
Tx Data Manager
MODULATION
Strobe Oscillator
Analog Data Filter and Slicer
DATA_RATE
WTCH_TESTOUT
XCO
RSSI_8BITS
RSSI 4 Bits A/D
Detector
AGC_CONTROL
FM_AM
PFD
Logarithmic Amplifier
IF Amplifier
AGC
FM-to-AM Converter
Fractional Divider
FREQUENCY_12BITS
1.5 MHz, BW 400 kHz
VCO
ANALOG_SIGNALS
Analog Test
TEST_CONTROL
PMA + I/Q Image Reject
AGC_CONTROL
/2
SLOPE_&_POWER_CONTROL
ACCLNA
LNA +I/Q Mixers
GAIN_SET
BAND
/2 or Buffer
VCC2RF
PA
RSSIOUT_TESTIN
SWITCH_TESTOUT
VCC2RF
RFIN
GNDLNA
VCC2VCO
RFOUT
GNDPA1
GNDPA2

Figure 1. Block Diagram

3 Pin Functions

Table 1. Pin Functions

Pin	Name	Description
1	RSSIOUT	RSSI analog output
2	VCC2RF	2.1 V to 2.7 V internal supply for LNA
3	RFIN	RF input
4	GNDLNA	Ground for LNA (low noise amplifier)
5	VCC2VCO	2.1 V to 2.7 V internal supply for VCO
6	GNDPA1	PA ground
7	RFOUT	RF output
8	GNDPA2	PA ground
9	XTALIN	Crystal oscillator input
10	XTALOUT	Crystal oscillator output
11	VCCINOUT	2.1 V to 3.6 V power supply/regulator output
12	VCC2OUT	2.1 V to 2.7 V voltage regulator output for analog and RF modules
13	VCCDIG	2.1 V to 3.6 V power supply for voltage limiter
14	VCCDIG2	1.5 V voltage limiter output for digital module
15	RBGAP	Reference voltage load resistance
16	GND	General ground
17	GNDDIG	Digital module ground
18	RSSIC	RSSI control input
19	DATACLK	Data clock output to microcontroller
20	CONFB	Configuration mode selection input
21	MISO	Digital interface I/O
22	MOSI	Digital interface I/O
23	SCLK	Digital interface clock I/O
24	SEB	Digital interface enable input
25	GNDIO	Digital I/O ground
26	VCCIN	2.1 V to 3.6 V or 5.5 V input
27	NC	No connection
28	STROBE	Strobe oscillator capacitor or external control input
29	GNDSUBD	Ground
30	VCC2IN	2.1 V to 2.7 V power supply for analog modules for decoupling capacitor
31	SWITCH	RF switch control output
32	GND	General ground

4 Maximum Ratings

Table 2. Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage on pin: VCCIN	V_{CCIN}	V_{GND}–0.3 to 5.5	V
Supply voltage on pins: VCCINOUT, VCCDIG	V_{CC}	V_{GND}–0.3 to 3.6	V
Supply voltage on pins: VCC2IN, VCC2RF, VCC2VCO	V_{CC2}	V_{GND}–0.3 to 2.7	V
Voltage allowed on each pin (except RFOUT and digital pins)	—	V_{GND}–0.3 to V_{CC2}	V
Voltage allowed on pin: RFOUT	V_{CCPA}	V_{GND}–0.3 to V_{CC}+2	V
Voltage allowed on digital pins: SEB, SCLK, MISO, MOSI, CONFB, DATACLK, RSSIC, STROBE	V_{CCIO}	V_{GND}–0.3 to V_{CC}+0.3	V
ESD HBM voltage capability on each pin[1]	—	±2000	V
ESD MM voltage capability on each pin[2]	—	±200	V
Solder heat resistance test (10 s)	—	260	°C
Storage temperature	T_S	–65 to +150	°C
Junction temperature	T_J	150	°C

NOTES:
1 Human body model, AEC-Q100-002 rev. C.
2 Machine model, AEC-Q100-003 rev. C.

5 Power Supply

Table 3. Supply Voltage Range Versus Ambient Temperature

Parameter	Symbol	Temperature Range[1]		Unit
		–40°C to +85°C	–20°C to +85°C	
Supply voltage on VCCIN, VCCINOUT, VCCDIG for 3 V operation	V_{CC3V}	2.7 to 3.6	2.1 to 3.6	V
Supply voltage on VCCIN for 5 V operation	V_{CC5V}	4.5 to 5.5	4.5 to 5.5	V
Supply voltage on VCCPA for 3 V or 5 V operation	V_{CCPA}	3.0 to 3.6	3.0 to 3.6	V

NOTES:
1 –40°C to +85°C: MC33696FCE/FJE.
–20°C to +85°C: MC33696FCAE/FJAE.

The circuit can be supplied from a 3 V voltage regulator or battery cell by connecting VCCIN, VCCINOUT, and VCCDIG (See Figure 43 or Figure 44). It is also possible to use a 5 V power supply connected to VCCIN; in this case VCCINOUT and VCCDIG should not be connected to VCCIN (See Figure 45 or Figure 46).

The RFOUT pin cannot be biased with a voltage higher than 3.6 V. For 5 V operation, biasing voltage is available on VCCINOUT.

An on-chip low drop-out voltage regulator supplies the RF and analog modules (except the strobe oscillator and the low voltage detector, which are directly supplied from VCCINOUT). This voltage regulator is supplied from pin VCCINOUT and its output is connected to VCC2OUT. An external capacitor (C8 = 100 nF) must be inserted between VCC2OUT and GND for stabilization and decoupling. The analog and RF modules must be supplied by VCC2 by externally wiring VCC2OUT to VCC2IN, VCC2RF, and VCC2VCO.

A second voltage regulator supplies the digital part. This regulator is powered from pin VCCDIG and its output is connected to VCCDIG2. An external capacitor (C10 = 100 nF) must be inserted between VCCDIG2 and GNDDIG, for decoupling. The supply voltage VCCDIG2 is equal to 1.6 V. In standby mode, this voltage regulator goes into an ultra-low-power mode, but VCCDIG2 = 0.7 × V_{CCDIG}.

This enables the internal registers to be supplied, allowing configuration data to be saved.

6 Supply Voltage Monitoring and Reset

At power-on, an internal reset signal (Power-on Reset, POR) is generated when supply voltage is around 1.3 V. All registers are reset.

When the LVDE bit is set, the low-voltage detection module is enabled. This block compares the supply voltage on VCCINOUT with a reference level of about 1.8 V. If the voltage on VCCINOUT drops below 1.8 V, status bit LVDS is set. The information in status bit LVDS is latched and reset after a read access.

NOTE

If LVDE = 1, the LVD module remains enabled. The circuit cannot be put in standby mode, but remains in LVD mode with a higher quiescent current, due to the monitoring circuitry. LVD function is not accurate in standby mode.

7 Receiver Functional Description

The receiver is based on a superheterodyne architecture with an intermediate frequency IF (see Figure 1). Its input is connected to the RFIN pin. Frequency down conversion is done by a high-side injection I/Q mixer driven by the frequency synthesizer. An integrated poly-phase filter performs rejection of the image frequency.

The low intermediate frequency allows integration of the IF filter providing the selectivity. The IF Filter center frequency is tuned by automatic frequency control (AFC) referenced to the crystal oscillator frequency.

Sensitivity is met by an overall amplification of approximately 96 dB, distributed over the reception chain, comprising low-noise amplifier (LNA), mixer, post-mixer amplifier, and IF amplifier. Automatic gain control (AGC), on the LNA and the IF amplifier, maintains linearity and prevents internal saturation. Sensitivity can be reduced using four programmable steps on the LNA gain.

Amplitude demodulation is achieved by peak detection. Frequency demodulation is achieved in two steps: the IF amplifier AGC is disabled and acts as an amplitude limiter; a filter performs a frequency-to-voltage conversion. The resulting signal is then amplitude demodulated in the same way as in the case of amplitude modulation with an adaptive voltage reference.

A low-pass filter improves the signal-to-noise ratio of demodulated data. A data slicer compares demodulated data with a fixed or adaptive voltage reference and provides digital level data.

This digital data is available if the integrated data manager is not used.

If used, the data manager performs clock recovery and decoding of Manchester coded data. Data and clock are then available on the serial peripheral interface (SPI). The configuration sets the data rate range managed by the data manager and the bandwidth of the low-pass filter.

An internal low-frequency oscillator can be used as a strobe oscillator to perform an automatic wakeup sequence.

It is also possible to define two different configurations for the receiver (frequency, data rate, data manager, modulation, etc.) that are automatically loaded during wakeup or under MCU control.

If the PLL goes out of lock, received data is ignored.

8 Transmitter Functional Description

The single-ended power amplifier is connected to the RFOUT pin.

In the case of amplitude modulation, coded data sent by the microcontroller unit (MCU) are used for on/off keying (OOK) the RF carrier. Rise and fall times of the RF transmission are controlled to minimize spurious emission.

In the case of frequency modulation, coded data sent by the MCU are used for frequency shift keying (FSK) the RF carrier.

RF output power can be reduced using four programmable steps.

Out-of-lock detection prevents any out-of-band emission, by stopping the transmission.

The logic output SWITCH enables control of an external RF switch for isolating the two RF pins. Its output toggles when the circuit changes from receive to transmit, and vice versa.

This signal can also be used to control an external power amplifier or LNA, or to indicate to the MCU the current state of the MC33696 (RX or TX).

9 Frequency Planning

9.1 Clock Generator

All clocks running in the circuit are derived from the reference frequency provided by the crystal oscillator (frequency f_{ref}, period t_{ref}). The crystal frequency is chosen in relation to the band in which the MC33696 has to operate. Table 4 shows the value of the CF bits.

Table 4. Crystal Frequency and CF Values Versus Frequency Band

RF Frequency (MHz)	CF1	CF0	LOF1	LOF0	F_{REF} (Crystal Frequency) (MHz)	F_{IF} (IF Frequency) (MHz)	Dataclk Divider	$F_{dataclk}$ (kHz)	Digclk Divider	F_{digclk} (kHz)	T_{digclk} (µs)
304	0	0	0	0	16.96745	1.414	60	282.791	30	565.582	1.77
315	0	0	1	0	17.58140	1.465	60	293.023	30	586.047	1.71
426	0	1	1	0	23.74913	1.484	80	296.864	40	593.728	1.68
433.92	0	1	0	1	24.19066	1.512	80	302.383	40	604.767	1.65
868.3	1	1	0	1	24.16139	1.510	80	302.017	40	604.035	1.66
916.5	1	1	1	1	25.50261	1.594	80	318.783	40	637.565	1.57

9.2 Intermediate Frequency

The IF filter is controlled by the crystal oscillator to guarantee the frequency over temperature and voltage range. The IF filter center frequency, FIF, can be computed using the crystal frequency f_{ref} and the value of the CF bits:

- If CF[0] = 0 : FIF = $f_{ref}/9\times1.5/2$

- If CF[0] = 1 : FIF = $f_{ref}/12 \times 1.5/2$

The cut-off frequency given in the parametric section can be computed by scaling to the FIF.

Example 1. Cut-off Frequency Computation

Compute the low cut-off frequency of the IF filter for a 16.9683 MHz crystal oscillator. For this reference frequency, FIF = 1.414 MHz.

So, the 1.387 MHz[1] low cut-off frequency specified for a 1.5 MHz IF frequency becomes $1.387 \times 1.414/1.5 = 1.307$ MHz.

9.3 Frequency Synthesizer Description

The frequency synthesizer consists of a local oscillator (LO) driven by a fractional N phase locked loop (PLL).

The LO is an integrated LC voltage controlled oscillator (VCO) operating at twice the RF frequency (for the 868 MHz frequency band) or four times the RF frequency (for the 434 MHz and 315 MHz frequency bands). This allows the I/Q signals driving the mixer to be generated by division.

The fractional divider offers high flexibility in the frequency generation for:

- Switching between transmit and receive modes.
- Achieving frequency modulation in FSK modulation transmission.
- Performing multi-channel links.
- Trimming the RF carrier.

Frequencies are controlled by means of registers. To allow for user preference, two programming access methods are offered (see Section 18.3, “Frequency Registers”).

- In friendly access, all frequencies are computed internally from the contents of the carrier frequency and deviation frequency registers.
- In direct access, the user programs direct all three frequency registers.

10 MCU Interface

The MC33696 and the MCU communicate via a serial peripheral interface (SPI). According to the selected mode, the MC33696 or the MCU manages the data transfer. The MC33696’s digital interface can be used as a standard SPI (master/slave) or as a simple interface (SPI deselected). In the following case, the interface’s pins are used as standard I/O pins. However, the MCU has the highest priority, as it can control the MC33696 by setting CONFB pin to the low level. During an SPI access, the STROBE pin must remain at high level to prevent the MC33696 from entering standby mode.

The interface is operated by six I/O pins.

- CONFB — Configuration control input

  The configuration mode is reached by setting CONFB to low level.

1. Refer to parameter 3.3 found in Section 21.3, “Receiver Parameters.”

- STROBE — Wakeup control input

  The STROBE pin controls the ON/OFF sequence of the MC33696. When STROBE is set to low level, the receiver is off—when STROBE is set to high level, the receiver is on. The current consumption in receive mode can be reduced by strobing the receiver. The periodic wakeup can be done by MCU only or by an internal oscillator thanks to an external capacitor (strobe oscillator must be previously enabled by setting SOE bit to 1). Refer to Section 12.3, "Receiver On/Off Control," for more details.

- SEB — Serial interface enable control input

  When SEB is set high, pins SCLK, MOSI, and MISO are set to high impedance, and the SPI bus is disabled. When SEB is set low, SPI bus is enabled. This allows individual selection in a multiple device system, where all devices are connected via the same bus. The rest of the circuit remains in the current state, enabling fast recovery times, but the power amplifier is disabled to prevent any uncontrolled RF transmission.

  If the MCU shares the SPI access with the MC33696 only, SEB control by the MCU is optional. If not used, it could be hardwired to 0.

- SCLK — Serial clock input/output

  Synchronizes data movement in and out of the device through its MOSI and MISO lines. The master and slave devices can exchange a byte of information during a sequence of eight clock cycles. Since SCLK is generated by the master device, this line is an input on the slave device.

- MOSI — Master output slave input/output

  In configuration mode, MOSI is an input.

  In transmission mode, MOSI is an input and receives encoded data from MCU.

  In receive mode, MOSI is an output. Received data is sent on MOSI (see Table 5).

  Transmits bytes when master, and receives bytes when slave, with the most significant bit first.

  When no data are output, SCLK and MOSI force a low level.

- MISO — Master input/slave output

  In configuration mode only, data read from registers is sent to the MCU with the MSB first. There is no master function. Data are valid on falling edges of SCLK. This means that the clock phase and polarity control bits of the microcontroller SPI have to be CPOL = 0 and CPHA = 1 (using Freescale acronyms).

Table 5 summarizes the serial digital interface feature versus the selected mode.

Table 5. Serial Digital Interface Feature versus Selected Mode

Selected Mode		MC33696 Digital Interface Use
Configuration		SPI slave, data received on MOSI, SCLK from MCU, MISO is output (SEB=0)
Transmit		SPI deselected, MOSI receives encoded data from MCU (SEB =0)
Receive	DME = 1	SPI master, data sent on MOSI with clock on SCLK (SEB=0)
	DME = 0	SPI deselected, received data are directly sent to MOSI (SEB=0)
Standby / LVD		SPI deselected, all I/O are high impedance (SEB =1)

Refer to Section 11, “State Machine,” and to Figure 2 for more details about all the conditions that must be complied with in order to change between two selected modes.

The data transfer protocol for each mode is described in the following section.

11 State Machine

This section describes how the MC33696 controller executes sequences of operations, relative to the selected mode. The controller is a finite state machine, clocked at T_{digclk}. An overview is presented in Figure 2 (note that some branches refer to other diagrams that provide more detailed information).

There are four different modes: configuration, transmit, receive, and standby/LVD. Each mode is exclusive and can be entered in different ways, as follows.

- External signal: CONFB for configuration mode
- External signal and configuration bits: CONFB, STROBE, TRXE, and/or MODE for all other modes
- External signal and internal conditions: see Figure 3 and Figure 12 for information on how to enter standby/LVD mode

After a Power-on Reset (POR), the circuit is in standby mode (see Figure 2) and the configuration register contents are set to the reset value.

At any time, a low level applied to CONFB forces the finite state machine into configuration mode, whatever the current state. This is not always shown in state diagrams, but must always be considered. Refer to (Section 16, “Power-On Reset and MC33696 Startup”) for timing sequence between standy mode and configuration mode.

State Machine

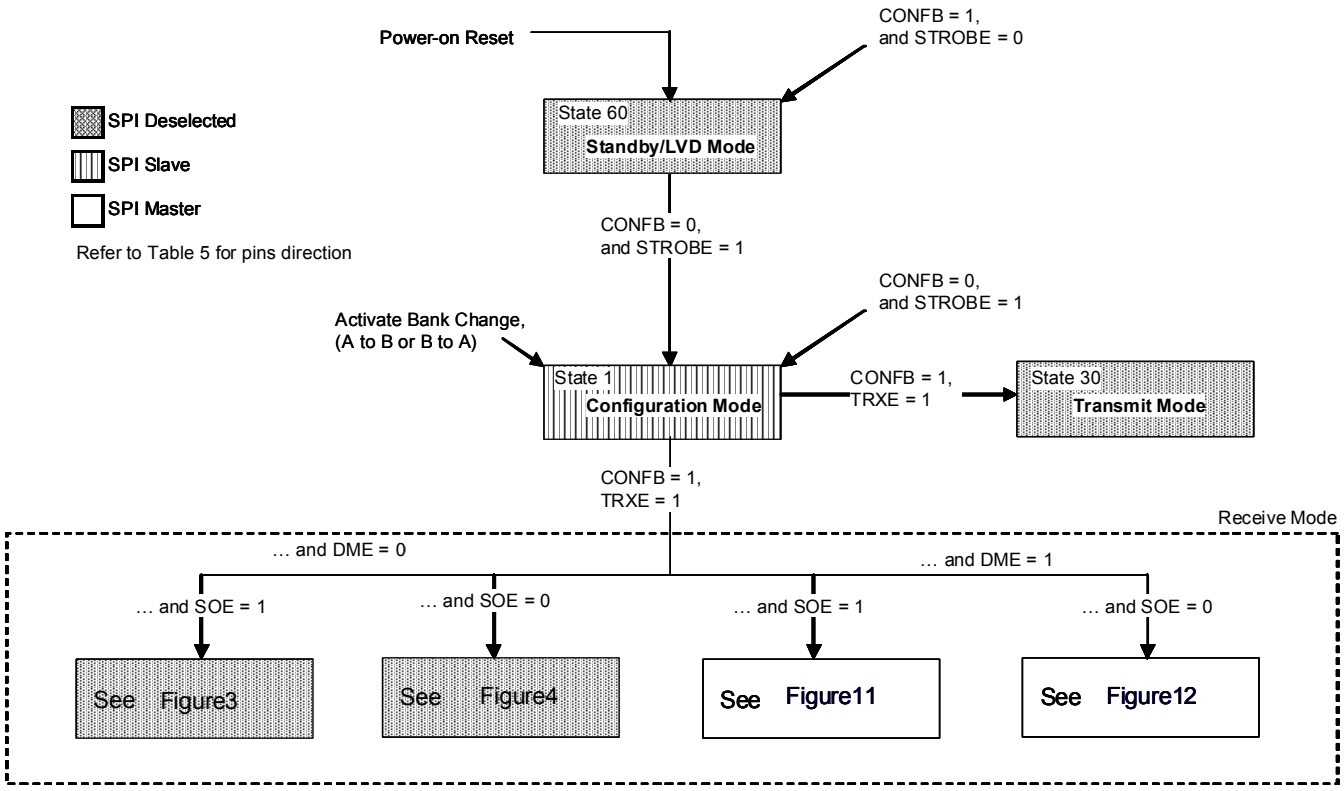


Figure 2. State Machine Overview

12 Receive Mode

The receiver is either waiting for an RF transmission or is receiving one. Two different processes are possible, as determined by the values of the DME bit. The transmitter part is kept off. A state diagram describes the sequence of operations in each case.

NOTE

If the STROBE pin is tied to a high level before switching to receive mode, the receiver does not go through an off or standby state.

12.1 Data Manager Disabled (DME=0)

Data manager disabled means that the SPI is deselected and raw data is sent directly on the MOSI line, while SCLK remains at low level.

Two different processes are possible, as determined by the values of the SOE bit.

12.1.1 Data Manager Disabled and Strobe Pin Control

Raw received data is sent directly on the MOSI line. Figure 3 shows the state diagram.

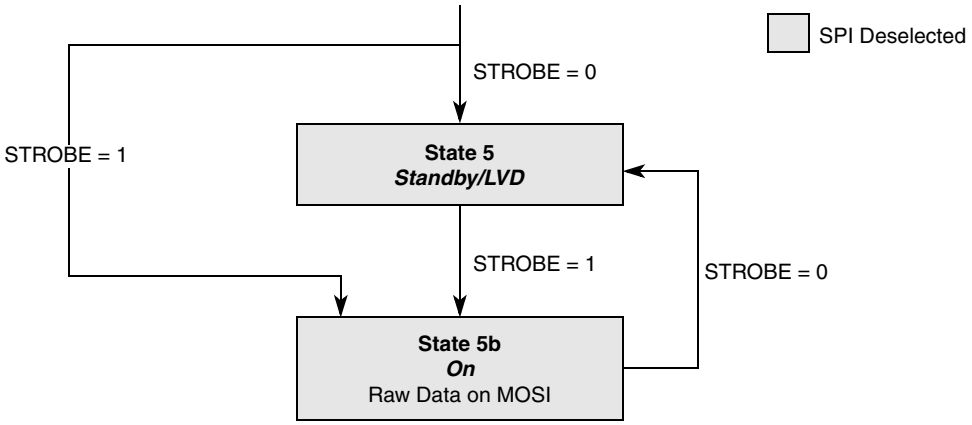


Figure 3. Receive Mode, DME = 0, SOE = 0

- State 5:

  The receiver is in standby/LVD mode. For further information, see Section 14, “Standby: LVD Mode.” A high level applied to STROBE forces the circuit to state 5b.
- State 5b:

  The receiver is kept on by the STROBE pin. Raw data is output on the MOSI line.

For all states: At any time, a low level applied to CONFB forces the state machine to state 1, configuration mode.

12.1.2 Data Manager Disabled and Strobe Oscillator Enabled

Raw received data is sent directly on the MOSI line. Figure 4 shows the state diagram.

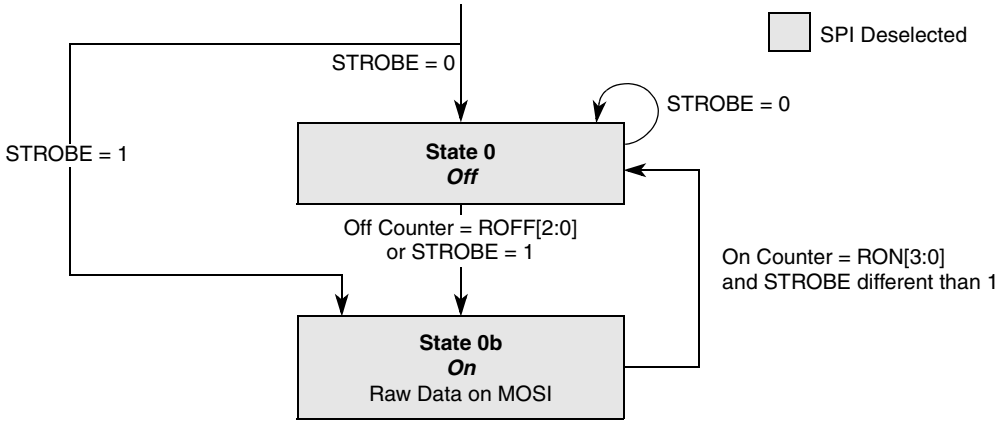


Figure 4. Receive Mode, DME = 0, SOE = 1

- State 0:

  The receiver is off, but the strobe oscillator and the off counter are running. Forcing the STROBE pin low freezes the strobe oscillator and maintains the system in this state.
- State 0b:

  If STROBE pin is set to high level or the off counter reaches the ROFF value, the receiver is on. Raw data is output on the MOSI line.

For all states: At any time, a low level applied to CONFB forces the state machine to state 1, configuration mode.

12.2 Data Manager Enabled (DME=1)

The data manager is enabled. The SPI is master. The MC33696 sends the recovered clock on SCLK and the received data on the MOSI line. Data is valid on falling edges of SCLK.

If an even number of bytes is received, the data manager may add an extra byte. The content of this extra byte is random. If the data received do not fill an even number of bytes, the data manager will fill the last byte randomly. Figure 5 shows a typical transfer.

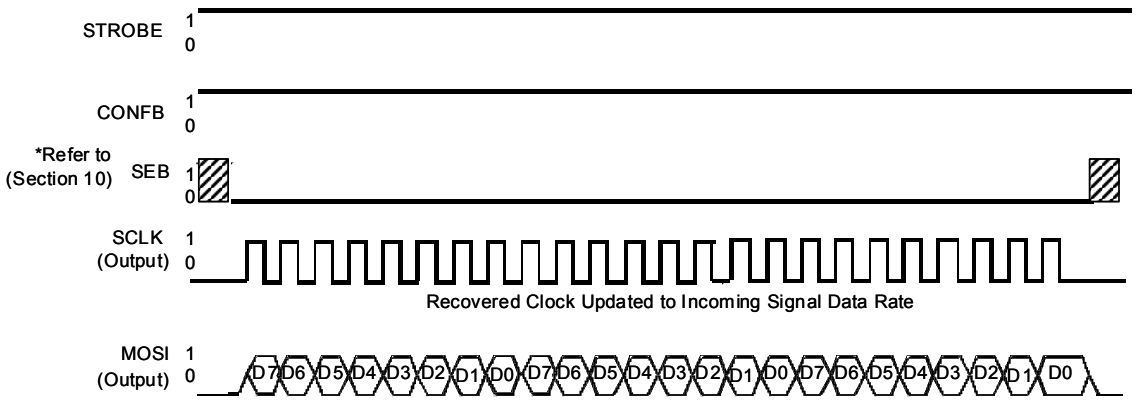


Figure 5. Typical Transfer in Receive mode with Data Manager

12.2.1 Data Manager Functions

In receive mode, Manchester coded data can be processed internally by the data manager. After decoding, the data is available on the digital interface, in SPI format. This minimizes the load on the MCU.

The data manager, when enabled (DME = 1), has five purposes:

- First ID detection: the received data are compared with the identifier stored in the ID register.
- Then the HEADER recognition: the received data is compared with the data stored in the HEADER register.
- Clock recovery: the clock is recovered during reception of the preamble and is computed from the shortest received pulse. While this signal is being received, the recovered clock is constantly updated to the data rate of the incoming signal.
- Output data and recovered clock on digital interface: see Figure 5.
- End-of-message detection: an EOM consists of two consecutive NRZ ones or zeroes.

Table 6 details some MC33696 features versus DME values.

Table 6. the **MC33696 Features versus DME**

DME	Digital Interface Use	Data Format	Output
0	SPI deselected, received data are directly sent to MOSI when CONFB = 1	Bit stream No clock	MOSI —
1	SPI master, data sent on MOSI with clock on SCLK when CONFB = 1	Data bytes Recovered clock	MOSI SCLK

12.2.2 Manchester Coding Description

The MC33696 data manager is able to decode Manchester-coded messages. For other codings, the data manager should be disabled (DME=0) for raw data to be available on MOSI.

DME = 0: The data manager is disabled. The SPI is deselected. Raw data is sent directly on the MOSI line, while SCLK remains at the low level.

Manchester coding is defined as follows: data is sent during the first half-bit; and the complement of the data is sent during the second half-bit. The signal average value is constant.

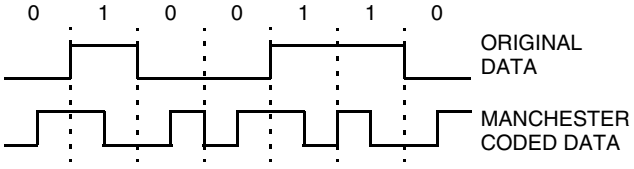


Figure 6. Example of Manchester Coding

Clock recovery can be extracted from the data stream itself. To achieve correct clock recovery, Manchester-coded data must have a duty cycle between 47% and 53%.

12.2.3 Frame Format

A complete telegram includes the following sequences: a preamble, an identifier (ID), a header, the message, and an end-of-message (EOM).

Figure 7. Example of Frame Format

These bit sequences are described below.

12.2.3.1 Preamble

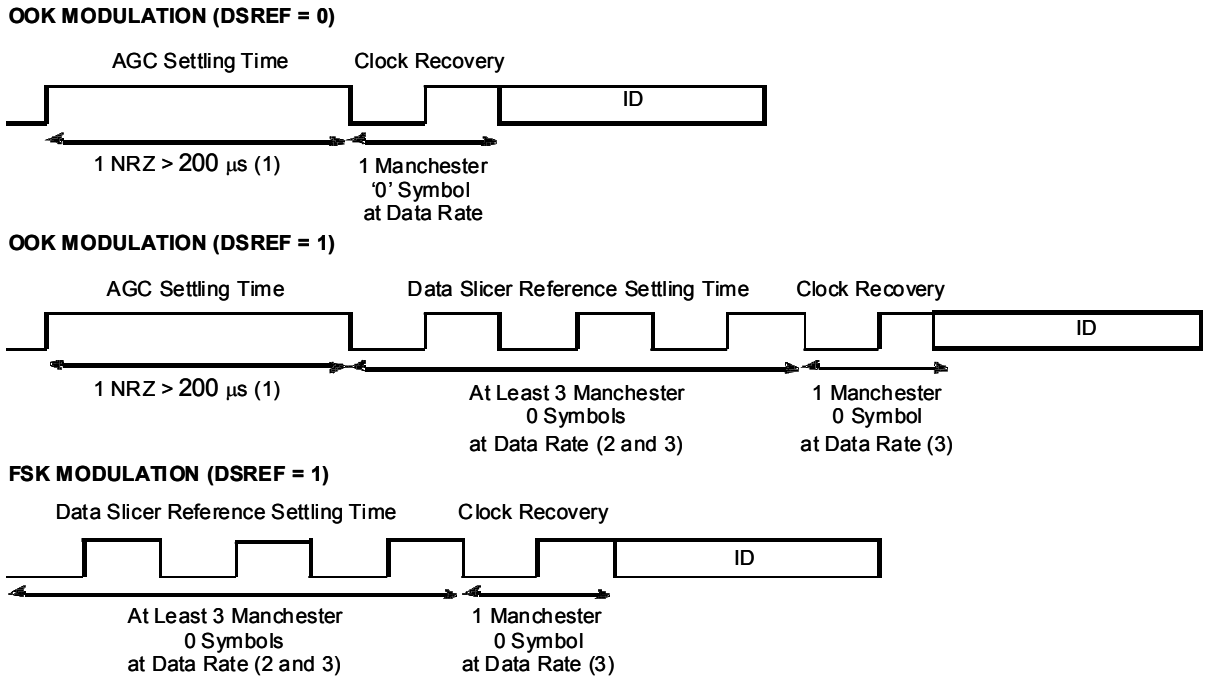
A preamble is required before the first ID detected. It enables:

- In the case of OOK modulation, the AGC to settle, and the data slicer reference voltage to settle if DSREF = 1
- In the case of FSK modulation, the data slicer reference voltage to settle
- The data manager to start clock recovery

No preamble is needed in case of several IDs are sent as shown in Figure 8. The ID field must be greater than two IDs. The first ID will have the same function as the preamble, and the second ID will have the same function as the single ID.

Figure 8. Example of Frame with Several IDs, No Preamble Needed

For both cases, the preamble content must be defined carefully, to ensure that it will not be decoded as the ID or the header. Figure 9 defines the different preamble in OOK and FSK modulation.



NOTES:
1. The AGC settling time pulse can be split over different pulses as long as the overall duration is at least 200 µs.
   The 200 µs pulse may be replaced by : (1 bit @ 2400 bps or 2 bits @ 4800 bps or 4 bits @ 9600 bps or 8 bits @ 19200 bps).
2. Table 14 defines the minimum number of Manchester symbols required for the data slicer operation versus the data and average filter cut-off frequencies.
3. The Manchester 0 symbol can be replaced by a 1.

Figure 9. Preamble Definition

12.2.3.2 ID

When clock recovery is done, the data manager verifies if an ID is received. The ID is used to identify a useful frame to receive. It is also necessary, when the receiver is strobed, to detect an ID in order to stay in run mode and not miss the frame.

The ID allows selection of the correct device in an RF transmission, as the content has been loaded previously in the ID register. Its length is variable, defined by the IDL[1:0] bits. The complement of the ID is also recognized as the identifier.

It is possible to build a tone to form the detection sequence by programming the ID register with a full sequence of ones or zeroes.

Once the ID is detected, a HEADER will be searched to detect the beginning of the useful data to send on the SPI port.

See Section 12.2.4, "State Machine in Receive Mode When DME=1" for more details when ID is not detected when SOE=1 or SOE=0.

12.2.3.3 HEADER

The HEADER defines the beginning of the message, as it is compared with the HEADER register. Its length is variable, defined by the HDL[1:0] bits. The complement of the header is also recognized as the header—in this case, output data is complemented. The header and its complement should not be part of the ID.

The ID and the header are sent at the same data rate as data.

12.2.3.4 Data and EOM

The data must follow the header, with no delay.

The message is completed with an end-of-message (EOM), consisting of two consecutive NRZ ones or zeroes (i.e., a Manchester code violation). Even in the case of FSK modulation, data must conclude with an EOM, and not simply by stopping the RF transmission.

12.2.4 State Machine in Receive Mode When DME=1

When the strobe oscillator is enabled (SOE = 1), the receiver is continuously cycling on/off. The ID must be recognized for the receiver to stay on. Consequently, the transmitted ID burst must be long enough to include two consecutive receiver-on cycles.

When the strobe oscillator is not enabled (SOE = 0), these timing constraints must be respected by the external control applied to pin STROBE.

Figure 11 shows the correct detection of an ID when STROBE is controled internally using the strobe oscillator (SOE=1) or externally by the MCU (SOE=0).

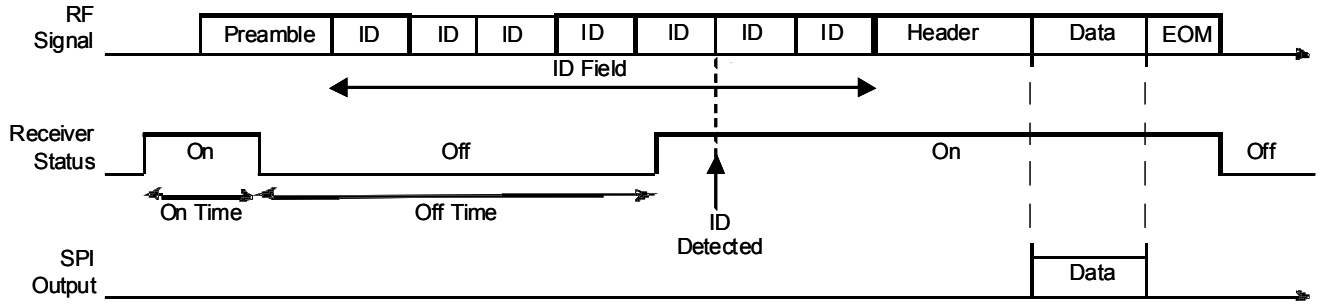


Figure 10. Complete Transmission with ID Detection

Two different processes are possible, as determined by the values of the SOE bit.

12.2.4.1 Data Manager Enabled and Strobe Oscillator Enabled

Figure 11 shows the state diagram when the data manager and the strobe oscillator are enabled. In this configuration, the receiver is controlled internally by the strobe oscillator. However, external control via the STROBE pin is still possible, and overrides the strobe oscillator command.

- State 10:

  The receiver is off, but the strobe oscillator and the off counter are running. Forcing STROBE pin to the low level maintains the system in this state.
- State 11:

  The receiver is waiting for a valid ID. If an ID, or its complement, is detected, the state machine advances to state 12; otherwise, the circuit goes back to state 10 at the end of the RON time, if STROBE ≠ 1.
- State 12:

  An ID or its complement has been detected. The data manager is now waiting for a header or its complement. If neither a header, nor its complement, has been received before a time-out of 256 bits at data rate, the system returns to state 10.
- State 13:

  A header, or its complement, has been received. Data and clock signals are output on the SPI port until EOM indicates the end of the data sequence. If the complement of the header has been received, output data are complemented also.

For all states: At any time, a low level applied to STROBE forces the circuit to state 10, and a low level applied on CONFB forces the state machine to state 1, configuration mode.

When an EOM occurs before the current byte is fully shifted out, dummy bits are inserted until the number of shifted bits is a multiple of 8.

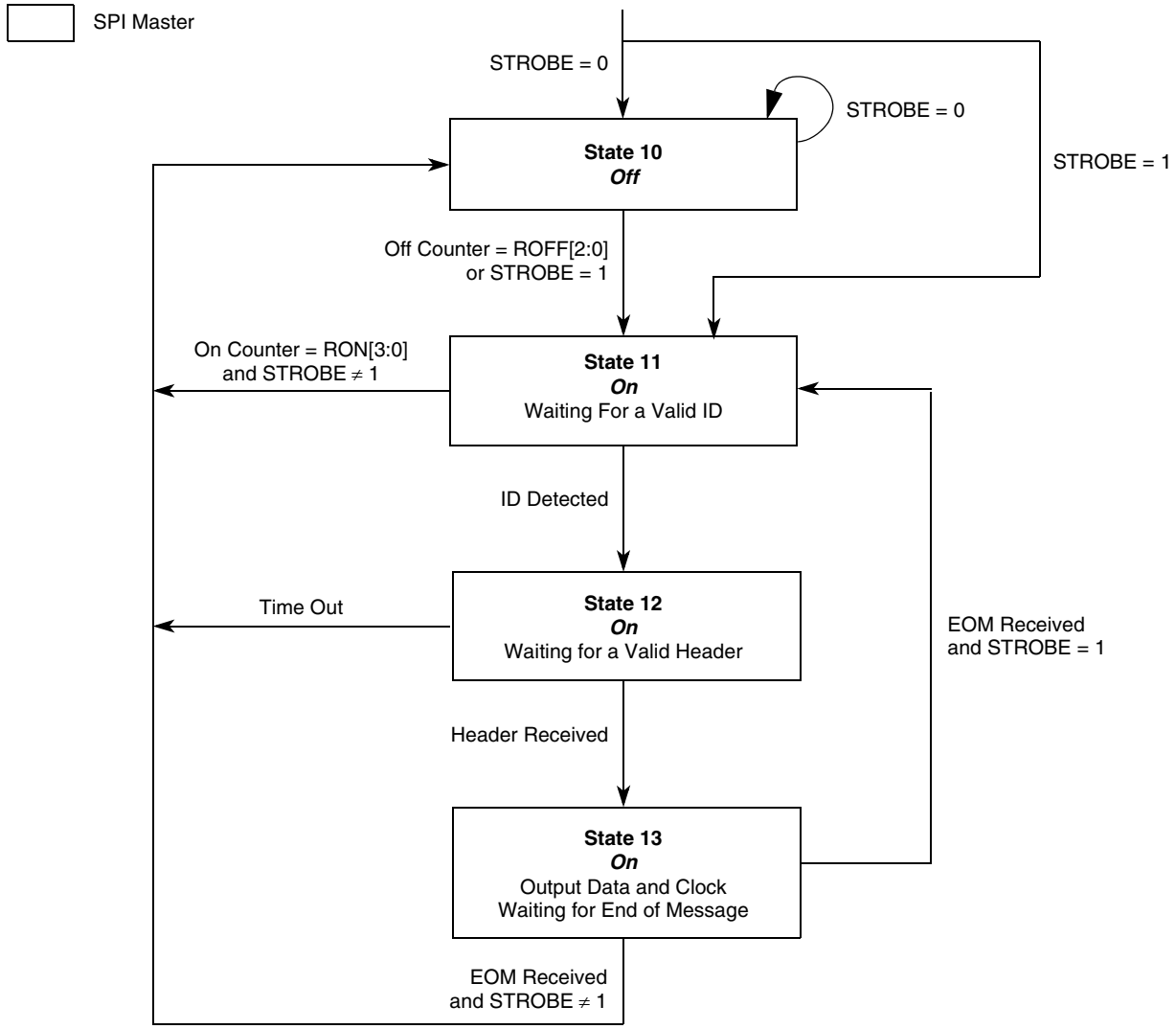


Figure 11. Receive Mode, DME = 1, SOE = 1

12.2.4.2 Data Manager Enabled and Receiver Controlled by Strobe Pin

Figure 12 shows the state diagram when the data manager is enabled and the strobe oscillator is disabled. In this configuration, the receiver is controlled only externally by the MCU.

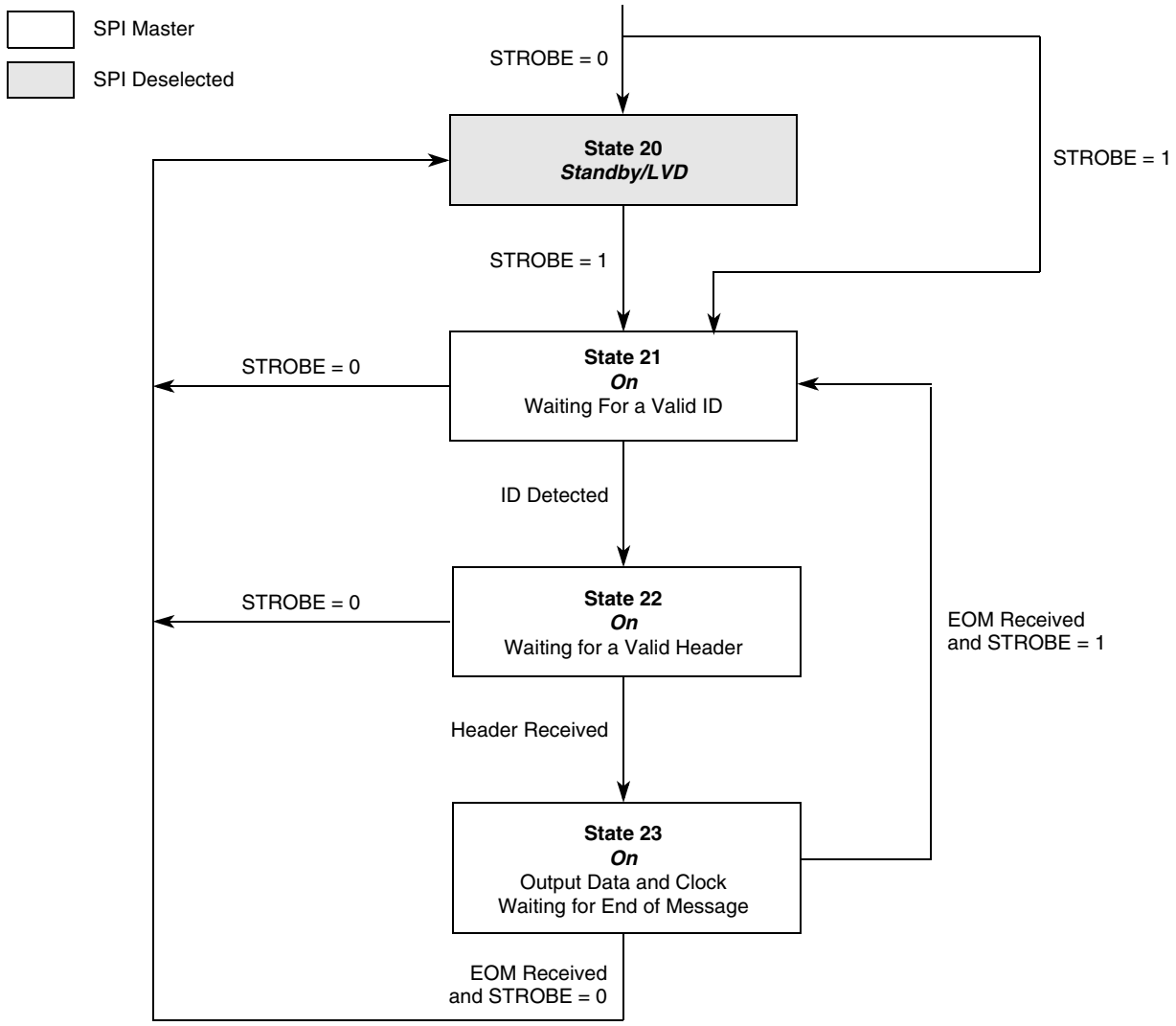


Figure 12. Receive Mode, DME = 1, SOE = 0

- State 20:

  The receiver is in standby/LVD mode. For further information, see Section 14, “Standby: LVD Mode.” A high level applied to STROBE forces the circuit to state 21.

- State 21:

  The circuit is waiting for a valid ID. If an ID, or its complement, is detected, the state machine advances to state 22; if not, the state machine will remain in state 21, as long as STROBE is high.

- State 22:

  If a header, or its complement, is detected, the state machine advances to state 23. If not, the state machine will remain in state 22, as long as STROBE is high.

- State 23:

  A header or its complement has been received; data and clock signals are output on the SPI port until an EOM indicates the end of the data sequence. If the complement of the header has been

received, output data are complemented also. When an EOM occurs before the current byte is fully shifted out, dummy bits are inserted until the number of shifted bits is a multiple of 8.

For all states: At any time, a low level applied to STROBE puts the circuit into state 20, and a low level applied to CONFB forces the state machine to state 1, configuration mode.

12.2.4.3 Timing Definition

As shown in Figure 13, a settling time is required when entering the on state.

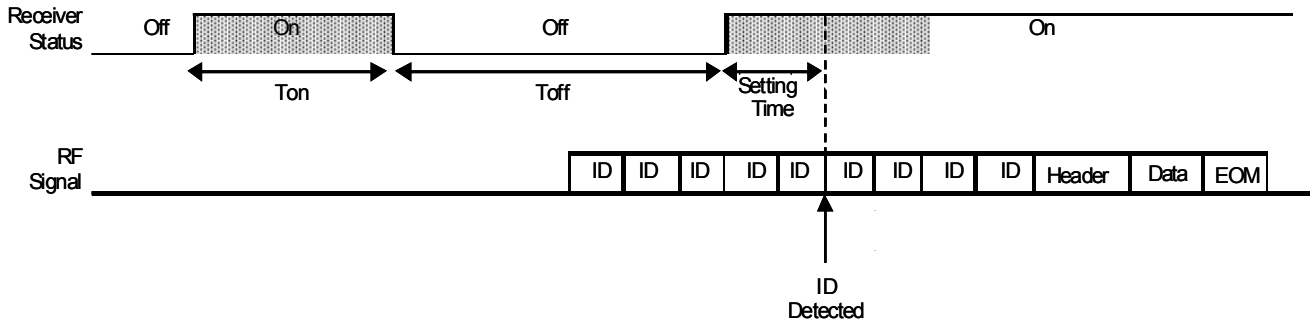


Figure 13. Receiver Usable Window

The goal for the receiver is to recognize at least one ID during Ton time. Many IDs are transmitted during that time.

During Ton, the receiver should be able to detect an ID, but as receiver and transmitter are not synchronized, an ID may already be transmitted when Ton time begins. That is the reason why Ton should be sized to receive two IDs: to be sure to recognize one, no matter what the time difference between beginning of transmission of the ID and beginning of run time for the receiver.

Ton should also include the setting time of the receiver. Setting time is composed of the crystal oscillator wakeup time[1], the PLL lock time[2], and setup of all analog parameters[3] (AGC and demodulator need some time to settle).

Toff should be sized to allow the positioning of an on state during the transmission of the ID field.

During the setting time, no reception is possible.

12.3 Receiver On/Off Control

In receive mode, on/off sequencing can be controlled internally using the strobe oscillator, or managed externally by the MCU through the input pin STROBE.

If the strobe oscillator is selected (SOE = 1):

- Off time is clocked by the strobe oscillator
- On time is clocked by the crystal oscillator, enabling accurate control of the on time, and therefore of the current consumption of the whole system

1. Refer to parameter 5.10 found in Section 21.5, “PLL & Crystal Oscillator.”
2. Refer to parameter 5.9 found in Section 21.5, “PLL & Crystal Oscillator.”
3. Refer to preamble definition found in Figure 9.

Each time is defined with the associated value found in the RXONOFF register.

- On time = RON[3:0] × 512 × T_{digclk} (see Table 19; begins after the crystal oscillator has started)
- Off time = receiver off time = N × T_{Strobe} + MIN (T_{Strobe} / 2, receiver on time), with N decoded from ROFF[2:0] (see Table 20)

The strobe oscillator is a relaxation oscillator in which an external capacitor C13 is charged by an internal current source (see Figure 46). When the threshold is reached, C13 is discharged and the cycle restarts. The strobe frequency is $F_{Strobe} = 1/T_{Strobe}$ with $T_{Strobe} = 10^6 \times C13$.

In receive mode, setting the STROBE pin to V_{CCIO} at any time forces the circuit on. As V_{CCIO} is above the oscillator threshold voltage, the condition on which the STROBE pin is set to V_{CCIO} is detected internally, and the oscillator pulldown circuitry is disabled. This limits the current consumption. After the STROBE pin is forced to high level, the external driver should pass via a “0” state to discharge the capacitor before going to high impedance state (otherwise, the on time would last a long time after the driver release).

When the strobe oscillator is running (i.e., during an off time), forcing the STROBE pin to V_{GND} stops the strobe clock, and therefore keeps the circuit off.

Figure 14 shows the associated timings.

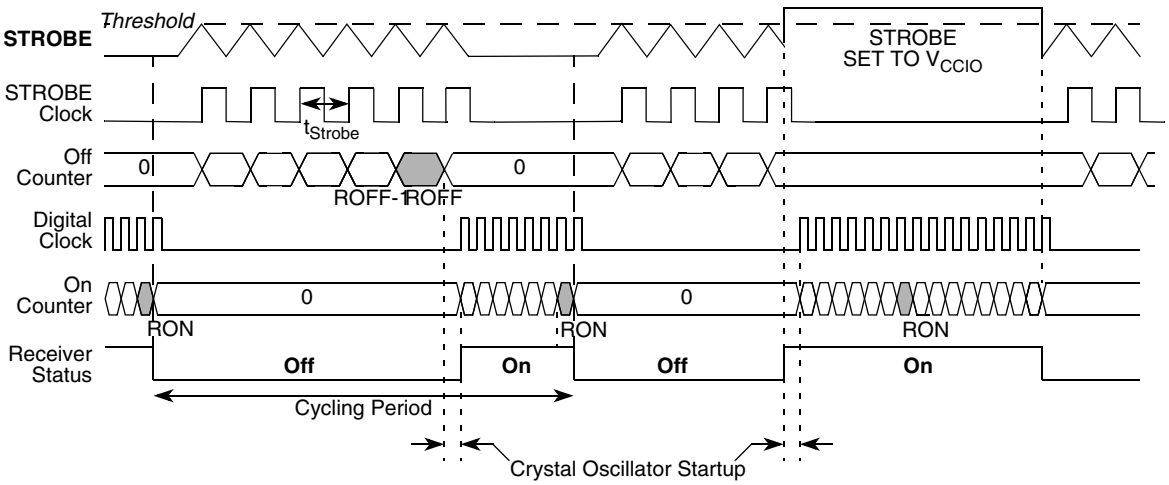


Figure 14. Receiver On/Off Sequence

12.4 Received Signal Strength Indicator (RSSI)

12.4.1 Module Description

In receive mode, a received signal strength indicator can be activated by setting bit RSSIE.

The input signal is measured at two different points in the receiver chain by two different means, as follows.

- At the IF filter output, a progressive compression logarithmic amplifier measures the input signal, ranging from the sensitivity level up to –50 dBm.

- At the LNA output, the LNA AGC control voltage is used to monitor input signals in the range –50 dBm to –20 dBm.

Therefore, the logarithmic amplifier provides information relative to the in-band signal, whereas the LNA AGC voltage senses the input signal over a wider band.

The RSSI information given by the logarithmic amplifier is available in:

- Analog form on pin RSSIOUT
- Digital form in the four least significant bits of the status register RSSI

The information from the LNA AGC is available in digital form in the four most significant bits of status register RSSI.

The whole content of status register RSSI provides 2 ¥ 4 bits of RSSI information about the incoming signal (see Section 18.6, “RSSI Register”).

Figure 15 shows a simplified block diagram of the RSSI function.

The quasi peak detector (D1, R1, C1) has a charge time of about 20 µs to avoid sensitivity to spikes.

R2 controls the decay time constant of about 5 ms to allow efficient smoothing of the OOK modulated signal at low data rates. This time constant is useful in continuous mode when S2 is permanently closed.

To allow high-speed RSSI updating in peak pulse measurement, a discharge circuit (S1) is required to reset the measured voltage and to allow new peak detection.

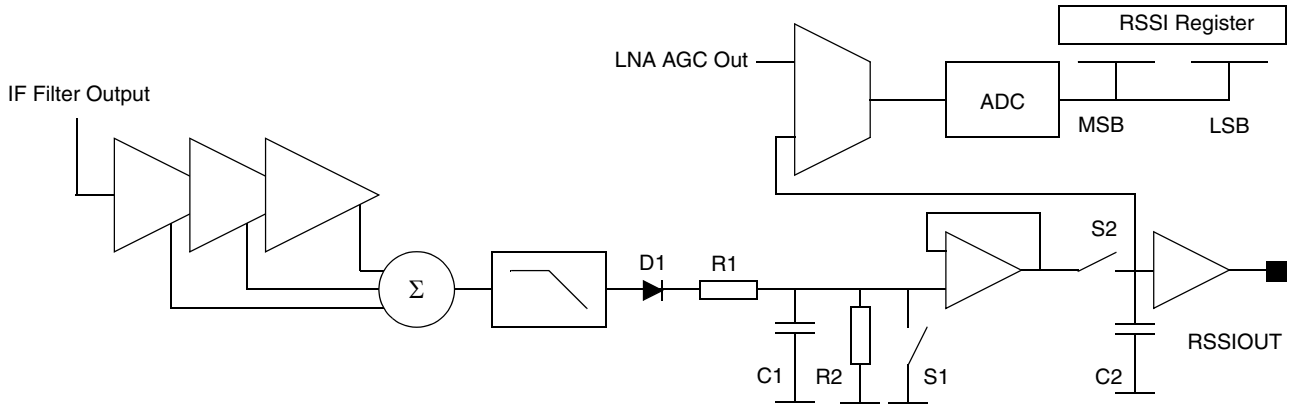


Figure 15. RSSI Simplified Block Diagram

S2 is used to sample the RSSI voltage to allow peak pulse measurement (S2 used as sample and hold), or to allow continuous transparent measurement (S2 continuously closed).

The 4-bit analog-to-digital convertor (ADC) is based on a flash architecture. The conversion time is $16 \times T_{diglck}$. As a single convertor is used for the two analog signals, the RSSI register content is updated on a $32 \times T_{digclk}$ timebase.

If RSSIE is reset, the whole RSSI module is switched off, reducing the current consumption. The output buffer connected to RSSIOUT is set to high impedance.

12.4.2 Operation

Two modes of operation are available: sample mode and continuous mode.

12.4.2.1 Sample Mode

Sample mode allows the peak power of a specific pulse in an incoming frame to be measured.

The quasi peak detector is reset by closing S1. After 7 × T_{digclk}, S1 is released. S2 is closed when RSSIC is set high. On the falling edge of RSSIC, S2 is opened. The voltage on RSSIOUT is sampled and held. The last RSSI conversion results are stored in the RSSI register and no further conversion is done.

The RSSI register is updated every 32 × T_{digclk}. Therefore, the minimum duration of the high pulse on RSSIC is 32 × T_{digclk}.

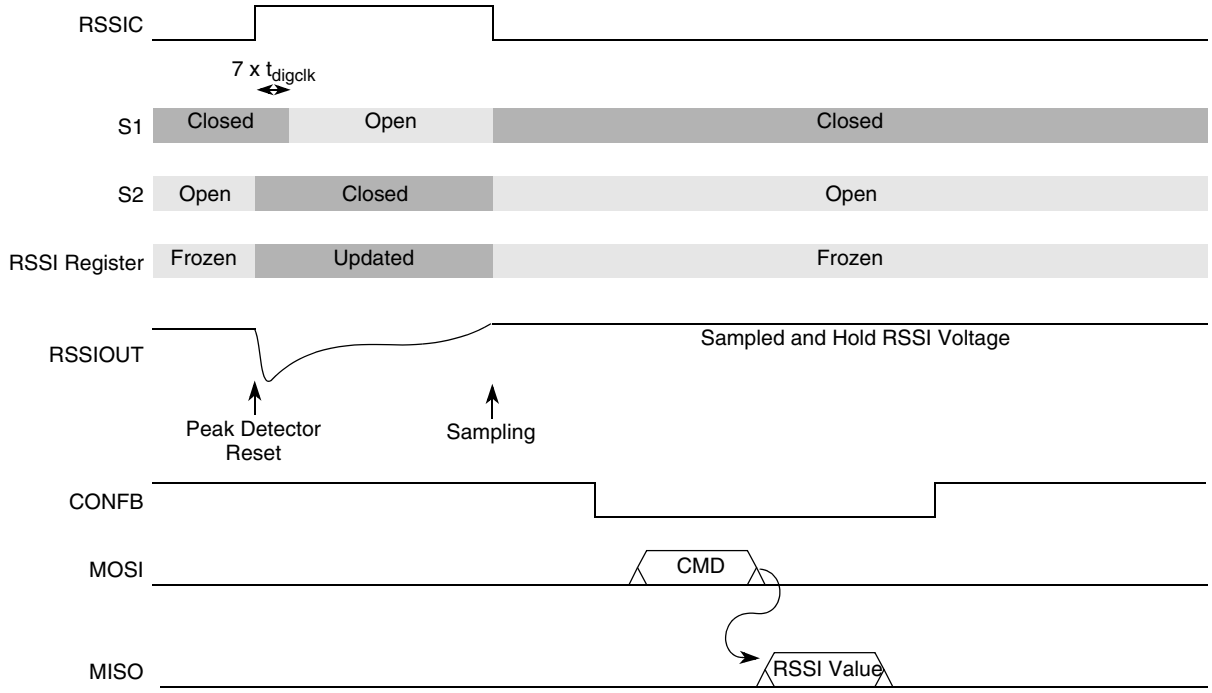


Figure 16. RSSI Operation in Sample Mode

12.4.2.2 Continuous Mode

Continuous mode is used to make a peak measurement on an incoming frame, without having to select a specific pulse to be measured.

The quasi peak detector is reset by closing S1. After 7 × T_{digclk}, S1 is opened. S2 is closed when RSSIC is set high. As long as RSSIC is kept high, S2 is closed, and RSSIOUT follows the peak value with a decay time constant of 5 ms.

The ADC runs continuously, and continually updates the RSSI register. Thus, reading this register gives the most recent conversion value, prior to the register being read. The minimum duration of the high pulse on CONFB is 32 × T_{digclk}.