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Document Number: MC33742
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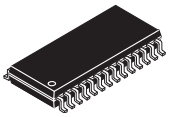
System Basis Chip with Enhanced High Speed CAN Transceiver

33742
33742S

SYSTEM BASIS CHIP



EG SUFFIX (PB-FREE)
98ASB42345B
28-PIN SOICW

EP SUFFIX
(PB-FREE)
98ASA00757D
48-PIN QFN

The 33742 and the 33742S SMARTMOS devices are SPI-controlled System Basis Chips (SBCs), combining many frequently used functions, along with a CAN 2.0-compliant transceiver, used in many automotive electronic control units (ECUs). The 33742 SBC has a fully protected fixed 5.0 V low dropout internal regulator, with current limiting, overtemperature prewarning, and reset. A second 5.0 V regulator can be implemented using external pass PNP bipolar junction pass transistor, driven by the SBC's external V2 sense input and V2 output drive pins.

The SBC has four main operating modes: Normal, Standby, Stop, and Sleep mode. Additionally, there is an internally switched high side power supply output, four wake-up inputs pins, a programmable window watchdog, interrupt, reset, and a SPI module for communication and control. The high speed CAN A and B transceiver is available for intermodule communication.

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33742PEG/R2	-40 °C to 125 °C	28 SOICW
MC33742SPEG/R2		
MC33742PEP/R2		48 QFN

Features

- 1.0 Mbps CAN transceiver bus interface with bus diagnostic capability
- SPI control at frequencies up to 4.0 MHz
- 5.0 V low dropout voltage regulator with current limiting, over-temperature prewarning, and output monitoring and reset
- A second 5.0 V regulator capability using an external series pass transistor
- Normal, Standby, Stop, and Sleep modes of operation with low Sleep and Stop mode current
- A high side switch output driver for controlling external circuitry

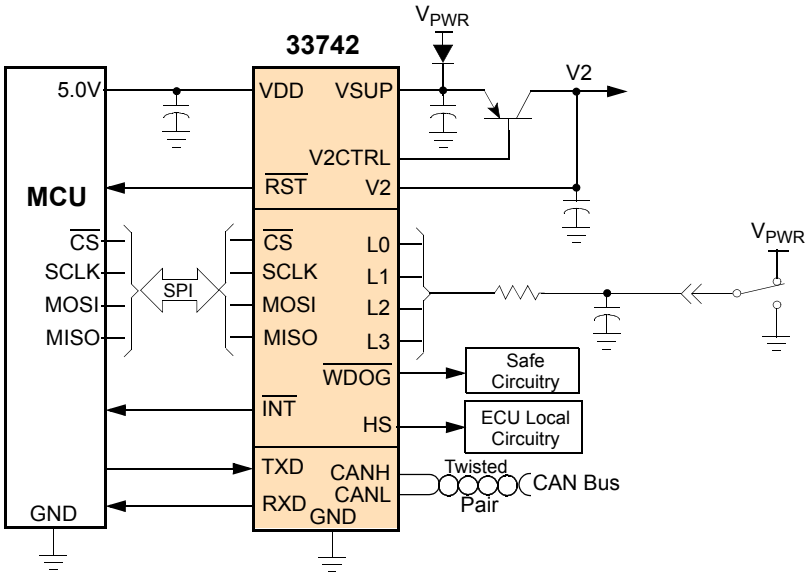


Figure 1. 33742 Simplified Application Diagram

DEVICE VARIATIONS

Table 1. Device Differences During a Reset Condition

Part No.	Reset Duration	Device Differences	See Page
33742	15 ms (typical)	The duration the $\overline{RST}$ pin is asserted low when the Reset mode is entered after the SBC is powered up, a V_{DD} under-voltage condition is detected, and the watchdog register is not properly triggered.	page 18
33742S	3.5 ms (typical)	The duration the $\overline{RST}$ pin is asserted low when the Reset mode is entered after the SBC is powered up, a V_{DD} under-voltage condition is detected, and the watchdog register is not properly triggered.	page 18

INTERNAL BLOCK DIAGRAM

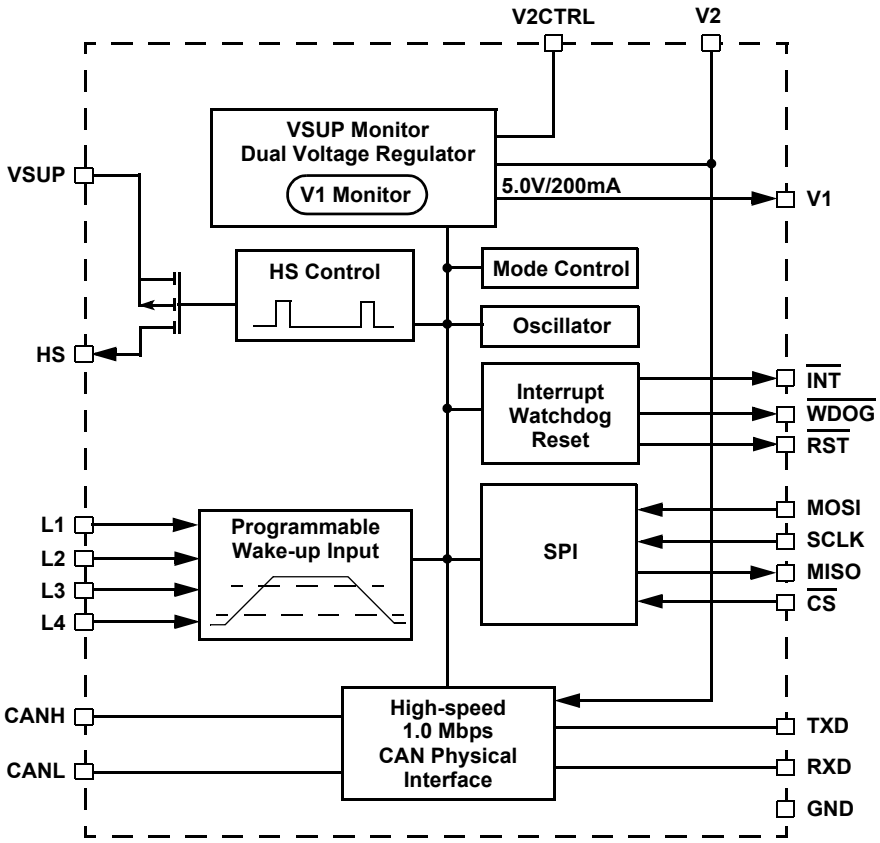


Figure 2. 33742 Simplified Internal Block Diagram

PIN CONNECTIONS

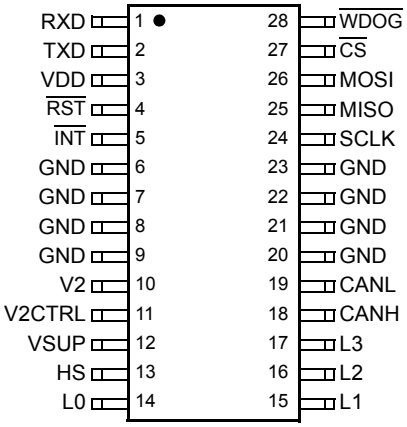


Figure 3. 33742 28-Pin Connections

Table 2. 33742 28-Pin Definitions

A functional description of each pin can be found in the Functional Pin description section beginning on page 22.

Pin	Pin Name	Formal Name	Definition
1	RXD	Receive Data	CAN bus receive data output pin.
2	TXD	Transmit Data	CAN bus transmit data input pin.
3	VDD	Voltage Digital Drain	5.0 V regulator output pin. Supply pin for the MCU.
4	$\overline{RST}$	Reset Output (Active LOW)	This is the device reset output pin whose main function is to reset the MCU. This pin has an internal -up current source to VDD.
5	$\overline{INT}$	Interrupt Output (Active LOW)	This output is asserted LOW when an enabled interrupt condition occurs. The output is a push-pull structure.
6–9 20–23	GND	Ground	These device ground pins are internally connected to the package lead frame to provide a 33742-to-PCB thermal path.
10	V2	Voltage Source 2	Sense input for the V2 regulator using an external series pass transistor. V2 is also the internal supply for the CAN transceiver.
11	V2CTRL	Voltage Source 2 Control	Output drive source for the V2 regulator connected to the external series pass transistor.
12	VSUP	Voltage Supply	Supply input pin for the 33742.
13	HS	High Side Output	Output of the internal high side switch. The output current is internally limited to 150 mA.
14–17	L0-L3	Level 0-3 Inputs	Inputs from external switches or from logic circuitry.
18	CANH	CAN High Output	CAN high output pin.
19	CANL	CAN Low Output	CAN low output pin.
24	SCLK	Serial Data Clock	Clock input pin for the Serial Peripheral Interface (SPI).
25	MISO	Master In Slave Out	SPI data sent to the MCU by the 33742. When CS is HIGH, the pin is in the high-impedance state.
26	MOSI	Master Out Slave In	SPI data received by the 33742.
27	$\overline{CS}$	Chip Select (Active LOW)	The CS input pin is used with the SPI bus to select the 33742. When the CS is asserted LOW, the 33742 is the selected device of the SPI bus.
28	$\overline{WDOG}$	Watchdog Output (Active LOW)	The WDOG output pin is asserted LOW if the software watchdog is not correctly triggered.

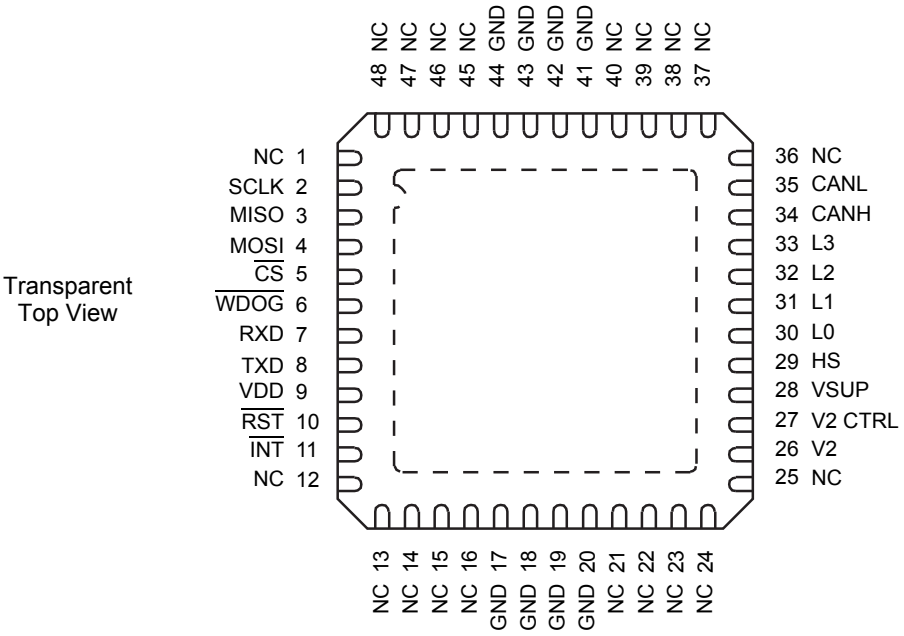


Figure 4. 33742 48-Pin Connections

Table 3. 33742 48-Pin Definitions

A functional description of each pin can be found in the Functional Pin description section beginning on page 22.

Pin	Pin Name	Formal Name	Definition
1, 12-16, 21-25, 36-40, 45-48	NC	No Connect	No connection.
2	SCLK	Serial Data Clock	Clock input pin for the Serial Peripheral Interface (SPI).
3	MISO	Master In Slave Out	SPI data sent to the MCU by the 33742. When CS is HIGH, the pin is in the high-impedance state.
4	MOSI	Master Out Slave In	SPI data received by the 33742.
5	$\overline{CS}$	Chip Select (Active LOW)	The CS input pin is used with the SPI bus to select the 33742. When the CS is asserted LOW, the 33742 is the selected device of the SPI bus.
6	$\overline{WDOG}$	Watchdog Output (Active LOW)	The WDOG output pin is asserted LOW if the software watchdog is not correctly triggered.
7	RXD	Receive Data	CAN bus receive data output pin.
8	TXD	Transmit Data	CAN bus transmit data input pin.
9	VDD	Voltage Digital Drain	5.0 V regulator output pin. Supply pin for the MCU.
10	$\overline{RST}$	Reset Output (Active LOW)	This is the device reset output pin whose main function is to reset the MCU. This pin has an internal pull-up current source to VDD.
11	$\overline{INT}$	Interrupt Output (Active LOW)	This output is asserted LOW when an enabled interrupt condition occurs. The output is a push-pull structure.
17-20 41-44	GND	Ground	These device ground pins are internally connected to the package lead frame to provide a 33742-to-PCB thermal path.

Table 3. 33742 48-Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin description section beginning on page 22.

Pin	Pin Name	Formal Name	Definition
26	V2	Voltage Source 2	Sense input for the V2 regulator using an external series pass transistor. V2 is also the internal supply for the CAN transceiver.
27	V2CTRL	Voltage Source 2 Control	Output drive source for the V2 regulator connected to the external series pass transistor.
28	VSUP	Voltage Supply	Supply input pin for the 33742.
29	HS	High Side Output	Output of the internal high side switch. The output current is internally limited to 150 mA.
30-33	L0-L3	Level 0-3 Inputs	Inputs from external switches or from logic circuitry.
34	CANH	CAN High Output	CAN high output pin.
35	CANL	CAN Low Output	CAN low output pin.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 4. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Power Supply Voltage at VSUP Continuous (Steady-state) Transient Voltage (Load Dump)	V_{SUP}	 -0.3 to 27 -0.3 to 40	V
Logic Signals (RXD, TXD, MOSI, MISO, $\overline{CS}$, SCLK, $\overline{RST}$, $\overline{WDOG}$, and $\overline{INT}$)	V_{LOG}	-0.3 to V_{DD} + 0.3	V
Output Voltage at VDD	V_{DD}	0.0 to 5.3	V
Output Current at VDD	I_{DD}	Internally Limited	A
HS Voltage Output Current	 V_{HS} I_{HS}	 -0.3 to V_{SUP} + 0.3 Internally Limited	 V A
ESD Capability, Human Body Model[1] MC33742 in 28-pin SOIC HS, L0, L1, L2, L3, CANH, CANL pins All Other pins MC33742 in 48-pin QFN All pins	V_{ESD1}	 ±4000 ±2000 ±2000	V
ESD Capability, Machine Model[1]	V_{ESD2}	±200	V
Input Voltage/Current at L0, L1, L2, L3 DC Input Voltage DC Input Current Transient Input Voltage attached to external circuitry[2]	 V_{DCIN} I_{DCIN} V_{TRINEC}	 -0.3 to 40 ±2.0 ±100	 V mA V
CANL and CANH Continuous Voltage Continuous Current	 $V_{CANH/L}$ $I_{CANH/L}$	 -27 to 40 200	 V mA
CANH and CANL Transient Voltage (Load Dump)[3]	$V_{LDH/L}$	40	V
CANH and CANL Transient Voltage[3]	$V_{TRH/L}$	±40	V

Notes

1. Testing done in accordance with the Human Body Model (C_{ZAP}=100 pF, R_{ZAP}=1500 Ω), Machine Model (C_{ZAP}=200 pF, R_{ZAP}=0 Ω).
2. Testing done in accordance with ISO 7637-1. See Figure 5.
3. Load dump testing done in accordance with ISO 7637-1, Transient test done in accordance with ISO 7637-1. See Figure 6.

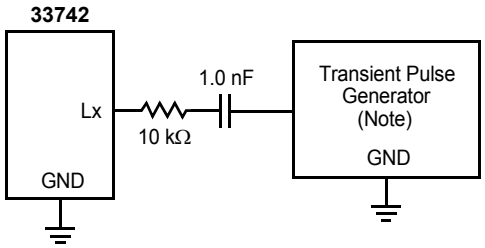
Table 4. Maximum Ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
THERMAL RATINGS			
Operating Temperature Ambient Junction	 T_A T_J	 -40 to 125 -40 to 150	°C
Storage Temperature	T_{STG}	-55 to 165	°C
Thermal Resistance	$R_{\theta JG}$	20	°C/W
Thermal Resistance Junction Case (QFN)	R_{TJC}-$R_{\theta JC}$	TBD	°C/W
Power Dissipation[4]	P_D	1.0	W
Peak Package Reflow Temperature During Reflow[6],[7]	T_{PPRT}	Note 7	°C

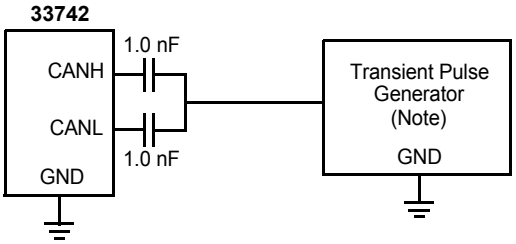
Notes

4. Maximum power dissipation is at 85 °C ambient temperature in free air and with no heatsink, according to JEDEC JESD51-2 and JESD51-3 specifications.
5. The package is not designed for immersion soldering. The maximum soldering time is 10 seconds at 240 °C on any pin. Exceeding the maximum temperature and time limits may cause permanent damage to the device.
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
7. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.



Note Waveform per ISO 7637-1. Test Pulses 1, 2, 3a, and 3b.

Figure 5. Transient Test Setup for L0:L3 Inputs



Note Waveform per ISO 7637-1. Test Pulses 1, 2, 3a, and 3b.

Figure 6. Transient Test Setup for CANH/CANL

STATIC ELECTRICAL CHARACTERISTICS

Table 5. Static Electrical Characteristics

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT PIN (VSUP)					
Supply Voltage	V_{SUP}				V
Nominal DC Voltage		5.5	—	18	
Extended DC Voltage: Full Functionality[8]		18	—	27	
Extended DC Voltage: Reduced Functionality[9]		4.5	—	5.5	
Load Dump		—	—	40	
Jump Start		—	—	27	
Supply Current in Standby Mode[10] (I_{OUT} at VDD = 40 mA, CAN Recessive or Sleep Mode)	$I_{SUP(STDBY)}$				mA
T_A ≥ 25 °C		—	42	45	
Supply Current in Normal Mode[10] (I_{OUT} at VDD = 40 mA, CAN Recessive or Sleep mode)	$I_{SUP(NORM)}$				mA
T_A ≥ 25 °C		—	42	45	
Supply Current in Sleep Mode[10] (VDD and V2 OFF, CAN in Sleep Mode with CAN Wake-up Disabled[11])	$I_{SUP(SLP-WD)}$				µA
V_{SUP} < 13.5 V, Oscillator Running[12]		—	85	105	
V_{SUP} < 13.5 V, Oscillator Not Running[13]		—	53	80	
V_{SUP} = 18 V, Oscillator Running[12]		—	110	140	
Supply Current in Sleep Mode[10] (V1 and V2 OFF, V_{SUP} < 13.5 V, Oscillator Not Running[13], CAN in Sleep Mode with Wake-up Enabled)	$I_{SUP(SLP-WE)}$				µA
T_A = -40 °C		—	80	—	
T_A = 25 °C		—	65	—	
T_A = 125 °C		—	55	—	
Supply Current in Stop Mode[10] (I_{OUT} at VDD < 2.0 mA, VDD ON, CAN in Sleep Mode with Wake-up Disabled[11])	$I_{SUP(STOP-WD)}$				µA
VSUP < 13.5 V, Oscillator Running[12]		—	—	160	
VSUP < 13.5 V, Oscillator Not Running[13]		—	80	160	
VSUP = 18 V, Oscillator Running[12]		—	100	210	

Notes

8. All functions and modes available and operating: Watchdog, HS turn ON/turn OFF, CAN transceiver operating, L0:L3 inputs operating, normal SPI operation. The 33742 may experience an over-temperature fault.
9. At VDD > 4.0 V, $\overline{RST}$ HIGH if reset 2 selected via SPI. The logic HIGH level will be degraded but the 33742 is functional.
10. Current measured at the VSUP pin.
11. If CAN Module is Sleep-enabled for wake-up, an additional current ($I_{CAN-SLEEP}$) must be added to specified value.
12. Oscillator running means one of the following function is active: Forced Wake-up *or* Cyclic Sense *or* Software Watchdog in Stop mode.
13. Oscillator not running means none of the following functions are active: Forced Wake-up *and* Cyclic Sense *and* Software Watchdog in Stop mode.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT PIN (VSUP) (CONTINUED)					
Supply Current in Stop Mode[14] (I_{OUT} at VDD < 2.0 mA, VDD ON, VSUP < 13.5 V, Oscillator Not Running, CAN in Sleep Mode with Wake-up Enabled)[15]	$I_{SUP(STOP-WE)}$				μA
T_A = -40 °C		—	100	—	
T_A = 25 °C		—	92	—	
T_A = 125 °C		—	80	—	
BATFAIL Flag Internal Threshold	V_{BF}	1.5	3.0	4.0	V
BATFAIL Flag Hysteresis[16]	$V_{BF(HYS)}$	—	1.0	—	V
Battery Fall Early Warning Threshold	$V_{BF(EW)}$				V
In Normal and Standby Modes		5.3	5.8	6.3	
Battery Fall Early Warning Hysteresis	$V_{BF(EW-HYST)}$				V
In Normal and Standby Modes[16]		0.1	0.2	0.3	
OUTPUT PIN (VDD)[17]					
VDD Output Voltage (2.0 mA < I_{V1} < 200 mA)	V_{DDOUT}				V
5.5 V < VSUP < 27 V		4.9	5.0	5.1	
4.5 V < VSUP < 5.5 V		4.0	—	—	
Dropout Voltage	V_{DDDRP1}				V
I_{DD} = 200 mA		—	0.2	0.5	
Dropout Voltage, Limited Output Current and Low V_{SUP}	V_{DDDRP2}				V
I_{DD} = 50 mA, 4.5 V < VSUP		—	0.1	0.25	
Output Current	I_{DD}				mA
Internally Limited		200	285	350	
Thermal Shutdown (Junction)	T_{SD}				°C
Normal or Standby Mode		160	—	200	
Over-temperature Pre-warning (Junction)	T_{PW}				°C
VDDTEMP Bit Set		125	—	160	

Notes

14. Current measured at the VSUP pin.
15. Oscillator not running means none of the following functions are active: Forced Wake-up *and* Cyclic Sense *and* Software Watchdog in Stop mode.
16. Guaranteed by design; it is not production tested.
17. I_{DD} is the total regulator output current. V1 specification with external capacitor. Stability requirement: Capacitance > 47 μF, ESR < 1.3 Ω (tantalum capacitor). In Reset, Normal Request, Normal and Standby modes. Measures with capacitance = 47 μF tantalum.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT PIN (VDD) (CONTINUED)[18]					
Temperature Threshold Difference	T_{SD} - T_{PW}	20	—	40	°C
Reset Threshold Threshold 1, Default Value after Reset, RSTTH Bit Set to Logic [0] Threshold 2, RSTTH Bit Set to Logic [1]	$V_{\overline{RSTTH}}$	 4.5 4.0	 4.6 4.2	 4.7 4.3	V
VDD for Reset Active	V_{DDR}	1.0	—	$V_{\overline{RSTTH}}$	V
Line Regulation (I_{DD} = 10 mA, Capacitance = 47 μF Tantalum at VDD) 9.0 V < V_{SUP} < 18 V 5.5 V < V_{SUP} < 27 V	V_{DDR}	 — —	 5.0 10	 25 25	mV
Load Regulation (Capacitance = 47 μF Tantalum at V1) 1.0 mA < I_{DD} < 200 mA	V_{LD}	 —	 25	 75	mV
Thermal Stability V_{SUP} = 13.5 V, I_{DD} = 100 mA[19]	$V_{THERM-S}$	 —	 30	 50	mV
OUTPUT PIN IN STOP MODE (VDD)[18]					
VDD Output Voltage I_{DD} ≤ 2.0 mA I_{DD} ≤ 10 mA	V_{DDSTOP}	 4.75 4.75	 5.0 5.0	 5.25 5.25	V
I_{DD} Output Current to Wake-up	I_{DDS-WU}	10	17	25	mA
Reset Threshold[18] Threshold 1, Default Value after Reset, RSTTH Bit Set to Logic [0] Threshold 2, RSTTH Bit Set to Logic [1]	$V_{\overline{RST}-STOP}$	 4.5 4.1	 4.6 4.2	 4.7 4.3	V
Line Regulation (Capacitance = 47 μF Tantalum at VDD) 5.5 V < V_{SUP} < 27 V, I_{DD} = 2.0 mA	$V_{LR-STOP}$	 —	 5.0	 25	mV
Load Regulation (Capacitance = 47 μF Tantalum at V1) 1.0 mA < I_{DD} < 10 mA	$V_{LD-STOP}$	 —	 15	 75	mV

Notes

18. I_{DD} is the total regulator output current. VDD specification with external capacitor. Stability requirement: capacitance > 47 μF, ESR < 1.3 Ω (tantalum capacitor). In Reset, Normal Request, Normal and Standby modes, measures with capacitance = 47 μF tantalum.Selectable by RSTTH bit in SPI Register Reset Control Register (RCR).
19. Guaranteed by characterization and design; it is not production tested.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
TRACKING VOLTAGE REGULATOR (V2)[20]					
V2 Output Voltage (Capacitance = 10 µF Tantalum at V2) 2.0 mA ≤ I_{V2} ≤ 200 mA, 5.5 V < V_{SUP} < 27 V	V_2	0.99	1.0	1.01	V_{DD}
I_{V2} Output Current (for Information Only) Depending on External Ballast Transistor	I_{V2}	200	—	—	mA
V2 Control Drive Current Capability[21] Worst Case at T_J = 125 °C	I_{V2CTRL}	0.0	—	10	mA
V2LOW Flag Threshold	V_{2LTH}	3.75	4.0	4.25	V
LOGIC OUTPUT PIN (MISO)[22]					
Low-level Output Voltage I_{OUT} = 1.5 mA	V_{OL}	0.0	—	1.0	V
High-level Output Voltage I_{OUT} = -250 µA	V_{OH}	V_{DD}-0.9	—	V_{DD}	V
Tri-stated MISO Leakage Current 0 V < V_{MISO} < V_{DD}	I_{HZ}	-2.0	—	2.0	µA
LOGIC INPUT PINS (MOSI, SCLK, **$\overline{CS}$**)					
High-level Input Voltage	V_{IH}	0.7 V_{DD}	—	V_{DD} + 0.3	V
Low-level Input Voltage	V_{IL}	-0.3	—	0.3 V_{DD}	V
High-level Input Current on $\overline{CS}$ V_{IN} = 4.0 V	I_{IH}	-100	—	-20	µA
Low-level Input Current on $\overline{CS}$ V_{IN} = 1.0 V	I_{IL}	-100	—	-20	µA
MOSI and SCLK Input Current 0 V < V_{IN} < V_{DD}	I_{IN}	-10	—	10	µA
OUTPUT PIN (RST)[23]					
High-level Output Current 0 V < V_{OUT} < 0.7 V_{DD}	I_{OH}	-300	-250	-150	µA
Low-level Output Voltage I_O = 1.5 mA, 5.5 V < V_{SUP} < 27 V I_O = 0 mA, 1.0 V <V_{SUP} < 5.5 V	V_{OL}	0.0 0.0	— —	0.9 0.9	V
$\overline{RST}$ Pull-down Current V > 0.9 V	I_{PDW}	2.3	—	5.0	mA

Notes
20. V2 specification with external capacitor. Stability requirement: capacitance > 42 µF and ESR < 1.3 Ω (tantalum capacitor), external resistor between base and emitter required. Measurement conditions: ballast transistor MJD32C, capacitance > 10 µF tantalum, 2.2 kΩ resistor between base and emitter of ballast transistor.
21. The guaranteed V2CTRL current capability is 10 mA. No active current limiting is used so the actual available current may be higher.
22. Push-pull structure with tri-state condition ($\overline{CS}$ HIGH).
23. Output pin only. Supply from VDD. Structure switch to ground with pull-up current source.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT PIN ($\overline{\text{WDOG}}$)[24]					
Low-level Output Voltage I_O = 1.5 mA, 1.0 V < V_{SUP} < 27 V	V_{OL}	0.0	—	0.9	V
High-level Output Voltage I_O = -250 µA	V_{OH}	V_{DD}-0.9	—	V_{DD}	V
OUTPUT PIN ($\overline{\text{INT}}$)[24]					
Low-level Output Voltage I_O = 1.5 mA	V_{OL}	0.0	—	0.9	V
High-level Output Voltage I_O = -250 µA	V_{OH}	V_{DD}-0.9	—	V_{DD}	V
OUTPUT PIN (HS)					
Driver Output ON Resistance T_A = 25 °C, I_{OUT} - 150 mA, V_{SUP} > 9.0 V T_A = 125 °C, I_{OUT} - 150 mA, V_{SUP} > 9.0 V T_A = 125 °C, I_{OUT} - 120 mA, 5.5 V < V_{SUP} < 9.0 V	$R_{DS(ON)}$	— — —	2.0 — 3.5	2.5 4.5 5.5	Ω
Output Current Limitation V_{SUP} - V_{HS} > 1.0 V	I_{LIM}	160	—	500	mA
HS Thermal Shutdown	T_{SD}	155	—	190	°C
HS Leakage Current	I_{LEAK}	—	—	10	µA
Output Clamp Voltage I_{OUT} = -10 mA, No Inductive Load Drive Capability	V_{CL}	-1.5	—	-0.3	V
INPUT PINS (L0, L1, L2, AND L3)					
Low-voltage Detection Threshold 5.5 V < V_{SUP} < 6.0 V 6.0 V < V_{SUP} < 18 V 18 V < V_{SUP} < 27 V	V_{THL}	2.0 2.5 2.7	2.5 3.0 3.2	3.0 3.6 3.7	V
High-voltage Detection Threshold 5.5 V < V_{SUP} < 6.0 V 6.0 V < V_{SUP} < 18 V 18 V < V_{SUP} < 27 V	V_{THH}	2.7 3.0 3.5	3.3 4.0 4.2	3.8 4.6 4.7	V
Hysteresis 5.5 V < V_{SUP} < 27 V	V_{HYS}	0.6	—	1.3	V
Input Current -0.2 V < V_{IN} < 40 V	I_{IN}	-10	—	10	µA

Notes
24. Push-pull structure.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CAN TRANSCEIVER CURRENT					
Supply Current of CAN Module					
CAN in Normal mode, Bus Recessive State	I_{RES}	—	1.3	3.0	mA
CAN in Normal mode, Bus Dominant State without Bus Load	I_{DOM}	—	1.5	3.5	mA
CAN in Sleep State, Wake-up Enabled, V2 Regulator OFF	$I_{CAN-SLEEP}$	—	12	24	µA
CAN in Sleep State, Wake-up Disabled, V2 Regulator OFF[25]	I_{DIS}	—	—	1.0	µA
PINS (CANH AND CANL)					
Bus Pin Common Mode Voltage	V_{CM}	-27	—	40	V
Differential Input Voltage (Common Mode Between -3.0 V and 7.0 V)	V_{CANH} - V_{CANL}				mV
Recessive State at RXD		—	—	500	
Dominant State at RXD		900	—	—	
Differential Input Hysteresis (RXD)	V_{HYS}	100	—	—	mV
Input Resistance	R_{IN}				kΩ
28-pin SOIC		5.0	—	100	
48-pin QFN		5.0	—	50	
Differential Input Resistance	R_{IND}	10	—	100	kΩ
CANH Output Voltage	V_{CANH}				V
TXD Dominant State		2.75	—	4.5	
TXD Recessive State		—	—	3.0	
CANL Output Voltage	V_{CANL}				V
TXD Dominant State		0.5	—	2.25	
TXD Recessive State		2.0	—	—	
Differential Output Voltage	Vo_H-Vo_L				
TXD Dominant State		1.5	—	3.0	V
TXD Recessive State		—	—	100	mV
Output Current Capability (Dominant State)					mA
CANH	I_{CANH}	—	—	-35	
CANL	I_{CANL}	35	—	—	
Over-temperature Shutdown	T_{SD}	160	180	—	°C
CANL Over-current Detection[26]					mA
CANL	$I_{CANL/OC}$	60	—	200	
CANH	$I_{CANH/OC}$	-200	—	-60	
CANH and CANL Input Current, Device Supplied (CAN Sleep mode with CAN Wake-up Enabled or Disabled)	I_{CAN1}				µA
V_{CANH}, V_{CANL} from 0 V to 5.0 V		—	3.0	10	
V_{CANH}, V_{CANL} = -2.0 V		-60	-50	—	
V_{CANH}, V_{CANL} = 7.0 V		—	60	75	

Notes
25. Guaranteed by design; it is not production tested.
26. Reported in CAN register. For a description of the contents of the CAN register, refer to CAN Register (CAN) on page 49

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
PINS (CANH AND CANL) (CONTINUED)					
CANH and CANL Input Current, Device Unsupplied	I_{CAN2}				μA
V_{CANH}, V_{CANL} = 2.5 V		—	40	100	
V_{CANH}, V_{CANL} = -2.0 V		-60	-50	—	
V_{CANH}, V_{CANL} = 7.0 V		—	190	240	
DIAGNOSTIC INFORMATION (CANH AND CANL)					
CANL to GND Threshold	V_{LG}	—	1.75	—	V
CANH to GND Threshold	V_{HG}	—	1.75	—	V
CANL to VSUP Threshold	V_{LVB}	—	V_{SUP} - 2.0	—	V
CANH to VSUP Threshold	V_{HVB}	—	V_{SUP} - 2.0	—	V
CANL to VDD Threshold	V_{L5}	—	V_{DD} - 0.43	—	V
CANH to VDD Threshold	V_{H5}	—	V_{DD} - 0.43	—	V
RXD Weak Pull-down Current Source[27]	I_{RXDW}				μA
RXD Permanent Dominant Failure Condition		—	100	—	
PINS (TXD AND RXD)					
TXD Input High-voltage	V_{IH}	0.7 V_{DD}	—	V_{DD} + 0.4	V
TXD Input Low-voltage	V_{IL}	-0.4	—	0.3 V_{DD}	V
TXD High-level Input Current	I_{IH}				μA
V_{TXD} = V_2		-10	—	10	
TXD Low-level Input Current	I_{IL}				μA
V_{TXD} = 0 V		-150	-100	-50	
RXD Output High Voltage[28]	V_{OH}				V
I_{RXD} = 250 μA		V_{DD} - 1.0	—	—	
RXD Output Low-voltage	V_{OL}				V
I_{RXD} = 1.0 mA		—	—	0.5	

Notes
27. Guaranteed by design; it is not production tested.
28. RXD is a push-pull structure between the V2 pin and GND.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 6. Dynamic Electrical Characteristics

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE TIMING (SCLK, $\overline{CS}$, MOSI, MISO)[29]					
SPI Operation Frequency	f_{REQ}	0.25	—	4.0	MHz
SCLK Clock Period	t_{PCLK}	250	—	N/A	ns
SCLK Clock High Time	t_{WSCLKH}	125	—	N/A	ns
SCLK Clock Low Time	t_{WSCLKL}	125	—	N/A	ns
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK	t_{LEAD}	100	—	N/A	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$	t_{LAG}	100	—	N/A	ns
MOSI to Falling Edge of SCLK	t_{SISU}	40	—	N/A	ns
Falling Edge of SCLK to MOSI	t_{SIH}	40	—	N/A	ns
MISO Rise Time[30] C_L = 220 pF	t_{RSO}	—	25	50	ns
MISO Fall Time[30] C_L = 220 pF	t_{FSO}	—	25	50	ns
Time from Falling or Rising Edges of $\overline{CS}$ MISO Low-impedance MISO High-impedance	 t_{SOEN} t_{SODIS}	 — —	 — —	 50 50	ns
Time from Rising Edge of SCLK to MISO Data Valid 0.2 V_{DD} ≤ MISO ≥ 0.8 V_{DD}, C_L = 200 pF	t_{VALID}	—	—	50	ns
STATE MACHINE TIMING ($\overline{CS}$, SCLK, MOSI, MISO, $\overline{WDOG}$, $\overline{INT}$)					
Delay Between $\overline{CS}$ LOW-to-HIGH Transition (at End of SPI Stop Command) and Stop mode Activation[31]	$t_{\overline{CS}\text{-STOP}}$	18	—	34	µs
Interrupt Low-level Duration Stop Mode	$t_{\overline{INT}}$	7.0	10	13	µs
Internal Oscillator Frequency[32]	f_{OSC}	—	100	—	kHz

Notes
29. See Figure 7, SPI Timing Diagram, page 20.
30. Not production tested. Guaranteed by design.
31. Not production tested. Guaranteed by design. Detected by V2 OFF.
32. f_{OSC} is indirectly measured (1.0 ms reset) and trimmed.

Table 6. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
STATE MACHINE TIMING ($\overline{CS}$, SCLK, MOSI, MISO, $\overline{WDOG}$, $\overline{INT}$) (CONTINUED)					
Watchdog Period Normal and Standby Modes	$t_{\overline{WDOG}}$				ms
28-pin SOIC					
Period 1		8.58	9.75	10.92	
Period 2		39.6	45	50.4	
Period 3		88	100	112	
Period 4		308	350	392	
48-pin QFN					
Period 1		8.3	9.75	10.92	
Period 2		38.5	45	50.4	
Period 3		86	100	112	
Period 4		300	350	392	
Normal Request Mode Timeout	t_{NRTOUT}				ms
28-pin SOIC		308	350	392	
48-pin QFN		300	350	392	
Watchdog Period Stop Mode	$t_{WD-STOP}$				ms
Period 1		6.82	9.75	12.7	
Period 2		31.5	45	58.5	
Period 3		70	100	130	
Period 4		245	350	455	
Watchdog Period Accuracy	t_{ACC}				%
Normal and Standby Modes		-12	—	12	
Stop Mode		-30	—	30	
Cyclic Sense/FWU Timing Sleep and Stop Modes	t_{CSFWU}				ms
Timing 1		3.22	4.6	5.98	
Timing 2		6.47	9.25	12	
Timing 3		12.9	18.5	24	
Timing 4		25.9	37	48.1	
Timing 5		51.8	74	96.2	
Timing 6		66.8	95.5	124	
Timing 7		134	191	248	
Timing 8		271	388	504	
Cyclic Sense ON Time	t_{ON}				µs
Sleep and Stop modes.		200	350	500	
Cyclic Sense/FWU Timing Accuracy	t_{ACC}				%
Sleep and Stop modes		-30	—	30	

Table 6. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
STATE MACHINE TIMING ($\overline{CS}$, SCLK, MOSI, MISO, $\overline{WDOG}$, $\overline{INT}$) (CONTINUED)					
Delay Between SPI Command and HS Turn ON[33] Normal or Standby mode, V_{SUP} > 9.0 V	t_{S-HSON}	—	—	22	µs
Delay Between SPI Command and HS Turn OFF[33] Normal or Standby mode, V_{SUP} > 9.0 V	$t_{S-HSOFF}$	—	—	22	µs
Delay Between SPI and V2 Turn ON[33] Standby mode	t_{S-V2ON}	9.0	—	22	µs
Delay Between SPI and V2 Turn OFF[33] Normal mode	$t_{S-V2OFF}$	9.0	—	22	µs
Delay Between Normal Request and Normal mode After Watchdog Trigger Command[33] Normal Request mode	t_{S-NR2N}	15	35	70	µs
STATE MACHINE TIMING ($\overline{CS}$, SCLK, MOSI, MISO, $\overline{WDOG}$, $\overline{INT}$) (CONTINUED)					
Delay Between SPI and CAN Normal mode[34] Normal mode[35]	t_{S-CAN_N}	—	—	10	µs
Delay Between SPI and CAN Sleep Mode[34] Normal mode [35]	t_{S-CAN_S}	—	—	10	µs
Delay Between $\overline{CS}$ Wake-up ($\overline{CS}$ LOW to HIGH) and Device in Normal Request mode (VDD ON and $\overline{RST}$ HIGH) Stop mode	$t_{W-\overline{CS}}$	15	40	90	µs
Delay Between $\overline{CS}$ Wake-up ($\overline{CS}$ LOW to HIGH) and First Accepted SPI Command Device in Stop mode After Wake-up	t_{W-SPI}	90	—	N/A	µs
Delay Between $\overline{INT}$ Pulse and First SPI Command Accepted Device in Stop mode After Wake-up	$t_{S-1STSPI}$	20	—	N/A	µs
Delay Between Two SPI Messages Addressing the Same Register	t_{2SPI}	25	—	—	µs
OUTPUT PIN (VDD)					
Reset Delay Time Measured at 50% of Reset Signal	t_D	4.0	—	30	µs
I_{DD} Over-current to Wake-up Deglitcher Time[35]	$t_{IDD-DGLT}$	40	55	75	µs

Notes
33. Delay starts at falling edge of clock cycle #8 of the SPI command and start of “Turn ON” or “Turn OFF” of HS or V2.
34. Delay starts at falling edge of clock cycle #8 of the SPI command and start of “Turn ON” or “Turn OFF” of HS or V2.
35. Guaranteed by design; it is not production tested.

Table 6. Dynamic Electrical Characteristics (continued)

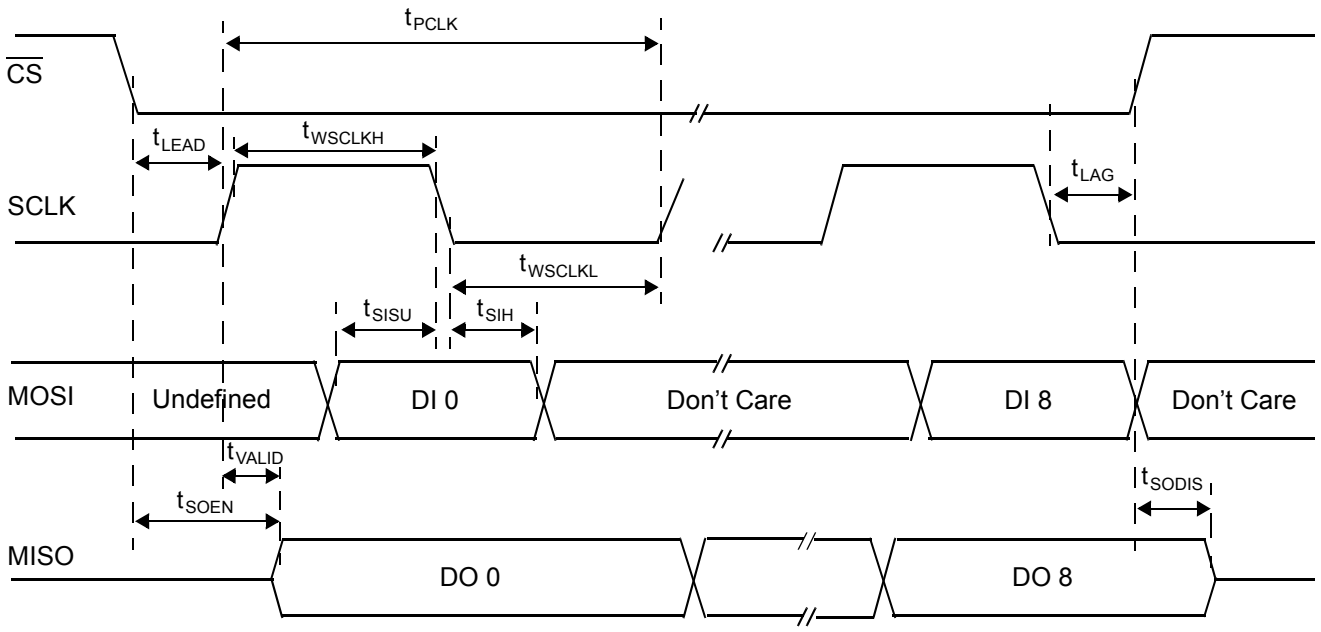
Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT PIN ($\overline{RST}$)					
Reset Duration After VDD HIGH					ms
33742	$t_{\overline{RST}DUR}$	12	15	18	
33742S	$t_{\overline{RST}DURS}$	3.0	3.5	4.0	
INPUT PINS (L0, L1, L2, AND L3)					
Wake-up Filter Time	t_{WUF}	8.0	20	38	µs
CAN MODULE–SIGNAL EDGE RISE AND FALL TIMES (CANH, CANL)					
Dominant State Timeout	t_{DOUT}	200	360	520	µs
Propagation Loop Delay TXD to RXD (Recessive to Dominant)(36)	t_{LRD}				ns
Slew Rate 3		60	100	210	
Slew Rate 2		70	110	225	
Slew Rate 1		80	130	255	
Slew Rate 0		110	200	310	
Propagation Delay TXD to CAN (Recessive to Dominant)(37)	t_{TRD}				ns
Slew Rate 3		20	65	110	
Slew Rate 2		25	80	150	
Slew Rate 1		35	100	200	
Slew Rate 0		50	160	300	
Propagation Delay CAN to RXD (Recessive to Dominant)(38)	t_{RRD}	10	50	140	ns
Propagation Loop Delay TXD to RXD (Dominant to Recessive)(36)	t_{LDR}				ns
Slew Rate 3		100	150	200	
Slew Rate 2		120	165	220	
Slew Rate 1		140	200	250	
Slew Rate 0		250	340	410	
Propagation Delay TXD to CAN (Dominant to Recessive)(37)	t_{TDR}				ns
Slew Rate 3		60	125	150	
Slew Rate 2		65	150	190	
Slew Rate 1		75	180	250	
Slew Rate 0		200	310	460	
Propagation Delay CAN to RXD (Dominant to Recessive)(38)	t_{RDR}	20	30	60	ns
Non-Differential Slew Rate (CANL or CANH)					V/µs
Slew Rate 3	t_{SL3}	4.0	19	40	
Slew Rate 2	t_{SL2}	3.0	13.5	20	
Slew Rate 1	t_{SL1}	2.0	8.0	15	
Slew Rate 0	t_{SL0}	1.0	5.0	10	
Bus Communication Rate	t_{BUS}	60k	—	1.0M	bps

Notes

36. See Figure 8, page 20.
37. See Figure 9, page 20.
38. See Figure 10, page 21.

TIMING DIAGRAMS



Note Incoming data at MOSI pin is sampled by the 33742 at SCLK falling edge. Outgoing data at MISO pin is set by the 33742 at SCLK rising edge (after t_{VALID} delay time).

Figure 7. SPI Timing Diagram

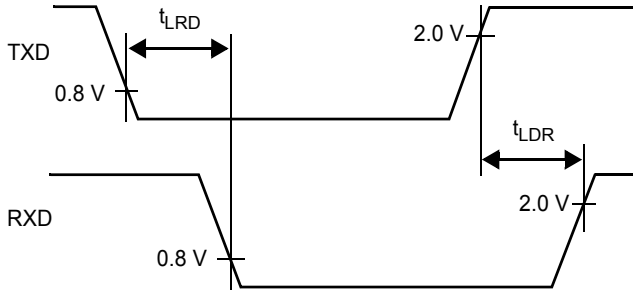
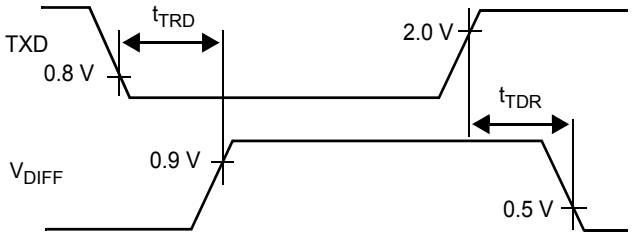


Figure 8. Propagation Loop Delay TXD to RXD



$V_{DIFF} = V_{CANH} - V_{CANL}$

Figure 9. Propagation Delay TXD to CAN

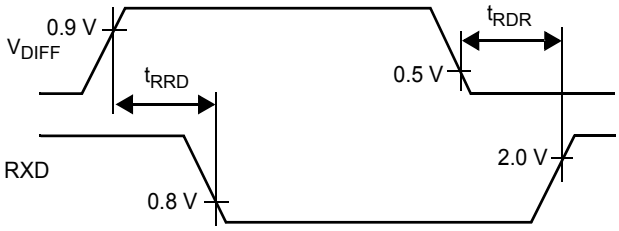


Figure 10. Propagation Delay CAN to RXD

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33742 and the 33742S are system basis chips (SBCs) dedicated to automotive applications. Their functions include the following:

- One fully protected 5.0 V voltage regulator with 200 mA total output current capability available at the VDD pin.
- VDD regulator under-voltage reset function, programmable window or time-out software watchdog function.
- Internal driver (V2) for an external series pass transistor to implement a second 5.0 V voltage regulator.
- Two running modes: Normal and Standby modes set by the system microcontroller.
- Sleep and Stop modes low power operating modes to reduce an application's current consumption while providing a wake-up capability from the CAN interface, L3:L0 wake-up inputs, or from a timer wake-up.
- Programmable wake-up input and cyclic sense wake-ups.
- CAN high-speed physical bus interface with TXD and RXD fault diagnostic capability and enhanced protection features.
- An SPI interface for use in communicating with a MCU and Interrupt outputs to report SBC status, perform diagnostics, and report wake-up events.

FUNCTIONAL PIN DESCRIPTION

RECEIVE AND TRANSMIT DATA (RXD AND TXD)

The RXD and TXD pins (receive data and transmit data pins, respectively) are connected to a microcontroller's CAN protocol handler. TXD is an input and controls the CANH and CANL line state (dominant when TXD is LOW, recessive when TXD is HIGH). RXD is an output and reports the bus state (RXD LOW when CAN bus is dominant, HIGH when CAN bus is recessive). The RXD terminal is a push-pull structure between the V2 pin and GND.

Voltage Digital Drain (VDD)

The VDD pin is the output pin of the 5.0 V internal regulator. It can deliver up to 200 mA. This output is protected against over-current and over-temperature. It includes an over-temperature pre-warning flag, which is set when the internal regulator temperature exceeds 130 °C typical. When the temperature exceeds the over-temperature shutdown (170 °C typical), the regulator is turned off.

VDD includes an under-voltage reset circuitry, which sets the $\overline{\text{RST}}$ pin LOW when VDD is below the under-voltage reset threshold.

RESET OUTPUT ($\overline{\text{RST}}$)

The RESET pin $\overline{\text{RST}}$, is an output that is set LOW when the device is in reset mode. The $\overline{\text{RST}}$ pin is set HIGH when the device is not in reset mode. $\overline{\text{RST}}$ includes an internal pull-up current source. When $\overline{\text{RST}}$ is LOW, the sink current capability is limited, allowing $\overline{\text{RST}}$ to be shorted to 5.0 V for software debug or software download purposes.

INTERRUPT OUTPUT ($\overline{\text{INT}}$)

The Interrupt pin $\overline{\text{INT}}$, is an output that is set LOW when an interrupt occurs. $\overline{\text{INT}}$ is enabled using the Interrupt Register (INTR). When an interrupt occurs, $\overline{\text{INT}}$ stays LOW until the interrupt source is cleared.

$\overline{\text{INT}}$ output also reports a wake-up event by a 10 μs typical pulse when the device is in Stop mode.

VOLTAGE SOURCE 2 (V2)

The V2 pin is the input sense for the V2 regulator. It is connected to the external series pass transistor. V2 is also the 5.0 V supply of the internal CAN interface. It is possible to connect V2 to an external 5.0 V regulator or to the VDD output when no external series pass transistor is used. In this case, the V2CTRL pin must be left open. Refer to Figure 31, SBC Typical Application Schematic, page 57.

VOLTAGE SOURCE 2 CONTROL (V2CTRL)

The V2CTRL pin is the output drive pin for the V2 regulator connected to the external series pass transistor.

VOLTAGE SUPPLY (VSUP)

The VSUP pin is the battery supply input of the device.

HIGH SIDE OUTPUT (HS)

The HS pin is the internal high side driver output. It is internally protected against over-current and over-temperature.

LEVEL 0-3 INPUTS (L0: L3)

The L0:L3 pins can be connected to contact switches or the output of other ICs for external inputs. The input states can be read by SPI. These inputs can be used as wake-up events for the SBC when operating in the Sleep or Stop mode.

CAN HIGH AND CAN LOW OUTPUTS (CANH AND CANL)

The CAN High and CAN Low pins are the interfaces to the CAN bus lines. They are controlled by TXD input level, and the state of CANH and CANL is reported through RXD output. A 60Ω termination resistor is connected between CANH and CANL pins.

SERIAL DATA CLOCK (SCLK)

SCLK is the Serial Data Clock input pin of the serial peripheral interface.

MASTER IN SLAVE OUT (MISO)

MISO is the Master In Slave Out pin of the serial peripheral interface. Data is sent from the SBC to the microcontroller through the MISO pin.

MASTER OUT SLAVE IN (MOSI)

MOSI is the Master Out Slave In pin of the serial peripheral interface. Control data from a microcontroller is received through this pin.

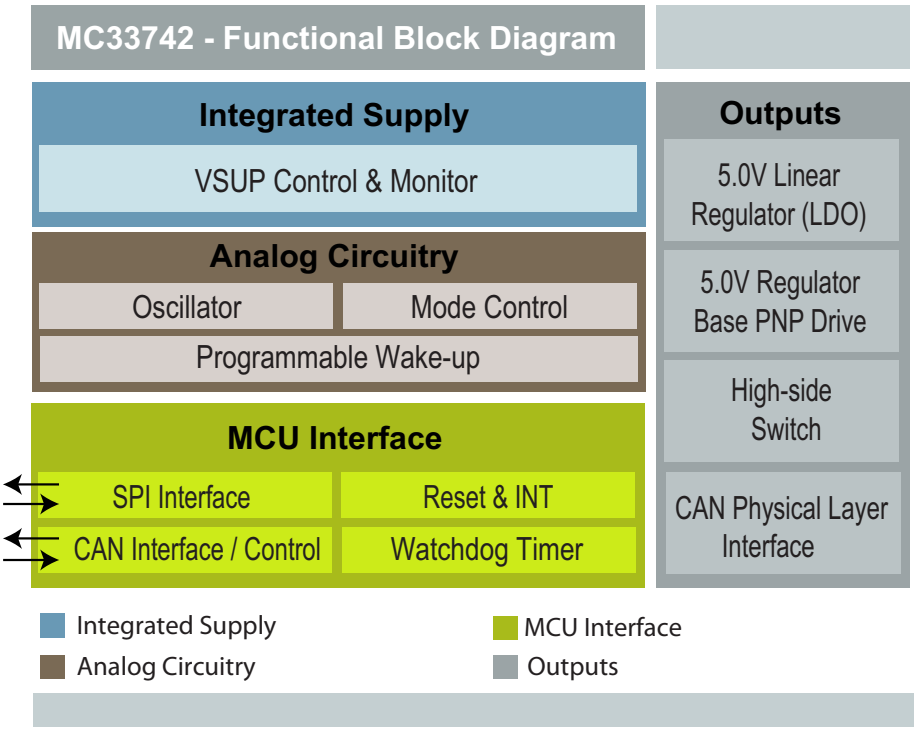
CHIP SELECT ($\overline{\text{CS}}$)

$\overline{\text{CS}}$ is the Chip Select pin of the serial peripheral interface. When this pin is LOW, the SPI port of the device is selected.

WATCHDOG OUTPUT ($\overline{\text{WDOG}}$)

The Watchdog output pin is asserted LOW to flag that the software watchdog has not been properly triggered.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION



OUTPUTS

5.0 V LINEAR REGULATOR (LDO)

This low dropout linear regulator (V1) outputs a regulated 5.0 V at 200 mA. The associated monitoring circuit provides detection of under-voltage, over-current, and short-circuit conditions, as well as over-temperature and a reset function.

5.0 V REGULATOR BASE PNP DRIVE

The V2 linear regulator control circuitry provides drive for an external series pass transistor (PNP type). The 5.0 V output tracks the V1 regulator

HIGH SIDE SWITCH

The high switch provides a 2.0 ohm (typ.) RDS_{ON} MOSFET driver connected to the VSUP pin. The output is protected against short-circuit conditions and provides over-temperature shutdown.

CAN PHYSICAL LAYER INTERFACE

This circuitry provides communication between the TXD & RXD pins, from/to the MCU, and the CANL & CANH pins of the CAN physical interface. The various modes of the CAN interface are controlled through the SPI control registers.

INTEGRATED SUPPLY

VSUP CONTROL & MONITOR

This circuitry protects the IC from transient conditions such as vehicle jump-start (27 V) and load dump (40 V). If the V_{SUP} voltage falls below 3.0 V (or a 6.0 V warning interrupt), an under-voltage detection is reported.

ANALOG CIRCUITRY

OSCILLATOR

This circuit is used to generate the internal timings for reset, watchdog, cyclic wake-up, filtering time, etc.

MODE CONTROL

The 4 operating modes of the IC are controlled through the SPI control registers. There are also several special modes possible.

PROGRAMMABLE WAKE-UP

The 4 inputs are used in conjunction with various SPI control register bits to determine the wake-up conditions and the reaction of the IC. They can be connected to contact switches or other ICs.

MCU INTERFACE

SPI INTERFACE

The IC and the MCU communicate using the SPI control and status reporting registers. The clock speed (SCLK) can be as high as 4.0 MHz.

RESET & INT

These 2 outputs notify the MCU when the IC is in reset mode, or when an enabled interrupt condition has occurred.

WATCHDOG TIMER

The timer can be used as a watchdog window or watchdog timeout function. The SPI control register provide the choice as well as the timeout value. When the watchdog timer is not properly serviced by the MCU, an error signal (WDOGN low) and a reset signal (RSTN low) are output.

CAN INTERFACE/CONTROL

The operation of the CAN interface is controlled by the MCU through the use of SPI control register bits.