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Two cylinder small engine control IC

33814

TWO CYLINDER SMALL ENGINE CONTROL IC

98ASA00737D
AE SUFFIX (PB-FREE)
48-PIN LQFP-EP

Powered by SMARTMOS technology, the 33814 delivers a cost-optimized IC solution for managing one and two-cylinder engines. With six drivers, three pre-drivers, a 5.0 V regulator for the MCU, a protected external sensor supply, and a high level of integration, the IC offers an ideal response to contemporary market requirements. The innovative VRS system optimizes noise immunity under cranking conditions. Diagnostic and protection features present on all outputs allow applications to operate with greater safety.

Features:

- Operates over supply voltage range of 4.5 V < V_{PWR} < 36 V
- Start-up/shut-down control and power sequence logic with KEYSW input
- MCU supply: V_{CC} is a 5.0 V (±2.0%, 200 mA) regulated supply
- Sensor supply: V_{PROT} (100 mA) is a V_{CC} tracking protected sensor supply
- Three configurable pre-drivers for IGBT or general purpose gate MOSFETs for ignition and O_2 sensor (HEGO) heater:
  - PWM
  - Overcurrent shutdown
  - Short-to-battery shutdown
- Six low-side drivers with full diagnostics, self-protection and PWM control:
  - Two fuel injector drivers, $R_{DS(on)}$ = 0.6 Ω, I_{LIMIT} = 1.8 A, to drive typical 12 Ω high-impedance injectors
  - Relay 1 driver, $R_{DS(on)}$ = 0.4 Ω, I_{LIMIT} = 3.0 A, to drive fuel pump
  - Relay 2 driver, $R_{DS(on)}$ = 1.5 Ω, I_{LIMIT} = 1.2 A, to drive power relay
  - Lamp driver, $R_{DS(on)}$ = 1.5 Ω, I_{LIMIT} = 1.2 A, to drive warning lamp or an LED
  - Programmable Tachometer Driver, $R_{DS(on)}$ = 20 Ω, $I_{shutdown}$ = 60 mA, to drive a Tachometer display
- Innovative configurable VRS conditioning circuit, with two different parameter settings for engine cranking and running mode and an optional automatic mode to improve noise immunity in cranking conditions
- K-line (ISO9141)
- MCU reset generator and programmable watchdog
- MCU Interface: 16-bit SPI and parallel interface with 5.0 V IO capability

Applications:

Small Engine Control for:

- Motor scooters
- Small motorcycles
- Lawn mowers
- Lawn trimmers
- Snow blowers
- Chain saws
- Gasoline-driven electrical generators
- Outboard motors

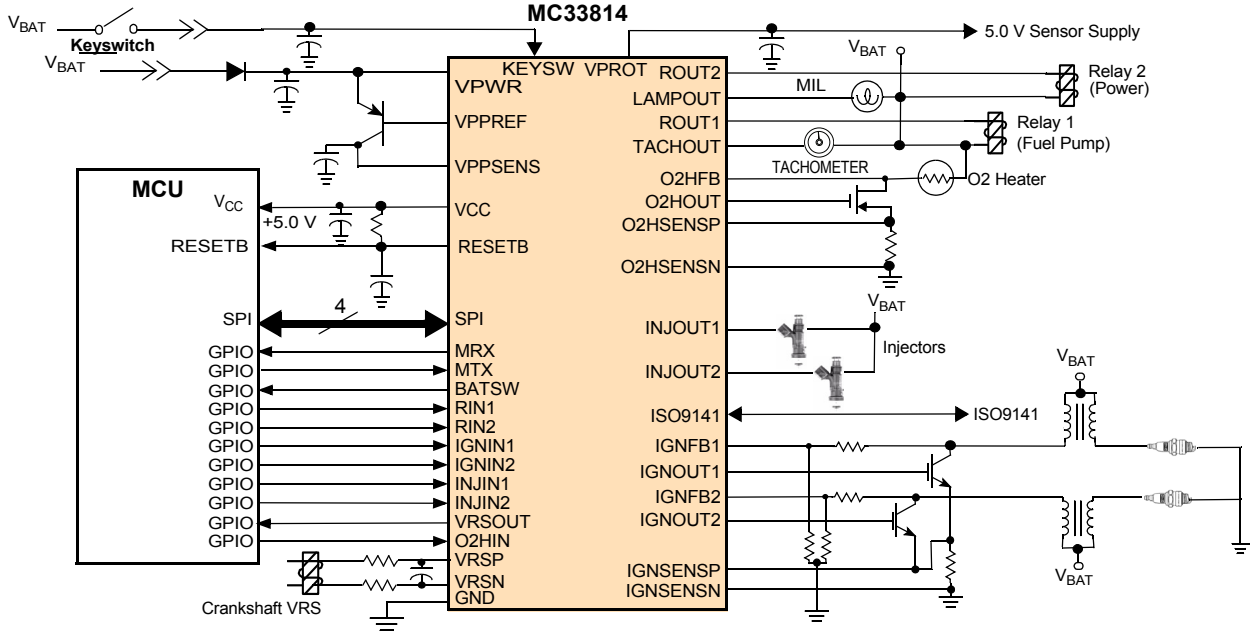

Figure 1. 33814 simplified application diagram

Table of Contents

1 Orderable parts

Table 1. Orderable part variations

Part Number [1]	Temperature (T_A)	Package
MC33814AE	-40 °C to 125 °C	48 LQFP-EP

Notes

1. To order parts in Tape and Reel, add the R2 suffix to the part number.

2 Internal block diagram

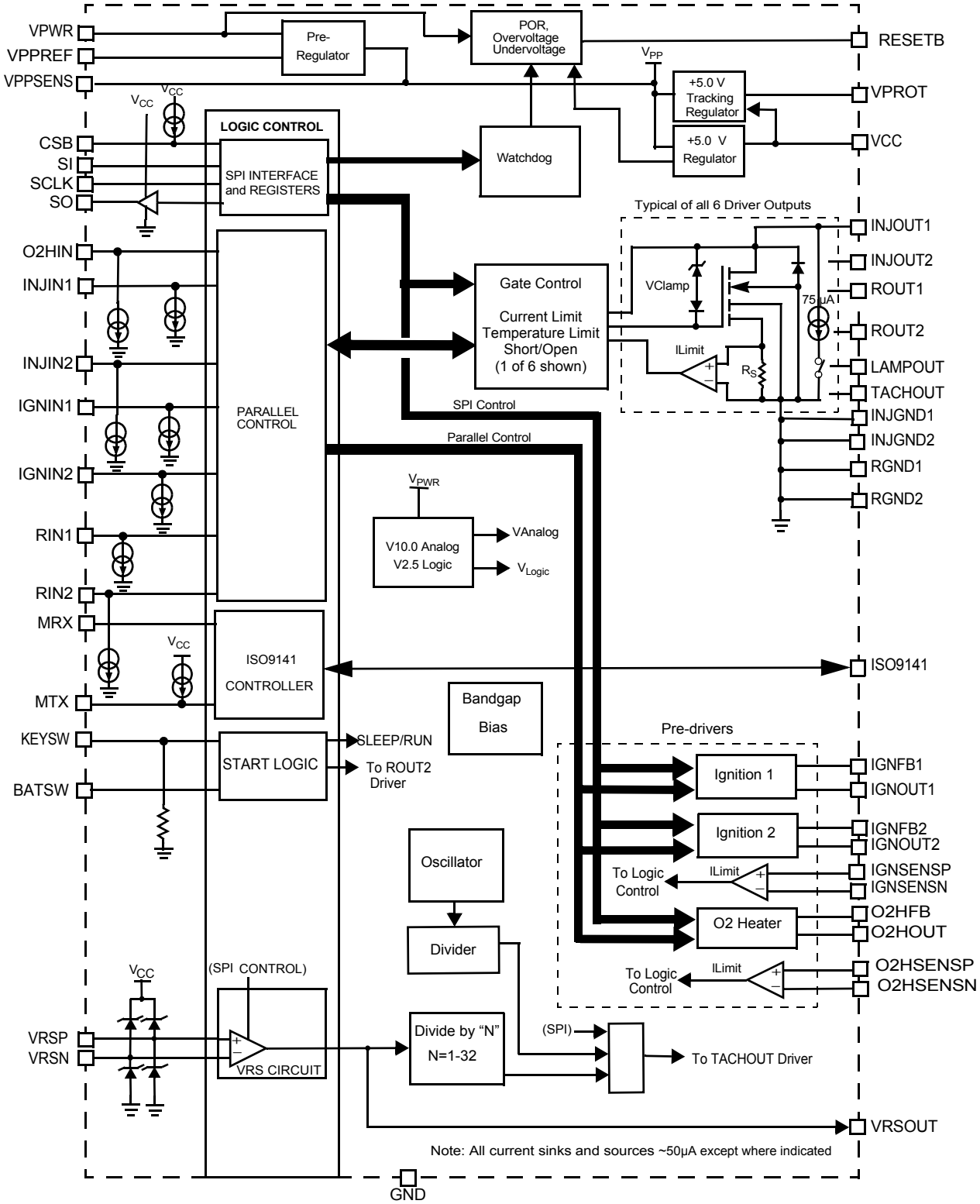

Figure 2. Simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

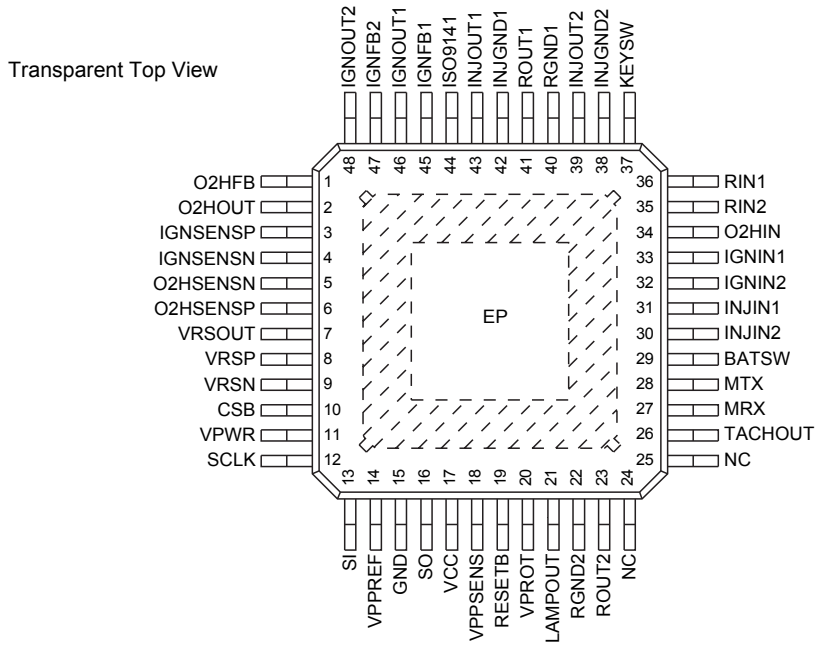

Figure 3. 33814 Pin connections

3.2 Pin definitions

Table 2. 33814 pin definitions

Pin	Pin Name	Pin Function	Formal Name	Description
1	O2HFB	Input	O2 Sensor Heater Feedback Input	Voltage feedback from drain of O2 Sensor Heater driver FET. If used as IGBT driver, voltage feedback from collector of IGBT through 10:1 voltage divider (9R:1R).
2	O2HOUT	Output	O2 Sensor Heater Output	Pre-driver output for O2 Sensor Heater driven by SPI input or O2HIN pin
3	IGNSENSP	Input	Ignition Current Sense Input Positive	Positive input to the ignition current sense differential amplifier. Measures current in IGBT emitter resistor (or MOSFET source resistor) for IGNOUT1 and IGNOUT2, if used
4	IGNSENSN	Input	Ignition Current Sense Input Negative	Negative input to the ignition current sense differential amplifier. Measures current in IGBT emitter resistor (or MOSFET source resistor) for IGNOUT1 and IGNOUT2, if used
5	O2HSENSN	Input	O2 Heater Current Sense Input Negative	Negative input to the O2 heater current sense differential amplifier. Measures current in of O2 heater driver MOSFET source resistor (or IGBT emitter resistor), if used
6	O2HSENSP	Input	O2 Heater Current Sense Input Positive	Positive input to the O2 heater current sense differential amplifier. Measures current in of O2 heater driver MOSFET source resistor (or MOSFET source resistor) for IGNOUT1 and IGNOUT2, if used
7	VRSOUT	Output	VRS Conditioned Output	5.0 V Logic Level Output from conditioned VRS differential inputs VRSP, VRSN

Table 2. 33814 pin definitions

Pin	Pin Name	Pin Function	Formal Name	Description
8	VRSP	Input	Variable Reluctance Sensor Positive Input	The VRSP and VRSN form a differential input for the Variable Reluctance Sensor attached to the crankshaft toothed wheel.
9	VRSN	Input	Variable Reluctance Sensor Negative Input	The VRSP and VRSN form a differential input for the Variable Reluctance Sensor attached to the crankshaft toothed wheel.
10	CSB	Input	SPI Chip Select	The Chip Select input pin is an active low signal sent by the MCU to indicate that the device is being addressed.
11	VPWR	Supply Input	Main Voltage Supply Input	VPWR is the main voltage supply input for the device. Should be connected to a 12 Volt battery with reverse battery protection and adequate transient protection.
12	SCLK	Input	SPI Clock Input	The SCLK input pin is used to clock in and out the serial data on the SI and SO pins while being addressed by the CSB.
13	SI	Input	SPI Data Input	The SI input pin is used to receive serial data into the device from the MCU.
14	VPPREF	Output	VPP Reference Base Drive	Base drive for external PNP pass transistor
15	GND	Ground	Ground	Ground pin, return for all voltage supplies
16	SO	Output	SPI Data Output	The SO output pin is used to transmit serial data from the device to the MCU.
17	VCC	Supply	VCC Supply Protected Output	5.0 Volt supply output for MCU V_{CC}. This output supplies the V_{CC} voltage for 5.0 Volt MCUs. It is short-circuit and overcurrent protected.
18	VPPSENS	Input	Voltage Sense from VPP	Feedback to internal V_{PP} 6.5 Volt regulator from external pass transistor
19	RESETB	Output	RESETB Output to MCU	5.0 V Logic level reset signal used to reset the MCU during under and overvoltage conditions and for initial power-up, down and watchdog timeouts
20	VPROT	Output	Sensor Supply Protected Output	The VPROT Output is a protected 5.0 Volt output that tracks the V_{CC} voltage but isolates the VCC output against shorts to ground and to battery. It is intended to supply sensors which are located off of the ECU board.
21	LAMPOUT	Output	Warning Lamp Output	Low-side driver output for MIL (warning lamp) driven by SPI input command
22	RGND2	Ground	ROUT2 Power Ground	Ground connection for ROUT 2 low-side driver. Must be tied to VPWR Ground.
23	ROUT2	Output	Relay Driver 2 Output	Low-side relay driver output # 2 driven by SPI input command or RIN2 logic input
24, 25	N.C.	No Connect	Unused pin	
26	TACHOUT	Output	Tachometer output	This pin provides the low-side drive for a tachometer gauge or alternatively as a SPI controlled low-side driver, or oscillator output.
27	MRX	Output	Low-side Driver Output	Output 5.0 V logic level ISO9141 data to the MCU from the ISO9141 IN/OUT pin
28	MTX	Input	ISO9141 MCU Data Input	Input 5.0 V logic level ISO9141 data from the MCU to the ISO9141 IN/OUT pin
29	BATSW	Output	Battery Switch	This output is a 5.0 V logic level that is high when KEYSW is high. It is only low when KEYSW is low. It can also be controlled via the SPI.
30	INJIN2	Input	Injector Driver Input 2	5.0 V logic level input from the MCU to control the injector 2 driver output. (Can also be controlled via the SPI)
31	INJIN1	Input	Injector Driver Input 1	5.0 V logic level input from the MCU to control the injector 1 driver output. (Can also be controlled via the SPI)
32	IGNIN2	Input	Ignition Input 2	5.0 V logic level input from MCU controlling the ignition coil # 2 current flow and spark. (Can also be controlled via the SPI)
33	IGNIN1	Input	Ignition Input 1	5.0 V logic level input from MCU controlling the ignition coil # 1 current flow and spark. (Can also be controlled via the SPI)
34	O2HIN	Input	O2 Sensor Heater Input	5.0 V logic level input used to turn on and off the O2HOUT driver. The O2HOUT driver can also be turned on and off via the SPI if this pin is not present in a different package.
35	RIN2	Input	Relay Driver Input 2	5.0 V logic level input from the MCU to control the relay 2 driver output ROUT2. The ROUT2 driver can also be turned on and off via the SPI if this pin is not present in a different package.

Table 2. 33814 pin definitions

Pin	Pin Name	Pin Function	Formal Name	Description
36	RIN1	Input	Relay Driver Input 1	5.0 V logic level input from the MCU to control the relay 1 driver output ROUT1. The ROUT1 driver can also be turned on and off via the SPI if this pin is not present in a different package.
37	KEYSW	Input	Key Switch Input	The Key Switch Input is a V_{PWR} level signal that indicates that the Key is inserted and turned to the ON/OFF position. In the ON position the (KEYSW = V_{BAT}) the IC is enabled and BATSW = HIGH (Relay 2 ON if programmed in the SPI). In the OFF position the IC is in Sleep mode, only when the PWREN bit in the SPI register is also low.
38	INJGND2	Ground	Injector Driver 2 Ground	Ground connection for injector 2 low-side driver. Must be tied to VPWR ground
39	INJOUT2	Output	Injector Driver 2 Output	Low-side driver output for injector 2 driven by the SPI input or by parallel input INJIN2
40	RGND1	Ground	ROUT1 Power Ground	Ground connection for ROUT 1 low-side driver. Must be tied to VPWR ground
41	ROUT1	Output	Relay Driver 1 Output	Low-side relay driver output # 1 driven by the SPI input command or RIN1 logic input
42	INJGND1	Ground	Injector Driver 1 Ground	Ground connection for injector 1 low-side driver. Must be tied to VPWR ground
43	INJOUT1	Output	Injector Driver 1 Output	Low-side driver output for injector 1 driven by the SPI input or by parallel input INJIN1
44	ISO9141	Input/Output	ISO9141 K-Line Bidirectional Serial Data Signal	ISO9141 pin is V_{PWR} level IN/OUT signal which is connected to an external ECU tester that uses the ISO9141 protocol.The output is open drain with an internal 32 kΩ pull-up resistor and the Input is a ratiometric V_{PWR} level threshold comparator.
45	IGNFB1	Input	Feedback from Collector 1	Voltage feedback from collector of ignition # 1 driver IGBT through 10:1 voltage divider (9R:1R)(or voltage feedback from the drain of the FET connected to IGNOUT1, if selected)
46	IGNOUT1	Output	Ignition Output 1	Output to gate of IGBT or GPGD for ignition # 1
47	IGNFB2	Input	Feedback from Collector 2	Voltage feedback from collector of ignition # 2 driver IGBT through 10:1 voltage divider (9R:1R)(or voltage feedback from the drain of the IGNOUT2 FET, if selected)
48	IGNOUT2	Output	Ignition Output 2	Output to gate of IGBT or GPGD for ignition # 2

4 General product characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground, unless mentioned otherwise. Exceeding these ratings may cause malfunction or permanent device damage.

Symbol	Parameter	Min.	Max.	Unit	Notes
ELECTRICAL RATINGS					
V_{PWR}	V_{PWR} Supply Voltage	-0.3	45	V_{DC}	
V_{PP_Ext}	V_{PP} Supply Voltage (If supplied externally and not using internal VPP regulator) • VPP_{REF} • VPP_{SENSE}	 -0.3 -0.3	 45 10	V_{DC}	
V_{CC}	V_{CC} Regulator	-0.3	7.0	V_{DC}	
V_{PROT}	V_{PROT} Regulator	-0.3	V_{PWR}	V_{DC}	
V_{IL}, V_{IH}	SPI Interface and Logic Input Voltage (V_{SI}, V_{SCLK}, V_{CSB}, V_{RIN1}, V_{RIN2}, V_{INJIN1}, V_{INJIN2}, V_{IGNIN1}, V_{IGNIN2}, V_{O2HIN}, V_{MTX})	-0.3	V_{CC}	V_{DC}	
V_{IL}, V_{IH}	SPI Interface and Logic Output Voltage (V_{SO}, V_{BATSW}, V_{MRX},V_{VRSOUT})	-0.3	V_{CC}	V_{DC}	
V_{OUTX}	All Low-side Drivers Drain Voltage ($V_{INJOUT1}$, $V_{INJOUT2}$, V_{ROUT1}, V_{ROUT2}, $V_{LAMPOUT}$, $V_{TACHOUT}$)	-0.3	V_{CLAMP}	V_{DC}	
V_{GDX}	All Pre-drivers Output Voltage ($V_{IGNOUT1}$, $V_{IGNOUT2}$, V_{O2HOUT})	-0.3	10	V_{DC}	
V_{GDFB}	All Pre-driver Feedback Inputs Voltage (V_{IGNFB1}, V_{IGNFB2}, V_{O2HFB})	-1.5	60	V_{DC}	
V_{ISENS}	All Pre-driver Current Sense Inputs Voltage ($V_{IGNSENSN}$, $V_{IGNSENSP}$, $V_{O2HSENSN}$,$V_{O2HSENSP}$)	-0.3	1.0	V_{DC}	
V_{KEYSW}	KEYSW Input Voltage (V_{KEYSW})	-18	V_{PWR}	V_{DC}	
V_{RESETB}	RESETB Output Voltage (V_{RESETB})	-0.3	V_{CC}	V_{DC}	
$V_{ISO9141}$	ISO9141 Input/Output Voltage ($V_{ISO9141}$)	-18	V_{PWR}	V_{DC}	
V_{VRS_IN}	Maximum Voltage for VRSN and VRSP inputs to ground	-0.5	6.0	V_{DC}	
I_{VRSX_IN}	Maximum Current for VRSN and VRSP inputs (internal diodes limit voltage)	-	15	mA	
E_{CLAMP}	Output Clamp Energy (INJOUT1, INJOUT2, ROUT1, ROUT2) • $T_{JUNCTION}$ = 150 °C, I_{OUT} = 1.0 A	-	100	mJ	
E_{CLAMP_LAMP}	Output Clamp Energy (LAMPOUT) • $T_{JUNCTION}$ = 150 °C, I_{OUT} = 0.5 A	-	35	mJ	
V_{ESD1} V_{ESD2} V_{ESD3}	ESD Voltage • Human Body Model (HBM) • Charge Device Model (CDM) (corner pins) • Charge Device Model (CDM)	 - - -	 ±2000 ±750 ±500	V	(2)

Notes

2. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω) and the Charge Device Model.

Table 3. Maximum ratings

All voltages are with respect to ground, unless mentioned otherwise. Exceeding these ratings may cause malfunction or permanent device damage.

Symbol	Parameter	Min.	Max.	Unit	Notes
THERMAL RATINGS					
T_A T_J T_C	Operating Temperature (Automotive grade version) • Ambient • Junction • Case	 -40 -40 -40	 125 150 125	°C	
T_{STG}	Storage Temperature	-55	150	°C	
T_{PPRT}	Peak Package Reflow Temperature During Reflow	-	Note 4	°C	(3), (4)
Thermal Resistance and Package Dissipation Ratings					
$R_{\theta JA}$ $R_{\theta JC}$	Thermal Resistance • Junction-to-Ambient (LQFP-48-EP Package) (Single Layer Board) • Junction-to-Case (LQFP-48-EP Package)	 29 2.4	 29 2.4	°C/W	

Notes

3. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
4. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes), enter the core ID to view all orderable parts and review parametrics.

4.2 Static electrical characteristics

Table 4. Power input static electrical characteristics

Characteristics noted under conditions of 6.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_{CASE} ≤ 125 °C and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 14 V, T_A = 25 °C.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
POWER INPUT (VPWR)						
$V_{PWR(LS)}$ $V_{PWR(FO)}$ $V_{PWR(FP)}$	Supply Voltage (measured at VPWR pin) • Logic Stable Range • Full Operational Range • Full Parameter Specification Range	 2.5 4.5 6.0	 - - -	 45 36 18	V	(5)
$I_{VPWR(ON)}$	Supply Current • All Outputs Disabled (Normal Mode), excludes base current to the external pnp	-	10.0	14.0	mA	
$I_{VPWR(SS)}$	Sleep State Supply Current (Must have PWREN = 0 and KEYSW ≤ 0.8 V for sleep state), • V_{PWR} = 18 V	-	10	20	µA	
$V_{PWR(OV)}$	V_{PWR} Overvoltage Shutdown Threshold Voltage (OV Reset)	37.5	39	42	V	(6)
$V_{PWR(OV-HYS)}$	V_{PWR} Overvoltage Shutdown Hysteresis Voltage	0.5	1.5	3.0	V	
$V_{CC(POR)}$	V_{CC} Power On Reset Voltage Threshold (POR), (rising voltage)	3.9	-	4.9	V	
$V_{CC(UV)}$	V_{CC} Undervoltage Shutdown Threshold Voltage (UV Reset), (falling voltage)	2.9	-	3.9	V	(7)
$V_{CC(UV/POR-HYS)}$	V_{CC} POR and Undervoltage Shutdown Hysteresis Voltage	100	-	-	mV	
$V_{CC,NONOVERLAP}$	V_{CC} POR and Undervoltage Non-overlap (POR-UV)	0.8	1.0	1.2	V	
VOLTAGE PRE-REGULATOR OUTPUT (VPPREF, VPPSENS)						
V_{PPSENS}	VPPSENS Output Voltage	5.85	6.5	7.15	V	
I_{VPPREF_CL}	VPPREF Current Limit	-5.0	-15	-20	mA	
V_{OCE}	Output Capacitance External (ceramic)	2.2	-	25	µF	
$I_{VPPSENS}$	VPPSENS Quiescent Current (excluding external PNP current)	-	-	3	mA	
$REGLINE_{\_VPP}$	Line Regulation I_{VCC} = 100 mA, I_{VPROT} = 50 mA, 9.0 V < V_{PWR} < 18 V and Diodes Inc. FZT753TA PNP	-	2.0	25	mV	
$V_{DROPOUT\_VPP}$	Dropout Voltage (Minimal Input/Output Voltage, tracks input below) I_{VCC} = 100 mA, I_{VPROT} = 50 mA and Diodes Inc. FZT753TA PNP	-	-	500	mV	
VOLTAGE REGULATOR OUTPUTS (VCC, VPROT)						
V_{CC}	VCC Output Voltage 0 ≤ I_{VCC} ≤ I_{VCC_C}	4.9	5.0	5.1	V	
I_{VCC_C}	VCC Output Current Continuous	-	-	200	mA	
$\lvert I_{VCC}\text{-}V_{PROT}\rvert$	VPROT Output Voltage (tracks VCC) I_{VCC} = 100 mA, I_{VPROT} = 50 mA 9.0 V < V_{PWR} < 18 V	-	-	25	mV	
I_{VPROT_C}	VPROT Output Current Continuous	-	-	100	mA	
I_{VCC_CL}	VCC Output Current Limiting	200	-	500	mA	(8)
I_{VPROT_CL}	VPROT Output Current Limiting	110	-	260	mA	
V_{OCE}	Output Capacitance External (V_{CC} and V_{PROT}) without reverse protection diode	2.2	-	47	µF	

Notes
5. This parameter is guaranteed by design but is not production tested.
6. Overvoltage thresholds minimum and maximum include hysteresis.
7. Undervoltage thresholds minimum and maximum include hysteresis
8. Guaranteed at 9.0 V ≤ V_{PWR} ≤ 18 V

Table 4. Power input static electrical characteristics

Characteristics noted under conditions of 6.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_{CASE} ≤ 125 °C and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 14 V, T_A = 25 °C.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
VOLTAGE REGULATOR OUTPUTS (VCC, VPROT) (CONTINUED)						
V_{CC}	VCC Output Voltage 0 ≤ I_{VCC} ≤ I_{VCC_C}	4.9	5.0	5.1	V	
REG_{LINE_VB}	Line Regulation (Both V_{CC} and V_{PROT}) I_{VCC} =100 mA, I_{PROT} = 50 mA, 9.0 V< V_{PWR} < 18 V	-	2.0	25	mV	
REG_{LOAD_VB}	Load Regulation (Both V_{CC} and V_{PROT}) measured from 10% - 90% of I_{VCC_C} and I_{PROT_C}, V_{PWR} = 13 V	-	20	35	mV	
$V_{DROPOUT\_VCC/VPROT}$	Dropout Voltage (Both V_{CC} and V_{PROT}) (Minimal Input/Output Voltage I_{VCC} = 100 mA, I_{VPROT} = 50 mA, tracks input below)	-	-	500	mV	
ALL LOW-SIDE DRIVERS (INJOUT1, INJOUT2, ROUT1, ROUT2, LAMPOUT, TACHOUT)						
$V_{OUT(FLT-TH)}$	Output Fault Detection Voltage Threshold, Outputs programmed OFF (Open Load), Outputs programmed ON (Short to Battery)	2.0	2.5	3.0	V	(9)
$I_{(OFF)OCO}$	Output OFF Open Load Detection Current (INJ1, INJ2, RELAY1, RELAY2 AND LAMP) • V_{DRAIN} = 18 V, Outputs Programmed OFF	40	75	115	µA	
$I_{(OFF)TACH}$	Output OFF Open Load Detection Current TachOut	10	-	30	µA	
$I_{OUT(LKG)}$	Output Leakage Current • V_{DRAIN} = 24 V, Open Load Detection Disabled and Output commanded OFF	-	-	20	µA	
T_{LIM}	Overtemperature Shutdown (OT)	155	-	185	°C	(9)
$T_{LIM(HYS)}$	Overtemperature Shutdown Hysteresis	5.0	10	15	°C	(9)
V_{OC}	Output Clamp Voltage • I_D = 20 mA	48	53	60	V	
INJOUT1, INJOUT2						
$R_{DS(ON)\_INJx}$	Drain-to-Source ON Resistance • I_{OUT} = 1.0 A T_J = 150 °C, V_{PWR} = 13 V	-	-	0.6	Ω	
$I_{OUT(LIM)\_INJx}$	Output Self Limiting Current	1.8	-	3.0	A	
ROUT1						
$R_{DS(ON)\_R1}$	Driver Drain-to-Source ON Resistance • I_{OUT} = 700 mA, T_J = 150 °C, V_{PWR} = 13 V	-	-	0.4	Ω	
$I_{OUT(LIM)\_R1}$	Output Self-limiting Current (Has inrush current timer)	3.0	-	6.0	A	
ROUT2						
$R_{DS(ON)\_R2}$	Driver Drain-to-Source ON Resistance • I_{OUT} = 350 mA, T_J = 150 °C, V_{PWR} = 13 V	-	-	1.5	Ω	
$I_{OUT(LIM)\_R2}$	Output Self-limiting Current	1.2	-	2.4	A	
LAMPOUT						
$R_{DS(ON)\_LAMP}$	Driver Drain-to-Source ON Resistance • I_{OUT} = 1.0 A, T_J = 150 °C, V_{PWR} = 13 V	-	-	1.5	Ω	
$I_{OUT(LIM)\_LAMP}$	Output Self-limiting Current (Has inrush current timer)	1.2	-	2.4	A	

Notes

9. This parameter is guaranteed by design, however it is not production tested.

Table 4. Power input static electrical characteristics

Characteristics noted under conditions of 6.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_{CASE} ≤ 125 °C and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 14 V, T_A = 25 °C.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
TACHOUT						
$R_{DS(ON)\_TACH}$	Driver Drain-to-Source ON Resistance • I_{OUT} = 50 mA, T_J = 150 °C, V_{PWR} = 13 V	-	-	20	Ω	
$I_{OUT(SHUTDOWN)\_TACH}$	Output Current Shutdown	60	-	110	mA	
ALL PRE-DRIVERS (IGNOUT1, IGNOUT2 AND O2HOUT)						
$V_{GS(ON)}$ $V_{GS(OFF)}$	Pre-driver Output Voltage, V_{PWR} = 13 V • I_{GD} = 500 µA • I_{GD} = -500 µA	7.0 0.0	8.0 0.375	9.0 0.5	V	
$I_{IGN\_GD\_H}$	IGNOUTx Output Source Current (IGNOUT1 and IGNOUT2 by default) • 1.0 ≤ V_{GD} ≤ 3.0, V_{PWR} = 13 V	10	-	-	mA	
$I_{(OFF)OCO}$	Output OFF Open Load Detection Current • V_{DRAIN} = 18 V, Outputs Programmed OFF	40	75	115	µA	
$I_{GPGD\_GD\_H}$	GPGD Output Source Current (O2HOUT by default) at 1.0 ≤ V_{GD} ≤ 3.0, V_{PWR} = 13 V	10	-	-	mA	
$V_{IGNFB(FLT-TH)}$ $V_{GPGD(FLT\_TH)}$	Pre-driver Fault Detection Voltage Threshold, Outputs programmed OFF (open load), Outputs programmed ON (short to battery) • I_{GD} = 500 µA • I_{GD} = -500 µA	100 1.0	250 2.5	400 4.0	mV V	
V_{CLAMP}	Output Clamp Voltage	48	53	60	V	
$V_{SENS-TH}$	Overcurrent Voltage Threshold for O2HOUT • $V_{O2HSENSN}$ to $V_{O2HSENSP}$	180	200	220	mV	
$V_{SENS-TH}$ $V_{SENS-TH}$	Overcurrent Voltage Threshold for IGNOUT1 and IGNOUT2 • $V_{IGNSENSN}$ to $V_{IGNSENSP}$ (IGNIN1 or IGNIN2 = 1) • $V_{IGNSENSN}$ to $V_{IGNSENSP}$ (IGNIN1 and IGNIN2 = 1)	180 360	200 400	220 440	mV	
$I_{SENS-OFFSET}$	Current Sense Input Offset Current (IGNSENSP,IGNSENSN, O2HSENSN, O2HSENSP)	-	-	15	µA	
$I_{SENS-BIAS}$	Current Sense Input Bias Current	-	-	15	µA	
ISO-9141 TRANSCEIVER PARAMETERS (8.0 V < V_{PWR} < 18 V)						
V_{IL_ISO}	Input Low Voltage at ISO I/O pin	-	-	0.3xV_{PWR}	V	
V_{IH_ISO}	Input High Voltage at ISO I/O pin	0.7*V_{PWR}	-	-	V	
V_{HYST_ISO}	Input Hysteresis at ISO I/O pin	0.15x V_{PWR}	-	-	V	
V_{OL_ISO}	Output Low-voltage at ISO I/O pin	-	-	0.2xV_{PWR}	V	
V_{OH_ISO}	Output High-voltage at ISO I/O pin	0.8x V_{PWR}R	-	-	V	
I_{PU}	Internal pull-up resistor to V_{PWR}	-	32	-	kΩ	
I_{LIM_ISO}	Output current limit at ISO I/O pin (MTX = 0)	50	100	150	mA	
C_{L_ISO}	Load capacitance at ISO I/O pin	0.01	3.0	10	nF	(10)
I_{ISO}	Output load current at ISO I/O pin (MTX = 0, RLOAD = 1.0 kΩ, ±10%)	-	12	-	mA	
T_{LIM}	Overtemperature Shutdown (OT)	155	-	185	°C	(10)
$T_{LIM(HYS)}$	Overtemperature Shutdown Hysteresis	5.0	10	15	°C	(10)

Notes

10. This parameter is guaranteed by design, however it is not production tested.

Table 4. Power input static electrical characteristics

Characteristics noted under conditions of 6.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_{CASE} ≤ 125 °C and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 14 V, T_A = 25 °C.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
VRS CONDITIONER INPUT						
V_{VRS_THRESH}	Comparator Thresholds	-	See Table variable via SPI or dynamically		mV	
$Accu_{THRESH}$	Threshold Accuracy Steady State Condition (±20% only valid for VRS DAC thresholds 110 mV and higher.All other thresholds guaranteed monotonic only.)	-	-	±20	%	
$I_{BIASRSX}$	Input Bias Current VRSP and VRSN (2.5 V common mode must be off)	-5.0		5.0	µA	
V_{CLAMP_P}	VRS Positive Clamp Voltage at I_{CLAMP} = 10 mA	5.5	-	5.8	V	
V_{CLAMP_N}	VRS Negative Clamp Voltage at I_{CLAMP} = 10 mA	-0.45	-	-0.22	V	
DIGITAL INTERFACE (MRX, MTX,CSB, SI, SCLK, SO, RINX,O2HIN, INJINX, IGNINX, BATSW, VRSOUT, RESETB)						
V_{IH}	Input Logic High-voltage Thresholds	0.7 x V_{CC}	-	V_{CC} + 0.3	V	
V_{IL}	Input Logic Low-voltage Thresholds	GND - 0.3	-	0.2 x V_{CC}	V	
V_{HYS}	Input Logic Voltage Hysteresis	500	-	-	mV	
C_{IN}	Input Logic Capacitance	-	-	20	pF	
I_{LOGIC_SS}	Sleep Mode Input Logic Current • KEYSW = 0 V	-10	-	10	µA	(11)
I_{LOGIC_PD}	Input Logic Pull-down Current INJIN1, INJIN2, RIN1, RIN2, SI, SCLK, IGNIN1, IGNIN2, O2HIN • 0.8 V to 5.0 V	30	50	100	µA	(11)
I_{TRISO}	SO Tri-state Output (in Tri-state mode, CSB = 1) • 0 V to 5.0 V	-10	-	10	µA	
I_{CSB}	$\overline{CSB}$ Input Current • CSB = V_{CC}	-10	-	10	µA	
I_{LOGIC_PU}	Input Logic Pull-up Current - CSB and MTX • 0.0 to 4.2 V	-20	-40	-90	µA	
$I_{CSB(LKG)}$	CSB Leakage Current to V_{CC} • CSB = 5.0 V, KEYSW = 0.0 V	-	-	10	µA	
V_{SO_HIGH} V_{MRX_HIGH}	SO, MRX High-state Output Voltage (CSB =0 for SO) • $I_{SO-HIGH}$ = -1.0 mA	V_{CC} - 0.4	-	-	V	
V_{SO_LOW} V_{MRX_LOW}	SO, MRX Low-state Output Voltage (CSB =0 for SO) • I_{SO-LOW} = 1.0 mA	-	-	0.4	V	
V_{BATSW_HIGH}	BATSW High-state Output Voltage • $I_{SO-HIGH}$ = -10 mA	V_{CC} - 1.0	-	-	V	
V_{BATSW_LOW}	BATSW Low-state Output Voltage • I_{SO-LOW} = 10 mA	-	-	1.0	V	
V_{KEYSW_HIGH}	KEYSW High-state Input Voltage	4.5	-	V_{PWR}	V	
V_{KEYSW_LOW}	KEYSW Low-state Input Voltage	-0.3	-	2.5	V	
V_{KEYSW_HYS}	KEYSW Hysteresis	100	-	-	mV	

Notes

11. This parameter is guaranteed by design, however it is not production tested.

Table 4. Power input static electrical characteristics

Characteristics noted under conditions of 6.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_{CASE} ≤ 125 °C and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 14 V, T_A = 25 °C.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
DIGITAL INTERFACE (MRX, MTX,CSB, SI, SCLK, SO, RINX,O2HIN, INJINX, IGNINX, BATSW, VRSOUT, RESETB) (CONTINUED)						
V_{VRSOUT_LOW}	VRS Low-state Output Voltage • $I_{VRS-LOW}$ = 1.0 mA	-	-	0.4	V	
V_{VRSOUT_HIGH}	VRS High-state Output Voltage • $I_{VRS-HIGH}$ = 1.0 mA	V_{CC} -0.4	-	5.0	V	
V_{RESET_LOW}	RESET Low-state Output Voltage • $I_{RESET-LOW}$ = 1.0 mA	-	-	0.4	V	
$I_{RESET\_LEAKAGE\_HIGH}$	RESET High-state Leakage Current	10	-	25	μA	
$R_{RESET\_PULDOWN}$	RESET Pull-down Resistor	200	-	500	kΩ	

4.3 Dynamic electrical characteristics

Table 5. Dynamic electrical characteristics [13]

Characteristics noted under conditions of 6.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_{CASE} ≤ 125 °C and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 14 V, T_A = 25 °C.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
POWER INPUT						
t_{RESET}	Required Low State Duration on V_{CC} for Power On Reset • V_{CC} ≤ 0.2 V	1.0	-	-	µs	
$t_{(POR)}$	Power on RESET pulse width	100	-	-	µs	
$t_{(KEYSW\_FILTER)}$	KEYSW Filter Time	-	12.7	-	ms	[12]
WATCHDOG TIMER						
WDMAX	Maximum Time Value Watchdog can be loaded with (default time)	-	-	10	sec.	
WD_{MIN}	Minimum Time Value Watchdog can be loaded with	1.0	-	-	ms	
WD_{RESET}	Reset Pulse Width when Watchdog times out	100	-	-	µs	
VRS CONDITIONING INPUT						
$OUTPUT_{BLANK}$	Output Blanking Time Programming Range (% of previous out pulse 0 to 15/32 in 1/32 steps, 15/32 = 46.9%)	0	-	50	%	
$OUTPUT_{DEGLITCH}$	Output Deglitch Filter Time (1/128 of the previous output pulse)	-	1.0	-	%	
$DELAY_{THRESH}$	Delay from CSB to Change in VRS Comparator Threshold	-	-	10	µs	[12]
$DELAY_{OBT}$	Delay from CSB to Change in VRS Output Blank Time	-	-	10	µs	[12]
ISO9141 TRANSCEIVER						
ISO_{BR}	Typical ISO9141 Data Rate	-	10	-	kbps	
t_{TXDF}	Turn OFF Delay MTX Input to ISO Output	-	-	2.0	µs	
t_{RXDF}, t_{RXDR}	Turn ON/OFF Delay ISO Input to MRX Output	-	-	1.0	µs	
t_{RXR}, t_{RXF}	Rise and Fall Time MRX Output (measured from 10% to 90%)	-	-	1.0	µs	
t_{TXR}, t_{TXF}	Maximum Rise and Fall Time MTX Input (measured from 10% to 90%)	-	-	1.0	µs	
ALL LOW-SIDE DRIVERS						
t_{SC1}	Output ON Current Limit Fault Filter Timer	30	60	90	µs	
t_{REF}	Output Retry Timer	7.0	10	13	ms	
t_{INRUSH}	Inrush Current Delay Timer	7.0	10	13	ms	[12]
$t_{(OFF)OC}$	Output OFF Open-circuit Fault Filter Timer	100	-	400	µs	
$t_{SR(RISE)}$	Output Slew Rate, INJOUT1, INJOUT2, ROUT1, ROUT2 and LAMPOUT • R_{LOAD} = 500 Ω, V_{LOAD} = 14 V	1.0	5.0	10	V/µs	
$t_{SR(FALL)}$	Output Slew Rate, INJOUT1, INJOUT2, ROUT1, ROUT2 and LAMPOUT • R_{LOAD} = 500 Ω, V_{LOAD} = 14 V	1.0	5.0	10	V/µs	
t_{PHL}	Propagation Delay (Input Rising Edge OR CSB to Output Falling Edge) • Input at 50% V_{DD} to Output voltage 90% of V_{LOAD} (INJ1, INJ2, ROUT1, ROUT2, LAMP)	-	1.0	5.0	µs	
t_{PHL}	Propagation Delay (Input Rising Edge OR CSB to Output Falling Edge) • Input at 50% V_{DD} to Output voltage 90% of V_{LOAD} (TACHOMETER)	-	1.0	6.0	µs	

Notes
12. Guaranteed by Design
13. internal oscillator of 4.0 MHz ±10% typical for V_{PWR} = 13 V, at room temp.

Table 5. Dynamic electrical characteristics (13)

Characteristics noted under conditions of 6.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_{CASE} ≤ 125 °C and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 14 V, T_A = 25 °C.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
ALL LOW-SIDE DRIVERS (CONTINUED)						
t_{PLH}	Propagation Delay (Input Falling Edge OR CSB to Output Rising Edge) • Input at 50% V_{DD} to Output voltage 10% of V_{LOAD} (INJ1, INJ2, ROUT1, ROUT2, LAMP)	-	1.0	5.0	µs	
t_{PLH}	Propagation Delay (Input Falling Edge OR CSB to Output Rising Edge) • Input at 50% V_{DD} to Output voltage 10% of V_{LOAD} (TACHOMETER)	-	1.0	6.0	µs	
$t_{SR(FALL)}$	Output Slew Rate, Tachout • R_{LOAD} = 500 Ω, V_{LOAD} = 14 V	6.0	-	14	V/µs	
ALL GATE PRE-DRIVER (IGN1, IGN2 AND O2H)						
$t_{(OFF)OC}$	Output OFF Open-circuit Fault Filter Timer	100	-	400	µs	
t_{SC1}	Overcurrent (short-circuit) Fault Filter Timer	30	-	90	µs	
t_{PLH}	Propagation Delay (Input Rising Edge OR CSB to Output Rising Edge) • Input at 50% V_{DD} to Output voltage 10% of $V_{GS(ON)}$	-	1.0	5.0	µs	
t_{PHL}	Propagation Delay (Input Falling Edge OR CSB to Output Falling Edge) • Input at 50% V_{DD} to Output voltage 90% of $V_{GS(ON)}$	-	1.0	5.0	µs	
SPI DIGITAL INTERFACE TIMING (14)						
t_{LEAD}	Falling Edge of CSB to Rising Edge of SCLK • Required Setup Time	100	-	-	ns	
t_{LAG}	Falling Edge of SCLK to Rising Edge of CSB • Required Setup Time	50	-	-	ns	
$t_{SI(SU)}$	SI to Rising Edge of SCLK • Required Setup Time	16	-	-	ns	
$t_{SI(HOLD)}$	Rising Edge of SCLK to SI • Required Hold Time	20	-	-	ns	
$t_{R(SI)}$	SI, CSB, SCLK Signal Rise Time (15)	-	5.0	-	ns	
$t_{F(SI)}$	SI, CSB, SCLK Signal Fall Time (15)	-	5.0	-	ns	
$t_{SO(EN)}$	Time from Falling Edge of CSB to SO Low-impedance (16)	-	-	55	ns	
$t_{SO(DIS)}$	Time from Rising Edge of CSB to SO High-impedance	-	-	55	ns	
t_{VALID}	Time from Falling Edge of SCLK to SO Data Valid (17)	-	25	55	ns	
t_{STR}	Sequential Transfer Rate (14) • Time required between data transfers	-	-	1.0	µs	

Notes

14. These parameters are guaranteed by design. Production test equipment uses 1.0 MHz, 5.0 V SPI interface (variable with magnitude input frequency).
15. Rise and Fall time of incoming SI, CSB and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
16. Time required for output states data to be terminated at SO pin.
17. Time required to obtain valid data out from SO following the fall of SCLK with 200 pF load.

4.4 Timing diagrams

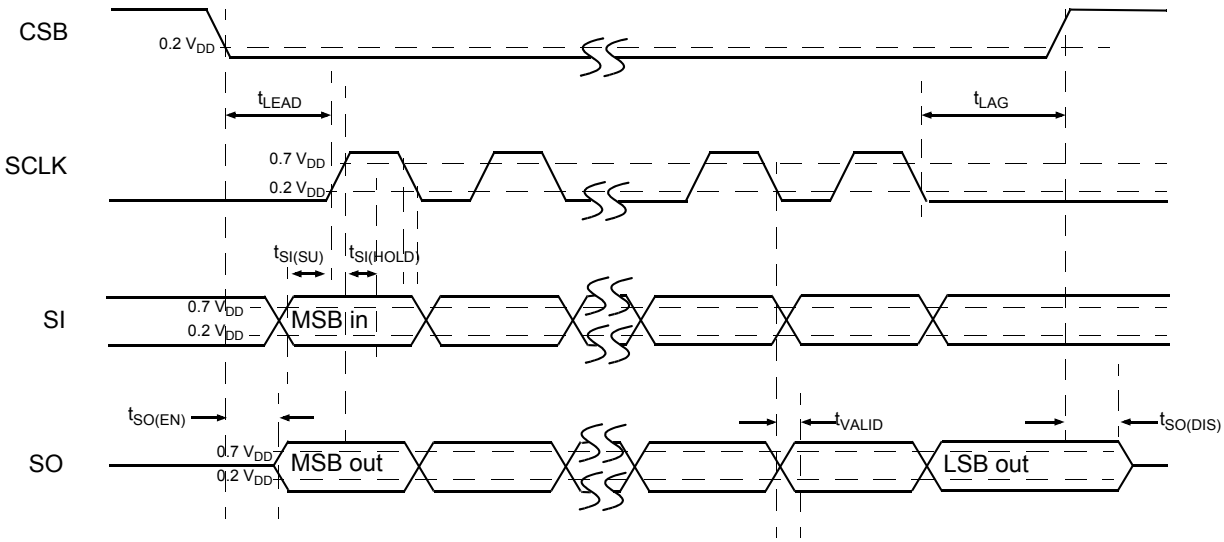

Figure 4. Timing diagram

4.5 Typical electrical characteristics

4.5.1 Driver and gate driver characteristics

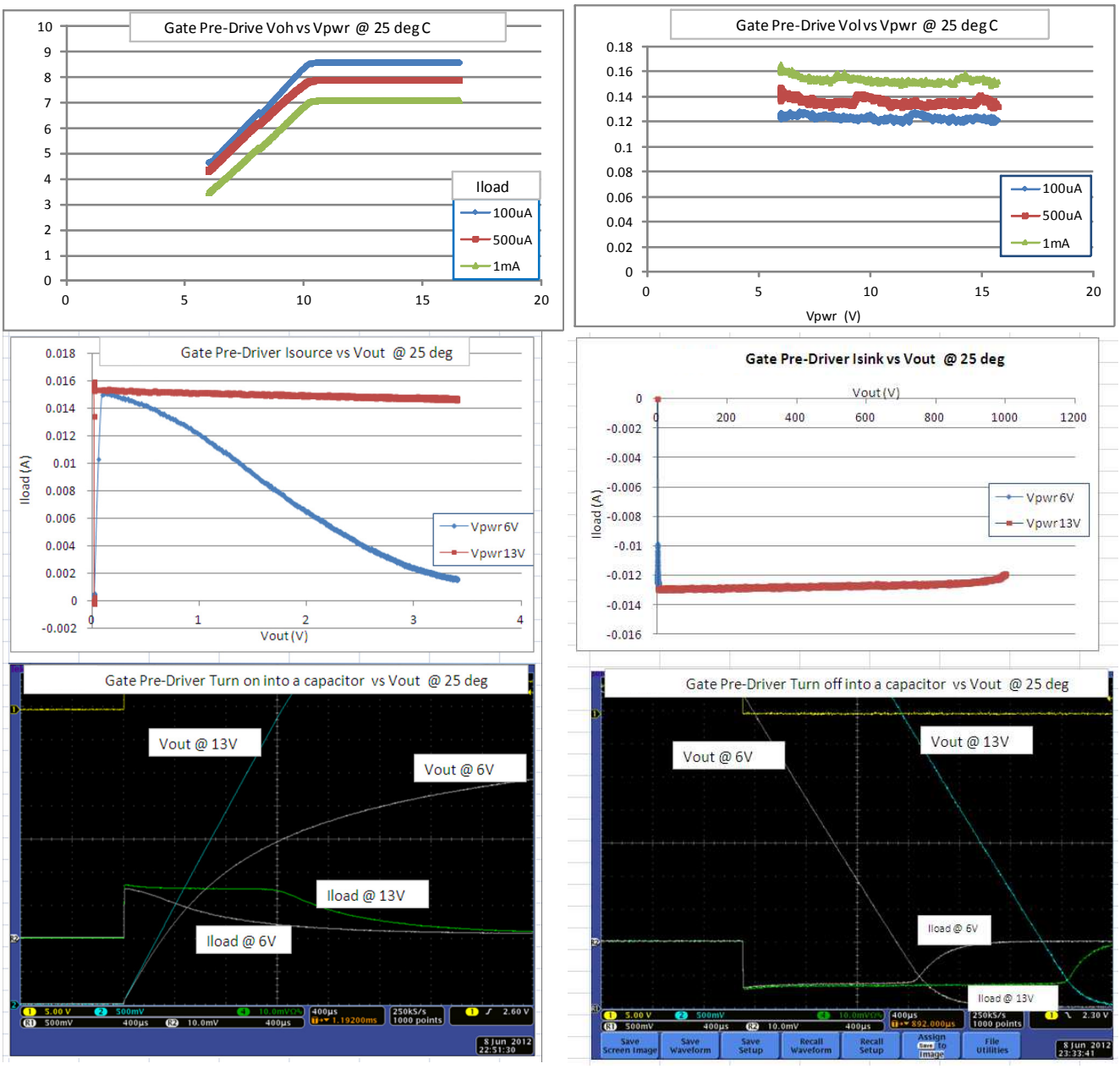

Figure 5. Typical electrical specifications

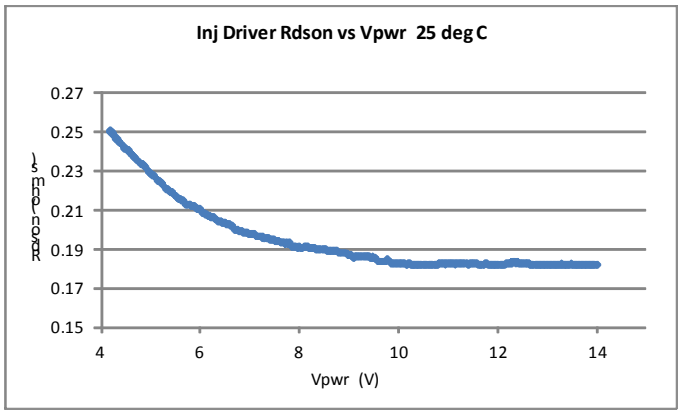

Figure 6. Typical electrical specifications (continued)

4.5.2 V_{CC} and V_{PROT} characteristics

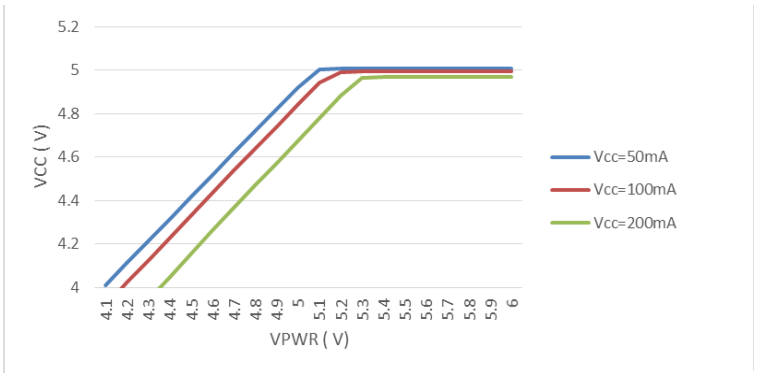

Figure 7. V_{CC} voltage vs. V_{PWR} at 125 °C

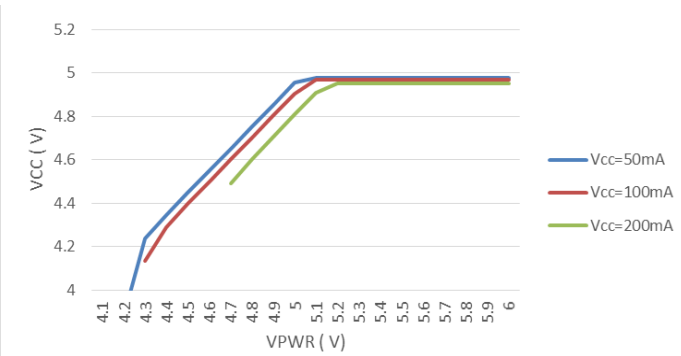

Figure 9. V_{CC} voltage vs. V_{PWR} at -40 °C

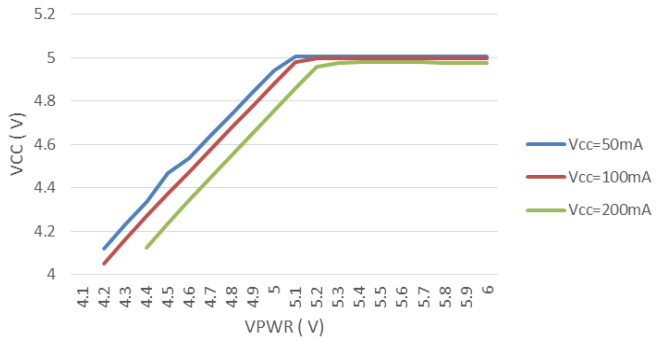

Figure 8. V_{CC} voltage vs. V_{PWR} at 25 °C

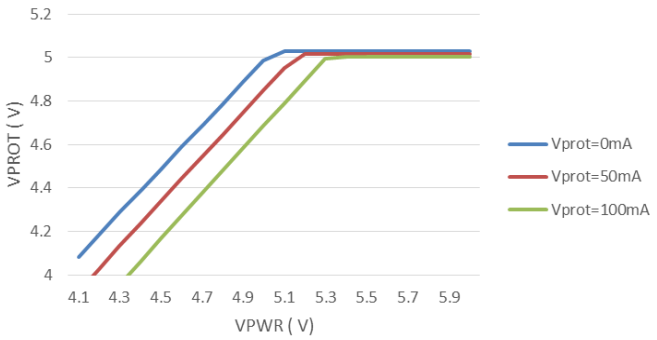

Figure 10. V_{PROT} voltage vs. V_{PWR} at 125 °C

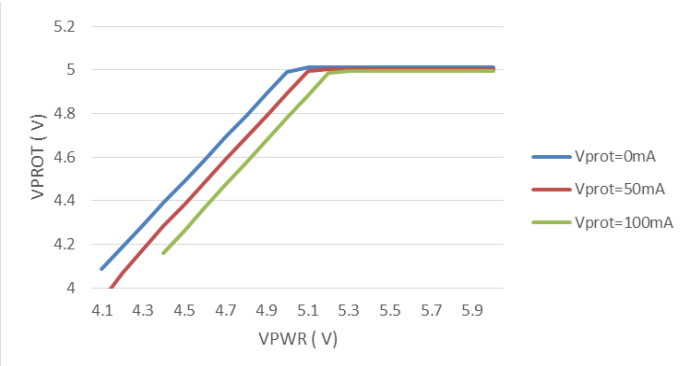

Figure 11. V_{PROT} voltage vs. V_{PWR} at 25 °C

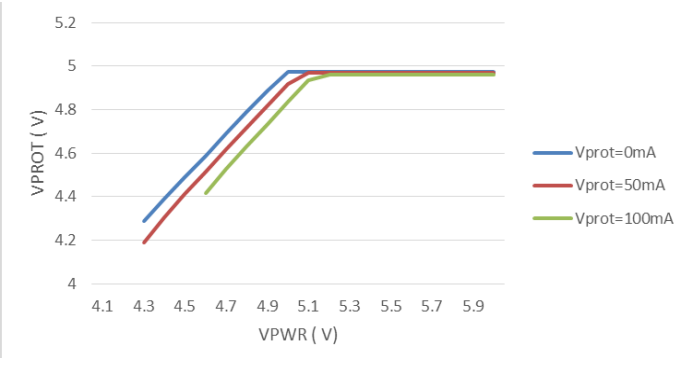

Figure 12. V_{PROT} voltage vs. V_{PWR} at -40 °C

5 General IC functional description and application information

5.1 System controller

5.1.1 System control signals

5.1.1.1 KEYSW input pin

KEYSW is the input from the vehicle ignition key switch. This signal is at V_{BAT} (12 V) when the key is inserted and turned to the ON position. When the key is in the OFF position and/or removed from the key switch, this input is pulled to ground by an internal pull-down resistor. This pin is internally protected against a reverse battery condition by an internal diode. The state of the KEYSW input is also available as a bit in the SPI Status Register.

5.1.1.2 BATSW output pin

The BATSW output pin is a 5.0 V logic level output, which by default is an indication of the state of the KEYSW input.

5.1.1.3 PWREN SPI control register BIT

The PWREN signal is a bit in the SPI Control Register #1 allowing “Prepare to shutdown” state transition.

5.1.2 Operating modes

5.1.2.1 Power On Reset (POR)

Applying V_{PWR} and bringing KEYSW high (VBAT), longer than the KEYSW filter time, generates a Power On Reset (POR) and places the device in the Normal operating state. The Power On Reset circuit incorporates a timer to prevent high frequency transients from causing an erroneous POR. Upon enabling the device (KEYSW High), outputs are activated based on the initial state of the control register or parallel input. All three supplies, V_{PP}, V_{CC} and V_{PROT}, are enabled when KEYSW is brought high.

Table 6. Operational states

KEYSW Input	PWREN SPI Bit Input	BATSWB Output	All Supplies	STATE
L	L	L	OFF	Sleep
H	L	H	ON	NORMAL
H	H	H	ON	NORMAL
L	H	L	ON	Prepare to shutdown

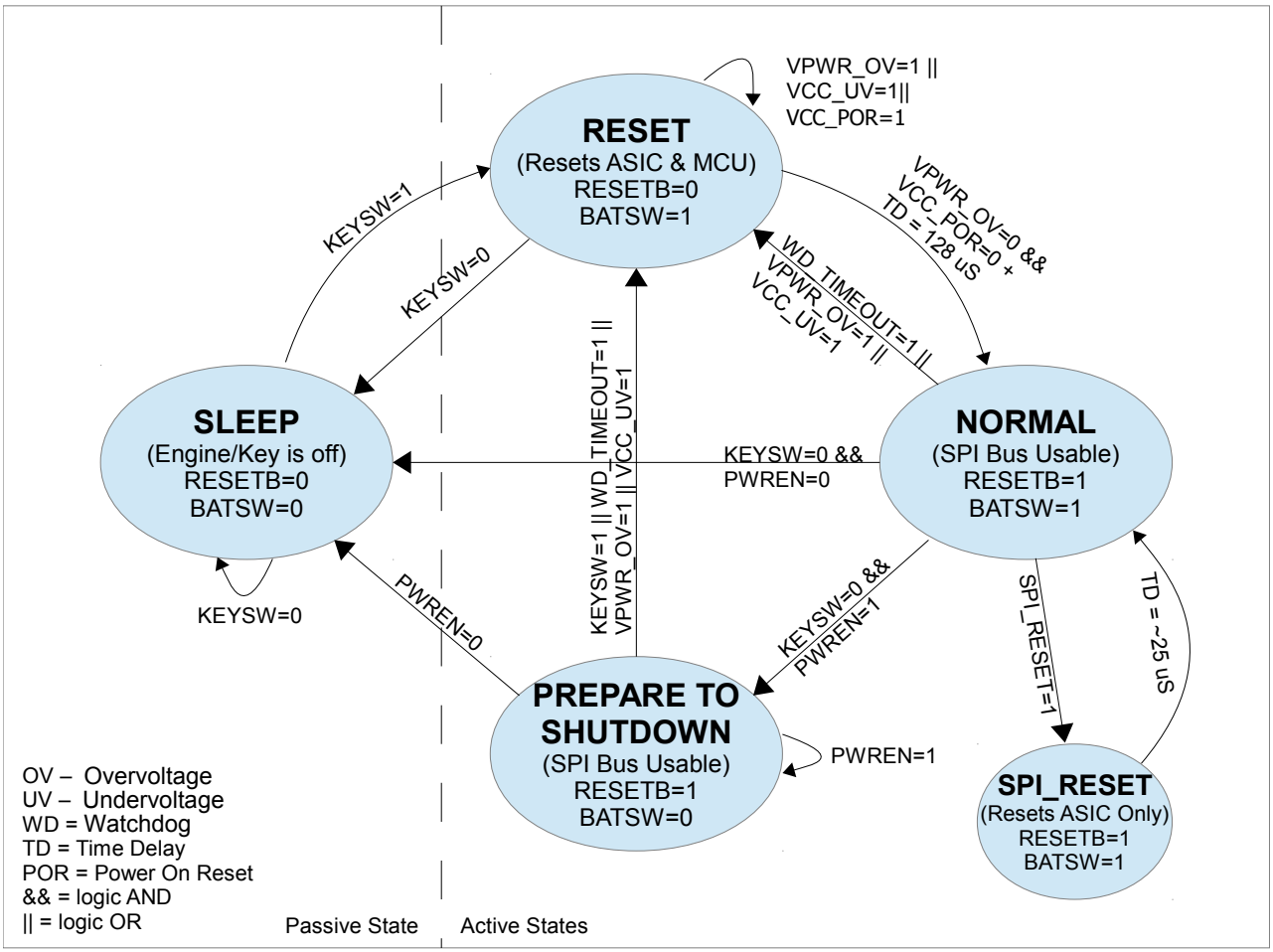

Figure 13. 33814 functional state diagram

5.1.2.2 Normal state

The default Normal state is entered when power is applied to the VPWR and KEYSW pins. Note that the device is designed to have VPWR present before KEYSW is brought high. It is acceptable to bring VPWR and KEYSW high simultaneously. However it is not recommended to bring KEYSW high while VPWR is low.

SPI register settings from Power On Reset (POR) are as follows:

- All outputs turned off
- Off State open load detection enabled (LSD)
- Default values in the SPI Configuration, Control and Status registers

5.1.2.3 Sleep state

When KEYSW signal is low and the PWREN SPI Control register bit is also low, the 33814 enters into Sleep mode. In the Sleep state, all outputs, current sources and sinks are off and the device consumes less than $I_{VPWR(SS)}$. When KEYSW signal goes high, it wakes up the IC, turns on the V_{PP} regulator and a Power On Reset signal is generated.

5.1.2.4 Prepare to shutdown state

The purpose of the PWREN signal is to allow the MCU to control the shutdown of power to itself when the user turns off the KEYSW. This may be necessary to allow the MCU the time required to perform its pre-shutdown routines. When the MCU wants to shutdown the power supplies in the 33814, it must write a logic zero (0) to the PWREN bit in the SPI Control register. Only the state of the PWREN bit in the SPI Control register controls the shutdown of the 33814 power supplies. In this state, only the outputs are turned off (except ROUT2 if the Shutdown Disable bit is set. See 5.5.3.3. Using ROUT2 as a power relay, page 35).

5.1.2.5 Power On Self-test (POST)

When a power on occurs after a POR, it may be desired to go through an initial Power On Self-test routine to ensure the SPI is working correctly and the status registers in the 33814 are viable. After a POR, all the registers in the 33814 contain their ‘default’ values, as indicated in the SPI register tables later in this document. The watchdog is also set to its default timeout value of 10 seconds, so any POST routine must be accomplished within this time frame or a WD reset may occur.

To perform a POST routine, the MCU should first send a SPI message to set the POST enable bit in the SPI control register 1, bit 6. Once this bit is set, the status registers are disconnected from the analog and logic portions of the 33814 and are connected only to the SPI circuitry. The POST can then write various data patterns to the status registers and verify that none of the bits are ‘stuck’ and state of the bit is accurately reflected. Note that bits in the status register labeled ‘x’ are not implemented and testing these bits may result in erroneous data. After testing all the status registers and confirming they are viable, the status registers can be set back to their default values by clearing the POST Enable bit back to 0. The POST enable bit allows the MCU to write ones (1s) to the Status registers.

Normally, the status register can only be cleared to zeros by the MCU and ones can be written to the status register only by the 33814 internal logic. This is designed to prevent the MCU from missing any reported fault bits and, for the 33814, to prevent system status errors resulting from the MCU erroneously writing a one (1) to a fault bit.

Once the POST enable bit is set back to a zero (0) by the MCU, the status register returns to the condition where the 33814 can only write ones (1s) to it and the MCU can only write zeros (0s) to it. Again, it is important to note that any POST routine should be designed to take less than 10 seconds to avoid a watchdog reset from occurring and truncating the POST routine, because the WD reset clears the POST Enable bit as well.

5.1.3 BATSW output functionality

The BATSW output pin has several functionalities:

- By default, the BATSW output pin is an indication of the state of the KEYSW input.
- The BATSW output can also be used to control an LS driver, such as the Relay ROUT2 driver by connecting the BATSW output to the RIN2 input.
- The BATSW output can also be configured as a low current LED high-side driver controlled through the SPI interface.

5.1.3.1 BATSW pin as a KEYSW input indication

When KEYSW is at V_{BAT} (12 V) level, the BATSW output is a logic 1 (5.0 V) and when KEYSW is at ground (0 V) level, BATSW is at a logic 0. The BATSW output may be used to inform the MCU the user is trying to shutdown the vehicle.

5.1.3.2 BATSW pin as an LS driver control

The BATSW output can also be used to control an LS driver, such as the Relay ROUT2 driver, by connecting the BATSW output to the RIN2 input. (see 5.5.3.3. Using ROUT2 as a power relay, page 35)

5.1.3.3 BATSW pin as an LED driver

If the BATSW signal is not needed by the MCU or to control the Relay 2 output, it can be configured as a low current LED high-side driver controlled through the SPI interface. As a high-side driver, BATSW can be PWM’d to allow an LED to be dimmed. A bit in the SPI Battery Switch Logic Output Configuration register called ‘HSD’, controls whether the BATSW output is a simple high-side driver, or controlled by KEYSW as indicated previously.

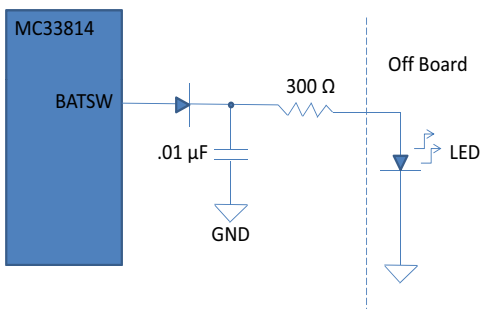

Figure 14. Recommended Circuit to Use BATSW as an LED Driver

If the BATSW output is used to control an LED, the LED cathode should be tied to ground and the LED anode should be connected to the BATSW pin through an external resistor. The value of the external resistor should be 340 Ω or greater. Care must be taken if the BATSW output is sent off-board due to the chance of shorts to the battery or shorts to ground, for which the output is not protected. At a minimum, this output should be protected by a diode, a current limit resistor and an ESD capacitor (0.01 µF ceramic).

5.1.4 System SPI registers

5.1.4.1 SPI configuration registers

Table 7. Battery switch logic output configuration register

Reg #	Hex			7	6	5	4	3	2	1	0
6	6	Battery Switch Logic Output	R/W	HSD Mode	x	x	x	x	x	PWM Freq.1	PWM Freq. 0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 8. Battery switch logic output configuration register field

Field	Description
7-HSD Mode	BATSW Mode selection 0 - BATSW is controlled by KEYSW 1 - BATSW is used as a high-side driver
1-0 PWM Freq.x	PWM Frequency and Duty Cycle Mode (18) 00 - PWM Freq.: None or Ext.Pin - D/C: None or ext.Pin 01 - PWM Freq.:100 Hz-D/C: Internal 10 - PWM Freq.: 1 KHz-D/C: Internal 11 - PWM Freq.:On ext. pin /100 -D/C: Internal

Notes
18. See 5.5.2.2. Pulse Width Modulation mode, page 33

5.1.4.2 SPI control registers

Table 9. Other OFF/ON control register

Reg #	Hex			7	6	5	4	3	2	1	0
1	1	Other OFF/ON Control	R/W	Pwren **OFF**/ON	POST Enable **OFF**/ON	X	VProt **ON**/OFF	X	Batsw **OFF**/ON	Tach OFF/**ON**	RESET internal only
			Reset	(0)	(0)	(0)	(1)	(0)	(0)	(1)	(0)
8	8	Batsw	R/W	X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 10. Other OFF/ON control register field description

Field	Description
7-Pwren OFF/ON	Power Enable 0-Power Disable (allowing sleep mode entry) 1-Power Enable (allowing Prepare to Shutdown mode entry)
6-POST Enable OFF/ON	Power On Self Test Enable 0-POST Disable 1-POST Enable
2-BATSW OFF/ON	BATSW Output Control 0-BATSW Output OFF 1-BATSW Output ON

Table 11. BATSW control register field description

Field	Description
6-0 PWM x	PWM Duty Cycle Setting with 1% increment 0000000 to 1100100 (Dec. 100) represent 0% to 100% 1100100 (Dec. 100) to 1111111 (Dec.127) all map to 100%.

5.1.4.3 SPI status registers

Table 12. Power supply and any system fault status register

Reg #	Hex			7	6	5	4	3	2	1	0
13	D	Power Supply and Any System Faults	R/W	Any System Faults	Keysw	Pwren	Batsw	SPI Error	V_{PROT} Short to Battery	V_{PROT} Overtemp OT	V_{PROT} Short to Ground
			Reset	(0)	(1)	(0)	(0)	(0)	(0)	(0)	(0)

Table 13. Power supply and any system fault status register field description

Field	Description
7-Any System Fault	System-wide any fault bit whose stats is the OR of all the other “Any fault” bits in the other status 0-No Fault reported 1-At least one Fault is reported [19]
6-Keysw	KEYSW Pin Status: 0-KEYSW is high (V_{BAT} Present) 1-KEYSW is low (Prepare to Shutdown mode)
5-PWREN	PWREN Status 0-PWREN Control bit is low 1-PWREN Control bit is high
4-Batsw	BATSW Pin Status 0-BATSW Pin is low 1-BATSW Pin is high

Notes
19. The MCU must interrogate all the other status registers to determine the actual fault(s) present.

5.2 Watchdog

5.2.1 Watchdog Normal operation

The watchdog is a programmable timer used to monitor the operation of the MCU. The timer programming is done by the Watchdog Parameters SPI Configuration Register by selection the Time Multiplier Value (bit 6-4) and the Time Value (bit 3-0).

Watchdog Timer = Time Multiplier Value (1.0 s,100 ms, or 10 ms) X Time Value (1 to 10)

Using this technique, time values from 1.0 ms. to 10 seconds can be programmed into the watchdog.(default value is 10 s)

When the MCU is executing code properly, its program code should contain instructions to periodically send a SPI message to the watchdog SPI control register to refresh the watchdog. The watchdog timer, once refreshed, reloads the time interval value stored in the SPI watchdog configuration register and begins counting time again. Under normal operating conditions this sequence continues until the MCU shuts down, typically, when the KEYSW is turned off.