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Power System Basis Chip with High Speed CAN transceiver

33907_08

POWER SYSTEM BASIS CHIP

AE SUFFIX (PB-FREE)
98ASA00173D
48-PIN LQFP-EP

The 33907_8 devices are multi-output, power supply, integrated circuit, including HSCAN transceiver, dedicated to the automotive market.

Multiple switching and linear voltage regulators, including low power mode are available with various wake-up capabilities. An advanced power management scheme is implemented to maintain high efficiency over wide input voltages and output current ranges.

The 33907_8 includes enhanced safety features, with multiple fail-safe outputs, becoming a full part of a safety oriented system partitioning, to reach a high integrity safety level.

The built-in enhanced high speed CAN interface fulfills the ISO11898-2 and -5 standards. Local and bus failure diagnostics, protection, and fail-safe operation mode are provided. This device is powered by SMARTMOS technology.

Features

- Highly flexible SMPS pre-regulator, allowing two topologies: non-inverting buck-boost or standard buck
- Switching mode power supply (SMPS) dedicated to MCU core supply, 1.2 V or 3.3 V delivering up to 1.5 A
- Linear voltage regulator dedicated to MCU A/D reference voltage or I/Os supply (VCCA). 5.0 V or 3.3 V
- Linear voltage regulator dedicated to auxiliary functions, or to a sensor supply (VCCA tracker or independent 5.0 V / 3.3 V)
- Multiple wake-up sources in low power mode: CAN and/or IOs
- Battery voltage sensing & MUX output terminal
- Enhanced safety block associated with fail-safe outputs
- Six configurable I/Os

Applications

- Electrical power steering
- Engine management
- Battery management
- Active suspension
- Gear box
- Transmission
- Electrical Vehicle (EV), Hybrid Electrical Vehicle (HEV)
- Advanced driver assistance systems

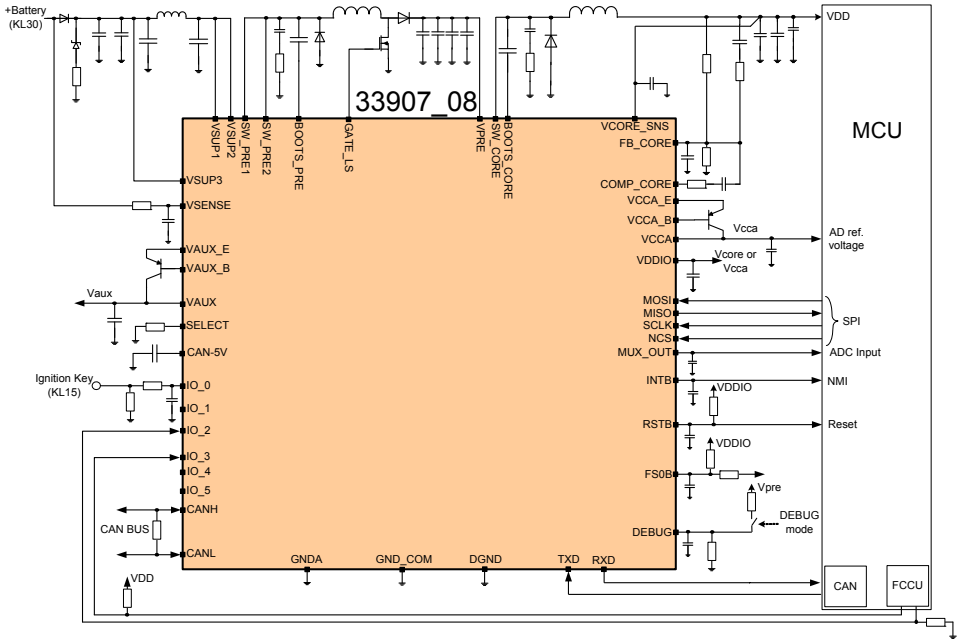

Figure 1. Simplified Application Diagram - Buck Boost Configuration

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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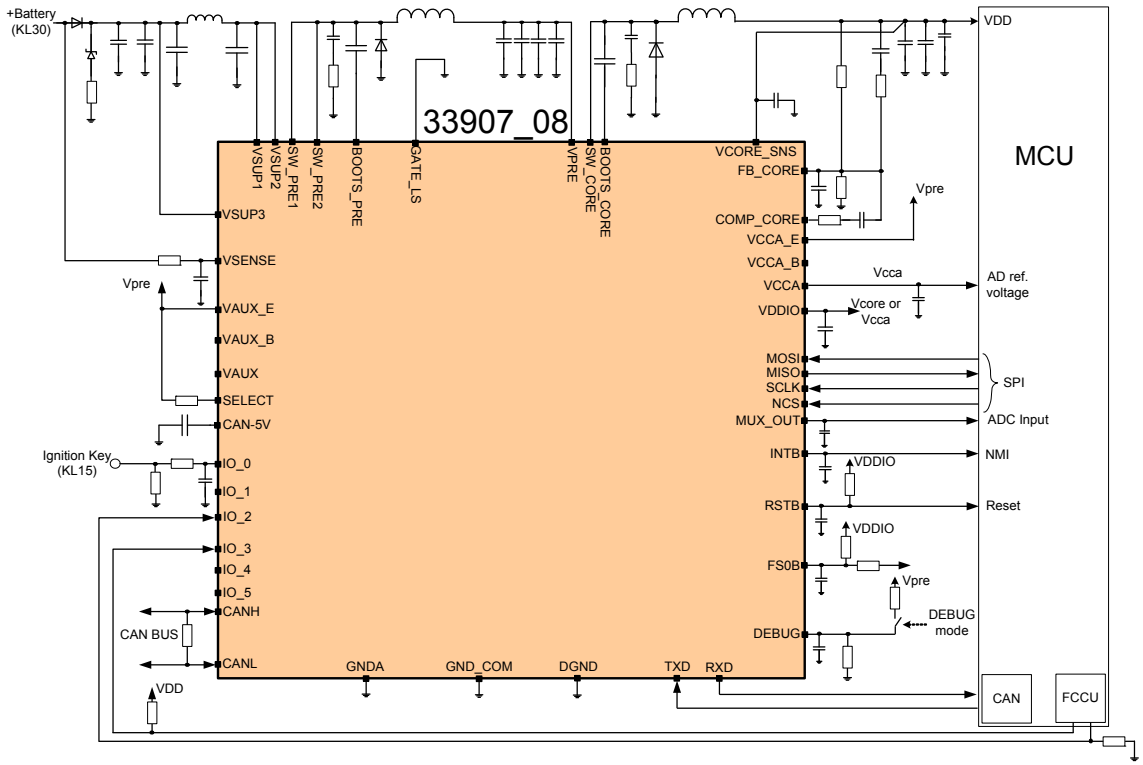

Figure 2. Simplified Application Diagram - Buck Configuration, V_{AUX} not used, V_{CCA} = 100 mA

1 Orderable Parts

Table 1. Orderable Part Variations

Part Number [1]	V_{CORE}	Temperature (T_A)	Package
MC33907AE	VCORE Output Current Capability in Normal Mode Page 12	-40 to 125 °C	48-pin LQFP exposed pad
MC33908AE			

Notes

1. To order parts in Tape & Reel, add the R2 suffix to the part number.

2 Internal Block Diagram

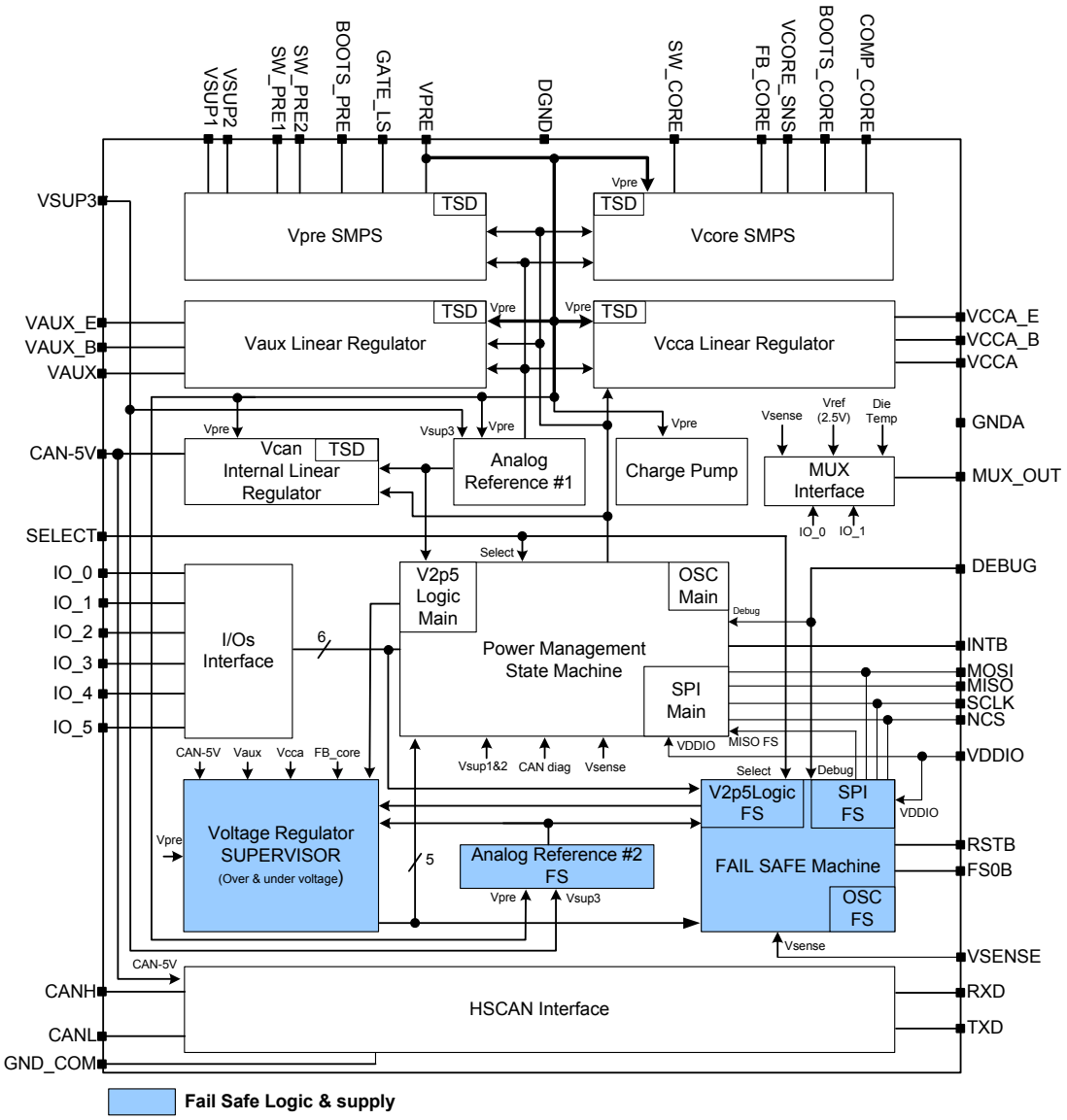

Figure 3. MC33907_08 Simplified Internal Block Diagram

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3 Pin connections

3.1 Pinout Diagram for 33907_8

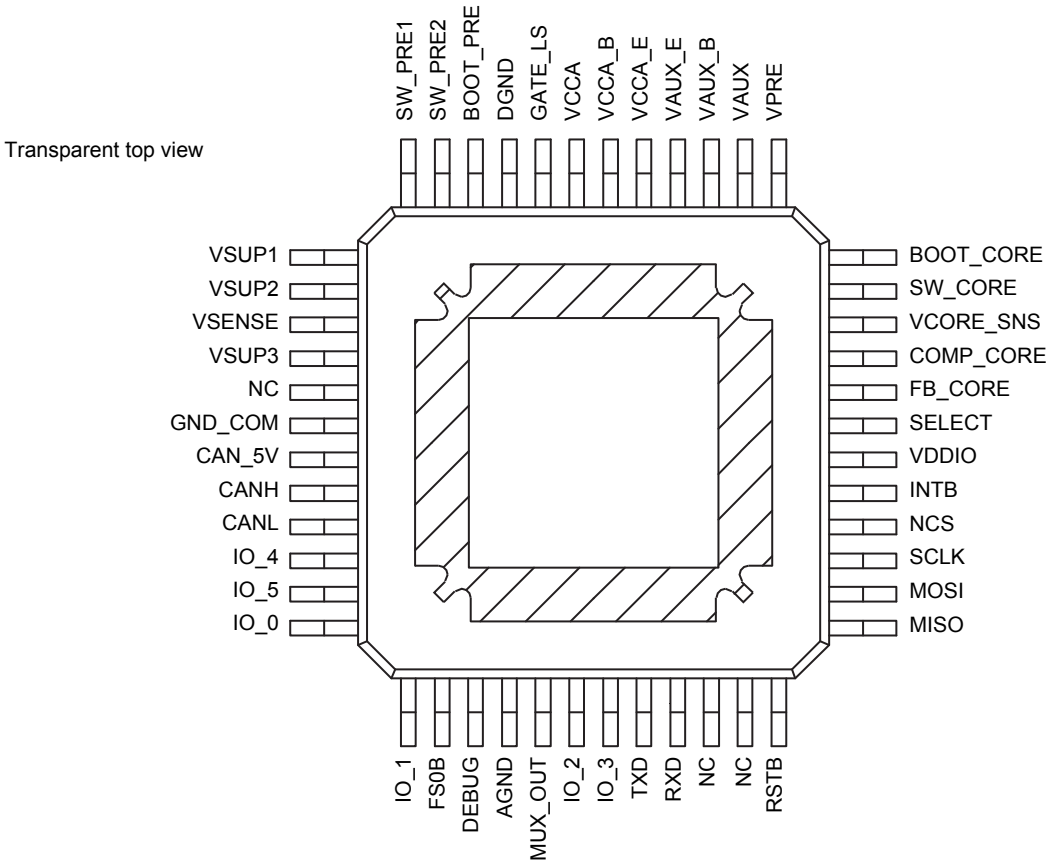

Figure 4. 33907_8 Pinout

3.2 Pin Definitions

A functional description of each pin can be found in the functional pin description section beginning on page 25.

Table 2. 33907_8 Pin Definition

Pin	Pin Name	Type	Definition
1	VSUP1	A_IN	Power supply of the device. An external reverse battery protection diode in series is mandatory
2	VSUP2	A_IN	Second power supply. Also protected by the external reverse battery protection diode used for VSUP1
3	VSENSE	A_IN	Sensing of the battery voltage. Must be connected prior to the reverse battery protection diode.
4	VSUP3	A_IN	Third power supply dedicated to the device supply. Also protected by the external reverse battery protection diode used for VSUP1. Shall be connected between the reverse protection diode and the input PI filter.
5, 22, 23	NC	N/A	Not connected. Pins must be left open.

Table 2. 33907_8 Pin Definition

Pin	Pin Name	Type	Definition
6	GND_COM	GROUND	Dedicated ground for CAN
7	CAN_5V	A_OUT	Output voltage for the embedded CAN interface
8	CANH	A_IN/OUT	HSCAN output High
9	CANL	A_IN/OUT	HSCAN output Low
10 11	IO_4:5	D_IN A_OUT	Can be used as digital input (load dump proof) with wake-up capability or as an output gate driver **Digital input**: Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes. **Wake-up capability:** Can be selectable to wake-up on a rising or falling edge, or on a transition **Output gate driver:** Can drive a logic level low side NMOS transistor. Controlled by the SPI.
12 13	IO_0:1	A_IN D_IN	Can be used as analog or digital input (load dump proof) with wake-up capability (selectable) **Analog input**: Pin status can be read through the MUX output terminal **Digital input:** Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes **Wake-up capability:** Can be selectable to wake-up on a rising or falling edge, or on a transition
14	FS0B	D_OUT	Output of the safety block (active low). The pin is asserted low at startup and when a fault condition is detected. Open drain structure.
15	DEBUG	D_IN	Debug mode entry input
16	AGND	GROUND	Analog ground connection
17	MUX_OUT	A_OUT	Multiplexed output to be connected to a MCU ADC. Selection of the analog parameter is available at MUX-OUT through the SPI.
18 19	IO_2:3	D_IN	Digital input pin with wake-up capability (logic level compatible) **Digital INPUT**: Pin status can be read through the SPI. Can be used to monitor error signals from MCU for safety purposes. **Wake-up capability:** Can be selectable to wake-up on a rising or falling edge, or on a transition.
20	TXD	D_IN	Transceiver input from the MCU which controls the state of the HSCAN bus
21	RXD	D_OUT	Receiver output which reports the state of the HSCAN bus to the MCU
24	RSTB	D_OUT	This output is asserted low when the safety block reports a failure. The main function is to reset the MCU. Reset input voltage is also monitored in order to detect external reset and fault condition. Open drain structure.
25	MISO	D_OUT	SPI bus. Master Input Slave Output
26	MOSI	D_IN	SPI bus. Master Output Slave Input
27	SCLK	D_IN	SPI Bus. Serial clock
28	NCS	D_IN	No Chip Select (Active low)
29	INTB	D_OUT	This output pin generates a low pulse when an Interrupt condition occurs. Pulse duration is configurable
30	VDDIO	A_IN	Input voltage for MISO output buffer. Allows voltage compatibility with MCU I/Os.
31	SELECT	D_IN	Hardware selection pin for VAUX and VCCA output voltages
32	FB_CORE	A_IN	VCORE voltage feedback. Input of the error amplifier.
33	COMP_CORE	A_IN	Compensation network. Output of the error amplifier.
34	VCORE_SNS	A_IN	Vcore output voltage sense
35	SW_CORE	A_IN	VCORE switching point
36	BOOT_CORE	A_IN/OUT	Bootstrap capacitor for VCORE internal NMOS gate drive

Table 2. 33907_8 Pin Definition

Pin	Pin Name	Type	Definition
37	VPRE	A_OUT	VPRE output voltage
38	VAUX	A_OUT	VAUX output voltage. External PNP ballast transistor. Collector connection
39	VAUX_B	A_OUT	VAUX voltage regulator. External PNP ballast transistor. Base connection
40	VAUX_E	A_OUT	VAUX voltage regulator. External PNP ballast transistor. Emitter connection
41	VCCA_E	A_OUT	VCCA voltage regulator. External PNP ballast transistor. Emitter connection
42	VCCA_B	A_OUT	VCCA voltage regulator. External PNP ballast transistor. Base connection
43	VCCA	A_OUT	VCCA output voltage. External PNP ballast transistor. Collector connection
44	GATE_LS	A_OUT	Low side MOSFET gate drive for “Non-inverting Buck-boost” configuration
45	DGND	GROUND	Digital ground connection
46	BOOT_PRE	A_IN/OUT	Bootstrap capacitor for the VPRE internal NMOS gate drive
47	SW_PRE2	A_IN	Second pre-regulator switching point
48	SW_PRE1	A_IN	Pre-regulator switching point

4 General Product Characteristics

4.1 Maximum Ratings

Table 3. Maximum Ratings

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit	Notes
ELECTRICAL RATINGS				
DC Voltage at Power Supply Pins	$V_{SUP1/2/3}$	-1.0 to 40	V	
DC voltage between VSUP1, 2, and VSUP3 ($V_{SUP1,2}$ > V_{SUP3})	$V_{SUP1/2/3}$	0.0 to 4.0	V	
DC Voltage at Battery Sense Pin	V_{SENSE}	-14 to 40	V	
DC Voltage at SW_PRE1 and SW_PRE2 Pins	$V_{SW}1, 2$	-1.0 to 40	V	
DC Voltage at VPRE Pin	V_{PRE}	-0.3 to 8	V	
DC Voltage at Gate_LS pin	V_{GATE_LS}	-0.3 to 8	V	
DC Voltage at BOOT_PRE pin	V_{BOOT_PRE}	-1.0 to 50	V	
DC Voltage at SW_CORE pin	V_{SW_CORE}	-1.0 to 8.0	V	
DC Voltage at VCORE_SNS pin	V_{CORE_SNS}	0.0 to 8.0	V	
DC Voltage at BOOT_CORE pin	V_{BOOT_CORE}	0.0 to 15	V	
DC Voltage at FB_CORE pin	V_{FB_CORE}	-0.3 to 2.5	V	
DC Voltage at COMP_CORE pin	V_{COMP_CORE}	-0.3 to 2.5	V	
DC Voltage at VAUX_E, VAUX_B pin	$V_{AUX\_E,B}$	-0.3 to 40	V	
DC Voltage at VAUX pin	V_{AUX}	-2.0 to 40	V	
DC Voltage at VCCA_B, VCCA_E pin	$V_{CCA\_B,E}$	-0.3 to 8.0	V	
DC Voltage at VCCA pin	V_{CCA}	-0.3 to 8.0	V	
DC Voltage at VDDIO	V_{DDIO}	-0.3 to 8.0	V	
DC Voltage at FS0B (with ext R mandatory)	V_{FS0}	-0.3 to 40	V	
DC Voltage at DEBUG	V_{DEBUG}	-0.3 to 40	V	
DC Voltage at IO_0:1; 4:5 (with ext R = 5.1 kΩ in series mandatory)	$V_{IO\_0,1,4,5}$	-0.3 to 40	V	
DC Voltage at INTB, RSTB, MISO, MOSI, NCS, SCLK, MUX_OUT, RXD, TXD, IO_2, IO_3	V_{DIG}	-0.3 to V_{DDIO}+0.3	V	
DC Voltage at SELECT	V_{SELECT}	-0.3 to 8.0	V	
DC Voltage on CANL, CANH	V_{BUS_CAN}	-27 to 40	V	
DC voltage on CAN_5 V	V_{CAN_5V}	-0.3 to 8.0	V	
IOs maximum current capability	$I_{\_IO}$	-5.0 to 5.0	mA	

Table 3. Maximum Ratings (continued)

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit	Notes
ESD Voltage				
Human Body Model (JESD22/A114) - 100 pF, 1.5 kΩ				
• All pins	$V_{ESD-HBM1}$	±2.0	kV	
• VSUP1, VSUP2, VSUP3, VSENSE, IO_0:1, IO_4:5, FS0B , DEBUG	$V_{ESD-HBM2}$	±3.5	kV	
• VAUX versus AGND	$V_{ESD-HBM3}$	±4.0	kV	
• CANH, CANL	$V_{ESD-HBM4}$	±6.0	kV	
Charge Device Model (JESD22/C101):				
• All Pins	$V_{ESD-CDM1}$	±500	V	
• Corner Pins	$V_{ESD-CDM2}$	±750	V	
System level ESD (Gun Test)				
• VSUP1, VSUP2, VSUP3, VSENSE, VAUX, IO_0:1, IO_4:5, FS0B				
330 Ω / 150 pF Unpowered According to IEC61000-4-2:	$V_{ESD-GUN1}$	±8.0	kV	
330 Ω / 150 pF Unpowered According to OEM LIN, CAN, FLexray Conformance	$V_{ESD-GUN2}$	±8.0	kV	
2.0 kΩ / 150 pF Unpowered According to ISO10605.2008	$V_{ESD-GUN3}$	±8.0	kV	
2.0 kΩ / 330 pF Powered According to ISO10605.2008	$V_{ESD-GUN4}$	±8.0	kV	
• CANH, CANL				
330 Ω / 150 pF Unpowered According to IEC61000-4-2:	$V_{ESD-GUN5}$	±15	kV	
330 Ω / 150 pF Unpowered According to OEM LIN, CAN, FLexray Conformance	$V_{ESD-GUN6}$	±12	kV	
2.0 kΩ / 150 pF Unpowered According to ISO10605.2008	$V_{ESD-GUN7}$	±15	kV	
2.0 kΩ / 330 pF Powered According to ISO10605.2008	$V_{ESD-GUN8}$	±15	kV	
THERMAL RATINGS				
Ambient Temperature	T_A	-40 to 125	°C	
Junction Temperature	T_J	-40 to 150	°C	
Storage Temperature	T_{STG}	-55 to 150	°C	
THERMAL RESISTANCE				
Thermal resistance junction to ambient	$R_{\theta JA}$	32	°C/W	(2)
Thermal resistance junction to Case Top	$R_{\theta JCTOP}$	23	°C/W	(3)
Thermal resistance junction to Case Bottom	$R_{\theta JCBOTTOM}$	1.3	°C/W	(4)

Notes

2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC - 883 Method 1012.1).
4. Thermal resistance between the die and the solder par on the bottom of the packaged based on simulation without any interface resistance.

4.2 Static Electrical Characteristics

Table 4. Operating Range

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
POWER SUPPLY						
I_{SUP}	Power Supply Current in Normal Mode (Vsup > Vsup_uv_7)	2.0	–	13.0	mA	
I_{SUP_LPOFF1}	Power Supply Current in LPOFF (14 V, @ T_A = 25 °C)	–	32	–	µA	
I_{SUP_LPOFF2}	Power Supply Current in LPOFF (18 V, @ T_A = 80 °C)	–	42	60	µA	
V_{SNS_UV}	Power Supply Undervoltage Warning	–	8.5	–	V	
$V_{SNS\_UV\_HYST}$	Power Supply Undervoltage Hysteresis	0.1	–	–	V	
$V_{SUP\_UV\_7}$	Power Supply Undervoltage Lockout (power-up)	7.0	–	8.2	V	
$V_{SUP\_UV\_5}$	Power Supply Undervoltage Lockout (power-up)	–	–	5.6	V	
$V_{SUP\_UV\_L}$	Power Supply Undervoltage Lockout (falling - Boost config.)	–	–	2.7	V	
$V_{SUP\_UV\_L\_B}$	Power Supply Undervoltage Lockout (falling - Buck config.)	–	–	4.6	V	
$V_{SUP\_UV\_HYST}$	Power Supply Undervoltage Lockout Hysteresis	–	0.1	–	V	(5)
V_{PRE} VOLTAGE PRE-REGULATOR						
V_{PRE}	V_{PRE} Output Voltage • Buck mode (V_{SUP} > Vsup_uv_7) • Buck mode ($V_{SUP\_UV\_7} \geq V_{SUP} \geq$ 4.6 V) • Boost mode ($V_{SUP} \geq$ 2.7 V)	 6.25 $V_{PRE\_UV\_4P3}$ 6.0	 – V_{SUP} - R_{DSON_PRE} * I_{PRE} –	 6.75 – 7.0	V	
I_{PRE}	V_{PRE} Maximum Output Current Capability • Buck or Boost with V_{SUP} > $V_{SUP\_UV\_7}$ • Buck with $V_{SUP\_UV\_7} \geq V_{SUP} \geq$ 4.6 V • Boost with $V_{SUP\_UV\_7} \geq V_{SUP} \geq$ 6.0 V • Boost with 6.0 V $\geq V_{SUP} \geq$ 4.0 V • Boost with 4.0 V $\geq V_{SUP} \geq$ 2.7 V	 2.0 0.5 2.0 1.0 0.3	 – 2.0 – – –	 – – – – –	A	(5)
I_{PRE_LPOFF}	V_{PRE} Maximum Output Current Capability in LPOFF at low Vsup voltage • Buck with $V_{SUP\_UV\_7} \geq V_{SUP} \geq$ 4.6 V • Boost with $V_{SUP\_UV\_7} \geq V_{SUP} \geq$ 6.0 V • Boost with 6.0 V $\geq V_{SUP} \geq$ 4.0 V • Boost with 4.0 V $\geq V_{SUP} \geq$ 2.7 V	 0.050 2.0 1.0 0.3	 – – – –	 – – – –	A	(5)
I_{PRE_LIM}	V_{PRE} Output Current Limitation with Vsup ≤ 28V	3.5	–	–	A	
I_{PRE_OC}	V_{PRE} Overcurrent Detection Threshold (in buck mode only) with $V_{SUP} \leq$ 28 V	5.0	–	–	A	
V_{PRE_UV}	V_{PRE} Undervoltage Detection Threshold (Falling)	5.5	–	6.0	V	
$V_{PRE\_UV\_HYST}$	V_{PRE} Undervoltage Hysteresis	0.05	–	0.15	V	(5)
$V_{PRE\_UV\_4P3}$	V_{PRE} Shut-off Threshold (Falling - buck mode)	4.2	–	4.5	V	

Notes
5. Guaranteed by design.

Table 4. Operating Range (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{PRE} VOLTAGE PRE-REGULATOR (CONTINUED)						
$V_{PRE\_UV\_4P3\_HYST}$	V_{PRE} Shut-off Hysteresis	0.05	–	0.15	V	(6)
R_{DSON_PRE}	V_{PRE} Pass Transistor On Resistance with $V_{SUP} \leq 28$ V	–	–	200	mΩ	
L_{IR_VPRE}	V_{PRE} Line Regulation	–	20	–	mV	(6)
LOR_{VPRE_BUCK}	V_{PRE} Load Regulation for C_{OUT} = 57 µF I_{PRE} from 50 mA to 2.0 A - Buck mode	–	100	–	mV	(6)
LOR_{VPRE_BOOST}	V_{PRE} Load Regulation for C_{OUT} = 57 µF I_{PRE} from 50 mA to 2.0 A - Boost mode	–	500	–	mV	(6)
$V_{PRE\_LL\_H}$ $V_{PRE\_LL\_L}$	V_{PRE} Pulse Skipping Thresholds	– –	200 180	– –	mV	
T_{WARN_PRE}	V_{PRE} Thermal Warning Threshold	–	125	–	°C	
T_{SD_PRE}	V_{PRE} Thermal Shutdown Threshold	160	–	–	°C	
$T_{SD\_PRE\_HYST}$	V_{PRE} Thermal Shutdown Hysteresis	–	10	–	°C	(6)
V_{SUP_IPFF}	I_{PFF} Input Voltage detection	18	–	24	V	
$V_{SUP\_IPFF\_HYST}$	I_{PFF} Input Voltage hysteresis	0.2	–	–	V	
$I_{PRE\_IPFF\_PK}$	I_{PFF} High Side Peak current detection with $V_{SUP} \leq 28$ V	1.7	–	–	A	
$V_{G\_LS\_OH}$	LS Gate driver High output voltage (I_{OUT} = 50 mA)	V_{PRE}-1	–	V_{PRE}	V	
$V_{G\_LS\_OL}$	LS Gate driver Low Level (I_{OUT} = 50 mA)	–	–	0.5	V	
V_{CORE} VOLTAGE REGULATOR						
V_{CORE_FB}	V_{CORE} Feedback Input Voltage	0.784	0.8	0.816	V	
I_{CORE}	V_{CORE} Output Current Capability in Normal Mode • MC33907 • MC33908	 – –	 – –	 0.8 1.5	A	
$I_{CORE\_LIM\_10}$ $I_{CORE\_LIM\_20}$	V_{CORE} Output Current Limitation • MC33907 • MC33908	 1.0 1.8	 – –	 2.0 3.5	A	
R_{DSON_CORE}	V_{CORE} Pass Transistor On Resistance	–	–	200	mΩ	
$LOR_{VCORE\_1.2}$	V_{CORE} Transient Load regulation - 1.2 V range	-60	–	60	mV	(6), (7)
$LOR_{VCORE\_3.3}$	V_{CORE} Transient Load regulation - 3.3 V range	-100	–	100	mV	(6), (7)
T_{WARN_CORE}	V_{CORE} Thermal Warning Threshold	–	125	–	°C	
T_{SD_CORE}	V_{CORE} Thermal Shutdown Threshold	160	–	–	°C	
$T_{SD\_CORE\_HYST}$	V_{CORE} Thermal Shutdown Hysteresis	–	10	–	°C	(6)

Notes

6. Guaranteed by design.
7. C_{OUT} = 40 µF, I_{CORE} = 10 mA to 1.5 A, $dI_{CORE}/dt \leq 2.0$ A/µs

Table 4. Operating Range (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{CCA} VOLTAGE REGULATOR						
V_{CCA}	V_{CCA} Output Voltage • 5.0 V config. with Internal ballast at 100 mA • 5.0 V config with external ballast at 200 mA • 5.0 V config with external ballast at 300 mA • 3.3 V config with Internal ballast at 100 mA • 3.3 V config with external ballast at 200 mA • 3.3 V config with external ballast at 300 mA	 4.95 4.9 4.85 3.2505 3.234 3.201	 5.0 5.0 5.0 3.3 3.3 3.3	 5.05 5.1 5.15 3.3495 3.366 3.399	V	 (8) (8)
I_{CCA_IN}	V_{CCA} Output Current (int. MOSFET)	–	–	100	mA	
I_{CCA_OUT}	V_{CCA} Output Current (external PNP)	–	–	300	mA	
$I_{CCA\_LIM\_INT}$	V_{CCA} Output Current Limitation (int. MOSFET)	100	–	675	mA	
$I_{CCA\_LIM\_OUT}$	V_{CCA} Output Current Limitation (external PNP)	300	–	675	mA	
$I_{CCA\_LIM\_FB}$	V_{CCA} Output Current Limitation Foldback	80	–	200	mA	
$V_{CCA\_LIM\_FB}$	V_{CCA} Output Voltage Foldback Threshold	0.5	–	1.1	V	
$V_{CCA\_LIM\_HYST}$	V_{CCA} Output Voltage Foldback Hysteresis	0.07	–	0.3	V	
$I_{CCA\_BASE\_SC}$	V_{CCA} Base Current Capability (internal pull-up)	–	20	30	mA	
$I_{CCA\_BASE\_SK}$	V_{CCA} Base Current Capability (Current sink)	20	65	–	mA	
T_{WARN_CCA}	V_{CCA} Thermal Warning Threshold (int. ballast only)	–	125	–	°C	
TSD_{CCA}	V_{CCA} Thermal Shutdown Threshold (int. ballast only)	160	–	–	°C	
TSD_{CCA_HYST}	V_{CCA} Thermal Shutdown Hysteresis	–	10	–	°C	(9)
$LORT_{VCCA}$	V_{CCA} Transient Load Regulation • I_{CCA} = 10 mA to 100 mA (internal MOSFET) • I_{CCA} = 10 mA to 300 mA (external ballast)	–	–	1.0	%	(9)

Notes

8. External PNP gain within 150 to 450
9. Guaranteed by design.

Table 4. Operating Range (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VAUX VOLTAGE REGULATOR						
V_{AUX_5}	V_{AUX} Output Voltage (5.0 V configuration)	4.85	5.0	5.15	V	
V_{AUX_33}	V_{AUX} Output Voltage (3.3 V configuration)	3.2	3.3	3.4	V	
V_{AUX_TRK}	V_{AUX} Tracking Error (V_{AUX_5} and V_{AUX_33})	-15	–	+15	mV	
I_{AUX_OUT}	V_{AUX} Output Current	–	–	300	mA	
I_{AUX_LIM}	V_{AUX} Output Current Limitation	300	–	700	mA	
$I_{AUX\_LIM\_FB}$	V_{AUX} Output Current Limitation Foldback	100	–	530	mA	
$V_{AUX\_LIM\_FB}$	V_{AUX} Output Voltage Foldback Threshold	0.5	–	1.1	V	
$V_{AUX\_LIM\_HYST}$	V_{AUX} Output Voltage Foldback Hysteresis	0.05	–	0.3	V	
$I_{AUX\_BASE\_SC}$ $I_{AUX\_BASE\_SK}$	V_{AUX} Base Current Capability	– 7.0	– –	-7.0 –	mA	
TSD_{AUX}	V_{AUX} Thermal Shutdown Threshold	160	–	–	°C	
TSD_{AUX_HYST}	V_{AUX} Thermal Shutdown Hysteresis	–	10	–	°C	(10)
LOR_{VAUX}	V_{AUX} Static Load Regulation (I_{AUX_OUT} = 10 to 300 mA)	–	15	–	mV	(10)
$LORT_{VAUX}$	V_{AUX} Transient Load Regulation • I_{AUX_OUT} = 10 mA to 300 mA	–	–	1.0	%	(10)
5V-CAN VOLTAGE REGULATOR						
V_{CAN}	V_{CAN} Output Voltage V_{SUP} > 6.0 V in Buck mode V_{SUP} > $V_{SUP\_UV\_L}$ in Boost mode	4.8	5.0	5.2	V	
I_{CAN_OUT}	V_{CAN} Output Current	–	–	100	mA	
I_{CAN_LIM}	V_{CAN} Output Current Limitation	100	–	250	mA	
TSD_{CAN}	V_{CAN} Thermal Shutdown Threshold	160	–	–	°C	
TSD_{CAN_HYST}	V_{CAN} Thermal Shutdown Hysteresis	–	10	–	°C	(10)
V_{CAN_UV}	V_{CAN} Undervoltage Detection Threshold	4.25	–	4.8	V	
$V_{CAN\_UV\_HYST}$	V_{CAN} Undervoltage Hysteresis	0.07	–	0.22	V	
V_{CAN_OV}	V_{CAN} Overvoltage Detection Threshold	5.2	–	5.55	V	
$V_{CAN\_OV\_HYST}$	V_{CAN} Overvoltage Hysteresis	0.07	–	0.22	V	
LOR_{VCAN}	V_{CAN} Load Regulation (from 0 to 50 mA)	–	100	–	mV	(10)

Notes
10. Guaranteed by design.

Table 4. Operating Range (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
FAIL-SAFE MACHINE VOLTAGE SUPERVISOR						
V_{PRE_OV}	V_{PRE} Overvoltage Detection Threshold	7.2	–	8.0	V	
$V_{PRE\_OV\_HYST}$	V_{PRE} Overvoltage Hysteresis	–	0.1	–	V	(11)
$V_{CORE\_FB\_UV}$	V_{CORE} FB Undervoltage Detection Threshold	0.67	–	0.773	V	
$V_{CORE\_FB\_UV\_D}$	V_{CORE} FB Undervoltage Detection Threshold - Degraded mode	0.45	–	0.58	V	
$V_{CORE\_FB\_UV\_HYST}$	V_{CORE} FB Undervoltage Hysteresis	10	–	27	mV	(11)
$V_{CORE\_FB\_OV}$	V_{CORE} FB Overvoltage Detection Threshold	0.84	–	0.905	V	
$V_{CORE\_FB\_OV\_HYST}$	V_{CORE} FB Overvoltage Hysteresis	10	–	30	mV	(11)
I_{PD_CORE}	V_{CORE} Internal Pull-down Current	5.0	12	25	mA	
$V_{CCA\_UV\_5}$	V_{CCA} Undervoltage Detection Threshold (5.0 V config)	4.5	–	4.75	V	
$V_{CCA\_UV\_5D}$	V_{CCA} Undervoltage Detection Threshold (Degraded 5.0 V)	3.0	–	3.2	V	
$V_{CCA\_UV\_33}$	V_{CCA} Undervoltage Detection Threshold (3.3 V config)	3.0	–	3.2	V	
$V_{CCA\_UV\_HYST}$	V_{CCA} Undervoltage Hysteresis	–	0.07	–	V	(11)
$V_{CCA\_OV\_5}$	V_{CCA} Overvoltage Detection Threshold (5.0 V config)	5.25	–	5.5	V	
$V_{CCA\_OV\_33}$	V_{CCA} Overvoltage Detection Threshold (3.3 V config)	3.4	–	3.6	V	
$V_{CCA\_OV\_HYST}$	V_{CCA} Overvoltage Hysteresis	–	0.15	–	V	(11)
R_{PD_CCA}	V_{CCA} Internal Pull-down Resistor (enabled when V_{CCA} is switched off)	50	–	160	Ω	
$V_{AUX\_UV\_5}$	V_{AUX} Undervoltage Detection Threshold (5.0 V config)	4.5	–	4.75	V	
$V_{AUX\_UV\_5D}$	V_{AUX} Undervoltage Detection Threshold (Degraded 5.0 V)	3.0	–	3.2	V	
$V_{AUX\_UV\_33}$	V_{AUX} Undervoltage Detection Threshold (3.3 V config)	3.0	–	3.2	V	
$V_{AUX\_UV\_HYST}$	V_{AUX} Undervoltage Hysteresis	–	0.07	–	V	(11)
$V_{AUX\_OV\_5}$	V_{AUX} Overvoltage Detection Threshold (5.0 V config)	5.25	–	5.5	V	
$V_{AUX\_OV\_33}$	V_{AUX} Overvoltage Detection Threshold (3.3 V config)	3.4	–	3.6	V	
$V_{AUX\_OV\_HYST}$	V_{AUX} Overvoltage Hysteresis	–	0.07	–	V	(11)
R_{PD_AUX}	V_{AUX} Internal Pull-down Resistor	50	–	170	Ω	

Notes

11. Guaranteed by design.

Table 4. Operating Range (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
FAIL-SAFE OUTPUTS						
V_{RSTB_OL}	Reset Low Output Level (I_RSTB = 2.0 mA and 2.0 V < V_{SUP} < 40 V)	–	–	0.5	V	(12)
I_{RSTB_LIM}	Reset Output Current Limitation	12	–	25	mA	
V_{RSTB_IL}	External Reset Detection Threshold (falling)	1.0	–		V	
V_{RSTB_IH}	External Reset Detection Threshold (rising)	–	–	2.0	V	
$V_{RSTB\_IN\_HYST}$	External Reset Input Hysteresis	0.2	–	–	V	
V_{FS0B_OL}	FS0B low Output Level (I_FS0b = 2.0 mA)	–	–	0.5	V	
I_{FS0B_LK}	FS0B Input Current Leakage (V_{FS0B} = 28 V)	–	–	1.0	µA	
I_{FS0B_LIM}	FS0B Output Current Limitation	6.0	–	12	mA	
MULTI-PURPOSE IOS						
ANALOG INPUT						
$V_{IO\_ANA\_WD}$	Measurable Input Voltage (wide range)	3.0	–	19	V	
$V_{IO\_ANA\_TG}$	Measurable Input Voltage (tight range)	3.0	–	9.0	V	
$I_{IO\_IN\_ANA}$	Input Current	–	–	100	µA	
DIGITAL INPUT						
V_{IO_IH}	High Input Voltage Detection Threshold (IO_0:1, IO_4:5) • Min Limit = 2.7 V at V_{SUP} = 40 V	2.6	–	–	V	
V_{IO23_IH}	High Input Voltage Detection Threshold (IO_2, IO_3)	2.0	–	–	V	
V_{IO_IL}	Digital Low Input Level (IO_0:1; IO_4:5)	–	–	2.1	V	
V_{IO_HYST}	Input Voltage Hysteresis (IO_0:1, IO_4:5)	50	120	500	mV	(13)
V_{IO23_IL}	Digital Low Input Level (IO_2, IO_3)	–	–	0.9	V	
V_{IO23_HYST}	Input Voltage Hysteresis (IO_2, IO_3)	200	450	700	mV	(13)
$I_{IO\_IN\_0:1}$	Input Current for IO_0:1	-5.0	–	100	µA	
$I_{IO\_IN\_2:5}$	Input Current for IO_2:5	-5.0	–	5.0	µA	
$I_{IO\_IN\_LPOFF}$	Input Current for IO_0:5 in LPOFF	-1.0	–	1.0	µA	
OUTPUT GATE DRIVER						
V_{IO_OH}	High Output Level at I_{IO_OUT} = -2.5 mA	V_{PRE} - 1.5	–	V_{PRE}	V	
V_{IO_OL}	Low Output Level at I_{IO_OUT} = +2.5 mA	0.0	–	1.0	V	
$V_{IO\_OUT\_SK}$ $V_{IO\_OUT\_SC}$	Output Current Capability	2.5 –	– –	– -2.5	mA	

Notes

12. For V_{SUP} < 2.0 V, all supplies are already off and external pull-up on RSTB (e.g V_{CORE} or V_{CCA}) pulls the line down.
13. Guaranteed by design.

Table 4. Operating Range (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
ANALOG MULTIPLEXER						
V_{AMUX_ACC}	Voltage Sense Accuracy (V_{SNS}, IO_0, IO_1) using 5.1 kΩ resistor	-5.0	–	5.0	%	(14)
$V_{AMUX\_WD\_5}$	Divider Ratio (wide input voltage range) at V_{DDIO} = 5.0 V	–	5.0	–		
$V_{AMUX\_WD\_3P3}$	Divider Ratio (wide input voltage range) at V_{DDIO} = 3.3 V	–	7.0	–		
$V_{AMUX\_TG\_5}$	Divider Ratio (tight input voltage range) at V_{DDIO} = 5.0 V	–	2.0	–		
$V_{AMUX\_TG\_3P3}$	Divider Ratio (tight input voltage range) at V_{DDIO} = 3.3 V	–	3.0	–		
V_{AMUX_REF1}	Internal Voltage Reference with 6.0 V < V_{SUP} < 19 V	2.475	2.5	2.525	V	
V_{AMUX_REF2}	Internal Voltage Reference with $V_{SUP} \leq$ 6.0 V or $V_{SUP} \geq$ 19 V	2.468	2.5	2.532	V	
$V_{AMUX\_TP\_CO}$	Internal Temperature Sensor Coefficient	–	9.9	–	mV/°C	
V_{AMUX_TP}	Temperature Sensor mux_output Voltage (at T_J = 165 °C)	2.08	2.15	2.22	V	(15)
INTERRUPT						
V_{INTB_OL}	Low output level (I_{INT} = 2.5mA)	–	–	0.5	V	
R_{PU_INT}	Internal pull-up resistor (connected to VDDIO)	–	10	–	KΩ	
I_{INT_LK}	Input leakage current	–	–	1	µA	
CAN TRANSCEIVER						
CAN LOGIC INPUT PIN (TXD)						
V_{TXD_IH}	TXD High Input Threshold	0.7 x V_{DDIO}	–	–	V	
V_{TXD_IL}	TXD Low Input Threshold	–	–	0.3 x V_{DDIO}	V	
$TXD_{PULL-UP}$	TXD Main Device Pull-up	20	33	50	KΩ	
TXD_{LK}	TXD Input Leakage Current, V_{TXD} = V_{DDIO}	-1.0	–	1.0	µA	
CAN LOGIC OUTPUT PIN (RXD)						
V_{RXD_OL1}	Low Level Output Voltage (I_{RXD} = 250 µA)	–	–	0.4	V	
V_{RXD_OL2}	Low Level Output Voltage (I_{RXD} = 1.5 mA)	–	–	0.9	V	
$VOUT_{HIGH}$	High Level Output Voltage (I_{RXD} = -250 µA, V_{DDIO} = 3.0 V to 5.5 V)	V_{DDIO} - 0.4V	–	–	V	

Notes

14. If a higher resistor value than recommended is used, the accuracy degrades.
15. Guaranteed by design.

Table 4. Operating Range (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
CAN OUTPUT PINS (CANH, CANL)						
DIFF_COM_MODE	Differential Input Comparator Common Mode Range	-12	–	12	V	
$V_{IN\_DIFF\_SLEEP}$	Differential Input Voltage Threshold in Sleep Mode	0.5	–	0.9	V	
V_{IN_HYST}	Differential Input Hysteresis (in Tx, Rx mode)	50	–	–	mV	
R_{IN_CHCL}	CANH, CANL Input Resistance	5.0	–	50	kΩ	
R_{IN_DIFF}	CAN Differential Input Resistance	10	–	100	kΩ	
R_{IN_MATCH}	Input Resistance Matching	-3.0	–	3.0	%	
V_{CANH}	CANH Output Voltage (45 Ω < R_{BUS} < 65 Ω) • TX dominant state • TX recessive state	 2.75 2.0	 – 2.5	 4.5 3.0	V	
V_{CANL}	CANL Output Voltage (45 Ω < R_{BUS} < 65 Ω) • TX dominant state • TX recessive state	 0.5 2.0	 – 2.5	 2.25 3.0	V	
V_{OH}-V_{OL}	Differential Output Voltage • TX dominant state (45 Ω < R_{BUS} < 65 Ω) • TX recessive state	 1.5 -50	 2.0 0.0	 3.0 50	 V mV	
$I_{CANL\text{-}SK}$	CANL Sink Current Under Short-circuit Condition (V_{CANL} ≤ 12 V, CANL driver ON, TXD low)	40	–	100	mA	
$I_{CANH\text{-}SC}$	CANH Source Current Under Short-circuit Condition (V_{CANH} = -2.0 V, CANH driver ON, TXD low)	-100	–	-40	mA	
$R_{INSLEEP}$	CANH, CANL Input Resistance Device Supplied and in CAN Sleep Mode	5.0	–	50	kΩ	
V_{CANLP}	CANL, CANH Output Voltage in Sleep Modes. No Termination load.	-0.1	0.0	0.1	V	
I_{CAN}	CANH, CANL Input Current, Device Unsupplied, V_{SUP} and V_{IO} connected to GND • V_{CANH}, V_{CANL} = 5.0 V	 -10	 –	 10	µA	
T_{OT}	Overtemperature Detection	160	–	–	°C	
T_{HYST}	Overtemperature Hysteresis	-10	–	+20	°C	
DIGITAL INTERFACE						
$MISO_H$	High Output Level on MISO (I_{MISO} = 1.5 mA)	V_{DDIO} - 0.4	–	–	V	
$MISO_L$	Low Output Level on MISO (I_{MISO} = 2.0 mA)	–	–	0.4	V	
I_{MISO}	Tri-state Leakage Current (V_{DDIO} = 5.0 V)	-5.0	–	5.0	µA	
V_{DDIO}	Supply Voltage for MISO Output Buffer	3.0	–	5.5	V	
SPI_{LK}	SCLK,NCS,MOSI Input Current	-1.0	–	1.0	µA	
V_{SPI_IH}	SCLK,NCS,MOSI High Input Threshold	2.0	–	–	V	
V_{SPI_IL}	SCLK,NCS,MOSI Low Input Threshold	–	–	0.8	V	
R_{SPI}	NCS,MOSI Internal Pull-up (pull-up to VDDIO)	200	400	800	KΩ	

Table 4. Operating Range (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
DEBUG						
V_{DEBUG_IL}	Low Input Voltage Threshold	2.1	2.35	2.6	V	
V_{DEBUG_IH}	High Input Voltage Threshold	4.35	4.6	4.97	V	
I_{DEBUG_LK}	Input Leakage Current	-10	–	10	µA	

4.3 Dynamic Electrical Characteristics

Table 5. Dynamic Electrical Characteristics

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
DIGITAL INTERFACE TIMING						
f_{SPI}	SPI Operation Frequency (50% DC)	0.5	–	8.0	MHz	
t_{MISO_TRANS}	MISO Transition Speed, 20 - 80% • V_{DDIO} = 5.0 V, C_{LOAD} = 50 pF • V_{DDIO} = 5.0 V, C_{LOAD} = 150 pF	 5.0 5.0	 – –	 30 50	ns	
t_{CLH}	Minimum Time SCLK = HIGH	62	–	-	ns	
t_{CLL}	Minimum Time SCLK = LOW	62	–	-	ns	
t_{PCLD}	Propagation Delay (SCLK to data at 10% of MISO rising edge)	–	–	30	ns	
t_{CSDV}	NCS = LOW to Data at MISO Active	–	–	75	ns	
t_{SCLCH}	SCLK Low Before NCS Low (setup time SCLK to NCS change H/L)	75	–	–	ns	
t_{HCLCL}	SCLK Change L/H after NCS = low	75	–	–	ns	
t_{SCLD}	SDI Input Setup Time (SCLK change H/L after MOSI data valid)	40	–	–	ns	
t_{HCLD}	SDI Input Hold Time (MOSI data hold after SCLK change H/L)	40	–	–	ns	
t_{SCLCL}	SCLK Low Before NCS High	100	–	–	ns	
t_{HCLCH}	SCLK High After NCS High	100	–	–	ns	
t_{PCHD}	NCS L/H to MISO at High-impedance	–	–	75	ns	
t_{ONNCS}	NCS Min. High Time	500	–	–	ns	
t_{NCS_MIN}	NCS Filter Time	10	–	40	ns	

Table 5. Dynamic Electrical Characteristics (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes

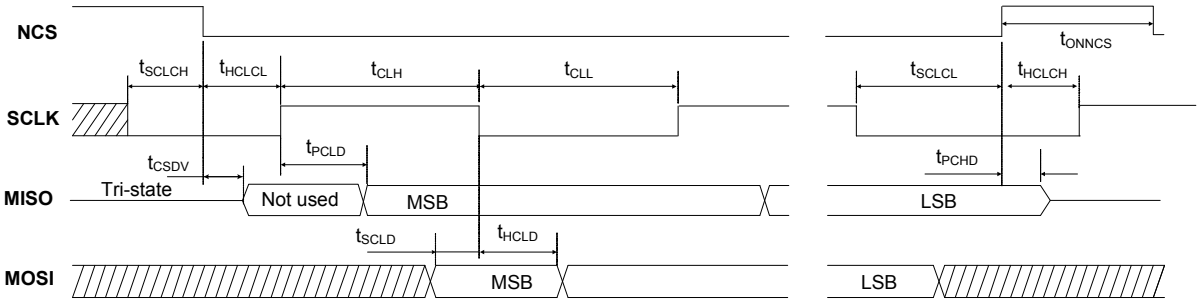

Figure 5. SPI Timing Diagram

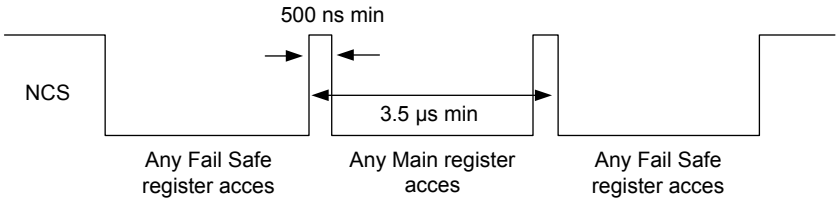

Figure 6. Register Access Restriction

Table 5. Dynamic Electrical Characteristics (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
CAN DYNAMIC CHARACTERISTICS						
t_{DOUT}	TXD Dominant State Timeout	0.8	–	5.0	ms	
t_{DOM}	Bus Dominant Clamping Detection	0.8	–	5.0	ms	
t_{LOOP}	Propagation Loop Delay TXD to RXD • R_{LOAD} = 120 Ω, C between CANH and CANL = 100 pF, C at RxD < 15 pF	–	–	255	ns	
t_{1PWU}	Single Pulse Wake-up Time	0.5	–	5.0	µs	
t_{3PWU}	Multiple Pulse Wake-up Time	0.5	–	1.0	µs	
t_{3PTO1}	Multiple Pulse Wake-up Timeout (120 µs bit selection)	110	120	–	µs	
t_{3PTO2}	Multiple Pulse Wake-up Timeout (360µs bit selection)	350	360	–	µs	
t_{CAN_READY}	Delay to enable CAN by SPI Command (NCS rising edge) to CAN to Transmit (device in normal mode and CAN interface in TxRx mode)	–	–	100	µs	(16)
FAIL-SAFE STATE MACHINE						
OSC_{FSSM}	Oscillator	400	–	500	kHz	
CLK_{FS_MIN}	Fail-safe Oscillator Monitoring	150	–	–	kHz	
t_{IC_ERR}	IO_0:5 Filter Time	4.0	–	20	µs	
t_{ACK_FS}	Acknowledgement Counter (used for IC error handling IO_1 and IO_5)	7.0	–	9.7	ms	
T_DFS_recovery	IO_0 filter time to recover from deep reset and fail state	0.8	–	1.3	ms	
FAIL-SAFE OUTPUT						
t_{RSTB_FB}	RSTB feedback filter time	8.0	–	15	µs	
t_{FSOB_FB}	FS0B feedback filter time	8.0	–	15	µs	
t_{RSTB_BLK}	RSTB feedback blanking time	180	–	320	µs	
t_{FSOB_BLK}	FS0B feedback blanking time	180	–	320	µs	
t_{RSTB_POR}	Reset delay time (after a Power On Reset or from LPOFF)	12	15.9	23.6	ms	
t_{RSTB_LG}	Reset duration (long pulse)	8.0	–	10	ms	
t_{RSTB_ST}	Reset duration (short pulse)	1.0	–	1.3	ms	
t_{RSTB_IN}	External Reset delay time	8.0	–	15	µs	
$T_{\_FS\_FB}$	RSTB, FS0B Feedback Filter Time	8.0	–	15	µs	
$T_{\_DIAG\_SC}$	Fail-safe Output Diagnostic Counter (FS0B)	550	–	800	µs	
VSUP VOLTAGE SUPPLY						
DV_{SUP}/DT	Supply Voltage Slew Rate	-2.0	–	2.0	V/µs	

Notes

16. For proper CAN operation, TXD must be set to high level before CAN being enabled by SPI, and must remain high for at least T_{CAN_READY}

Table 5. Dynamic Electrical Characteristics (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{PRE} VOLTAGE PRE-REGULATOR						
f_{SW_PRE}	V_{PRE} Switching Frequency	418	440	462	kHz	
t_{SW_PRE}	V_{SW_PRE} On and Off Switching Time	–	–	30	ns	(17)
t_{PRE_SOFT}	V_{PRE} Soft Start Duration ($C_{OUT} \leq$ 100 µF)	500	–	700	µs	
$t_{PRE\_BLK\_LIM}$	V_{PRE} Current Limitation Blanking Time	200	–	600	ns	
t_{IPRE_OC}	V_{PRE} Overcurrent Filtering Time	30	–	120	ns	(17)
t_{PRE_UV}	V_{PRE} Undervoltage Filtering Time	20	–	40	µs	
$t_{PRE\_UV\_4p3}$	Vpre Shut-off Filtering Time	3.0	–	6.0	µs	
$d_{IPRE/DT}$	V_{PRE} Load Regulation Variation	–	–	25	A/ms	(17)
t_{PRE_WARN}	V_{PRE} Thermal Warning Filtering Time	30	–	40	µs	
t_{PRE_TSD}	V_{PRE} Thermal Detection Filtering Time	1.3	–	–	µs	
t_{VSUP_IPFF}	I_{PFF} Input Voltage Filtering Time	1.0	–	4.0	µs	
t_{IPRE_IPFF}	I_{PFF} High Side Peak Current Filter Time	100	–	300	ns	
$t_{LS\_RISE/FALL}$	LS Gate Voltage Switching Time (I_{OUT} = 300 mA)	–	–	50	ns	
V_{SENSE} VOLTAGE REGULATOR						
t_{VSNS_UV}	V_{SNS} Undervoltage Filtering Time	1.0	–	3.0	µs	
V_{CORE} VOLTAGE REGULATOR						
$t_{CORE\_BLK\_LIM}$	V_{CORE} Current Limitation Blanking Time	20	–	40	ns	
f_{SW_CORE}	V_{CORE} Switching Frequency	2.28	2.4	2.52	MHz	
t_{SW_CORE}	V_{SW_CORE} On and Off Switching Time	6.0	–	12	ns	
V_{CORE_SOFT}	V_{CORE} Soft Start (C_{OUT} = 100 µF max)	–	–	10	V/ms	
t_{CORE_WARN}	V_{CORE} Thermal Warning Filtering Time	30	–	40	µs	
t_{CORE_TSD}	V_{CORE} Thermal Detection Filtering Time	0.5	–	–	µs	
V_{CCA} VOLTAGE REGULATOR						
t_{CCA_LIM}	V_{CCA} Output Current Limitation Filter Time	1.0	–	3.0	µs	
$t_{CCA\_LIM\_OFF1}$ $t_{CCA\_LIM\_OFF2}$	V_{CCA} Output Current Limitation Duration	10 50	– –	– –	ms	
t_{CCA_WARN}	V_{CCA} Thermal Warning Filtering Time	30	–	40	µs	
t_{CCA_TSD}	V_{CCA} Thermal Detection Filter Time (int. MOSFET)	1.5	–	–	µs	
dI_{LOAD}/dt	V_{CCA} Load Transient	–	2.0	–	A/ms	(17)
V_{CCA_SOFT}	V_{CCA} Soft Start (5.0 V and 3.3 V)	–	–	50	V/ms	

Notes

17. Guaranteed by characterization.

Table 5. Dynamic Electrical Characteristics (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{AUX} VOLTAGE REGULATOR						
t_{AUX_LIM}	V_{AUX} Output Current Limitation Filter Time	1.0	–	3.0	µs	
$t_{AUX\_LIM\_OFF1}$ $t_{AUX\_LIM\_OFF2}$	V_{AUX} Output Current Limitation Duration	10 50	– –	– –	ms	
t_{AUX_TSD}	V_{AUX} Thermal Detection Filter Time	1.5	–	–	µs	
dI_{AUX}/dt	V_{AUX} Load Transient	–	2.0	–	A/ms	(18)
V_{AUX_SOFT}	V_{AUX} Soft Start (5.0 V and 3.3 V)	–	–	50	V/ms	
5V-CAN VOLTAGE REGULATOR						
t_{CAN_LIM}	Output Current Limitation Filter Time	2.0	–	4.0	µs	
t_{CAN_TSD}	V_{CAN} Thermal Detection Filter Time	1.0	–	–	µs	
t_{CAN_UV}	V_{CAN} Undervoltage Filtering Time	4.0	–	6.0	µs	
t_{CAN_OV}	V_{CAN} Overvoltage Filtering Time	100	–	200	µs	
dI_{CAN}/dt	V_{CAN} Load Transient	–	100	–	A/ms	(18)
FAIL-SAFE MACHINE VOLTAGE SUPERVISOR						
t_{PRE_OV}	V_{PRE} Overvoltage Filtering Time	128	–	234	µs	
t_{CORE_UV}	V_{CORE} FB Undervoltage Filtering Time	4.0	–	10	µs	
t_{CORE_OV}	V_{CORE} FB Overvoltage Filtering Time	128	–	234	µs	
t_{CCA_UV}	V_{CCA} Undervoltage Filtering Time	4.0	–	10	µs	
t_{CCA_OV}	V_{CCA} Overvoltage Filtering Time	128	–	234	µs	
t_{AUX_UV}	V_{AUX} Undervoltage Filtering Time	4.0	–	10	µs	
t_{AUX_OV}	V_{AUX} Overvoltage Filtering Time	128	–	234	µs	
MULTI-PURPOSE IOS						
DIGITAL INPUT						
F_{IO_IN}	Digital Input Frequency Range	0.0	–	100	kHz	
ANALOG MULTIPLEXER						
t_{MUX_READY}	SPI Selection to Data Ready to be Sampled on Mux_out • V_{DDIO} = 5.0 V, C_{MUX_OUT} = 1.0 nF	–	–	10	µs	
INTERRUPT						
t_{INTB_LG}	INTB Pulse Duration (long)	100	–	–	µs	
t_{INTB_ST}	INTB Pulse Duration (short)	25	–	–	µs	
FUNCTIONAL SATE MACHINE						
t_{WU_GEN}	General Wake-up Signal Deglitch Time (for IO wu signal)	50	70	90	µs	

Notes

18. Guaranteed by characterization.

5 Functional Description

5.1 Introduction

The 33907_8 is the third generation of the System Basis Chip, combining:

- High efficiency switching voltage regulator for MCU, and linear voltage regulators for integrated CAN interface, external ICs such as sensors, and accurate reference voltage for A to D converters.
- Built in enhanced high speed CAN interface (ISO11898-2 and -5), with local and bus failure diagnostic, Protection and Fail-safe operation mode.
- Low power mode, with ultra low current consumption.
- Various wake-up capabilities
- Enhanced safety features with multiple fail-safe outputs and scheme.

5.2 Functional Pin Description

5.2.1 Power Supply(VSUP1, VSUP2, VSUP3)

VSUP1 and VSUP2 are the inputs pins for internal supply dedicated to SMPS regulators. VSUP3 is the input pin for internal voltage reference. VSUP1, 2, and 3 are robust against ISO7637 pulses.

5.2.2 VSENSE Input (VSENSE)

This pin must be connected to the battery line (before the reverse battery protection diode), via a serial resistor. It incorporates a threshold detector to sense the battery voltage, and provide a battery early warning. It also includes a resistor divider to measure the VSENSE voltage via the MUX-OUT pin. VSENSE pin is robust against ISO7637 pulse.

5.2.3 VCORE Output (1.2 V, 3.3 V)

On 33907 and 33908 product versions, the VCORE block is an SMPS regulator. The main difference between both versions is the current capability of the V_{CORE} regulator.

On 33907 and 33908 product versions, the voltage regulator is a step down DC-DC converter operating in voltage control mode. The output voltage is selectable (1.2 V or 3.3 V) through an external resistor divider connected between V_{CORE} and the feedback pin (FB_Core) (Figure 1). The stability of the converter is done externally, by using the COMP_Core pin.

5.2.4 VAUX OUTPUT, 5.0 V, 3.3 V Selectable

The VAUX pin provides an auxiliary output voltage (5.0 V, 3.3 V) selectable through an external resistor connected to SELECT pin. It uses an external PNP ballast transistor for flexibility and power dissipation constraints.

The VAUX output voltage regulator can be used as “sensor supply” (external ECU supply) or “auxiliary supply” (local ECU supply).

Overcurrent, overvoltage, and undervoltage detectors are provided.

V_{AUX} can be turned ON or OFF (if not configured as safety critical) via a SPI command. V_{AUX} overcurrent and overvoltage information disables V_{AUX}, reported in the dedicated register, and generates an Interrupt.

V_{AUX} is enabled by default.