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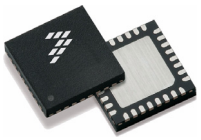
22 channel multiple switch detection interface with programmable wetting current

33978
34978

MULTIPLE SWITCH DETECTION INTERFACE

EK SUFFIX (PB-FREE)
98ASA10556D
32-PIN SOICW-EP



ES SUFFIX (PB-FREE)
98ASA00656D
32-PIN QFN (WF-TYPE)

The 33978 is designed to detect the closing and opening of up to 22 switch contacts. The switch status, either open or closed, is transferred to the microprocessor unit (MCU) through a serial peripheral interface (SPI). This SMARTMOS device also features a 24-to-1 analog multiplexer for reading the input channels as analog inputs. The analog selected input signal is buffered and provided on the AMUX output pin for the MCU to read.

Independent programmable wetting currents are available as needed for the application. A battery and temperature monitor are included in the IC and available via the AMUX pin.

The 33978 device has two modes of operation, Normal and Low-power mode (LPM). Normal mode allows programming of the device and supplies switch contacts with pull-up or pull-down current as it monitors the change of state on the switches. The LPM provides low quiescent current, which makes the 33978 ideal for automotive and industrial products requiring low sleep-state currents.

Features

- Fully functional operation 4.5 V ≤ V_{BATP} ≤ 36 V
- Full parametric operation 6.0 V ≤ V_{BATP} ≤ 28 V
- Operating switch input voltage range from -1.0 V to 36 V
- Eight programmable inputs (switches to battery or ground)
- 14 switch-to-ground inputs
- Selectable wetting current (2, 6, 8, 10, 12, 14, 16, or 20 mA)
- Interfaces directly to an MCU using 3.3 V / 5.0 V SPI protocol
- Selectable wake-up on change of state
- Typical standby current I_{BATP} = 30 µA and I_{DDQ} = 10 µA
- Active interrupt (INT_B) on change-of-switch state
- Integrated battery and temperature sensing

Applications

- Automotive
  - Heating ventilation and air conditioning (HVAC)
  - Lighting
  - Central gateway/in-vehicle networking
  - Gasoline engine management
- Industrial
  - Programmable logic control (PLC)
  - Process control, temperature control
  - Input-output control (I/O Control)
  - Single board computer
  - Ethernet switch

Notes

1. The IC is functional from 4.5 V < V_{BATP} < 6.0 V, but with degraded parametric values. The parameters may not meet the minimum and maximum specifications when VBATP drops below 6.0 V.

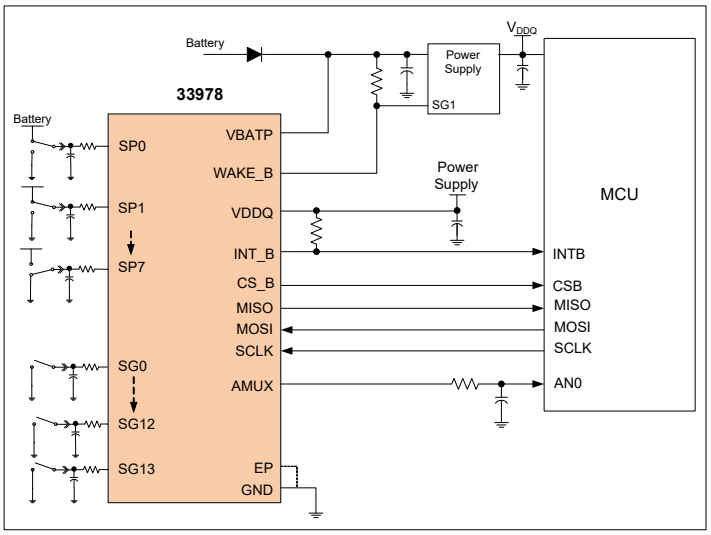


Figure 1. 33978 simplified application diagram

Table of Contents

1 Orderable parts . . . 3
2 Internal block diagram . . . 4
3 Pin connections . . . 5
3.1 Pinout . . . 5
3.2 Pin definitions . . . 5
4 General product characteristics . . . 7
4.1 Maximum ratings . . . 7
4.2 Thermal characteristics . . . 8
4.3 Operating conditions . . . 9
4.4 Electrical characteristics . . . 9
5 General description . . . 17
5.1 Features . . . 17
5.2 Functional block diagram . . . 18
6 General IC functional description . . . 19
6.1 Battery voltage ranges . . . 19
6.2 Power sequencing conditions . . . 20
7 Functional block description . . . 21
7.1 State diagram . . . 21
7.2 Low-power mode operation . . . 22
7.3 Input functional block . . . 24
7.4 Oscillator and timer control functional block . . . 26
7.5 Temperature monitor and control functional block . . . 26
7.6 WAKE_B control functional block . . . 26
7.7 INT_B functional block . . . 27
7.8 AMUX functional block . . . 27
7.9 Serial peripheral interface (SPI) . . . 28
7.10 SPI control register definition . . . 31
8 Typical applications . . . 53
8.1 Application diagram . . . 53
8.2 Bill of materials . . . 53
8.3 Abnormal operation . . . 54
9 Packaging . . . 55
9.1 Package mechanical dimensions . . . 55
10 Reference section . . . 62
11 Revision history . . . 63

1 Orderable parts

This section describes the part numbers available to be purchased along with their differences.

Table 1. Orderable part variations

Part number	Temperature (T_A)	Package	Notes
MC33978EK	-40 °C to 125 °C	SOICW-EP 32 pins	(2), (3)
MC33978AEK			(2)
MC33978AES		QFN (WF-TYPE) 32 pins	
MC34978EK	-40 °C to 105 °C	SOICW-EP 32 pins	(2), (3)
MC34978AEK			(2)
MC34978AES		QFN (WF-TYPE) 32 pins	

Notes

2. To order parts in tape and reel, add the R2 suffix to the part number.
3. Refer to errata MC33978ER ER01 for details on current conditions present on the MC33978EK and MC34978EK devices only.

2 Internal block diagram

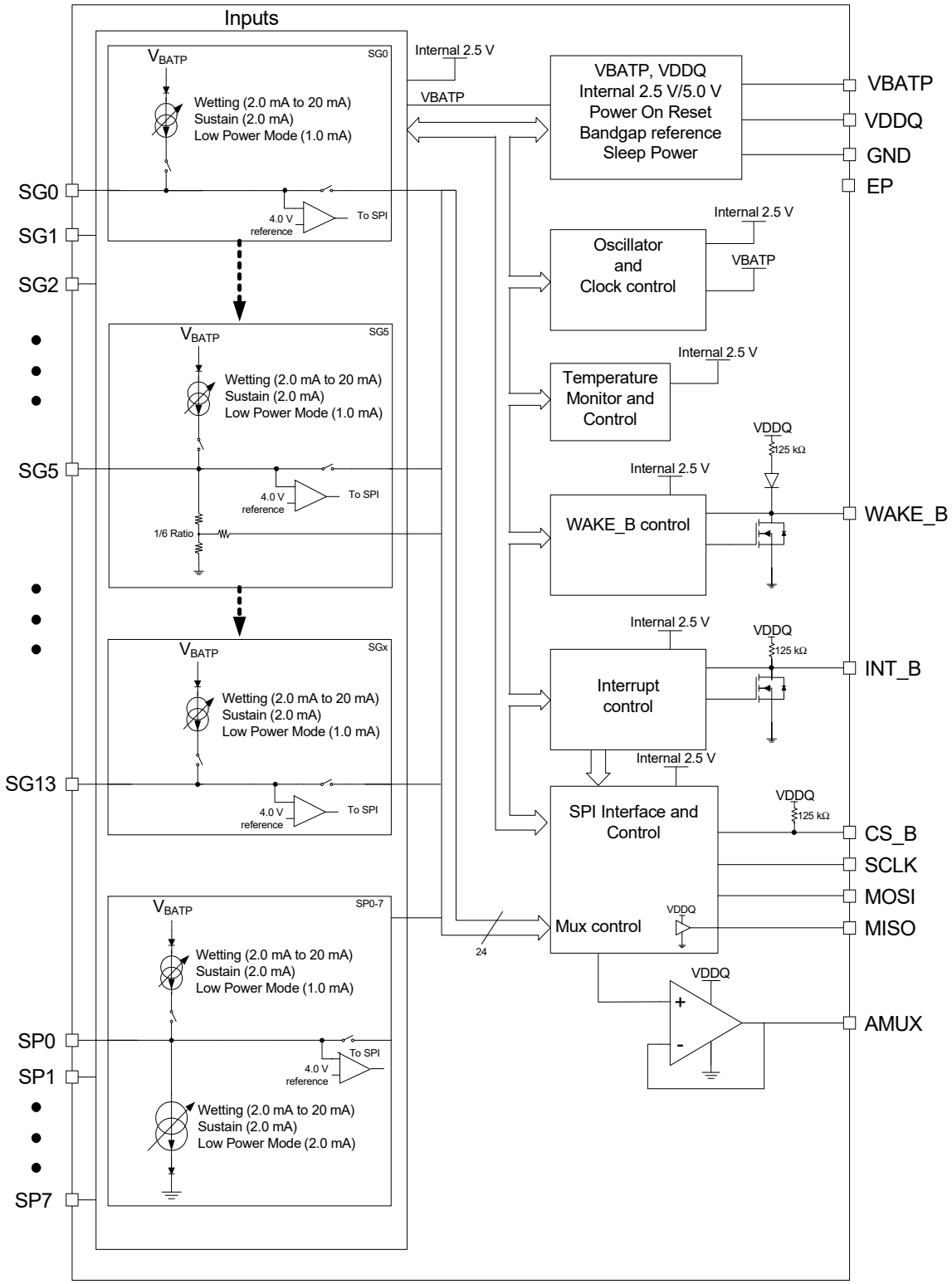


Figure 2. 33978 internal block diagram

3 Pin connections

3.1 Pinout

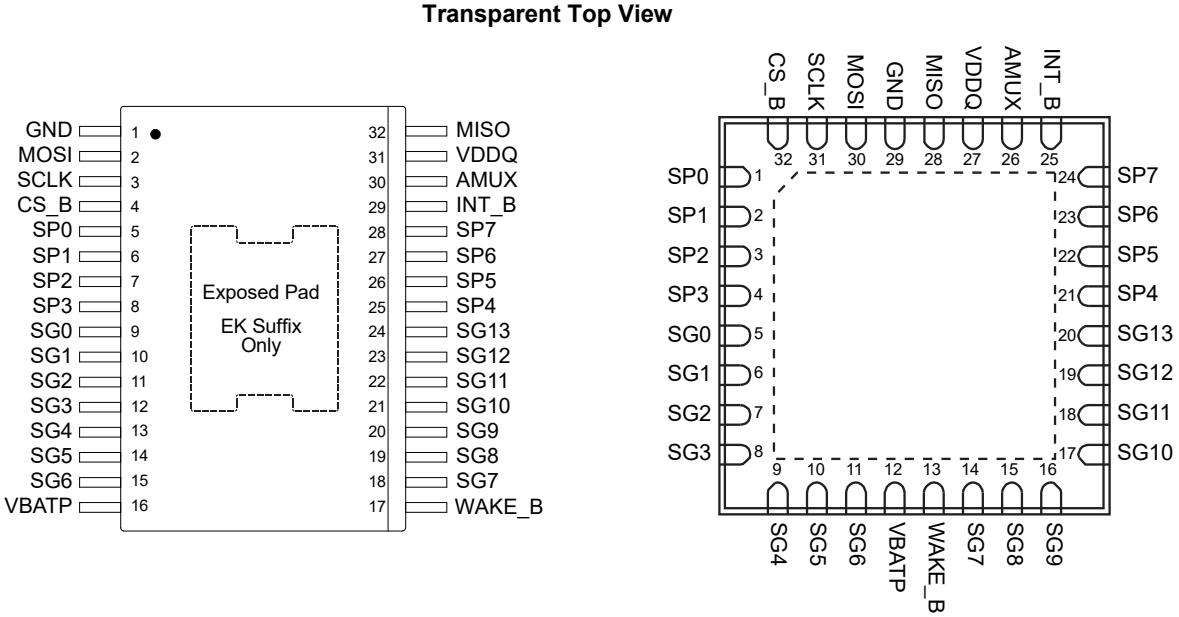


Figure 3. 33978 SOICW-EP and QFN (WF-Type) pinouts

3.2 Pin definitions

Table 2. 33978 pin definitions

Pin number SOIC	Pin number QFN	Pin name	Pin function	Formal name	Definition
1	29	GND	Ground	Ground	Ground for logic, analog
2	30	MOSI	Input/SPI	SPI Slave In	SPI control data input pin from the MCU
3	31	SCLK	Input/SPI	Serial Clock	SPI control clock input pin
4	32	CS_B	Input/SPI	Chip Select	SPI control chip select input pin
5–8 25–28	1 - 4 21 - 24	SP0–3 SP4–7	Input	Programmable Switches 0–7	Switch to programmable input pins (SB or SG)
9–15, 18–24	5 - 11 14 - 20	SG0–6, SG7–13	Input	Switch-to-Ground Inputs 0–13	Switch-to-ground input pins
16	12	VBATP	Power	Battery Input	Battery supply input pin. Pin requires external reverse battery protection
17	13	WAKE_B	Input/Output	Wake-up	Open drain wake-up output. Designed to control a power supply enable pin. Input used to allow a wake-up from an external event.
29	25	INT_B	Input/Output	Interrupt	Open-drain output to MCU. Used to indicate an input switch change of state. Used as an input to allow wake-up from LPM via an external INT_B falling event.
30	26	AMUX	Output	Analog Multiplex Output	Analog multiplex output.
31	27	VDDQ	Input	Voltage Drain Supply	3.3 V/5.0 V supply. Sets SPI communication level for the MISO driver and I/O level buffer

Table 2. 33978 pin definitions (continued)

Pin number SOIC	Pin number QFN	Pin name	Pin function	Formal name	Definition
32	28	MISO	Output/SPI	SPI Slave Out	Provides digital data from the 33978 to the MCU.
		EP	Ground	Exposed Pad	It is recommended that the exposed pad is terminated to GND (pin 1) and system ground.

4 General product characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min.	Max.	Unit	Notes
Electrical ratings					
VBATP	Battery Voltage	-0.3	40	V	
VDDQ	Supply Voltage	-0.3	7.0	V	
CS_B, MOSI, MISO, SCLK	SPI Inputs/Outputs	-0.3	7.0	V	
SGx, SPx	Switch Input Range	-14[4]	38	V	
AMUX	AMUX	-0.3	7.0	V	
INT_B	INT_B	-0.3	7.0	V	
WAKE_B	WAKE_B	-0.3	40	V	
V_{ESD1-2} V_{ESD1-3} V_{ESD3-1} V_{ESD2-1} V_{ESD2-2}	ESD Voltage • Human Body Model (HBM) (VBATP versus GND) MC33978 and MC34978 MC33978A and MC34978A • Human Body Model (HBM) (All other pins) • Machine Model (MM) • Charge Device Model (CDM) (Corners pins) • Charge Device Model (CDM) (All other pins)		 ±2000 ±4000 ±2000 ±200 ±750 ±500	V	(5)
V_{ESD5-3} V_{ESD5-4} V_{ESD6-1} V_{ESD6-2}	Contact Discharge • VBATP[8] • WAKE_B (series resistor 10 kΩ) • SGx and SPx pins with 100 nF capacitor (100 Ω series R) based on external protection performance[7] • SGx and SPx pins with 100 nF capacitor (50 Ω series R)		 ±8000 ±8000 ±15000 ±8000	V	(6)

Notes

4. Minimum value of -18 V is guaranteed by design for switch input voltage range (SGx, SPx).
5. ESD testing is performed in accordance AEC Q100, with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model (CDM).
6. C_{ZAP} = 330 pF, R_{ZAP} = 2.0 kΩ (Powered and unpowered) / C_{ZAP} = 150 pF, R_{ZAP} = 330 Ω (Unpowered)
7. ±15000V capability in powered condition, ±8000V in all other conditions.
8. External component requirements at system level:
   C_{bulk} = 100uF aluminum electrolytic capacitor
   C_{bypass}= 100nF ±37 % ceramic capacitor
   Reverse blocking diode from Battery to VBATP (0.6 V < V_F < 1 V). See Figure 23, Typical application diagram.

4.2 Thermal characteristics

Table 4. Thermal ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min.	Max.	Unit	Notes
Thermal ratings					
T_A T_J	Operating Temperature • Ambient • Junction	 -40 -40	 125 150	°C	
T_{STG}	Storage Temperature	-65	150	°C	
T_{PPRT}	Peak Package Reflow Temperature During Reflow	–	–	°C	
Thermal resistance					
$R_{\Theta JA}$	Junction-to-Ambient, Natural Convection, Single-Layer Board • 32 SOIC-EP • 32 QFN		 79 94	°C/W	(9), (10)
$R_{\Theta JB}$	Junction-to-Board • 32 SOIC-EP • 32 QFN		 9.0 12	°C/W	(11)
$R_{\Theta JC}$	Junction-to-Case (Bottom) • 32 SOIC-EP • 32 QFN		 3.0 2.0	°C/W	(12)
Ψ_{JT}	Junction-to-Package (Top), Natural convection • 32 SOIC-EP • 32 QFN		 11 2.0	°C/W	(13)
Package dissipation ratings					
T_{SD}	Thermal Shutdown • 32 SOIC-EP • 32 QFN	155	185	°C	
T_{SDH}	Thermal Shutdown Hysteresis • 32 SOIC-EP • 32 QFN	3.0	15	°C	

Notes

9. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
10. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
11. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
12. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
13. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.3 Operating conditions

This section describes the operating conditions of the device. Conditions apply to the following data, unless otherwise noted.

Table 5. Operating conditions

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Min.	Max.	Unit	Notes
VBATP	Battery Voltage	4.5	36	V	
VDDQ	Supply Voltage	3.0	5.25	V	
CS_B, MOSI, MISO, SCLK	SPI Inputs / Outputs	3.0	5.25	V	
SGx, SPx	Switch Input Range	-1.0	36	V	
AMUX, INT_B	AMUX, INT_B	0.0	5.25	V	
WAKE_B	WAKE_B	0.0	36	V	

4.4 Electrical characteristics

4.4.1 Static electrical characteristics

Table 6. Static electrical characteristics

T_A = - 40 °C to +125 °C, VDDQ = 3.1 V to 5.25 V, VBATP = 6.0 V to 28.0 V, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Units	Notes
Power input						
$V_{BATP(POR)}$	VBATP Supply Voltage POR • VBATP Supply Power on Reset voltage.	2.7	3.3	3.8	V	
V_{BATPUV}	VBATP Undervoltage Rising Threshold	—	4.3	4.5	V	
$V_{BATPUVHYS}$	VBATP Undervoltage Hysteresis	250	—	500	mV	
V_{BATPOV}	VBATP Overvoltage Rising Threshold	32	—	37	V	
$V_{BATPOVHYS}$	VBATP Overvoltage Hysteresis	1.5	—	3.0	V	
$I_{BAT(ON)}$	VBATP Supply Current • All switches open, Normal mode, Tri-state disabled (all channels)	—	7.0	12	mA	
$I_{BATP,IQ,LPM,P}$ $I_{BATP,IQ,LPM,F}$	VBATP Low-power Mode Supply Current (polling disabled) • Parametric V_{BATP}, 6.0 V < V_{BATP} < 28 V • Functional Low V_{BATP}, 4.5 V < V_{BATP} < 6.0 V	— —	— —	40 40	µA	
$I_{POLLING,IQ}$	VBATP Polling Current • Polling 64 ms, 11 inputs of wake enabled	—	—	20	µA	(14)
$I_{VDDQ,NORMAL}$	Normal mode (I_{VDDQ}) • SCLK, MOSI, WakeB = 0 V, CS_B, INT_B =V_{DDQ}, no SPI communication, AMUX selected no input	—	—	500	uA	
$I_{VDDQ,LPM}$	Logic Low-power mode Supply Current • SCLK, MOSI = 0 V, CS_B, INT_B, WAKE_B = V_{DDQ}, no SPI communication	—	—	10	µA	
$V_{GNDOFFSET}$	Ground Offset • Ground offset of Global pins to IC ground	-1.0	—	1.0	V	
$VDDQ_{UV}$	VDDQ Undervoltage Falling Threshold	2.2	—	2.8	V	
$VDDQ_{UVHYS}$	VDDQ Undervoltage Hysteresis	150	—	350	mV	

Table 6. Static electrical characteristics (continued)

T_A = - 40 °C to +125 °C, VDDQ = 3.1 V to 5.25 V, VBATP = 6.0 V to 28.0 V, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Units	Notes
Switch input						
I_{LEAKSG_GND}	Leakage (SGx/SPx pins) to GND • Inputs tri-stated, analog mux selected for each input, voltage at SGx = VBATP	—	—	2.0	µA	
I_{LEAKSG_BAT}	Leakage (SGx/SPx pins) to Battery • Inputs tri-stated, analog mux selected for each input, voltage at SGx = GND	—	—	2.0	µA	
I_{SUSSG}	SG Sustain current / Mode 0 Wetting current • VBATP 6.0 to 28 V	1.6	2.0	2.4	mA	
$I_{SUSSGLV}$	SG Sustain current / Mode 0 Wetting current LV • VBATP 4.5 V to 6.0 V	1.0	—	2.4	mA	(15)
I_{SUSSB}	SB Sustain current / Mode 0 Wetting current	1.75	2.2	2.85	mA	
I_{WET}	Wetting current level (SG & SB) • Mode 1 = 6mA • Mode 2 = 8mA • Mode 3 = 10mA • Mode 4 = 12mA • Mode 5 = 14mA • Mode 6 = 16mA • Mode 7 = 20mA	—	 6 8 10 12 14 16 20	—	mA	
I_{WETSG}	SG wetting current tolerance • Mode 1 to 7	-10	—	10	%	
$I_{WETSGLV}$	SG wetting current tolerance LV (VBATP 4.5 to 6.0V)(15) • Mode 1 = 6mA • Mode 2 = 8mA • Mode 3 = 10mA • Mode 4 = 12mA • Mode 5 = 14mA • Mode 6 = 16mA • Mode 7 = 20mA	 2.0 2.0 2.0 2.0 2.0 2.0 2.0	 — — — — — — —	 6.6 8.8 11.0 13.2 15.4 17.6 22.0	mA	
I_{WETSB}	SB wetting current tolerance • Mode 1 to 7	-20	—	20	%	
$I_{MATCH(SUS)}$	Sustain Current Matching Between Channels	—	—	10	%	(16), (17)
$I_{MATCH(WET)}$	Wetting Current Matching Between Channels	—	—	6.0	%	(18), (19)
V_{ICTHR}	Switch Detection Threshold	3.7	4.0	4.3	V	(20)
$V_{ICTHRLV}$	Switch Detection Threshold Low Battery • VBATP 4.5 V to 6.0 V	0.55 * V_{BATP}	—	4.3	V	
$V_{ICTHRLPM}$	Switch Detection Threshold Low-power Mode (SG only)	100	—	300	mV	(21)
V_{ICTHRH}	Switch Detection Threshold Hysteresis (4.0 V threshold)	80	—	300	mV	
$V_{ICTH2P5}$	Input Threshold 2.5 V, • Used for Comp Only and for AMUX Hardwired Select (SG1/2/3)	2.0	2.5	3.0	V	
$I_{ACTIVEPOLLSG}$	Low-power Mode Polling Current SG • VBATP 4.5 V to 28 V	0.7	1.0	1.44	mA	
$I_{ACTIVEPOLLSB}$	Low-power Mode Polling Current SB	1.75	2.2	2.85	mA	

Table 6. Static electrical characteristics (continued)

T_A = - 40 °C to +125 °C, VDDQ = 3.1 V to 5.25 V, VBATP = 6.0 V to 28.0 V, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Units	Notes
Digital interface						
I_{HZ}	Tri-state Leakage Current (MISO) • VDDQ = 0.0 to VDDQ	-2.0	—	2.0	µA	
$V_{INLOGIC}$	Input Logic Voltage Thresholds • SI, SCLK, CS_B, INT_B	V_{DDQ} * 0.25	—	V_{DDQ} * 0.7	V	
$V_{INLOGICHYS}$	Input Logic Hysteresis • SI, SCLK, CS_B, INT_B	300	—	—	mV	
$V_{INLOGICWAKE}$	Input Logic Voltage Threshold WAKE_B	0.8	1.25	1.7	V	
$V_{INWAKEBHYS}$	Input Logic Voltage Hysteresis WAKE_B	200	—	800	mV	
I_{SCLK}, I_{MOSI}	SCLK / MOSI Input Current • SCLK / MOSI = 0 V	-3.0	—	3.0	µA	
I_{SCLK}, I_{MOSI}	SCLK / MOSI Pull-down Current • SCLK / MOSI = VDDQ	30	—	100	µA	
I_{CS_BH}	CS_B Input Current • CS_B = VDDQ	-10	—	10	µA	
R_{CS_BL}	CS_B Pull-up Resistor to VDDQ • CS_B = 0.0 V	40	125	270	kΩ	
V_{OHMISO}	MISO High-side Output Voltage • I_{OHMISO} = -1.0 mA	V_{DDQ} – 0.8	—	V_{DDQ}	V	
V_{OLMISO}	MISO Low-side Output Voltage • I_{OLMISO} = 1.0 mA	—	—	0.4	V	
C_{IN}	Input Capacitance on SCLK, MOSI, Tri-state MISO (GBD)	—	—	20	pF	
Analog MUX output						
V_{OFFSET}	Input Offset Voltage When Selected as Analog • EK suffix (SOICW) • ES suffix (QFN at T_A = -40 °C to 25 °C)	 -10 -15	 — —	 10 15	mV	(22)
V_{OLAMUX}	Analog Operational Amplifier Output Voltage • Sink 1.0 mA	—	—	50	mV	
V_{OHAMUX}	Analog Operational Amplifier Output Voltage • Source 1.0 mA	V_{DDQ} – 0.1	—	—	V	
AMUX selectable outputs						
Temp-Coeff	Chip Temperature Sensor Coefficient	—	8.0	—	mV/°C	
$V_{BATSNSACC}$	Battery Sense (SG5 config) Accuracy • Battery voltage (SG5 input) divided by 6 • Accuracy over full temperature range	-5.0	—	5.0	%	
$V_{BATSNSDIV}$	Divider By 6 coefficient accuracy • Offset over operating voltage range (VBATP=6.0 V to 28 V)	-3.0	—	3.0	%	(23)

Table 6. Static electrical characteristics (continued)

T_A = - 40 °C to +125 °C, VDDQ = 3.1 V to 5.25 V, VBATP = 6.0 V to 28.0 V, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Units	Notes
INT_B						
V_{OLINT}	INT_B Output Low Voltage • I_{OUT} = 1.0 mA	—	0.2	0.5	V	
V_{OHINT}	INT_B Output High Voltage • INT_B = Open-circuit	V_{DDQ} – 0.5	—	V_{DDQ}	V	
R_{PU}	Pull-up Resistor to VDDQ	40	125	270	kΩ	
$I_{LEAKINT\_B}$	Leakage Current INT_B • INT_B pulled up to VDDQ	—	—	1.0	µA	
Temperature limit						
t_{FLAG}	Temperature Warning • First flag to trip	105	120	135	°C	
t_{LIM}	Temperature Monitor	155	—	185	°C	(24)
$t_{LIM(HYS)}$	Temperature Monitor Hysteresis	5.0	—	15	°C	(24)
WAKE_B						
$R_{WAKE\_B(RPU)}$	WAKE_B Internal pull-up Resistor to VDDQ	40	125	270	kΩ	
$V_{WAKE\_B(VOH)}$	WAKE_B Voltage High • WAKE_B = Open-circuit	V_{DDQ} -1.0	—	V_{DDQ}	V	
$V_{WAKE\_B(VOL)}$	WAKE_B Voltage Low • WAKE_B = 1.0 mA (R_{PU} to V_{BATP} = 16 V)	—	—	0.4	V	
I_{WAKE_BLEAK}	WAKE_B Leakage • WAKE_B pulled up to V_{BATP} = 16 V through 10 kΩ	—	—	1.0	µA	

Notes

14. Guaranteed by design
15. During low voltage range operation SG wetting current may be limited when there is not enough headroom between VBATP and SG pin voltage.
16. $(I_{SUS(MAX)} - I_{SUS(MIN)})$ X 100/$I_{SUS(MIN)}$
17. Sustain current source (SGs only)
18. $(I_{WET(MAX)} - I_{WET(MIN)})$ X 100/$I_{WET(MIN)}$
19. Wetting current source (SGs only)
20. The input comparator threshold decreases when $V_{BATP} \leq 6.0$ V.
21. SP (as SB) only use the 4.0 V V_{ICTHR} for LPM wake-up detection.
22. For applications requiring a tight AMUX offset through the whole operating range, it is recommended to use the MC33978AEK or MC34978AEK (SOICW package) variant.
23. Calibration of divider ratio can be done at V_{BAT} = 12 V, 25 °C to achieve a higher accuracy. See Figure 4 for AMUX offset linearity waveform through the operating voltage range.
24. Guaranteed by characterization in the Development Phase, parameter not tested.

4.4.2 Dynamic electrical characteristics

Table 7. Dynamic electrical characteristics

T_A = -40 °C to +125 °C. VDDQ = 3.1 V to 5.25 V, VBATP = 6.0 V to 28 V, unless otherwise specified. All SPI timing is performed with a 100 pF load on MISO, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
General						
t_{ACTIVE}	POR to Active time • Undervoltage to Normal mode	250	340	450	µs	
Switch input						
$t_{PULSE(ON)}$	Pulse Wetting Current Timer • Normal mode	17	20	23	ms	
$t_{INT-DLY}$	Interrupt Delay Time • Normal mode	—	—	18.5	µs	
$t_{POLLING\_TIMER}$	Polling Timer Accuracy • Low-power mode	—	—	15	%	
$t_{INT-TIMER}$	Interrupt Timer Accuracy • Low-power mode	—	—	15	%	
$t_{ACTIVEPOLLSGTIME}$	Tactivepoll Timer SG	49.5	58	66.5	µs	
$t_{ACTIVEPOLLSBTIME}$	Tactivepoll Timer SB • SBPOLLTIME=0 • SBPOLLTIME=1	 1.0 49.5	 1.2 58	 1.4 66.5	 ms µs	
$t_{GLITCHTIMER}$	Input Glitch Filter Timer • Normal mode	5.0	—	18	µs	
$t_{DEBOUNCE}$	LPM Debounce Additional Time • Low-power mode	1.0	1.2	1.4	ms	
AMUX output						
$AMUX_{VALID}$	AMUX Access Time (Selected Output to Selected Output) • C_{MUX} = 1.0 nF, Rising edge of CS_B to selected	—	(26)	—	µs	
$AMUX_{VALIDTS}$	AMUX Access Time (Tristate to ON) • C_{MUX} = 1.0 nF, Rising edge of CS_B to selected	—	—	20	µs	
Oscillator						
OSC_{TOLLPM}	Oscillator Tolerance at 192 kHz in Low-power Mode	-15	—	15	%	
OSC_{TOLNOR}	Oscillator Tolerance Normal Mode at 4.0 MHz	-15	—	15	%	
Interrupt						
INT_{PULSE}	INT Pulse Duration • Interrupt occurs or INT_B request	90	100	110	µs	
SPI interface						
f_{OP}	Transfer Frequency	—	—	8.0	MHz	
t_{SCK}	SCLK Period • Figure 7 - 1	160	—	—	ns	
t_{LEAD}	Enable Lead Time • Figure 7 - 2	140	—	—	ns	
t_{LAG}	Enable Lag Time • Figure 7 - 3	50	—	—	ns	
t_{SCKHS}	SCLK High Time • Figure 7 - 4	56	—	—	ns	

Table 7. Dynamic electrical characteristics (continued)

T_A = -40 °C to +125 °C. VDDQ = 3.1 V to 5.25 V, VBATP = 6.0 V to 28 V, unless otherwise specified. All SPI timing is performed with a 100 pF load on MISO, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
SPI interface (continued)						
t_{SCKLS}	SCLK Low Time • Figure 7 - 5	56	—	—	ns	
t_{SUS}	MOSI Input Setup Time • Figure 7 - 6	16	—	—	ns	
t_{HS}	MOSI Input Hold Time • Figure 7 - 7	20	—	—	ns	
t_A	MISO Access Time • Figure 7 - 8	—	—	116	ns	
t_{DIS}	MISO Disable Time (25) • Figure 7 - 9	—	—	100	ns	
t_{VS}	MISO Output Valid Time • Figure 7 - 10	—	—	116	ns	
t_{HO}	MISO Output Hold Time (No cap on MISO) • Figure 7 - 11	20	—	—	ns	
t_{RO}	Rise Time • Figure 7 - 12	—	—	30	ns	(25)
t_{FO}	Fall Time • Figure 7 - 13	—	—	30	ns	(25)
t_{CSN}	CS_B Negated Time • Figure 7 - 14	500	—	—	ns	
WAKE-UP						
t_{CSB_WAKEUP}	LPM mode wake-up time triggered by edge of CS_B	—	755	1000	µs	**(27)**

Notes

25. Guaranteed by characterization.
26. AMUX settling time to be within the 10 mV offset specification. $AMUX_{VALID}$ is dependant of the voltage step applied on the input SGx/SPx pin or the difference between the first and second channel selected as the multiplexed analog output. See Figure 9 for a typical AMUX access time VS voltage step waveform.
27. The parameter is guaranteed at VBATP = 4.5 V to 28 V.

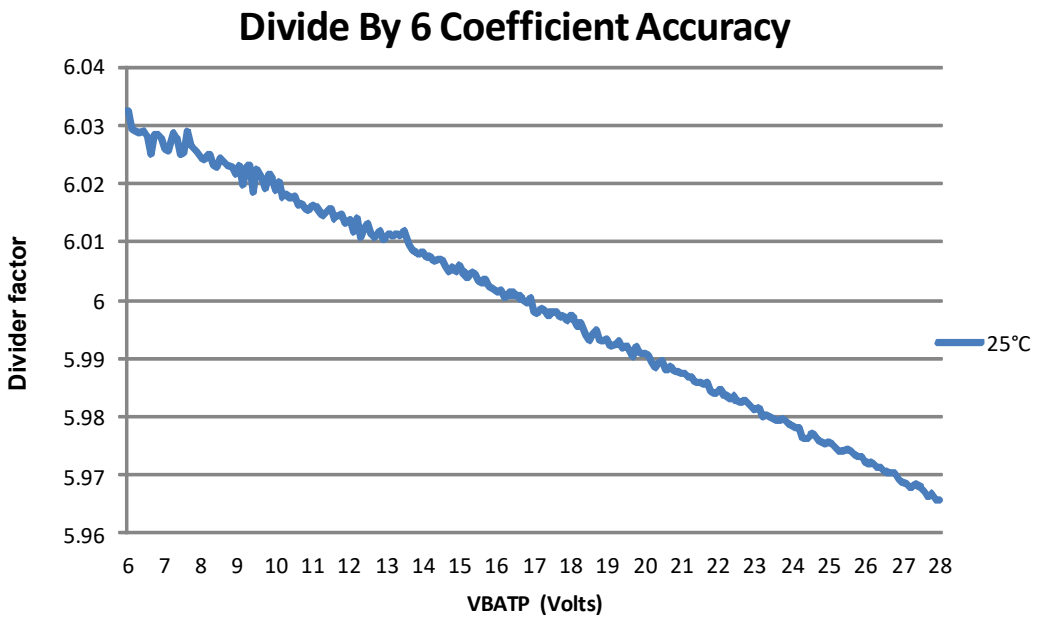


Figure 4. Divide by 6 coefficient accuracy

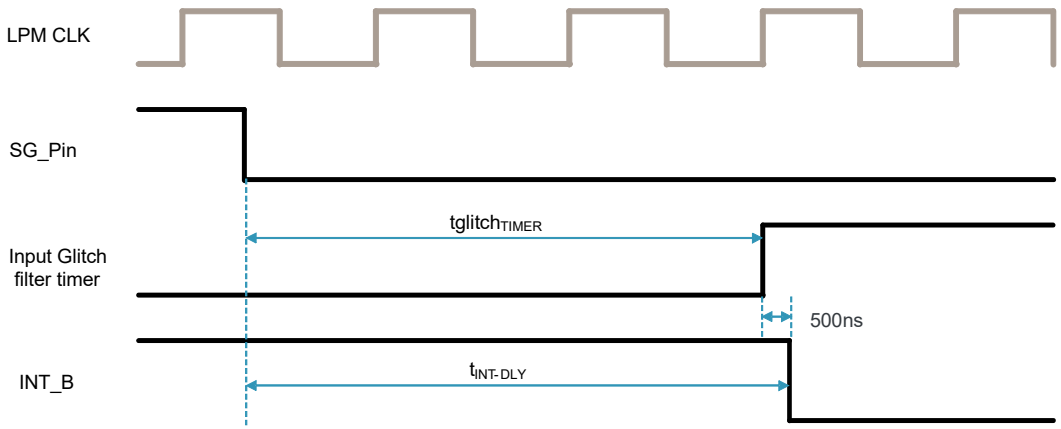


Figure 5. Glitch filter and interrupt delay timers

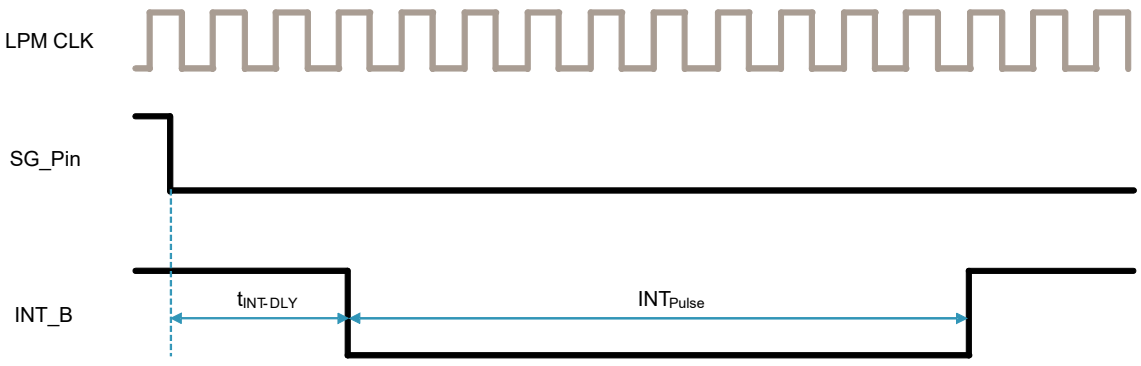


Figure 6. Interrupt pulse timer

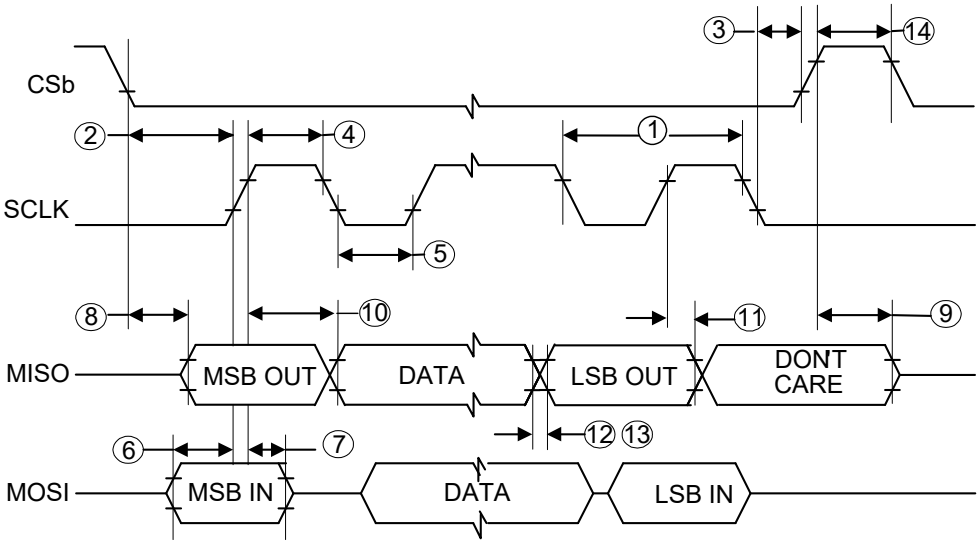


Figure 7. SPI timing diagram

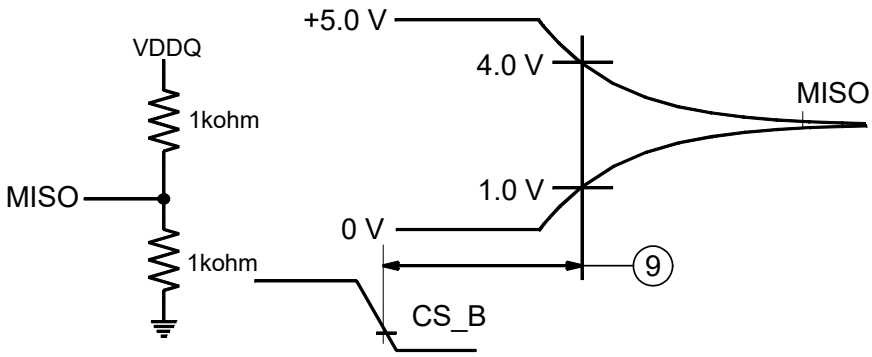


Figure 8. MISO loading for disable time measurement

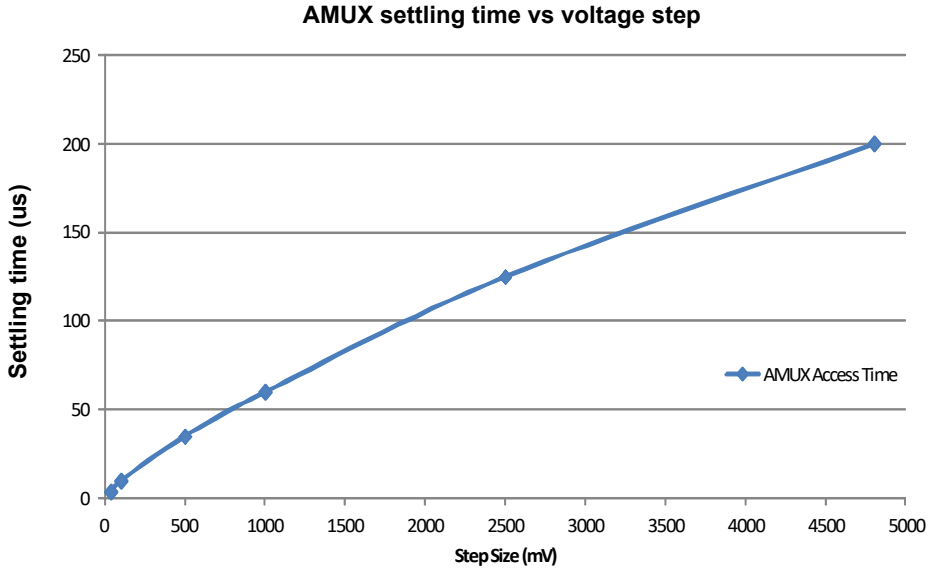


Figure 9. AMUX access time waveform

5 General description

The 33978 is designed to detect the closing and opening of up to 22 switch contacts. The switch status, either open or closed, is transferred to the microprocessor unit (MCU) through a serial peripheral interface (SPI). Individually selectable input currents are available in Normal and Low-power (LPM) modes, as needed for the application.

It also features a 24-to-1 analog multiplexer for reading inputs as analog. The analog input signal is buffered and provided on the AMUX output pin for the MCU to read. A battery and temperature monitor are included in the IC and available via the AMUX pin.

The 33978 device has two modes of operation, Normal and Low-power mode (LPM). Normal mode allows programming of the device and supplies switch contacts with pull-up or pull-down current as it monitors the change of state of switches. The LPM provides low quiescent current, which makes the 33978 ideal for automotive and industrial products requiring low sleep-state currents.

5.1 Features

- Fully functional operation from 4.5 V to 36 V
- Full parametric operation from 6.0 V to 28 V
- Low-power mode current I_{BATP} = 30 μA and I_{DDQ} = 10 μA
- 22 Switch detection channels
  - 14 Switch-to-Ground (SG) inputs
  - Eight Programmable switch (SP) inputs
    - Switch-to-Ground (SG) or Switch-to-Battery (SB)
  - Operating switch input voltage range from -1.0 V to 36 V
  - Selectable wetting current (2, 6, 8, 10, 12, 14, 16, or 20 mA)
  - Programmable wetting operation (Pulse or Continuous)
  - Selectable wake-up on change of state
- 24 to 1 Analog Multiplexer
  - Buffered AMUX output from SG/SP channels
  - Integrated divider by 6 on SG5 for battery voltage sensing
  - Integrated die temperature sensing through AMUX output
  - Two or three pin hardwire AMUX selection.
- Active interrupt (INT_B) on change-of-switch state
- Direct MCU Interface through 3.3 V / 5.0 V SPI protocol

5.2 Functional block diagram

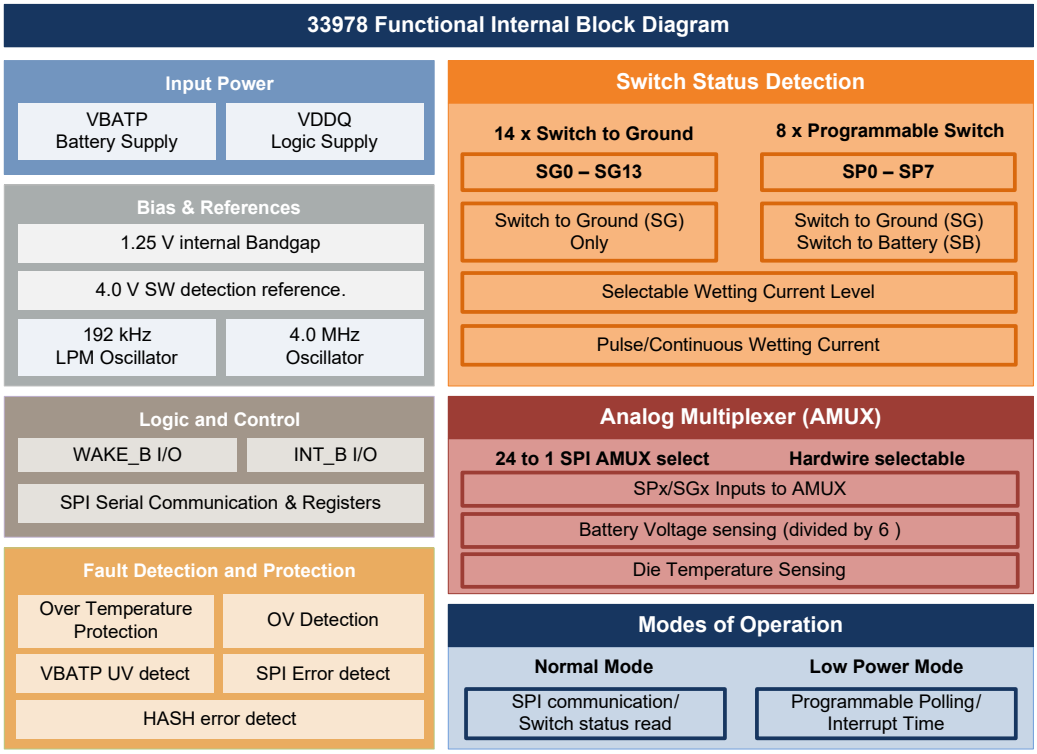


Figure 10. Functional block diagram

6 General IC functional description

The 33978 device interacts with many connections outside the module and near the end user. The IC detects changes in switch state and reports the information to the MCU via the SPI protocol. The input pins generally connected to switches located outside the module and in proximity to battery in car harnesses. Consequently, the IC must have some external protection including an ESD capacitor and series resistors, to ensure the energy from the various pulses are limited at the IC.

The IC requires a blocking diode be used on the VBATP pin to protect from a reverse battery condition. The inputs are capable of surviving reverse battery without a blocking diode and also contain an internal blocking diode from the input to the power supply (V_{BATP}), to ensure there is no backfeeding of voltage/current into the IC, when the voltage on the input is higher than the VBATP pin.

6.1 Battery voltage ranges

The 33978 device operates from 4.5 V ≤ V_{BATP} ≤ 36 V and is capable to withstand up to 40 V. The IC operates functionally from 4.5 V < V_{BATP} < 6.0 V, but with degraded parametrics values. Voltages in excess of 40 V must be clamped externally in order to protect the IC from destruction. The VBATP pin must be isolated from the main battery node by a diode.

6.1.1 Load dump (overvoltage)

During load dump the 33978 operates properly up to the V_{BATP} overvoltage. Voltages greater than load dump (~32 V) causes the current sources to be limited to ~2.0 mA, but the register values are maintained. Upon leaving this overvoltage condition, the original setup is returned and normal operation begins again.

6.1.2 Jump start (double battery)

During a jump start (double battery) condition, the device functions normally and meets all the specified parametric values. No internal faults are set and no abnormal operation noted as a result of operating in this range.

6.1.3 Normal battery range

The normal voltage range is fully functional with all parametrics in the given specification.

6.1.4 Low-voltage range (degraded parametrics)

In the V_{BATP} range between 4.5 V to 6.0 V the 33978 functions normally, but has some degraded parametric values. The SPI functions normally with no false reporting. The degraded parameters are noted in Table 6 and Table 7. During this condition, the input comparator threshold is reduced from 4.0 V and remain ratiometrically adjusted, according to the battery level.

6.1.5 Undervoltage lockout

During undervoltage lockout, the MISO output is tri-stated to avoid any data from being transmitted from the 33978. Any CS_B pulses are ignored in this voltage range. If the battery enters this range at any point (even during a SPI word), the 33978 ignores the word and enters lockout mode. A SPI bit register is available to notify the MCU that the 33978 has seen an undervoltage lockout condition once the battery is high enough to leave this range.

6.1.6 Power on reset (POR) activated

The Power on Reset is activated when the VBATP is within the 2.7 V to 3.8 V range. During the POR all SPI registers are reset to default values and SPI operation is disabled. The 33978 is initialized after the POR is de-asserted. A SPI bit in the device configuration register is used to note a POR occurrence and all SPI registers are reset to the default values.

6.1.7 No operation

The device does not function and no switch detection is possible.

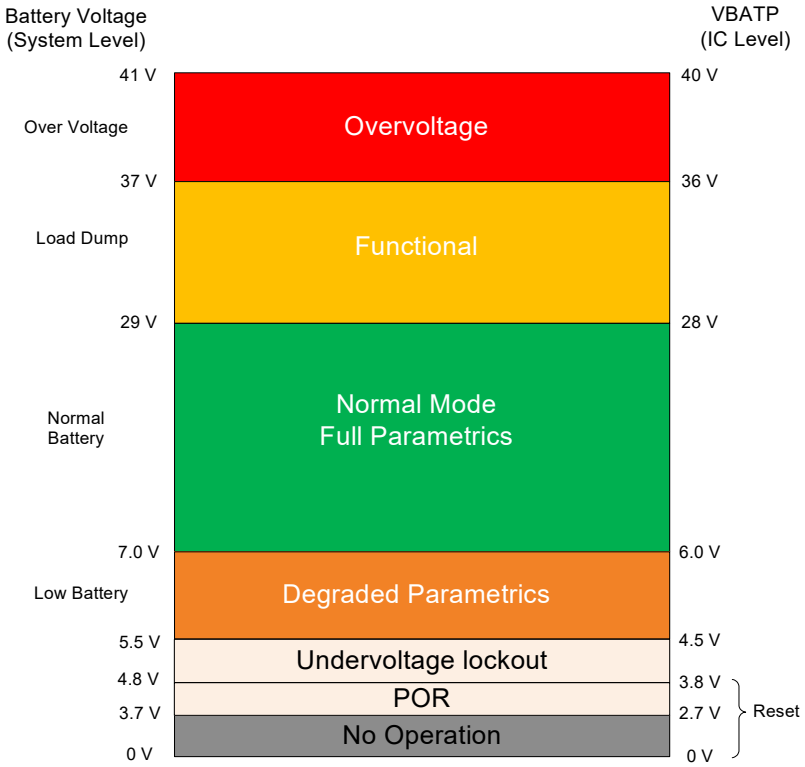


Figure 11. Battery voltage range

6.2 Power sequencing conditions

The chip uses two supplies as inputs into the device for various usage. The pins are VBATP and VDDQ. The VBATP pin is the power supply for the chip where the internal supplies are generated and power supply for the SG circuits. The VDDQ pin is used for the I/O buffer supply to talk to the MCU or other logic level devices, as well as AMUX. The INT_B pin is held low upon POR until the IC is ready to operate and communicate. Power can be applied in various ways to the 33978 and the following states are possible:

6.2.1 V_{BATP} before V_{DDQ}

The normal condition for operation is the application of V_{BATP} and then V_{DDQ}. The chip begin to operate logically in the default state but without the ability to drive logic pins. When the V_{DDQ} supply is available the chip is able to communicate correctly. The IC maintains its logical state (register settings) with functional behavior consistent with logical state. No SPI communications can occur.

6.2.2 V_{DDQ} before V_{BATP}

The V_{DDQ} supply in some cases may be available before the V_{BATP} supply is ready. In this scenario, there is no back feeding current into the VDDQ pin that could potentially turn on the device into an unknown state. VDDQ is isolated from VBATP circuits and the device is off until VBATP is applied; when V_{BATP} is available the device powers up the internal rails and logic within t_{ACTIVE} time. Communication is undefined until the t_{ACTIVE} time and becomes available after this time frame.

6.2.3 V_{BATP} okay, V_{DDQ} lost

After power up, it is possible that the V_{DDQ} may turn off or be lost. In this case, the chip remains in the current state but is not able to communicate. After the VDDQ pin is available again, the chip is ready to communicate.

6.2.4 V_{DDQ} okay, V_{BATP} lost

After power up, the V_{BATP} supply could be lost. The operation is consistent as when V_{DDQ} is available before V_{BATP}.

7 Functional block description

7.1 State diagram

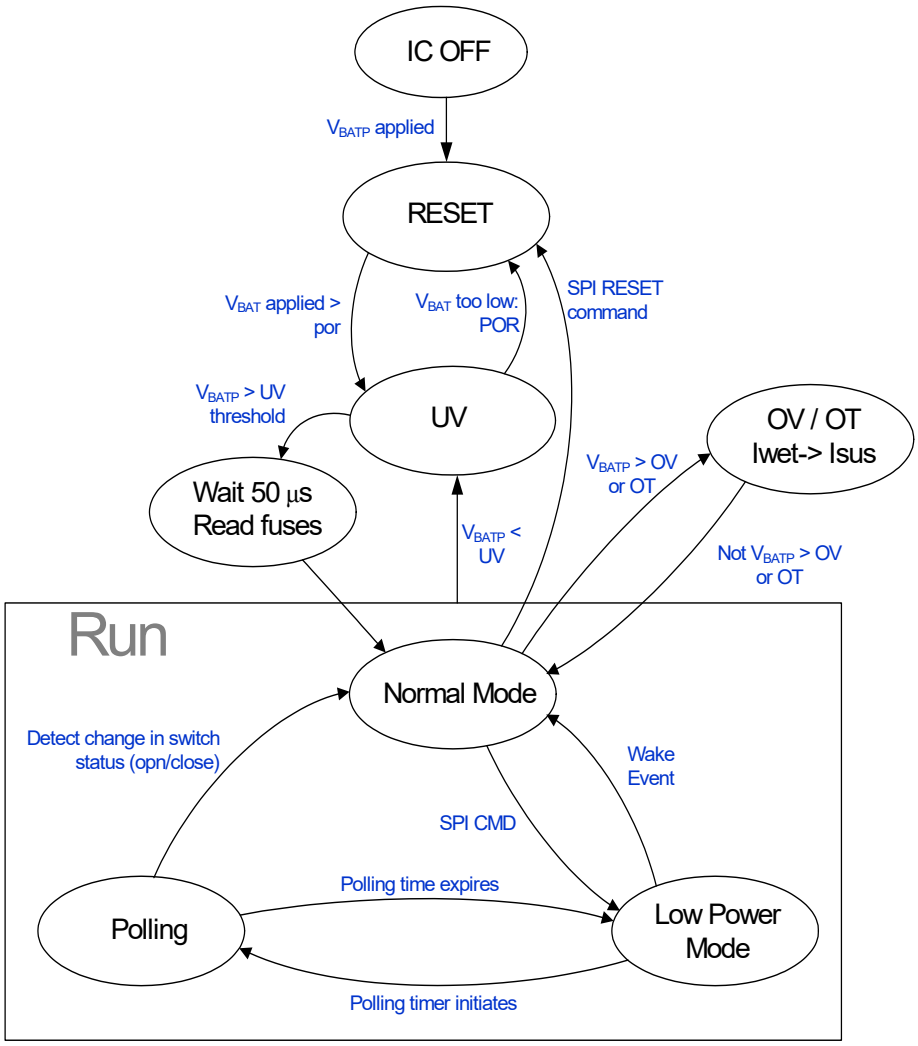


Figure 12. 33978 state diagram

7.1.1 State machine

After power up, the IC enters into the device state machine, as illustrated in Figure 12. The voltage on VBATP begins to power the internal oscillators and regulator supplies. The POR is based on the internal 2.5 V digital core rail. When the internal logic regulator reaches approximately 1.8 V (typically 3.3 V on the VBATP node), the IC enters into the UV range. Below the POR threshold, the IC is in RESET mode where no activity occurs.

7.1.2 UV: undervoltage lockout

After the POR circuit has reset the logic, the IC is in undervoltage. In this state, the IC remembers all register conditions, but is in a lockout mode, where no SPI communication is allowed. The AMUX is inactive and the current sources are off. The user does not receive a valid response from the MISO, as it is disabled in this state. The chip oscillators (4.0 MHz for most normal mode activities, 192 kHz for LPM, and limited normal mode functions) are turned on in the UV state. The chip moves to the Read fuses state when the V_{BATP} voltage rises above the UV threshold (~4.3 V rising). The internal fuses read in approximately 50 µs and the chip enters the Normal mode.

7.1.3 Normal mode

In normal mode, the chip operates as selected in the available registers. Any command may be loaded in normal mode, although not all (Low-power mode) registers are used in the Normal mode. All the LPM registers must be programmed in Normal mode as the SPI is not active in LPM. The Normal mode of the chip is used to operate the AMUX, communicate via the SPI, Interrupt the IC, wetting and sustain currents, as well as the thresholds available to use. The WAKE_B pin is asserted (low) in Normal mode and can be used to enable a power supply (ENABLE_B). Various fault detections are available in this mode including overvoltage, overtemperature, thermal warning, SPI errors, and Hash faults.

7.1.4 Low-power mode

When the user needs to lower the IC current consumption, a low-power mode is used. The only method to enter LPM is through a SPI word. After the chip is in low-power mode, the majority of circuitry is turned off including most power rails, the 4.0 MHz oscillator, and all the fault detection circuits. This mode is the lowest current consumption mode on the chip. If a fault occurs while the chip is in this mode, the chip does not see or register the fault (does not report via the SPI when awakened). Some items may wake the IC in this mode, including the interrupt timer, falling edge of INT_B, CS_B, or WAKE_B (configurable), or a comparator only mode switch detection.

7.1.5 Polling mode

The 33978 uses a polling mode which periodically (selectable in LPM config register) interrogates the input pins to determine in what state the pins are, and decide if there was a change of state from when the chip was in Normal mode. There are various configurations for this mode, which allow the user greater flexibility in operation. This mode uses the current sources to pull-up (SG) or down (SB) to determine if a switch is open or closed. More information is available in section 7.2, “Low-power mode operation".

In the case of a low V_{BATP}, the polling pauses and waits until the V_{BATP} rises out of UV or a POR occurs. The pause of the polling ensures all of the internal rails, currents, and thresholds are up at the required levels to accurately detect open or closed switches. The chip does not wake-up in this condition and simply waits for the V_{BATP} voltage to rise or cause a POR.

After the polling ends, the chip either returns to the low-power mode, or enters Normal mode when a wake event was detected. Other events may wake the chip as well, such as the falling edge of CS_B, INT_B, or WAKE_B (configurable). A comparator only mode switch detection is always on in LPM or Polling mode, so a change of state for those inputs would effectively wake the IC in Polling mode as well.

If the Wake-up enable bits are disable on all channels (SG and SP) the device will not wake up with a change of state on any of the input pins; in this case, the device will disable the polling timer to allow the lowest current consumption during low-power mode.

7.2 Low-power mode operation

Low-power mode (LPM) is used to reduce system quiescent currents. LPM may be entered only by sending the Enter Low-power mode command. All register settings programmed in Normal mode are maintained while in LPM.

The 33978 exits LPM and enter Normal mode when any of the following events occur:

- Input switch change of state (when enabled)
- Interrupt timer expire
- Falling edge of WAKE_B (as set by the device configuration register)
- Falling edge of INT_B (with V_{DDQ} = 5.0 V)
- Falling edge of CS_B (with V_{DDQ} = 5.0 V)
- Power-ON Reset (POR)

The V_{DDQ} supply may be removed from the device during LPM, however removing V_{DDQ} from the device disables a wake-up from falling edge of INT_B and CS_B. The IC checks the status of VDDQ after a falling edge of WAKE_B (as selected in the device configuration register), INT_B and CS_B. The IC returns to LPM and does not report a Wake event, if V_{DDQ} is low. If the V_{DDQ} is high, the IC wakes up and reports the Wake event. In cases where CS_B is used to wake the device, the first MISO data message is not valid.

The LPM command contains settings for two programmable registers: the interrupt timer and the polling timer, as shown in Table 26. The interrupt timer is used as a periodic wake-up timer. When the timer expires, an interrupt is generated and the device enters Normal mode. The polling timer is used periodically to poll the inputs during Low-power mode to check for change of states. The $t_{ACTIVEPOLL}$ time is the length of time the part is active during the polling timer to check for change of state. The Low-power mode voltage threshold allows the user to determine the noise immunity versus lower current levels that polling allows. Figure 14 shows the polling operation.

When polling and Interrupt timer coincide, the Interrupt timer wakes the device and the polling does not occur. When an input is determined to meet the condition Open (when entering LPM), yet while Open (on polling event) the chip does not continue the polling event for that input(s) to lower current in the chip (Figure 13 shows SG, SB is logically the same).

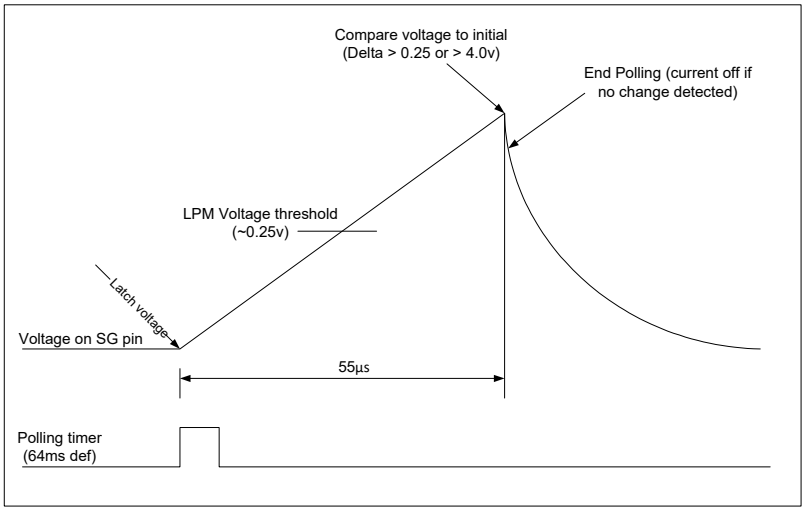


Figure 13. Low-power mode polling check

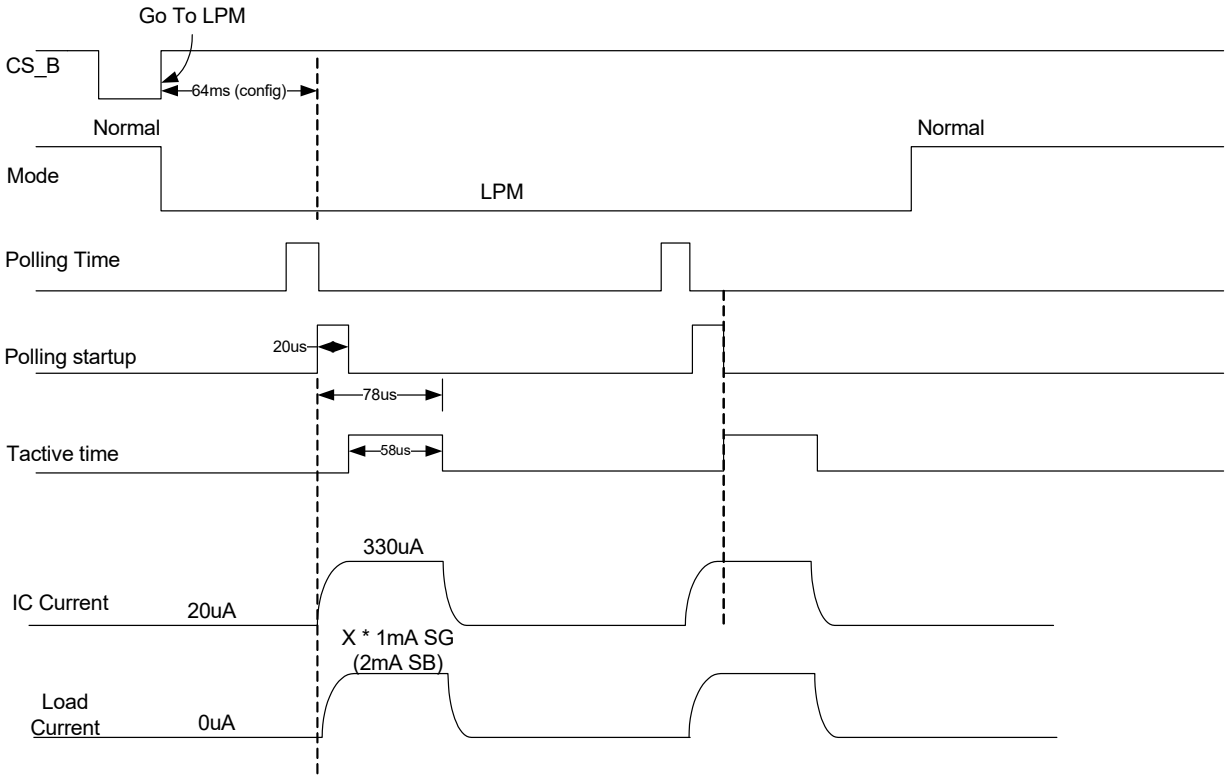


Figure 14. Low-power mode typical timing

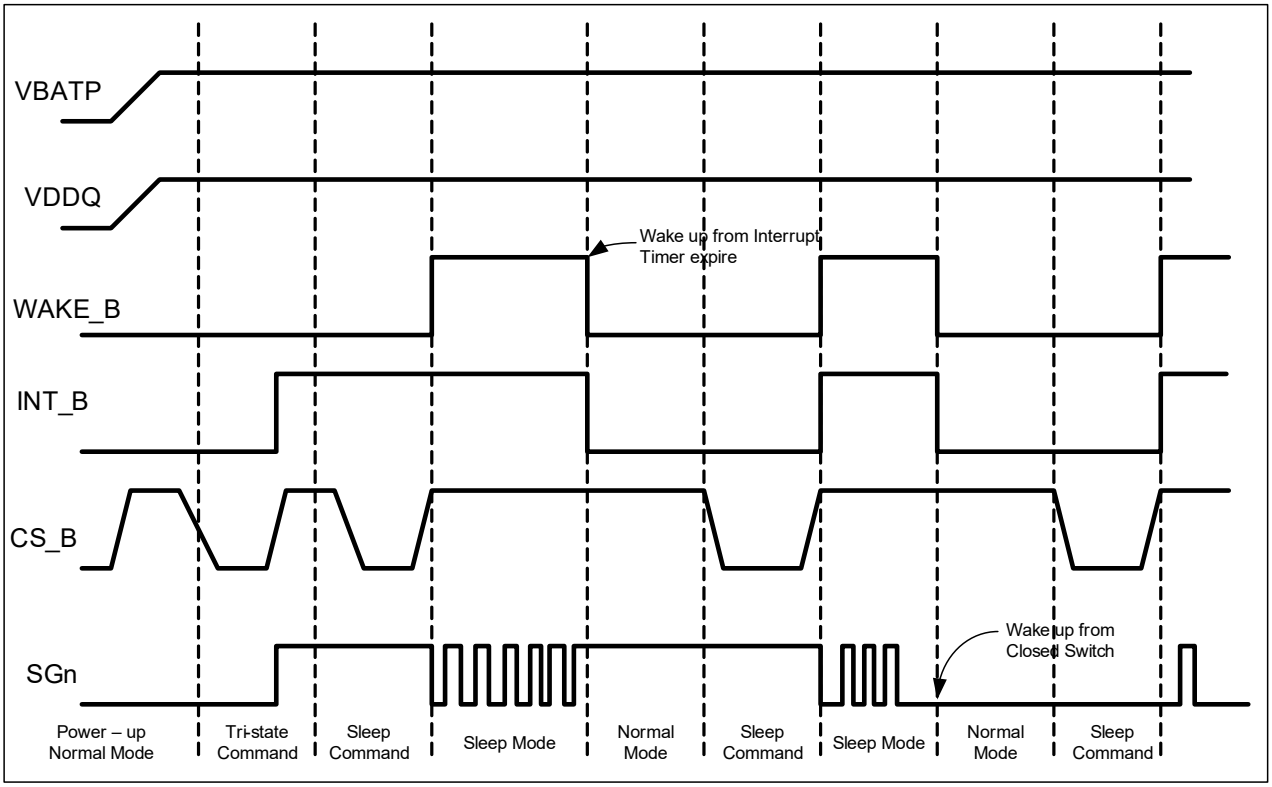


Figure 15. Low-power mode to normal mode operation

7.3 Input functional block

The SGx pins are switch-to-ground inputs only (pull-up current sources).

The SPx pins are configurable as either switch to ground or switch to battery (pull-up and pull-down current sources).

The input is compared with a 4.0 V (input comparator threshold configurable) reference. Voltages greater than the input comparator threshold value are considered open for SG pins and closed for SB configuration.

Voltages less than the input comparator threshold value are considered closed for SG pins and open for the SB configurations.

Programming features are defined in the SPI control register definition section of this data sheet.

The input comparator has hysteresis with the thresholds based on the closing of the switch (falling on SG, rising on SB).

The user must take care to keep power conditions within acceptable limits (package is capable of 2.0 W). Using many of the inputs with continuous wetting current levels causes overheating of the IC and may cause an overtemperature (OT) event to occur.

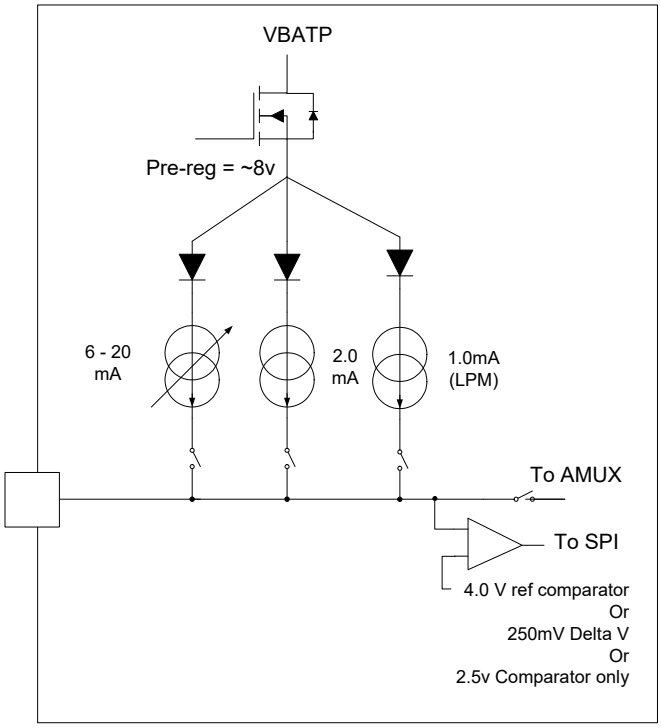


Figure 16. SG block diagram