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Programmable solenoid controller

PT2000

PROGRAMMABLE SOLENOID CONTROLLER

AF SUFFIX
98ASA00505D
80 LQFP

The PT2000 is a SMARTMOS programmable gate driver IC for precision solenoid control applications, which makes the component very flexible and relieves the main microcontroller from the heavy task of the actuator control. The chip integrates six microcores used to control, seven external MOSFET high-side pre-drivers, eight external MOSFET low-side pre-drivers (two of them with higher switching frequency can be used for DC/DC converters), an integrated end of injection detection, six current measurements, and diagnostics for both the high-side and low-side.

PT2000 includes two internal regulators with overvoltage and undervoltage monitoring and protection, V_{CCP} fed from the battery line supplying the pre-driver section and V_{CC2P5} fed from an external 5.0 V generating supply for the digital block.

Interface with the MCU is achieved via serial peripheral interface (SPI) and 16 configurable I/O signals. I/O are supplied by an external 3.3 V or 5.0 V regulator connected to V_{CCIO}.

These features along with cost effective packaging, make the PT2000 ideal for power train engine control applications.

Features

- Battery voltage range, 5.0 V < V_{BATT} < 72 V
- Battery and boost voltage monitoring
- Pre-drive operating voltage up to 72 V
- Seven high-side/ eight low-side pre-drive PWM capability up to 100 kHz-30 nC
- All pre-drivers have four selectable slew rates
- Eight selectable, pre-defined V_{DS} monitoring thresholds
- Measurement function for end of injection detection
- Encryption for microcode protection
- Integrated 1.0 MHz back-up clock

Applications

- Automotive (12 V), truck and industrial (24 V) power train
- Diesel and gasoline direct injection (three banks)
- Transmission
- Valve control

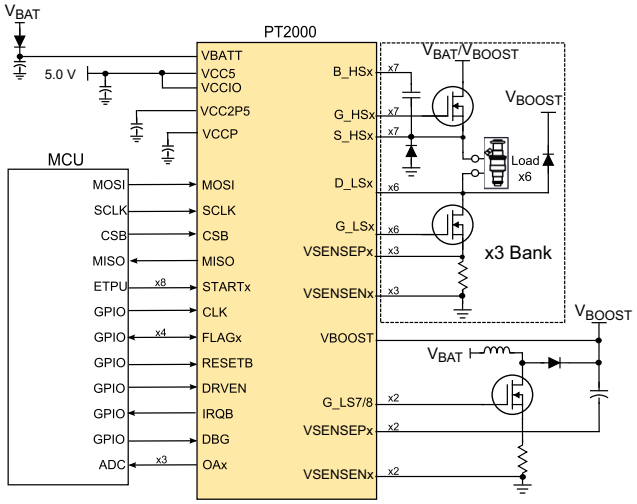

Figure 1. PT2000 simplified application diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table of Contents

1 Orderable parts

Table 1. Orderable part variations

Part number	Temperature (T_A)	Package
MC33PT2000AF [(1)]	-40 °C to 125 °C	80-pin LQFP with exposed pad

Notes
1. To order parts in tape and reel, add the R2 suffix to the part number.

1.1 Cipher key

Contact a NXP sales representative to obtain devices with a specific encryption key and the associated code encryptor.

2 Internal block diagram

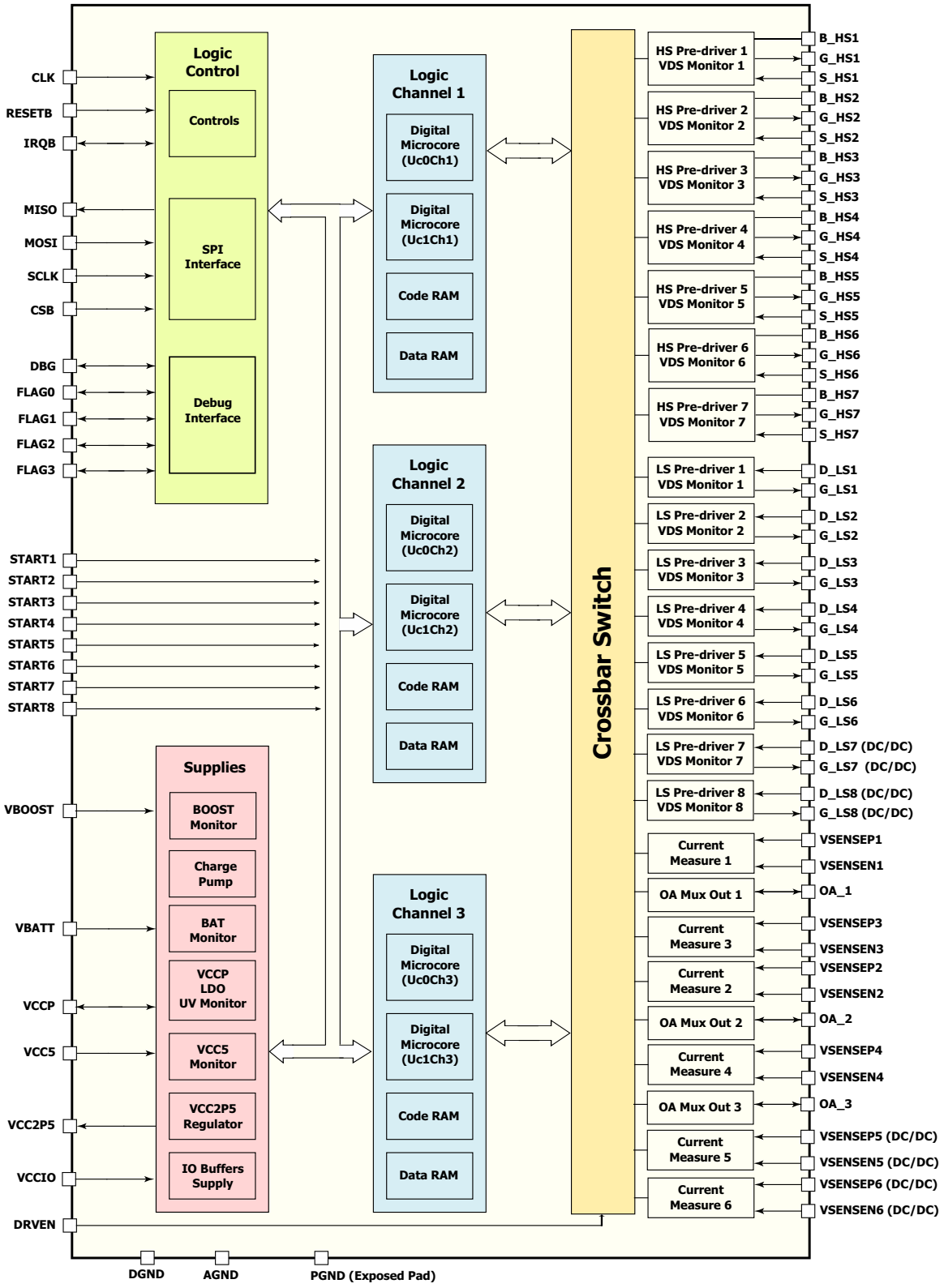

Figure 2. PT2000 simplified internal block diagram

3 Pin connections

Transparent top view

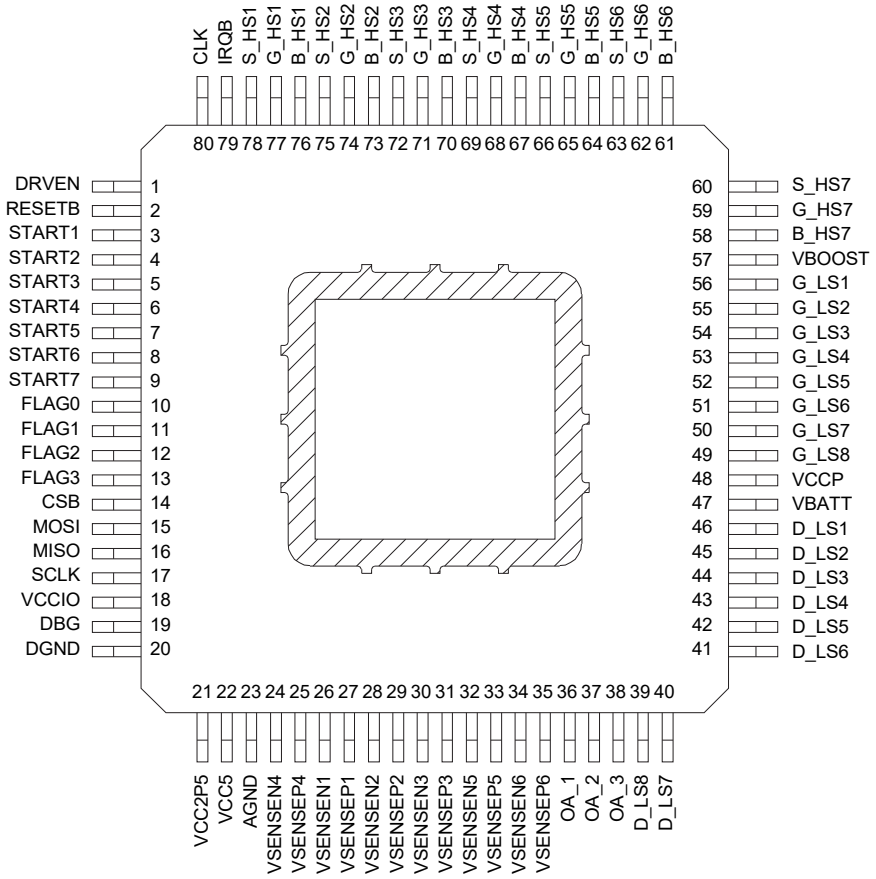

Figure 3. PT2000 pin connections

Functional descriptions of many of these pins can be found in the Functional block description section beginning on page 34.

Table 2. PT2000 pin definitions (2), (3), (4)

Pin	Pin name	Pin function	Pull configuration	Definition
1	DRVEN	Input	Weak PD	Driver enable input
2	RESETB	Input	Weak PU	Reset pin
3	START1	Input/output	PU/PD Configurable	Trigger pin actuator 1 / Flag_bus(5)
4	START2	Input/output	PU/PD Configurable	Trigger pin actuator 2 / Flag_bus(6)
5	START3	Input/output	PU/PD Configurable	Trigger pin actuator 3 / Flag_bus(7)
6	START4	Input/output	PU/PD Configurable	Trigger pin actuator 4 / Flag_bus(8)
7	START5	Input/output	PU/PD Configurable	Trigger pin actuator 5 / Flag_bus(9)

Table 2. PT2000 pin definitions [(2), (3), (4)](continued)

Pin	Pin name	Pin function	Pull configuration	Definition
8	START6	Input/output	PU/PD Configurable	Trigger pin actuator 6 / Flag_bus(10)
9	START7	Input/output	PU/PD Configurable	Trigger pin actuator 7 / Flag_bus(11)
10	FLAG 0	Input/output	Weak PD	Flag_bus(0) (general purpose I/O)/command for external free-wheeling MOSFTET pre-driver 1
11	FLAG 1	Input/output	Weak PD	Flag_bus(1) (general purpose I/O)/command for external free-wheeling MOSFTET pre-driver 2
12	FLAG 2	Input/output	Weak PD	Flag_bus(2) (general purpose I/O)/command for external free-wheeling MOSFTET pre-driver 3
13	FLAG 3	Input/output	Weak PD	Flag_bus(3) (general purpose I/O)/command for external free-wheeling MOSFTET pre-driver 4
14	CSB	Input	PU	SPI chip select
15	MOSI	Input	Weak PU	SPI slave input
16	MISO	Output	—	SPI slave output
17	SCLK	Input	Weak PU	SPI clock
18	VCCIO	Input	—	Digital I/O voltage supply 3.3 V or 5.0 V (supplied externally)
19	DBG	Input/output	Weak PU	Debug port / Flag_bus (15)
20	DGND	Ground	—	Digital ground
21	VCC2P5	Output	—	Internal 2.5 V voltage regulator decoupling
22	VCC5	Input	—	Power supply 5.0 V (supplied externally)
23	AGND	Ground	—	Analog ground
24	VSENSEN4	Input/output	PU/PD Configurable	Current sense input comparator - / Start8 / Flag(12)
25	VSENSEP4	Input/output	Weak PD	Current sense input comparator + /Flag(4) (general purpose I/O)
26	VSENSEN1	Input	—	Current sense input comparator 1 -
27	VSENSEP1	Input	—	Current sense input comparator 1 +
28	VSENSEN2	Input	—	Current sense input comparator 2 -
29	VSENSEP2	Input	—	Current sense input comparator 2 +
30	VSENSEN3	Input	—	Current sense input comparator 3 -
31	VSENSEP3	Input	—	Current sense input comparator 3 +
32	VSENSEN5	Input	—	DC-DC current sense input comparator -
33	VSENSEP5	Input	—	DC-DC current sense input comparator +
34	VSENSEN6	Input	—	DC-DC current sense input comparator -
35	VSENSEP6	Input	—	DC-DC current sense input comparator +
36	OA_1	Output	—	Analog output 1
37	OA_2	Input/output	Weak PD	Analog output 2/Flag_bus (14)
38	OA_3	Output	—	Analog output 3
39	D_LS8	Input	—	Drain pin low-side MOSFET for DC/DC converter
40	D_LS7	Input	—	Drain pin low-side MOSFET for DC/DC converter
41	D_LS6	Input	—	Drain pin low-side MOSFET actuator 6
42	D_LS5	Input	—	Drain pin low-side MOSFET actuator 5

Table 2. PT2000 pin definitions [(2), (3), (4)](continued)

Pin	Pin name	Pin function	Pull configuration	Definition
43	D_LS4	Input	—	Drain pin low-side MOSFET actuator 4
44	D_LS3	Input	—	Drain pin low-side MOSFET actuator 3
45	D_LS2	Input	—	Drain pin low-side MOSFET actuator 2
46	D_LS1	Input	—	Drain pin low-side MOSFET actuator 1
47	VBATT	Input	—	Battery voltage input
48	VCCP	Input/output	—	Output: Internal 7.0 V voltage regulator Input: External 7.0 V voltage regulator (supplied externally)
49	G_LS8	Output	—	Gate pin low-side high speed MOSFET can be used for DC/DC converter
50	G_LS7	Output	—	Gate pin low-side high speed MOSFET can be used for DC/DC converter
51	G_LS6	Output	—	Gate pin low-side MOSFET actuator 6
52	G_LS5	Output	—	Gate pin low-side MOSFET actuator 5
53	G_LS4	Output	—	Gate pin low-side MOSFET actuator 4
54	G_LS3	Output	—	Gate pin low-side MOSFET actuator 3
55	G_LS2	Output	—	Gate pin low-side MOSFET actuator 2
56	G_LS1	Output	—	Gate pin low-side MOSFET actuator 1
57	VBOOST	Input	—	Boost voltage and drain pin for boost pre-drivers
58	B_HS7	-	—	Bootstrap pin high-side MOSFET 7
59	G_HS7	Output	—	Gate pin high-side MOSFET 7
60	S_HS7	Input	—	Source pin high side MOSFET 7
61	B_HS6	-	—	Bootstrap pin Boost MOSFET 6
62	G_HS6	Output	—	Gate pin Boost MOSFET 6
63	S_HS6	Input	—	Source pin Boost MOSFET 6
64	B_HS5	-	—	Bootstrap pin high-side MOSFET 5
65	G_HS5	Output	—	Gate pin high-side MOSFET 5
66	S_HS5	Input	—	Source pin high side MOSFET 5
67	B_HS4	-	—	Bootstrap pin boost MOSFET 4
68	G_HS4	Output	—	Gate pin boost MOSFET 4
69	S_HS4	Input	—	Source pin boost MOSFET 4
70	B_HS3	-	—	Bootstrap pin high-side MOSFET 3
71	G_HS3	Output	—	Gate pin high-side MOSFET 3
72	S_HS3	Input	—	Source pin high-side MOSFET 3
73	B_HS2	-	—	Bootstrap pin boost MOSFET 2
74	G_HS2	Output	—	Gate pin boost MOSFET 2
75	S_HS2	Input	—	Source pin boost MOSFET 2
76	B_HS1	-	—	Bootstrap pin high-side MOSFET 1
77	G_HS1	Output	—	Gate pin high-side MOSFET 1
78	S_HS1	Input	—	Source pin high-side MOSFET 1
79	IRQB	Input/output	Weak PD	Interrupt output/Flag_bus (13)
80	CLK	Input	Weak PU	Clock pin (low-frequency reference for internal PLL)

Table 2. PT2000 pin definitions [2], [3], [4](continued)

Pin	Pin name	Pin function	Pull configuration	Definition
ePAD	PGND	Ground	—	Power ground (to be soldered on GND PCB)

Notes

2. External 7.0 V is required in case the typical battery voltage is 24 V (See External VCCP (vccp_ext_en='1') on page 35).
3. Except for supply and ground, it is guaranteed by design unused pins can be kept open without any impact on the device.
4. Unused VSENSEPx and VSENSENx pins can both be connected to GND.

Table 3. Resistor types

Pin type	Description
PU	Pull-up to VCCIO (nominal value: 120 kΩ)
Weak PU	Weak pull-up to VCCIO (nominal value: 480 kΩ)
PD	Pull-down to AGND (nominal value: 120 kΩ)
Weak PD	Weak pull-down to AGND (nominal value: 480 kΩ)

4 Functional description

4.1 Introduction

The PT2000 is a mixed signal IC for engine injector and electrical valve control, which provides a cost effective, flexible, and smart, high-side and low-side MOSFET gate driver. The device includes both individual charge pump outputs for each high-side pre-driver and high-voltage DC/DC converter pre-driver. Gate drive, diagnostics, and protection against external faults, are managed through six independent and concurrent digital microcores. Each of the three logic channels including two microcores and their own code RAM and data RAM. The internal microcode is protected against theft via encryption and corruption via check sums. Those microcores are optimized to control power MOSFET with a small latency time. The PT2000 can control three banks of two injectors each or three banks with one injector per bank for full overlap,

4.2 Features

High-side and low-side pre-drivers

- Seven high-side pre-drivers for logic level N-channel MOSFETs using four programmable slew rates
- Six low-side pre-drivers for logic level N-channel MOSFETs using four programmable slew rates
- Integrated bootstrap circuitry for each high-side pre-driver
- Integrated charge pump circuitry for each high-side pre-driver with 100% duty cycle capability
- Configurable automatic freewheeling capability between high-side and low-side

DC/DC converter

- Two low-side pre-driver, for a logic level N-channel MOSFET, can be optionally dedicated to providing a boost DC-DC converter with four programmable slew rates
- Three different control modes to reduce power dissipation (manual, hysteretic, resonant)

Current measurement

- Four independent current measurement blocks
- Two current measurements (channel 5 and 6) are optionally configurable to support DC/DC converters

Diagnostics and monitoring

- V_{DS} and V_{SRC} monitoring (programmable values) for fault protection and diagnostics
- V_{BOOST} monitoring
- V_{BAT} monitoring
- Temperature monitoring

Integrated end of injection detection

- Accurate detection of end of injection for each high-side source and low-side drain without any external component needed.

Power supplies

- Integrated 7.0 V linear regulator (VCCP) for the HS/LS gate power supply (2)
- Integrated 2.5 V linear regulator (VCC2P5) for the digital core supply based on the VCC5 input supply
- External 5.0 V supply (VCC5)
- Selectable VCCIO external supply (5.0 V or 3.3 V) for digital I/O

Digital block

- Six digital microcores, each with their own ALU, and full access to the system crossbar switch
- Three memory banks: 1024 x 16-bit of code RAM with built-in error detection and 64 x 16-bit of data RAM
- Memory BIST and Logic BIST activated by the SPI, with pass/fail status

Control interface

- 16-bit slave SPI up to 10 MHz - two protocols - programmable slew rate
- 16 general purpose digital IOs able to sustain up to 36 V
- Independent direct pre-driver inhibition input for safety purposes

5 Electrical characteristics

5.1 Maximum ratings

Table 4. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Min.	Max.	Unit	Notes
Electrical ratings					
$V_{BOOSTMAX}$	DC voltage at VBOOST	0	72	V	
V_{BATT}	DC voltage at VBATT	-0.3	72	V	
V_{CC5}	DC voltage at VCC5	-0.3	36	V	
V_{CCIO}	DC voltage at VCCIO	-0.3	36	V	
V_{CC2P5}	DC voltage at VCC2P5	-0.3	3.0	V	
V_{DIG}	DC voltage at CLK, MISO, MOSI, SCLK, CSB, IRQB, RESETB	-0.3	36	V	
V_{DRV_EN}	DC voltage at DRVEN	-0.3	36	V	
V_{STARTX}	DC voltage at STARTx	-0.3	36	V	
V_{FLAGX}	DC voltage at FLAGx	-0.3	36	V	
$V_{START8\_}V_{SENSE}$	Start8 voltage of pins multiplexed with $V_{SENSEN4}$	-1.0 -1.0	18 36	V	(5)
$V_{FLAG4\_}V_{SENSE}$	Flag4 voltage of pins multiplexed with $V_{SENSEP4}$	-2.5 -2.5	18 36	V	(5)
V_{DBG}	DC voltage at DBG	-0.3	36	V	
V_{OA_OUTX}	DC voltage at OA_1, OA_2, OA_3	-0.3	36	V	
V_{DGND}	DC voltage at DGND	-0.3	0.3	V	
V_{AGND}	DC voltage at AGND	-0.3	0.3	V	
V_{CCP}	DC voltage at VCCP	-0.3	9.0	V	
V_{S_HSX}	S_HSx • DC voltage • Transients t <800 ns • Transients t <400 ns	 -3.0 -6.0 -8.0	 $V_{BOOSTMAX}$ $V_{BOOSTMAX}$ $V_{BOOSTMAX}$	V	— (6) (6)
V_{B_HSX}	B_HSx • V_{BATT} -V_{B_HSx} must not exceed 40 V • Transients t <800 ns • Transients t <400 ns	 -0.3 -2.0 -4.0	 V_{S_HSX} + $V_{BS\_HSX\_CL}$	V	— (6) (6)
V_{G_HSX}	DC voltage at G_HSx	V_{S_HSx} - 0.3	V_{B_HSx} +0.3	V	
V_{G_LSX}	G_LSx • DC voltage • Transients t < 5.0 µs; V_{CCP_MAX} = 8.0 V; energy of pulses < 0 V or > V_{CCP} is limited to 2.0 µJ due to capacitive coupling	-0.3 -1.5	V_{CCP} + 0.3 V_{CCP} + 1.5	V	— (6)
V_{D_LSX}	D_LSx • DC voltage • Transients t < 400 ns	-3.0 -8.0	75 75	V	— (6)

Table 4. Maximum ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Min.	Max.	Unit	Notes
$V_{VSENSEN1/2/3}$	DC voltage at VSENSEN1/2/3 • Static at VCC5 < 10 V • Dynamic for max 5.0 µs, 1.0 kHz repetition rate at VCC5, 5.25 V • Dynamic for max 1.0 µs at VCC5 < 5.25 V	 -1.0 -5.0 -15	 1.0 5.0 15	V	— (6) (6)
$V_{VSENSEP1/2/3}$	DC voltage at VSENSEP1/2/3 • DC voltage at VCC5 < 10 V • Dynamic for max 5.0 µs, 1.0 kHz repetition rate at VCC5 < 5.25 V • Dynamic for max 1.0 µs at VCC5 < 5.25 V	 -2.5 -5.0 -15	 2.5 5.0 15	V	— (6) (6)
$V_{VSENSEN5/6}$	DC voltage at VSENSEN5/6 • DC voltage at VCC5 < 10 V • Dynamic for max 5.0 µs, 1.0 kHz repetition rate at VCC5 < 5.25 V • Dynamic for max 1.0 µs at VCC5 < 5.25 V	 -3.0 -5.0 -15	 1.0 5.0 15	V	— (6) (6)
$V_{VSENSEP5/6}$	DC voltage at VSENSEP5/6 • DC voltage at VCC5 < 10 V • Dynamic for max 5.0 µs, 1.0 kHz repetition rate at VCC5 < 5.25 V • Dynamic for max 1.0 µs at VCC5 < 5.25 V	 -4.2 -5.0 -15	 2.5 5.0 15	V	— (6) (6)
ESD voltage					
$V_{ESD-HBM1}$ $V_{ESD-HBM2}$ $V_{ESD-HBM3}$ $V_{ESD-CDM1}$ $V_{ESD-CDM2}$	ESD voltage • Human body model (HBM) VBOOST, VBATT, S_HSx D_LSx All other pins • Machine model Corner pins All other pins	 -4000 -8000 -2000 -750 -500	 4000 8000 2000 750 500	V	(7), (8)
Thermal ratings					
T_A T_J	Operating temperature • Ambient • Junction	 -40 -40	 125 150	°C	
$T_{THRESHOLD}$	Temperature monitoring threshold	167	187	°C	
T_{STG}	Storage ambient temperature	-55	150	°C	
Thermal resistance					
$R_{\theta JA}$	Thermal resistance junction to ambient	—	25.3	°C/W	(9)
$R_{\theta JCTOP}$	Thermal resistance junction to case top	—	13.2	°C/W	(10)
$R_{\theta JCBOTTOM}$	Thermal resistance junction to case bottom	—	0.8	°C/W	(11)

Notes

5. With series resistor of 3.3 kΩ ±20% at the pin
6. Guaranteed by design.
7. Human body model (HBM) per JESD22-A114 - 100 pF, 1.5 kΩ
8. Charge device model (CDM) per JESD22-C101.
9. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal
10. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC - 883 Method 1012.1).
11. Thermal resistance between the die and the solder pad on the bottom of the package based on the simulation without internal resistance

5.2 Power supply electrical characteristics

Table 5. PT2000 static electrical characteristics

Characteristics noted under conditions -40 ºC < T_A < +125 ºC, referenced to ground, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
VBATT input supply						
V_{BATT}	VBATT power supply input voltage, normal operation • Internal VCCP regulator • External VCCP regulator	 5.0 5.0	 13.5 —	 16 72	V	(12)
$V_{BATT\_LOADDUMP}$	VBATT power supply input voltage during load dump duration < 500 ms • Internal VCCP regulator	18	—	40	V	
I_{VBATT_LEAK}	VBATT power supply current in reset state, V_{CC5} = V_{CCIO} = 0.0 V • V_{BATT} = 13.5 V • V_{BATT} = 40 V	 — —	 150 600	 180 800	µA	
I_{VBATT_OPER}	VBATT power supply current in normal operation V_{BATT} = 16 V • DRVEN low, internal VCCP reg. off • DRVEN low, Internal VCCP reg. on • DRVEN high, VCCP max. load 100 mA	 — — —	 0.9 4.5 104.5	 2.5 6.0 106	mA	
I_{VBATT_LEAK}	VBATT power supply current in reset state, V_{CC5} = V_{CCIO} = 0.0 V • V_{BATT} = 13.5 V • V_{BATT} = 40 V	 — —	 150 600	 180 800	µA	
VBOOST input supply						
I_{VBOOST_LEAK}	Leakage current from V_{BOOST}, during reset state with V_{CC5} = V_{CCIO} = 5.0 V • V_{BOOST} = V_{BAT} = 13.5 V • V_{BOOST} = V_{BAT} = 40 V • V_{BOOST} = V_{BAT} = 65 V Contributors (13.5 V): V_{BOOST} volt. div.: 65 µA	 65 240 400	 — — —	 90 370 600	µA	
I_{VBOOST_OPER}	Operating current from V_{BOOST} = 65 V	—	3.9	5.75	mA	
VCC5 input supply						
V_{CC5}	VCC5 supply input voltage	4.75	5.0	5.25	V	
$V_{CC5\_DIGITAL}$	VCC5 supply input voltage for digital part functional only	4.0	5.0	5.25	V	(12)
I_{VCC5}	VCC5 supply current • f_{SYS} = 24 MHz, 7 HS load biasing enabled, no microcore running • f_{SYS} = 24 MHz, 7 HS load biasing enabled, all microcores running • LBIST running, bias disabled	 — — —	 53 65 40	 66.4 81.4 50	mA	(12)
V_{OVVCC5}	VCC5 overvoltage threshold	7.5	8.5	10	V	
V_{OVVCC5_VCCP}	VCC5 overvoltage threshold for VCCP shutdown	6.2	6.9	7.5	V	
$V_{UVVCC5-}$	VCC5 undervoltage low-voltage threshold	4.3	4.45	4.7	V	
$V_{UVVCC5+}$	VCC5 undervoltage high-voltage threshold	4.35	4.5	4.75	V	
V_{UVVCC5_HYST}	VCC5 undervoltage hysteresis	30	50	85	mV	

Notes

12. Guaranteed by design.

Table 5. PT2000 static electrical characteristics (continued)

Characteristics noted under conditions -40 ºC < T_A < +125 ºC, referenced to ground, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
VCC5 input supply (continued)						
T_{FILTER_UVVCC5}	VCC5 UV anti-glitch filter delay time	0.8	1.3	2.0	µs	
VCCIO INPUT SUPPLY						
V_{CCIO}	VCCIO supply input voltage	3.0	—	5.25	V	
I_{VCCIO}	VCCIO supply current • f_{SYS} = 24 MHz, no microcore running • f_{SYS} = 24 MHz, all microcores running	 — —	 38 1.5	 70 —	 µA mA	 — (13)
VCCP input supply						
V_{CCP}	VCCP output voltage, 0.0 mA < I_{VCCP} < 100 mA	6.5	7.0	7.5	V	
V_{CCP_EXT}	V_{CCP} input voltage range (V_{CCP} externally supplied)	5.0	—	9.0	V	
C_{VCCP}	V_{CCP} external output capacitor	1.0	4.7	14	µF	(14)
ΔV_{VCCP}	V_{BATT} to V_{CCP} voltage dropout • V_{BATT} = 5.0 V and I_{VCCP} = -50 mA • V_{BATT} = 5.0 V and I_{VCCP} = -30 mA • V_{BATT} = 5.0 V and I_{VCCP} = -10 mA • V_{BATT} = 5.0 V and I_{VCCP} = -100 mA	 — — — —	 — — — —	 180 110 40 350	 mV	
$V_{UVVCCP-}$	VCCP undervoltage low-voltage threshold	4.3	4.5	4.68	V	
$V_{UVVCCP+}$	VCCP undervoltage high-voltage threshold	4.4	4.55	4.73	V	
V_{UVVCCP_HYST}	VCCP undervoltage hysteresis	30	50	70	mV	
I_{VCCP}	V_{CCP} output current (average during PWM operation) 9.0 V < V_{BATT} < 18 V	—	—	100	mA	
I_{VCCP_MAX}	VCCP output current limitation	150	200	250	mA	
t_{FILTER_UVVCCP}	VCCP UV anti-glitch filter delay time	0.8	1.3	2.0	µs	
VCC2P5 internal regulator						
V_{CC2P5}	VCC2P5 supply output voltage	2.375	2.5	2.625	V	
V_{cc5_BGmin}	Voltage required on VCC5 to start VCC2P5	—	—	3.8	V	
C_{VCC2P5}	VCC2P5 external output capacitor	0.5	1.0	3.0	µF	(15)
I_{VCC2P5}	VCC2P5 supply output current • f_{SYS} = 24 MHz, all microcores running	—	-15	-50	mA	
I_{VCC2P5_LIM}	VCC2P5 supply output current limit	-50	93	140	mA	
$V_{PORESETB-}$	VCC2P5 voltage threshold for asserting PORESETB	2.0	2.11	2.21	V	
$V_{PORESETB+}$	VCC2P5 voltage threshold for deasserting PORSETB	2.07	2.19	2.3	V	
$V_{PORESETB\_HYST}$	PORESETB voltage hysteresis	50	75	100	mV	
$t_{D\_PORESETB}$	PORESETB switching time	—	0.7	1.5	µs	

Notes

13. Guaranteed by design.
14. For VCCP: “For EMC purpose adding 1.0 µF + 100 nF caps in parallel connected to PGND is recommended
15. For VCC2P5: “For EMC purpose adding 1.0 µF + 100 nF caps in parallel connected to DGND is recommended

Table 5. PT2000 static electrical characteristics (continued)

Characteristics noted under conditions -40 ºC < T_A < +125 ºC, referenced to ground, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Battery voltage monitor						
$V_{BATT\_MONITOR}$	Input voltage range	5.0	—	36	V	(16)
R_{VBATT_IN}	Input impedance	350	500	—	kΩ	
G_{VBATT_DIV}	V_{BATT} voltage divider ratio	—	1/16	—		
f_{CVBATT_DIV}	V_{BATT} analog filter cutoff frequency	10	15.5	20	kHz	
V_{VBATT_REF}	DAC reference voltage	2.475	2.5	2.525	V	
$V_{VBATT\_DAC\_LSB}$	DAC LSB	—	39.06	—	mV	
$V_{VBATT\_DAC\_OUT\_MIN}$	DAC minimum output voltage • DAC code = 0h	—	0.0	—	V	
$V_{VBATT\_DAC\_OUT\_MAX}$	DAC maximum output voltage • DAC code = 3Fh	—	2.461	—	V	
ε_{VBATT}	V_{BATT} measurement total error (V_{BATT} > 5.0 V)	-5.0	1.0	5.0	%	
t_{VBATT_DAC}	V_{BATT} DAC settling time	—	—	0.9	µs	
Boost voltage monitor						
$V_{BOOSTMAX}$	Input voltage range	0.0	—	72	V	
R_{VBOOST_IN}	Input impedance	400	640	—	kΩ	
G_{VBOOST_DIV}	V_{BOOST} voltage divider ratio (boost monitor mode)	1/32* 0.996	1/32	1/32* 1.004		
$G_{UV\_VBOOST\_DIV}$	V_{BOOST} voltage divider ratio (UV V_{BOOST} mode)	1/4* 0.996	1/4	1/4* 1.004		
$V_{VBOOST\_DAC\_LSB}$	DAC LSB	—	9.77	—	mV	
ε_{VBOOST}	V_{BOOST} measurement total error (4.85 V to 72 V)	-2.0	—	2.0	%	

Notes

16. This limitation is only for the V_{BAT} ADC, if V_{BAT} is > 36 V, then V_{BAT} monitoring results will saturate. It means in case V_{BAT} > 36 V, the V_{BAT} monitoring feature will not work but device will be 100 % functional until V_{BAT} = 72 V.

5.3 High-side pre-driver electrical characteristics

Table 6. High-side pre-driver electrical characteristics

Characteristics noted under conditions -40 ºC < T_A < +125 ºC, referenced to ground, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
High-side pre-driver						
V_{S_HSX}	S_HSx pin operating voltage Transients t <400 ns Transients t <800 ns	-3.0 -6.0 -8.0	— — —	$V_{BOOSTMAX}$ — —	V	(17)
V_{B_HSX}	B_HSx pin operating voltage	V_{S_HSX} + 4.0	—	V_{S_HSX} + 8.0	V	(17)
$V_{BS\_HSX\_CL}$	B_HSx-S_HSx clamp voltage	6.5	7.3	8.0	V	(18)
V_{G_HSX}	G_HSx operating voltage	V_{S_HSX}	—	V_{B_HSX}	V	(17)
$I_{S\_HSX\_SINK\_OFF}$	S_HSx leakage current biasing switched Off: • V_{S_HSX} = $V_{BOOSTMAX}$ • V_{S_HSX} = 13.5 V • V_{S_HSX} = 7.0 V • V_{S_HSX} = 4.0 V	 — — — —	 — — — —	 1000 250 120 100	µA	
$I_{S\_HSX\_SINK\_ON}$	S_HSx leakage current when pre-driver on (biasing switched Off) • V_{S_HSX} = 7.0 V	—	—	220	µA	
$f_{G\_HSX\_PWM}$	PWM frequency • Internal V_{CCP} and V_{BATT} ≥ 9.0 V • Internal V_{CCP} and 5.0 V ≤ V_{BATT}≤ 9.0 V • External V_{CCP} and 9.0 V ≤ V_{BATT}	 0.0 0.0 0.0	 — — —	 100 50 100	kHz	(17)
DC_{G_HSX}	Duty cycle	0.0	—	100	%	
$t_{ON\_HSX\_MIN}$	High-side driver minimum PWM on time	—	—	1.0	µs	(17)
Q_{G_HSX}	External high-side MOSFET effective gate charge • f_{PWM} ≤ $f_{G\_HSx\_PWM}$ • f_{PWM} ≤ 67 kHz	 — —	 40 55	 50 75	nC	
$I_{G\_HSX\_PWM}$	G_HSx current (average during PWM operation) Q_G = Q_{G_HSX}, f_{PWM} = 100 kHz	—	4.0	5.0	mA	(17)
$I_{G\_HSx\_SRC}$	Peak source gate drive current	—	230	—	mA	(17)
$I_{G\_HSx\_SINK}$	Peak sink gate drive current	—	440	—	mA	(17)
High-side pre-driver dynamic						
$t_{R\_G\_HSX}$	Turn on rise time, 10%-90% of out voltage, V_{CCP} = 7.0 V, at open pin	4.5	—	25	ns	(17)
$t_{F\_G\_HSX}$	Turn off fall time, 90%-10% of out voltage, V_{CCP} = 7.0 V, at open pin	5.0	—	25	ns	(17)
SR_{S_HSX}	Max permissible slew rate at the S_HSX pin	-125	—	600	V/µs	(17)
$t_{DON\_G\_HSX\_300}$	Turn on propagation delay at 300 V/µs slew rate	40	—	100	ns	(17)(19)
$t_{DOFF\_G\_HSX\_300}$	Turn off propagation delay at 300 V/µs slew rate	40	—	100	ns	(17)(19)
$t_{DON\_G\_HSX\_50}$	Turn on propagation delay at 50 V/µs slew rate	65	—	125	ns	(17)(19)
$t_{DOFF\_G\_HSX\_50}$	Turn off propagation delay at 50 V/µs slew rate	50	—	100	ns	(17)(19)

Notes

17. Guaranteed by design.
18. VB_HSx has to be 2.0 V above PGND for full function (switch on) of the pre-driver
19. 10% of output voltage change, C_{LOAD} = 4.7 nF; R_G = 40.2 Ω, V_{CCP} = 7.0 V

Table 6. High-side pre-driver electrical characteristics (continued)

Characteristics noted under conditions -40 ºC < T_A < +125 ºC, referenced to ground, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
High-side pre-driver dynamic (continued)						
$t_{DON\_G\_HSX\_25}$	Turn on propagation delay at 25 V/µs slew rate	100	—	200	ns	(20)(21)
$t_{DOFF\_G\_HSX\_25}$	Turn off propagation delay at 25 V/µs slew rate	70	—	150	ns	(20)(21)
$t_{DON\_G\_HSX\_12.5}$	Turn on propagation delay at 12.5 V/µs slew rate,	160	—	310	ns	(20)(21)
$t_{DOFF\_G\_HSX\_12.5}$	Turn off propagation delay at 12.5 V/µs slew rate	90	—	170	ns	(20)(21)
HS pre-driver safe off						
R_{PD_HSX}	G_HSX to S_HSX pull-down resistor	500	—	2000	kΩ	
Slew rate control						
$R_{DS\_HSX\_P\ (00)}$	G_HSx pMOS $R_{DS(on)}$ (00) 300 V/µs	7.5	14.6	31.4	Ω	
$R_{DS\_HSX\_N\ (00)}$	G_HSx nMOS $R_{DS(on)}$ (00) 300 V/µs	2.5	5.9	16.5	Ω	
$R_{DS\_HSX\_P\ (01)}$	G_HSx pMOS $R_{DS(on)}$ (01) 50 V/µs	61	85	115	Ω	
$R_{DS\_HSX\_N\ (01)}$	G_HSx nMOS $R_{DS(on)}$ (01) 50 V/µs	23	35	50	Ω	
$R_{DS\_HSX\_P\ (10)}$	G_HSx pMOS $R_{DS(on)}$ (10) 25 V/µs	122	169	230	Ω	
$R_{DS\_HSX\_N\ (10)}$	G_HSx nMOS $R_{DS(on)}$ (10) 25 V/µs	47	69	100	Ω	
$R_{DS\_HSX\_P\ (11)}$	G_HSx pMOS $R_{DS(on)}$ (11) 12.5 V/µs	245	337	460	Ω	
$R_{DS\_HSX\_N\ (11)}$	G_HSx nMOS $R_{DS(on)}$ (11) 12.5 V/µs	94	138	199	Ω	

Notes

20. Guaranteed by design.
21. 10% of output voltage change, C_{LOAD} = 4.7 nF; R_G = 40.2 Ω, V_{CCP} = 7.0 V

5.4 Low-side (LS1-LS6) pre-driver electrical characteristics

Table 7. Low-side pre-driver electrical characteristics

Characteristics noted under conditions -40 ºC < T_A < +125 ºC, referenced to ground, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Low-side pre-driver LS1-6						
V_{G_LSx}	G_LSx operating voltage	0.0	—	V_{CCP}	V	(22)
$I_{S\_LSx\_sink}$	D_LSx leakage current (biasing switched off) • V_{D_LSx} = 13.5 V • V_{D_LSx} = 40 V	 10 10	 — —	 110 320	µA	
$f_{G\_LSx\_PWM}$	PWM frequency • Nominal • Short period of switching during 50 µs every 1ms	 0.0 0.0	 — —	 100 200	kHz	(22)
DC_{G_LSx}	Duty cycle	0.0	—	100	%	(22)
Q_{G_LSx}	External low-side MOSFET effective gate charge • $f_{PWM} \leq f_{G\_LSx\_PWM}$ • $f_{PWM} \leq 67$ kHz • $f_{PWM} \leq 50$ kHz	 — — —	 30 55 —	 50 75 100	nC	

Notes

22. Guaranteed by design.

Table 7. Low-side pre-driver electrical characteristics (continued)

Characteristics noted under conditions -40 ºC < T_A < +125 ºC, referenced to ground, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Low-side pre-driver LS1-6 (continued)						
$I_{G\_LSx\_PWM}$	G_LSx current (average during PWM operation) • QG = QG_LSX; f_{PWM} = 100 kHz	—	3.0	5.0	mA	(23)
$I_{G\_LSx\_SRC}$	Peak source gate drive current	—	230	—	mA	(23), (24)
$I_{G\_LSx\_SINK}$	Peak sink gate drive current	—	440	—	mA	(23), (24)
Dynamic low-side pre-driver LS1-6						
$T_{R\_G\_LSX}$	Turn on rise time, 10% to 90% of output voltage; VCCP = 7.0 V; at open pin	5.0	—	25	ns	(23)
$T_{F\_G\_LSX}$	Turn off fall time, 90% to 10% of output voltage; VCCP = 7.0 V; at open pin	5.0	—	25	ns	(23)
$T_{DON\_G\_LSX\_300}$	Turn on propagation delay at 300 V/µs slew rate	10	—	70	ns	(23), (25)
$T_{DOFF\_G\_LSX\_300}$	Turn off propagation delay at 300 V/µs slew rate	10	—	70	ns	(23), (25)
$T_{DON\_G\_LSX\_50}$	Turn on propagation delay at 50 V/µs slew rate	10	—	80	ns	(23), (25)
$T_{DOFF\_G\_LSX\_50}$	Turn off propagation delay at 50 V/µs slew rate	10	—	80	ns	(23), (25)
$T_{DON\_G\_LSX\_25}$	Turn on propagation delay at 25 V/µs slew rate	15	—	120	ns	(23), (25)
$T_{DOFF\_G\_LSX\_25}$	Turn off propagation delay at 25 V/µs slew rate	15	—	120	ns	(23), (25)
$T_{DON\_G\_LSX\_12.5}$	Turn on propagation delay at 12.5 V/µs slew rate	15	—	150	ns	(23), (25)
$T_{DOFF\_G\_LSX\_12.5}$	Turn off propagation delay at 12.5 V/µs slew rate	15	—	150	ns	(23), (25)
LS pre-driver safe off						
R_{PD_LSX}	G_LSX to PGND pull-down resistor	25	50	90	kΩ	
Low-side pre-driver LS1-6						
$R_{DS\_LSX\_P\ (00)}$	G_LSx pMOS $R_{DS(on)}$ (00) 300 V/µs	7.5	14.6	31.3	Ω	
$R_{DS\_LSX\_N\ (00)}$	G_LSx nMOS $R_{DS(on)}$ (00) 300 V/µs	2.5	5.9	16.5	Ω	
$R_{DS\_LSX\_P\ (01)}$	G_LSx pMOS $R_{DS(on)}$n (01) 50 V/µs	61	84	115	Ω	
$R_{DS\_LSX\_N\ (01)}$	G_LSx nMOS $R_{DS(on)}$ (01) 50 V/µs	23	35	50	Ω	
$R_{DS\_LSX\_P\ (10)}$	G_LSx pMOS $R_{DS(on)}$ (10) 25 V/µs	122	170	230	Ω	
$R_{DS\_LSX\_N\ (10)}$	G_LSx nMOS $R_{DS(on)}$ (10) 25 V/µs	47	69	100	Ω	
$R_{DS\_LSX\_P\ (11)}$	G_LSx pMOS $R_{DS(on)}$ (11) 12.5 V/µs	245	337	460	Ω	
$R_{DS\_LSX\_N\ (11)}$	G_LSx nMOS $R_{DS(on)}$ (11) 12.5 V/µs	94	138	199	Ω	

Notes

23. Guaranteed by design.
24. V_{CCP} = V_{GS} = 7.0 V and fastest slew rate
25. 10% of output voltage change; C_{LOAD} = 4.7 nF; R_G = 40.2 Ω; V_{CCP} = 7.0 V

5.5 Low-side high-speed (LS7-LS8) pre-driver electrical characteristics

Table 8. High-speed low-side pre-driver electrical characteristics

Characteristics noted under conditions -40 ºC < T_A < +125 ºC, referenced to ground, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Low-side pre-driver 7 and 8						
$V_{G\_LS7/8}$	G_LS7/8 operating voltage	0.0	—	V_{CCP}	V	(26)
$f_{G\_LS7/8\_PWM}$	PWM frequency	0.0	—	400	kHz	(27)
$DC_{G\_LS7/8}$	Duty cycle	0.0	—	100	%	(27)
$Q_{G\_LS7/8}$	External low-side MOSFET gate charge • f_{PWM} = 400 kHz • f_{PWM} = 300 kHz • f_{PWM} = 240 kHz	 — — —	 30 30 30	 60 75 100	nC	
$I_{G\_LS7/8\_PWM}$	G_LS7/8 current (average during PWM operation) • f_{PWM} = 400 kHz • f_{PWM} = 300 kHz • f_{PWM} = 100 kHz • f_{PWM} = 50 kHz	 — — — —	 12 9.0 3.0 1.5	 24 22.5 7.5 3.75	mA	(27)
$I_{G\_LS7/8\_SRC}$	Peak source gate drive current	—	680	—	mA	(27), (27)
$I_{G\_LS7/8\_SINK}$	Peak sink gate drive current	—	2200	—	mA	(27), (27)
Dynamic low-side pre-driver L7 and 8						
$t_{R\_G\_LS7/8\_1500}$	Turn on rise time • at 1500 V/µs slew rate 10% to 90% of out voltage; V_{CCP} =7.0 V; at the open pin	3.5	—	11	ns	(27)
$t_{F\_G\_LS7/8\_1500}$	Turn off fall time • at 1500 V/µs slew rate 90% to 10% of out voltage; V_{CCP} = 7.0 V; at the open pin	3.5	—	11	ns	(27)
$t_{R\_G\_LS7/8}$	Turn on rise time • at 300-25 V/µs slew rate 10% to 90% of out voltage; V_{CCP} = 7.0 V; at the open pin	5.0	—	25	ns	(27)
$t_{F\_G\_LS7/8}$	Turn off fall time • at 300-25 V/µs slew rate 90% to 10% of out voltage; V_{CCP} = 7.0 V; at the open pin	5.0	—	25	ns	(27)
$t_{DON\_G\_LS7\_1500}$	Turn on propagation delay • at 1500 V/µs slew rate 10% of out voltage change	10	—	50	ns	(27), (28)
$t_{DOFF\_G\_LS7\_1500}$	Turn off propagation delay • at 1500 V/µs slew rate 10% of out voltage change	10	—	50	ns	(27), (28)
$t_{DON\_G\_LS7\_300}$	Turn on propagation delay • at 300 V/µs slew rate 10% of out voltage change	10	—	70	ns	(27), (28)
$t_{DOFF\_G\_LS7\_300}$	Turn off propagation delay • at 300 V/µs slew rate 10% of out voltage change	10	—	70	ns	(27), (28)

Notes

26. Guaranteed by design.
27. At the fastest slew rate setting with minimum R_{G_LS8} of 2.0 Ω and V_{CCP}/V_{GS} = 7.0 V
28. C_{LOAD} = 4.7 nF; R_G = 40.2 Ω, V_{CCP} = 7.0 V

Table 8. High-speed low-side pre-driver electrical characteristics (continued)

Characteristics noted under conditions -40 ºC < T_A < +125 ºC, referenced to ground, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Dynamic low-side pre-driver L7 and 8						
$t_{DON\_G\_LS7\_50}$	Turn on propagation delay • at 50 V/µs slew rate 10% of out voltage change	15	—	100	ns	(29), (30)
$t_{DOFF\_G\_LS7\_50}$	Turn off propagation delay • at 50 V/µs slew rate 10% of out voltage change	15	—	100	ns	(29), (30)
$t_{DOFF\_G\_LS7\_25}$	Turn off propagation delay • at 25 V/µs slew rate 10% of out voltage change	15	—	120	ns	(29), (30)
$t_{DOFF\_G\_LS7\_25}$	Turn off propagation delay • at 25 V/µs slew rate 10% of out voltage change	15	—	120	ns	(29), (30)
$R_{PD\_LS7/8}$	G_LS7/8 to PGND pull-down resistor	25	50	90	kΩ	
Slew rate control low-side 7 and 8						
$R_{DS\_HSX\_P\ (00)}$	G_LS7/8 pMOS $R_{DS(on)}$ (00) 1500 V/µs	2.6	5.0	10.7	Ω	
$R_{DS\_HSX\_N\ (00)}$	G_LS7/8 nMOS $R_{DS(on)}$ (00) 1500 V/µs	0.5	1.1	2.9	Ω	
$R_{DS\_HSX\_P\ (01)}$	G_LS7/8 pMOS $R_{DS(on)}$ (01) 300 V/µs	7.5	14.6	31.3	Ω	
$R_{DS\_HSX\_N\ (01)}$	G_LS7/8 nMOS $R_{DS(on)}$ (01) 300 V/µs	2.5	5.9	16.5	Ω	
$R_{DS\_HSX\_P\ (10)}$	G_LS7/8 pMOS $R_{DS(on)}$ (10) 50 V/µs	61	85	115	Ω	
$R_{DS\_HSX\_N\ (10)}$	G_LS7/8 nMOS $R_{DS(on)}$ (10) 50 V/µs	23	35	50	Ω	
$R_{DS\_HSX\_P\ (11)}$	G_LS7/8 pMOS $R_{DS(on)}$ (11) 25 V/µs	122	170	230	Ω	
$R_{DS\_HSX\_N\ (11)}$	G_LS7/8 nMOS $R_{DS(on)}$ (11) 25 V/µs	47	69	100	Ω	

Notes

29. Guaranteed by design.
30. C_{LOAD} = 4.7 nF; R_G = 40.2 Ω, V_{CCP} = 7.0 V

5.6 High-side VDS VSRC monitoring electrical characteristics

Table 9. High-side VDS/SRC monitor electrical characteristics

Characteristics noted under conditions -40 ºC < T_A < +125 ºC, referenced to ground, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
High-side $V_{DS/SRC}$ monitor						
$V_{S\_HS\_VDS}$	High-side $V_{DS/SRC}$ monitoring functional range S_HSx • DC voltage • Transients t < 400 ns • Transients t < 800 ns	 -3.0 -6.0 -8.0	 — — —	 72 72 72	V	(31)
V_{VBATT_VDS}	High-side $V_{DS/SRC}$ monitoring functional range S_HSx • Full functionality • Limited functionality ($V_{DS\_HS\_Th}$ 3.5 V is at 3.0 V min)	 5.5 5.0	 — —	 72 5.5	V	
V_{VBOOST_VDS}	High-side $V_{DS/SRC}$ monitoring functional range VBOOST • Full functionality • Limited functionality ($V_{DS\_HS\_Th}$ 3.5 V is at 3.0 V min)	 5.5 5.0	 — —	 72 5.5	V	

Notes

31. Guaranteed by design.

Table 9. High-side VDS/SRC monitor electrical characteristics (continued)

Characteristics noted under conditions -40 ºC < T_A < +125 ºC, referenced to ground, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
High-side $V_{DS/SRC}$ monitor (continued)						
$V_{DS\_HS\_TH\ (0000)}$	High-side V_{DS} threshold (0000)	-0.03	0.0	0.03	V	
$V_{DS\_HS\_TH\ (1001)}$	High-side V_{DS} threshold (1001)	0.07	0.10	0.13	V	
$V_{DS\_HS\_TH\ (1010)}$	High-side V_{DS} threshold (1010)	0.155	0.2	0.245	V	
$V_{DS\_HS\_TH\ (1011)}$	High-side V_{DS} threshold (1011)	0.25	0.3	0.35	V	
$V_{DS\_HS\_TH\ (1100)}$	High-side V_{DS} threshold (1100)	0.345	0.4	0.455	V	
$V_{DS\_HS\_TH\ (0001)}$	High-side V_{DS} threshold (0001)	0.44	0.5	0.56	V	
$V_{DS\_HS\_TH\ (0010)}$	High-side V_{DS} threshold (0010)	0.9	1.0	1.1	V	
$V_{DS\_HS\_TH\ (0011)}$	High-side V_{DS} threshold (0011)	1.35	1.5	1.65	V	
$V_{DS\_HS\_TH\ (0100)}$	High-side V_{DS} threshold (0100)	1.8	2.0	2.2	V	
$V_{DS\_HS\_TH\ (0101)}$	High-side V_{DS} threshold (0101)	2.29	2.45	2.61	V	
$V_{DS\_HS\_TH\ (0110)}$	High-side V_{DS} threshold (0110)	2.76	2.95	3.14	V	
$V_{DS\_HS\_TH\ (0111)}$	High-side V_{DS} threshold (0111) • V_{VBATT_VDS} = 5.5 V to 72 V, V_{VBOOST_VDS} = 5.5 V to 72 V • V_{VBATT_VDS} = 5.0 V to 5.5 V, V_{VBOOST_VDS} = 5.0 V to 5.5 V	 3.23 3.00	 3.45 3.45	 3.67 3.67	V	
t_{TH_HSVDS}	High-side $V_{DS/SRC}$ threshold settling time	—	0.4	1.0	µs	
$V_{SRC\_HS\_TH\ (0000)}$	High-side V_{SRC} threshold (0000)	-0.03	0.0	0.03	V	
$V_{SRC\_HS\_TH\ (1001)}$	High-side V_{SRC} threshold (1001)	0.07	0.10	0.13	V	
$V_{SRC\_HS\_TH\ (1010)}$	High-side V_{SRC} threshold (1010)	0.155	0.2	0.245	V	
$V_{SRC\_HS\_TH\ (1011)}$	High-side V_{SRC} threshold (1011)	0.25	0.3	0.35	V	
$V_{SRC\_HS\_TH\ (1100)}$	High-side V_{SRC} threshold (1100)	0.345	0.4	0.455	V	
$V_{SRC\_HS\_TH\ (0001)}$	High-side V_{SRC} threshold (0001)	0.44	0.5	0.56	V	
$V_{SRC\_HS\_TH\ (0010)}$	High-side V_{SRC} threshold (0010)	0.9	1.0	1.1	V	
$V_{SRC\_HS\_TH\ (0011)}$	High-side V_{SRC} threshold (0011)	1.35	1.5	1.65	V	
$V_{SRC\_HS\_TH\ (0100)}$	High-side V_{SRC} threshold (0100)	1.8	2.0	2.2	V	
$V_{SRC\_HS\_TH\ (0101)}$	High-side V_{SRC} threshold (0101)	2.38	2.55	2.72	V	
$V_{SRC\_HS\_TH\ (0110)}$	High-side V_{SRC} threshold (0110)	2.85	3.0	3.15	V	
$V_{SRC\_HS\_TH\ (0111)}$	High-side V_{SRC} threshold (0111)	3.33	3.5	3.68	V	

5.7 Low-side VDS VSRC monitoring electrical characteristics

Table 10. Low-side $V_{DS/SRC}$ monitor electrical characteristics

Characteristics noted under conditions -40 ºC < T_A < +125 ºC, referenced to ground, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Low-side V_{DS} monitor						
$V_{D\_LSX\_VDS}$	Low-side V_{DS} monitoring functional range D_LSx • DC voltage • Transients t < 400 ns	 -3.0 -8.0	 — —	 75 75	V	
$V_{DS\_LS\_TH\ (0000)}$	Low-side V_{DS} threshold (0000)	-0.03	0.0	0.03	V	
$V_{DS\_LS\_TH\ (1001)}$	Low-side V_{DS} threshold (1001)	0.07	0.10	0.13	V	
$V_{DS\_LS\_TH\ (1010)}$	Low-side V_{DS} threshold (1010)	0.155	0.2	0.245	V	
$V_{DS\_LS\_TH\ (1011)}$	Low-side V_{DS} threshold (1011)	0.25	0.3	0.35	V	
$V_{DS\_LS\_TH\ (1100)}$	Low-side V_{DS} threshold (1100)	0.345	0.4	0.455	V	
$V_{DS\_LS\_TH\ (0001)}$	Low-side V_{DS} threshold (0001)	0.44	0.5	0.56	V	
$V_{DS\_LS\_TH\ (0010)}$	Low-side V_{DS} threshold (0010)	0.9	1.0	1.1	V	
$V_{DS\_LS\_TH\ (0011)}$	Low-side V_{DS} threshold (0011)	1.35	1.5	1.65	V	
$V_{DS\_LS\_TH\ (0100)}$	Low-side V_{DS} threshold (0100)	1.8	2.0	2.2	V	
$V_{DS\_LS\_TH\ (0101)}$	Low-side V_{DS} threshold (0101)	2.38	2.5	2.63	V	
$V_{DS\_LS\_TH\ (0110)}$	Low-side V_{DS} threshold (0110)	2.85	3.0	3.15	V	
$V_{DS\_LS\_TH\ (0111)}$	Low-side V_{DS} threshold (0111)	3.33	3.5	3.68	V	
t_{TH_LSVDS}	Low-side V_{DS} threshold settling time	—	0.4	1.0	µs	(32)
Low-side V_{DS} monitor D_ls7/D_ls8 for DC/DC						
$V_{D\_LSX\_VDS}$	Low-side V_{DS} voltage range D_LSx	-3.0	—	75	V	
$V_{DS\_LS\_TH\_DC\ (0100)}$	Low-side V_{DS} threshold for DC/DC (0100)	1.8	2.06	2.2	V	
$V_{DS\_LS\_TH\_DC\ (0101)}$	Low-side V_{DS} threshold for DC/DC (0101)	2.25	2.5	2.75	V	
$t_{VDS\_DCDC\_PD}$	Comparator propagation delay time	—	—	50	ns	(32)
$R_{VDS\_78\_IN}$	Input impedance V_{DS_78}	200	350	—	kΩ	

Notes

32. Guaranteed by design.

5.8 Load bias electrical characteristics

Table 11. Load bias electrical characteristics

Characteristics noted under conditions -40 ºC < T_A < +125 ºC, referenced to ground, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Load biasing structures						
I_{BIAS_HS}	Current source normal S_HSx (x = 1…7)	2.8	4.0	5.2	mA	(33)
$I_{BIAS\_HS\_STRONG}$	Current source strong S_HSx (x = 2, 4)	4.2	6.0	7.8	mA	(34)
$I_{BIAS\_HS\_BOTH}$	Current source strong + normal S_HSx (x = 2, 4)	7.0	10	13	mA	(35)
$I_{BIAS\_HS\_MAX}$	Total maximum current source S_HSx source current	36.4	—	—	mA	
I_{BIAS_LS}	Current source D_LSx sink saturation current	0.98	1.09	1.2	mA	
V_{BIAS_HS}	S_HSx bias voltage regulation • V_{BATT} > 8.0 V, V_{CC5} > 4.75 V • V_{BATT} < 8.0 V, V_{CC5} > 4.75 V	3.8 (V_{BATT}/2) -200 mV	— (V_{BATT}/2)	V_{CC5} (V_{BATT}/2) 200 mV	V	
R_{BIAS_LS}	Equivalent resistance of LS current source • V_{D_LSx} < 1.0 V	0.5	—	1.5	kΩ	

Notes

33. Current source can be connected to maximum two D_LSx
34. Current source can be connected to maximum three D_LSx
35. Current source can be connected to maximum five D_LSx

5.9 Current measurement electrical characteristics

5.9.1 Current measurement for positive current

This section is applicable for all current measurement paths for positive currents:

- Current measurement channel 1- 4
  - Differential amplifier 1- 4
  - DAC 1- 4
  - Comparator 1- 4
- Current measurement channel 5 - 6
  - Differential amplifier 5 - 6
  - DAC 5 - 6H and DAC 5 - 6L
  - Comparator 5 - 6H and 5 - 6L

Table 12. Current measurement for positive currents

Symbol	Characteristic	Statistically evaluated	Unit	Notes
ε_{CS}	Overall current sense error including gain errors and offsets at DAC range of 75% - 100%, after analog offset compensation • at GDA_diff (00) = 5.8 • at GDA_diff (01) = 8.7 • at GDA_diff (10) = 12.6 • at GDA_diff (11) = 19.3	 ±3.5 ±3.5 ±3.5 ±3.5	%	(36), (37)
	At DAC range of 25% to 75%, after analog offset compensation • at GDA_diff (00) = 5.8 • at GDA_diff (01) = 8.7 • at GDA_diff (10) = 12.6 • at GDA_diff (11) = 19.3	 ±5.3 ±5.3 ±5.3 ±5.3	%	(36), (37)

Notes

36. Guaranteed by design.
37. The tolerance of the 10 mΩ shunt resistor is assumed as ±2.0% (at 4.5 σ). All other input tolerances from the device specification are assumed at 6 σ.

Table 13. Differential amplifier 1, 2, 3, 4, 5, and 6

Characteristics noted under conditions -40 ºC < T_A < +125 ºC, referenced to ground, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
$V_{VSENSENX\_DA}$	Differential amplifier x functional range $V_{SENSENx}$ (x = 1…6)	-1.0	—	1.0	V	
$V_{VSENSEPX\_DA}$	Differential amplifier x functional range $V_{SENSEPx}$ (x = 1…6)	-1.0	—	1.5	V	
$V_{DA\_DIFF\_IN\ (00)}$	Differential input voltage range (00) • $G_{DA\_DIFF(00)}$ = 5.8	-25.9	—	387	mV	
$V_{DA\_DIFF\_IN\ (01)}$	Differential input voltage range (01) • $G_{DA\_DIFF(01)}$ = 8.7	-17.3	—	258	mV	
$V_{DA\_DIFF\_IN\ (10)}$	Differential input voltage range (10) • $G_{DA\_DIFF(10)}$ = 12.6	-12	—	179	mV	
$V_{DA\_DIFF\_IN\ (11)}$	Differential input voltage range (11) • $G_{DA\_DIFF(11)}$ = 19.3	-7.8	—	116	mV	
$G_{DA\_DIFF\ (00)}$	Differential voltage gain (00)	5.71	5.79	5.87		
$G_{DA\_DIFF\ (01)}$	Differential voltage gain (01)	8.55	8.68	8.81		
$G_{DA\_DIFF\ (10)}$	Differential voltage gain (10)	12.32	12.53	12.74		

Table 13. Differential amplifier 1, 2, 3, 4, 5, and 6 (continued)

Characteristics noted under conditions -40 ºC < T_A < +125 ºC, referenced to ground, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
$G_{DA\_DIFF\ (11)}$	Differential voltage gain (11)	18.92	19.25	19.58		
$t_{DA\_GAIN\_SW}$	Gain switching settling time		—	2.0	µs	(38)
$R_{VSENSENX\_IN}$	Input impedance $V_{SENSENx}$ (x = 1…4) • 1.0 V common mode voltage	10	—	26	kΩ	
$R_{VSENSEPX\_IN}$	Input impedance $V_{SENSEPx}$ (x = 1…4) • 1.0 V common mode voltage	10	—	26	kΩ	
C_{VSENSE}	Differential amplifier EMI filter C. It is recommended to place a filter C between V_{SENSE}N and P close to the IC for EMI.	—	330	—	pF	
V_{DA_BIAS}	Output bias voltage	240	250	265	mV	
$V_{DA\_OUT\_OFF}$	Maximum output offset voltage error at maximum gain	-140	—	220	mV	
V_{DA_OUT}	Differential amplifier x output voltage range	0.1	—	2.7	V	
DAC 1, 2, 3, 4, 5L, 5H, 6H, and 6L (8-bit)						
V_{DAC_LSB}	DAC LSB	—	9.77	—	mV	
$V_{DAC\_OUT\_MIN}$	DAC minimum output voltage • DAC code = 0h	—	0.0	—	V	
$V_{DAC\_OUT\_MAX}$	DAC maximum output voltage • DAC code = FFh	—	2.49	—	V	
ε_{DAC_DNL}	DAC differential linearity error	-0.5	—	0.5	LSB	
ε_{DAC_INL}	DAC integral linearity error	-1.0	—	1.0	LSB	
$V_{DAC\_OUT\_OFF}$	DAC maximum output offset	0.0	—	10	mV	
t_{DAC}	DAC settling time	—	—	0.9	µs	
Voltage comparator 1, 2, 3, 4, 5H, 5L, 6H, and 6L						
V_{COMP_IN}	Comparator input voltage	0.0	—	2.7	V	
$V_{COMP\_IN\_OFF}$	Comparator input offset voltage	-25	—	10	mV	
Current measurement channel 1, 2, 3, 4, 5, and 6 detection delays						
t_{D_CS}	Detection delay coming from differential amplifier and comparator at GDA_DIFF(00) = 5.8	20		500	ns	(38)

Notes

38. Guaranteed by design.