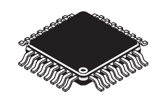
Dual DSI master transceiver

33SA0528

Automotive restraint system



AC SUFFIX (PB-FREE)
98ASH70029A
32-PIN LQFP

The 33SA0528 is a third generation SMARTMOS standalone, dual-channel distributed system interface (DSI) master device.

Each of the two independent channels contain a differential driver and a dual adder receiver. The embedded DSI protocol engine converts the DSI data between the physical interface and the two redundant SPI interfaces. The MCU can control and configure the 33SA0528 and extract all of the slaves transceivers data from it via the dual SPI.

To ensure the communication reliability, the 33SA0528 uses an on-chip band gap reference regulator to monitor all of the supply voltages, and uses an on-chip oscillator to monitor the PLL clock for the external clock error detection.

Features

- Two independent DSI master channels
- Supports command and response mode for slave configuration
- Supports periodic data collection mode (PDCM) for periodic slave data transfers
- Supports discovery mode for slave physical address self-programming
- 10 MHz 32-bit dual SPI: main SPI for device configuration and DSI operation, and redundant SPI for safety purposes
- Point-to-point, parallel, daisy chain bus topologies
- Various diagnostic features

Applications

- Automotive airbag and safety
- Industrial systems
- Sense and trigger applications

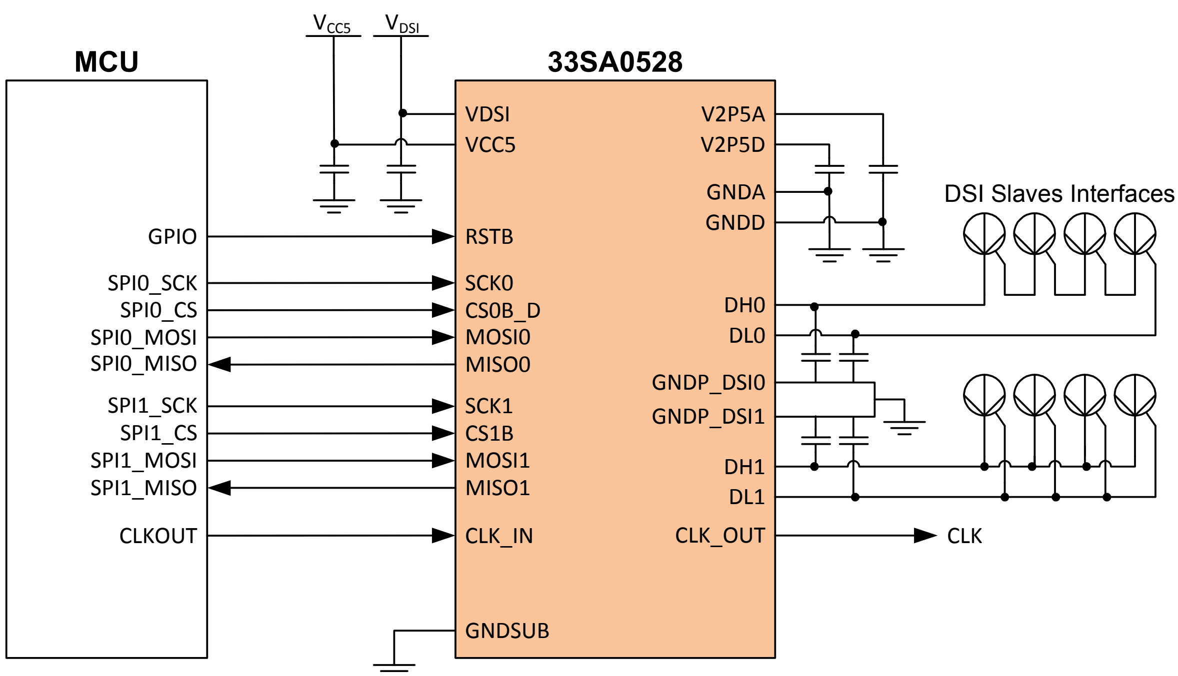


Figure 1. 33SA0528 simplified application diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table of Contents

1 Orderable parts

This section describes the part numbers available to be purchased along with their differences.

Table 1. Orderable part variations

Part number	Notes	Temperature (T_A)	Package
MC33SA0528AC	[1]	-40 °C to 125 °C	32-PIN LQFP

Notes

1. To order parts in tape & reel, add the R2 suffix to the part number.

2 Internal block diagram

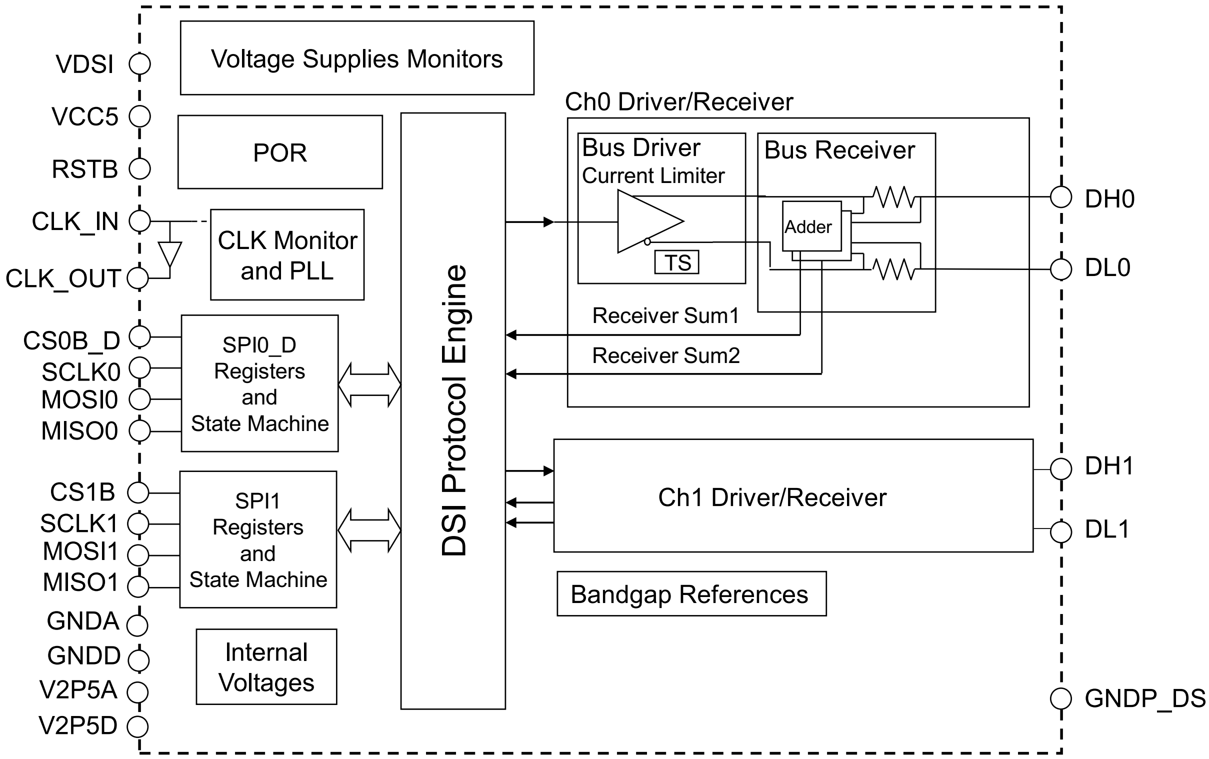


Figure 2. 33SA0528 simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

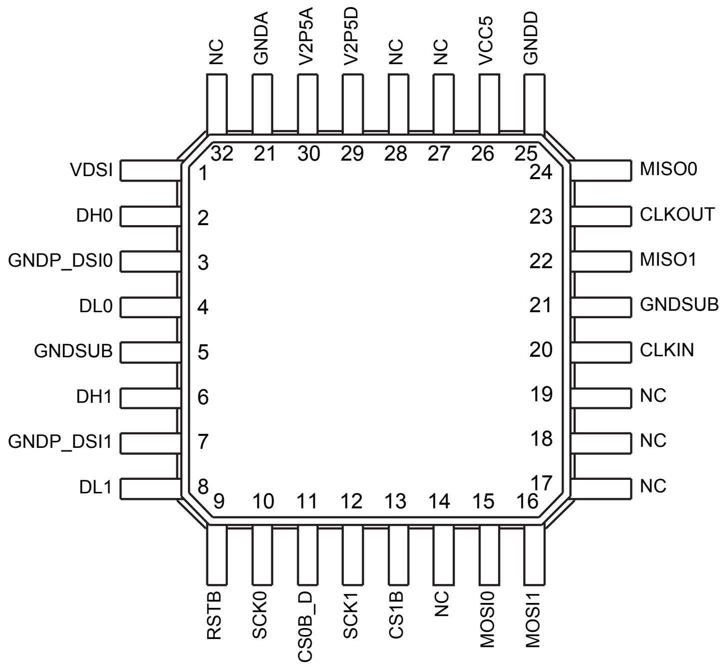


Figure 3. 33SA0528 32-pin LQFP pinout diagram

3.2 Pin definitions

A functional description of each pin can be found in the functional pin description section beginning on page 9.

Table 2. 33SA0528 pin definitions

Pin number	Pin name	Pin function	Definition
1	VDSI	Power	This supply input is used to provide the positive level output of buses
2	DH0	Output driver	Bus 0 high-side
3	GND_DSI0	Ground	Bus power return
4	DL0	Output driver	Bus 0 low-side
5	GNDSUB	Ground	This pin must be tied to ground in the application.
6	DH1	Output driver	Bus 1 high-side
7	GND_DSI1	Ground	Bus power return
8	DL1	Output driver	Bus 1 low-side
9	RSTB	Reset	A low level on this pin returns all registers to a known initial state.
10	SCK0	Input	Clocks data in from and out to DSI_SPI0. MISO0 data changes on the negative transition of SCLK0. MOSI0 is sampled on the positive edge of SCLK0
11	CS0B_D	Input	When this signal is high, SPI signals on DSI_SPI0 are ignored. Asserting this pin low starts a DSI_SPI0 transaction. The DSI_SPI0 transaction is signaled as completed when this signal returns high
12	SCK1	Input	Clocks data in from and out to DSI_SPI1. MISO1 data changes on the negative transition of SCLK1. MOSI1 is sampled on the positive edge of SCLK1

Table 2. 33SA0528 pin definitions(continued)

Pin number	Pin name	Pin function	Definition
13	CS1B	Input	When this signal is high, SPI signals on DSI_SPI1 are ignored. Asserting this pin low starts a DSI_SPI1 transaction. The DSI_SPI1 transaction is signaled as completed when this signal returns high
14	N.C	—	This pin is not internally connected and must be left unconnected or tied to ground in the application
15	MOSI0	Input	SPI data into DSI_SPI0. This data input is sampled on the positive edge of SCLK0
16	MOSI1	Input	SPI data into DSI_SPI1. This data input is sampled on the positive edge of SCLK1
17	N.C	—	This pin is not internally connected and must be left unconnected or tied to ground in the application
18	N.C	—	This pin is not internally connected and must be left unconnected or tied to ground in the application
19	N.C	—	This pin is not internally connected and must be left unconnected or tied to ground in the application
20	CLK_IN	Input	4.0 MHz clock input
21	GNDSUB	Ground	This pin must be tied to ground in the application
22	MISO1	Output	DSI_SPI1 data sent to the MCU by this device. This data output changes on the negative edge of SCLK1. When CS1B_D is high, this pin is high
23	CLK_OUT	Output	Output buffered clock signal that is input from CLK_IN
24	MISO0	Output	DSI_SPI0 data sent to the MCU by this device. This data output changes on the negative edge of SCLK0. When CS0B_D is high, this pin is set at high impedance
25	GNDD	Ground	Ground for the digital circuits. Ground for IDDQ. This pin should be tied to MCU ground
26	VCC5	Power	Regulated 5.0 V input
27	N.C	—	This pin is not internally connected and must be left unconnected or tied to ground in the application
28	N.C	—	This pin is not internally connected and must be left unconnected or tied to ground in the application
29	V2P5D	Output	0.1 μF capacitor should be connected between this pin and ground
30	V2P5A	Output	0.1 μF capacitor should be connected between this pin and ground
31	GNDA	Ground	Ground for the analog circuits. This pin is not connected internally to the other grounds on the chip. It should be connected to a quiet ground on the board
32	N.C	—	This pin is not internally connected and must be left unconnected or tied to ground in the application

4 General product characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min.	Max.	Unit	Notes
Electrical ratings					
V_{DSI}	DSI bus voltage supply • Steady-state	-0.3	10	V	
V_{CC5}	V_{CC} logic supply voltage	-0.3	7.0	V	
V_{2P5A}	Regulated output voltage	-0.3	3.0	V	
V_{2P5D}	Regulated output voltage	-0.3	3.0	V	
V_{LOGIC}	Voltage on logic input/output pins	-0.3	V_{CC5} + 3.0	V	
I_{LOGIC}	Current on logic input/output pins	—	20	mA	
V_{BUS}	Voltage on DSI bus pins	-0.3	20	V	
I_{BUS}	Current on DSI bus pins	—	200	mA	
V_{ESD}	ESD voltage • Human body model (HBM) • Machine model (MM) • Charge device model (CDM)	 — — —	 ±2000 ±150 ±500	V	(2)

Notes

2. ESD testing is performed in accordance with the human body model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the machine model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the charge device model.

4.2 Thermal characteristics

Table 4. Thermal ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min.	Max.	Unit	Notes
T_A T_J	Operating temperature • Ambient • Junction	 -40 -40	 105 150	°C	
T_{STG}	Storage temperature	-55	150	°C	
T_{SD}	Thermal shutdown (bus driver)	155	195	°C	

4.3 Operating conditions

This section describes the operating conditions of the device. Conditions apply to all the following data, unless otherwise noted.

Table 5. Operating conditions

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Min.	Max.	Unit	Notes
V_{DSI}	Full characteristics are guaranteed	9.0	9.6	V	
V_{DSI}	Some characteristics are out of specification, but the 33SA0528 can communicate with the bus slaves	8.8	9.0	V	
V_{DSI}	Some characteristics are out of specification, but the V_{DSI} monitor is active, so the RNE bit is never set	8.2	8.8	V	
V_{CC5}	Functional operating VCC5 voltage	4.8	5.25	V	

4.4 Supply currents

This section describes the current consumption characteristics of the device, as well as the conditions for the measurements.

Table 6. Supply currents

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device. Typical values noted reflect the approximate parameter mean at T_A = 25 °C.

Symbol	Ratings	Min.	Typ.	Max.	Unit	Notes
I_{VDSI}	Current on DSI bus • 9.6 V (disabled) • 9.6 V (enabled 1.0 mA/channel) • 9.6 V (enabled 40 mA/channel)	 8.0 18 96	 11 24 108	 13 30 114	mA	(3)
I_{VCC}	Current on VCC5 supply	—	—	2.0	mA	

Notes

3. I_{OUT} is the total current for all sensors connected to two DSI interfaces. For example: If 40 mA is flowing out (DHx to DLx) on each DSI channel, then I_{OUT} = 2 x 40 mA = 80 mA. The max. internal current flowing from VDSI to GND is '28 mA + (80 mA/14) = 34 mA'. The max. total current is flowing from VDSI (includes sensor current) is '34 mA + 80 mA = 114 mA'. If the DSI channel-0 is enabled and 40 mA is flowing out (DHx to DLx), the other DSI channel (ch1) is the disabled case. The max. internal current flowing from VDSI to GND is '19 mA + (40 mA/14) = 22 mA'. The Max. total current flowing from VDSI (include sensor current) is '22 mA + 40 mA = 62 mA'.

5 General IC functional description

5.1 Block diagram

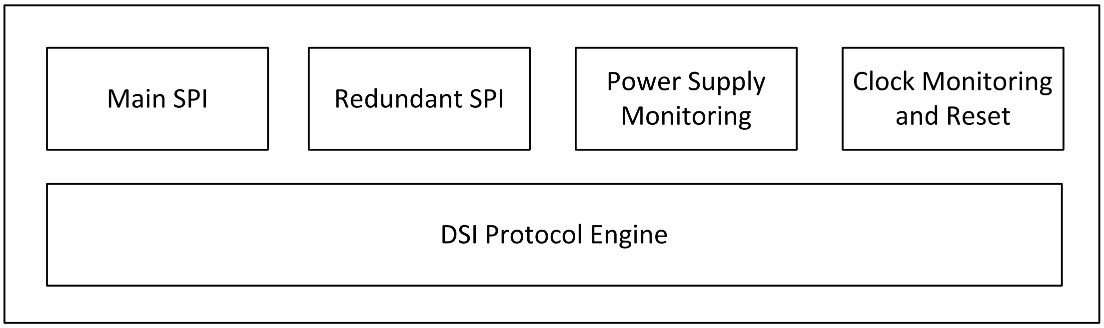


Figure 4. 33SA0528 functional block diagram

5.2 Features

- Main SPI at 10 MHz and 32-bit frame size provides access to all main registers
- Redundant SPI with the same format provides access to redundant registers with slaves' data, for safety purposes
- DSI protocol engine provides two independent channels to communicate and decode up to eight sensors
- Power supplies monitor detects and informs undervoltages on all four power pins (VDSI, VCC5, V2P5A, V2P5D)
- Internal PLL block generates 10 MHz stable frequency from 4.0 Mhz input clock
- Internal clock generator (no resonator) provides internal 4.0 MHz reference for clock frequency watchdog block
- Clock monitor sets proper flags if any abnormality is detected in clock or PLL frequencies

5.3 Functional description

The 33SA0528 is a DSI master device behaving as an interface between the MCU and the DSI slaves connected to the system bus. It supports up to four slaves connected to each of the two available DSI channels, allowing for a total of eight slaves. The MCU can access the registers in the 33SA0528 via two independent SPIs, the first one being for configuration purposes and to interact with the DSI slaves. The second one provides full redundancy of slaves' responses, which is designed for safety applications. The 33SA0528 can also act as a DSI Companion Chip when working together with a DSI SBC, expanding this last chip's capacity regarding the maximum number of DSI slaves it can decode.

5.4 Communication

5.4.1 SPI

Both SPI channels share the same speed and format, so only one MCU configuration scheme is needed to communicate with the 33SA0528. The maximum frequency of this interface is clocked at 10 MHz and provided by the internal PLL, generated from the 4.0 MHz clock input. Each command follows a 32-bit format, with the 5th byte being optional. The SPI is in-command full-duplex, which means the 33SA0528 responds during the same SPI frame in which it demands to read a register, meaning the device can write or read any register in just one SPI command.

5.4.2 DSI

The 33SA0528 provides an interface for a DSI Differential bus, having two independent channels. Each channel can drive and decode up to four slaves connected in either point-to-point, parallel, or resistor-based daisy-chained bus. For each channel, the DSI Receiver block provides a doubled redundancy when composing the differential (high/send and low/return) values read from the bus, which makes this device is ideal for safety applications. For more information on the DSI protocol, refer to its consortium web site: http://www.dsiconsortium.org.

6 Functional block description

6.1 SPI

6.1.1 Block diagram

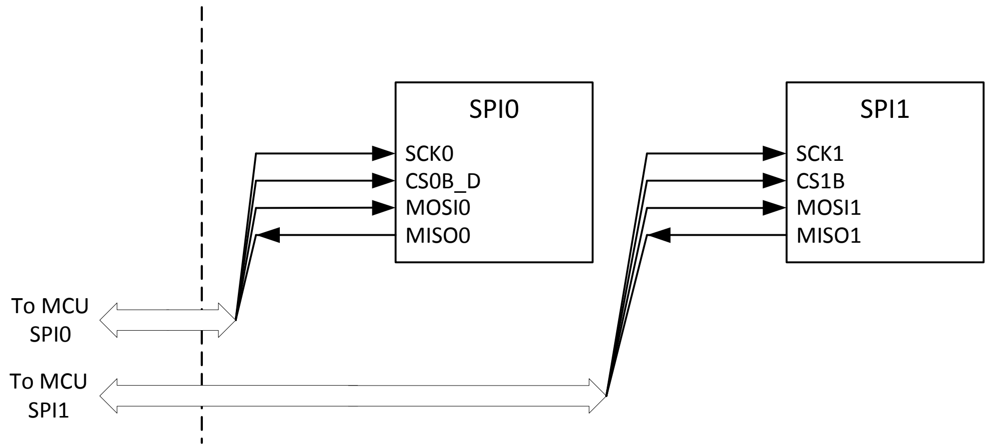


Figure 5. SPI modules pins and block diagram

6.1.2 Timings and configuration

The timings and commands format is the same for both SPI modules.

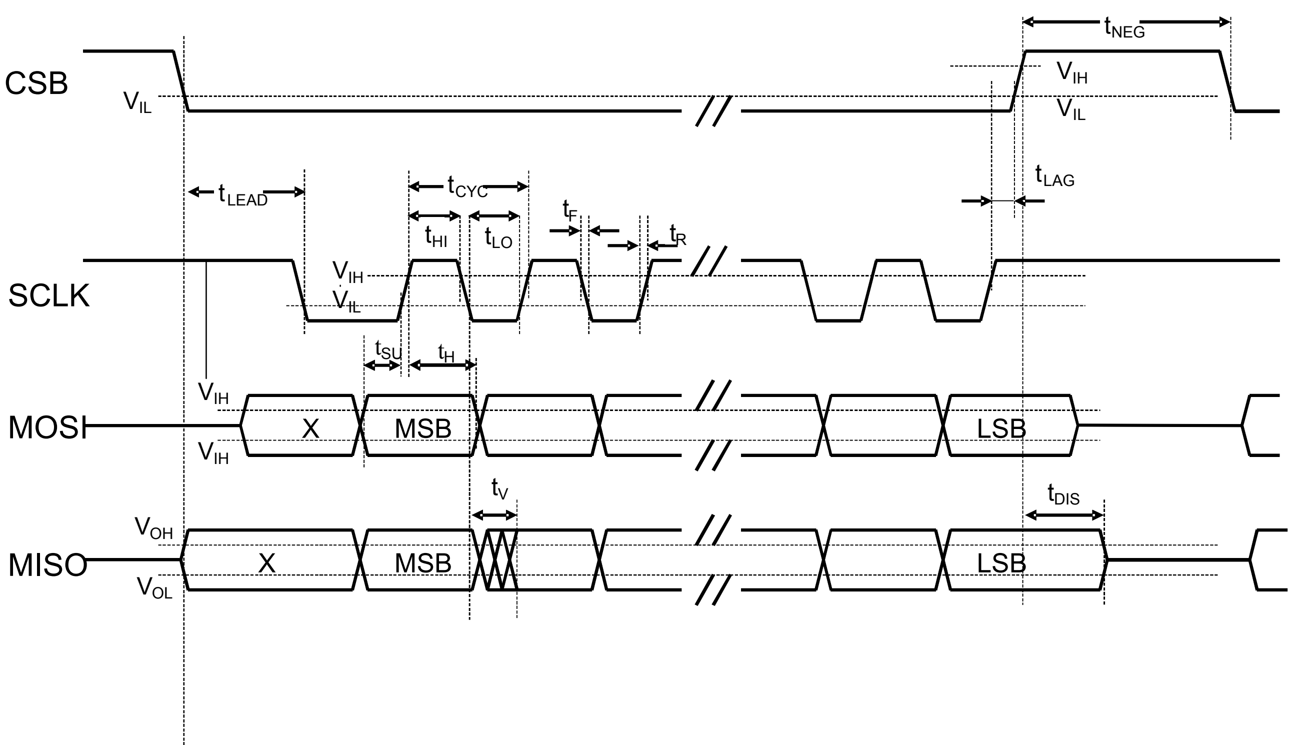


Figure 6. SPI modules timings

Table 7. SPI modules timings

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
t_{CYC}	SPI clock cycle time	99	—	—	ns	
t_{HI}	SPI clock high time	40	—	—	ns	
t_{LO}	SPI clock low time	40	—	—	ns	
t_{LEAD}	SPI chip select lead time	50	—	—	ns	
t_{LAG}	SPI chip select lag time	50	—	—	ns	
t_{SU}	Data setup time • MOSI valid after SCK rising edge	10	—	—	ns	
t_{H}	Data hold time • MOSI valid after SCK rising edge	10	—	—	ns	
t_{V}	Data valid time • SCK falling edge to MISO valid, C = 50 pF	—	—	25	ns	
t_{DIS}	Output disable time • CSB rise to MISO high-impedance	—	—	50	ns	
t_{R}	Rise time (30% V_{CC} to 70% V_{CC}) • SCK, MOSI	—	—	10	ns	
t_{F}	Fall time (70% V_{CC} to 30% V_{CC}) • SCK, MOSI	—	—	10	ns	
t_{NEG}	Chip select negate timer (read/write)	600	—	—	ns	

6.1.3 Frame format

The SPI module transactions start with a command and address byte and can be followed by three or four bytes of data. The start of a SPI transaction is signaled by the CSB signal being asserted low. The first bit sent (bit 7) of the first byte signals a read (bit = ‘0’) or write (bit = ‘1’) operation. The last seven bits (bit 6 to 0) of the first byte indicate the address of the desired register. Both 4-byte access and 5-byte access are valid for all register address. During a SPI transaction the 33SA0528 checks for SPI framing errors. A framing error is defined as any number of clocks received which is neither 32 nor 40. If this occurs, all bits sent by the SPI master are discarded and no registers are updated.

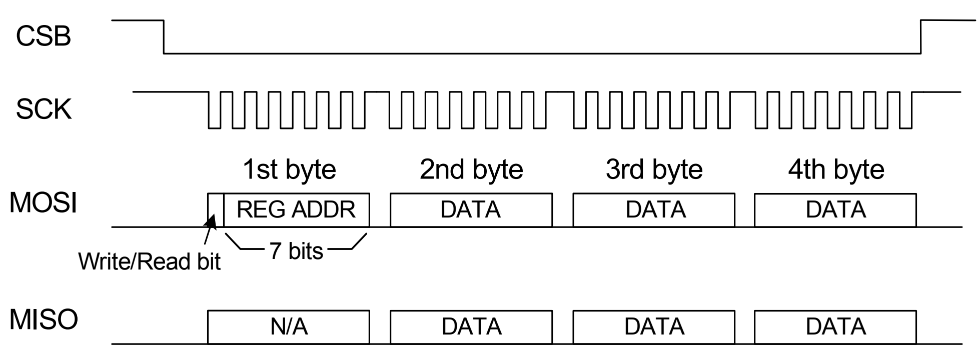


Figure 7. SPI module frames format - 4 byte access

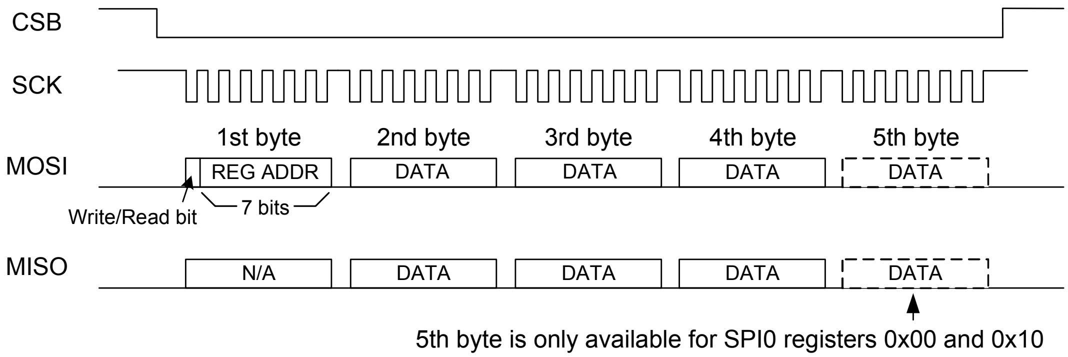


Figure 8. SPI modules frames format - 5 bytes access

6.1.4 Register maps

Table 8. SPI0 register map

Address	Name	Type	2nd byte	3rd byte	4th byte	5th byte (optional)
0x00	CRM Tx/Rx Data Buffer D0	R/W	D0DATA2	D0DATA1	D0DATA0	D0RES_STAT
0x01	CRM Tx/Rx Data Buffer D0	R	D0DATA1	D0DATA0	D0RES_STAT	—
0x02	PDCM Data Buffer D0R0	R	D0R0DATA2	D0R0DATA1	D0R0DATA0	—
0x04	PDCM Data Buffer D0R1	R	D0R1DATA2	D0R1DATA1	D0R1DATA0	—
0x06	PDCM Data Buffer D0R2	R	D0R2DATA2	D0R2DATA1	D0R2DATA0	—
0x08	PDCM Data Buffer D0R3	R	D0R3DATA2	D0R3DATA1	D0R3DATA0	—
0x0A	PDCM Control D0	R/W	D0PDCM_CTRL	D0PDCM_DLY	N/A	—
0x0B	Channel Control D0	R/W	D0CTRL	D0DPC	D0STAT	—
0x0C	PDCM Configuration D0	R/W	D0CHIP_TIME	D0SID_R0R1	D0SID_R2R3	—
0x0E	Channel Clear D0	R/W	D0CLR	N/A	N/A	—
0x10	CRM Tx/Rx Data Buffer D1	R/W	D1DATA2	D1DATA1	D1DATA0	D1RES_STAT
0x11	CRM Tx/Rx Data Buffer D1	R	D1DATA1	D1DATA0	D1RES_STAT	—
0x12	PDCM Data Buffer D1R0	R	D1R0DATA2	D1R0DATA1	D1R0DATA0	—
0x14	PDCM Data Buffer D1R1	R	D1R1DATA2	D1R1DATA1	D1R1DATA0	—
0x16	PDCM Data Buffer D1R2	R	D1R2DATA2	D1R2DATA1	D1R2DATA0	—
0x18	PDCM Data Buffer D1R3	R	D1R3DATA2	D1R3DATA1	D1R3DATA0	—
0x1A	PDCM Control D1	R/W	D1PDCM_CTRL	D1PDCM_DLY	N/A	—
0x1B	Channel Control D1	R/W	D1CTRL	D1DPC	D1STAT	—
0x1C	PDCM Configuration D1	R/W	D1CHIP_TIME	D1SID_R0R1	D1SID_R2R3	—
0x1E	Channel Clear D1	R/W	D1CLR	N/A	N/A	—
0x40	NCKPTN	R	0xAA	0xAA	0xAA	—
0x41	CHKPTN	R	0x55	0x55	0x55	—
0x42	MASKID	R	MASKID	—	—	—

Notes

4. Dn registers refer to the DSI channel n, so D0 corresponds to channel 0 and D1 corresponds to channel 1.
5. Rm registers refer to the DSI slave addressed at m, so R0 corresponds to slave at address 0 and so on.
6. The registers that correspond to different DSI channels and addresses have the same format and description.

Table 9. SPI1 register map

Address	Name	Type	2nd byte	3rd byte	4th byte	5th byte (optional)
0x02	PDCM Data Buffer D0R0	R	D0R0DATA2	D0R0DATA1	D0R0DATA0	-
0x04	PDCM Data Buffer D0R1	R	D0R1DATA2	D0R1DATA1	D0R1DATA0	-
0x06	PDCM Data Buffer D0R2	R	D0R2DATA2	D0R2DATA1	D0R2DATA0	-
0x08	PDCM Data Buffer D0R3	R	D0R3DATA2	D0R3DATA1	D0R3DATA0	-
0x12	PDCM Data Buffer D1R0	R	D1R0DATA2	D1R0DATA1	D1R0DATA0	-
0x14	PDCM Data Buffer D1R1	R	D1R1DATA2	D1R1DATA1	D1R1DATA0	-
0x16	PDCM Data Buffer D1R2	R	D1R2DATA2	D1R2DATA1	D1R2DATA0	-
0x18	PDCM Data Buffer D1R3	R	D1R3DATA2	D1R3DATA1	D1R3DATA0	-
0x40	NCKPTN	R	0xAA	0xAA	0xAA	-
0x41	CHKPTN	R	0x55	0x55	0x55	-

Notes

- These registers have the same format and description as their SPI0 counterparts, as they are just for redundancy purposes.

6.1.5 Registers description

6.1.5.1 CRM Tx/Rx data buffer Dn

Table 10. 2nd byte - DnDATA2

Bit	7	6	5	4	3	2	1	0
R W	DnDATA[23]	DnDATA[22]	DnDATA[21]	DnDATA[20]	DnDATA[19]	DnDATA[18]	DnDATA[17]	DnDATA[16]
Reset	0	0	0	0	0	0	0	0

Table 11. 3rd byte - DnDATA1

Bit	7	6	5	4	3	2	1	0
R W	DnDATA[15]	DnDATA[14]	DnDATA[13]	DnDATA[12]	DnDATA[11]	DnDATA[10]	DnDATA[9]	DnDATA[8]
Reset	0	0	0	0	0	0	0	0

Table 12. 4th byte - DnDATA

Bit	7	6	5	4	3	2	1	0
R W	DnDATA[7]	DnDATA[6]	DnDATA[5]	DnDATA[4]	DnDATA[3]	DnDATA[2]	DnDATA[1]	DnDATA[0]
Reset	0	0	0	0	0	0	0	0

Table 13. 5th byte - DnRES_STAT

Bit	7	6	5	4	3	2	1	0
R	ER	-	-	UV	TE	RNE	0	1

Table 13. 5th byte - DnRES_STAT

Bit	7	6	5	4	3	2	1	0
W								
Reset	0	0	0	0	1	0	0	1

Table 14. CRM Tx/Rx data buffer Dn fields description

Field	Description
DnDATA[23:0]	CRM data to transmit or CRM data received from slaves If the DSI channel EN bit is set, and the 33SA0528 is not in PDCM, data is transmitted after being written to the register. Also, slaves' CRM data is written back to the buffer as soon as it is received through the bus.
ER	Error bit This bit indicates, for received data, there is either a CRC error, an undefined symbol error, or data mismatch between the dual DSI receivers.
UV	Undervoltage This bit indicates VDSI dropped below its minimum threshold for a specified time. Refer to Power supply monitor on page 30.
TE	Transmit empty This bit indicates there is no data in the transmit buffer.
RNE	Receiver not empty This bit indicates there is data available that has been received from the slaves.

6.1.5.2 PDCM data buffer DnRm

Table 15. 2nd byte - DnRmDATA2

Bit	7	6	5	4	3	2	1	0
R	ER	-	RNE	UV	DnRmData[19]	DnRmData[18]	DnRmData[17]	DnRmData[16]
W								
Reset	0	0	0	0	0	0	0	0

Table 16. 3rd byte - DnRmDATA1

Bit	7	6	5	4	3	2	1	0
R	DnRmData[15]	DnRmData[14]	DnRmData[13]	DnRmData[12]	DnRmData[11]	DnRmData[10]	DnRmData[9]	DnRmData[8]
W								
Reset	0	0	0	0	0	0	0	0

Table 17. 4th byte - DnRmDATA0

Bit	7	6	5	4	3	2	1	0
R	DnRmData[7]	DnRmData[6]	DnRmData[5]	DnRmData[4]	DnRmData[3]	DnRmData[2]	DnRmData[1]	DnRmData[0]
W								
Reset	0	0	0	0	0	0	0	0

Table 18. PDCM data buffer DnRm fields description

Field	Description
DnRmDATA[19:0]	PDCM data received from slaves DnRmDATA[19:16] represent the source ID field of the slave, and it is used as seed for CRC calculation.
ER	Error bit This bit indicates, for received data, that there is either a CRC error, an undefined symbol error, or data mismatch between the dual DSI receivers.
UV	Undervoltage This bit indicates VDSI dropped below its minimum threshold for a specified time. Refer to Power supply monitor on page 30.
RNE	Receiver not empty This bit indicates there is data available that has been received from the slaves.

6.1.5.3 PDCM control Dn

Table 19. 2nd byte - DnPDCM_CTRL

Bit	7	6	5	4	3	2	1	0
R W	DnBRC	-	-	-	-	-	DnAUTO	DnPDCM_EN
Reset	0	0	0	0	0	0	0	0

Table 20. 3rd byte - DnPDCM_DLY

Bit	7	6	5	4	3	2	1	0
R W	DELAY[7]	DELAY[6]	DELAY[5]	DELAY[4]	DELAY[3]	DELAY[2]	DELAY[1]	DELAY[0]
Reset	0	0	0	0	0	0	0	0

Table 21. PDCM control Dn fields description

Field	Description
DnBRC	Broadcast read command Each time this bit is set, a manual BRC is transmitted through the DSI bus. Only valid when DnPDCM_EN is 1 and DnAUTO is 0.
DnAUTO	Automatic BRC When this bit is set, a BRC is transmitted automatically through the DSI bus every 500 μs. Write access to this bit is ignored when DnPDCM_EN is 0.
DnPDCM_EN	Periodic data collection mode enable Once this bit is set, the 33SA0528 enters PDCM, preventing any CRM communication or any configuration change. This bit can be cleared by clearing the channel, by writing to the channel clear Dn register.
DELAY[7:0]	Broadcast read command delay This bits set the delay to be applied to both manual and automatic BRCs, from BRC bit set to its transmission through the DSI bus. It is calculated as $\text{Delay time} = \text{DELAY}[7:0] \times 5\text{clockcounts}$, with a range of 0 ‘~ 127.5 μs and a 0.5 μs step at 10 MHz.

6.1.5.4 Channel control Dn

Table 22. 2nd byte - DnCTRL

Bit	7	6	5	4	3	2	1	0
R	0	0	0	0	UVDSI_ON	EN	BCK[1]	BCK[0]
W								
Reset	0	0	0	0	0	0	0	0

Table 23. 3rd byte - DnDPC

Bit	7	6	5	4	3	2	1	0
R	0	0	0	0	0	DPC[2]	DPC[1]	DPC[0]
W								
Reset	0	0	0	0	0	0	0	0

Table 24. 4th byte - DnSTAT

Bit	7	6	5	4	3	2	1	0
R	CFM3	CFM2	GNDA_OP	GNDD_OP	OCS	TS	0	UV
W	w0c	w0c	w0c	w0c	w0c	w0c		w0c
Reset	0	0	0	0	0	0	0	0

Table 25. Channel control Dn fields description

Field	Description
UVDSI_ON	VDSI undervoltage monitor test function This bit forces an undervoltage detection on the UVDSI monitor, for test purposes, by forcing its input to ground. 0: Normal operation. UVDSI module monitors the voltage in VDSI pin. 1: Test operation. UVDSI is forced to ground, so the UV bit in status registers should be set.
EN	DSI channel enable 0: Disable the DSI channel, if conditions are met. 1: Enable the DSI channel, if conditions are met.
BCK[1:0]	Buffer check mode If both these bits are set simultaneously (in the same SPI transaction), the 33SA0528 enters BCM. Refer to the DSI protocol engine module. Note that the BCK[1:0] bits have higher priority than EN and DPC[2:0], meaning if are three fields are written at the same time, only BCK[1:0] is considered.
DPC[2:0]	Discovery pulses count If conditions are met, setting these bits transmits the set number of discovery pulses through the DSI bus. Refer to DSI protocol engine on page 20 for required conditions.
CFM3 and CFM2	Clock failure monitor flags CFM3=0 and CFM2=0: Normal case. Each bit can be cleared by writing a 0 to them. CFM3=1: The internal PLL in charge of generating the internal 10 MHz frequency is unlocked. CFM2=1: The clock watchdog indicates CLKIN is out of its 4.0 MHz accepted range.
GNDA_OP	GNDA open pin 0: Normal case. The bit can be cleared by writing a 0 to it. 1: GNDA pin is open.
GNDD_OP	GNDD open pin 0: Normal case. The bit can be cleared by writing a 0 to it. 1: GNDD pin is open.
OCS	Overcurrent shutdown 0: Normal case. The bit can be cleared by writing a 0 to it. 1: The DSI bus current limiter has worked for a certain amount of time. Refer to Power supply monitor on page 30.

Table 25. Channel control Dn fields description (continued)

Field	Description
TS	Thermal shutdown 0: Normal case. The bit can be cleared by writing a 0 to it. 1: The DSI bus thermal limit has been reached. Refer to Power supply monitor on page 30.
UV	Undervoltage 0: Normal case. The bit can be cleared by writing a 0 to it. 1: VDSI dropped below its minimum threshold for a specified time. Refer to Power supply monitor on page 30.

6.1.5.5 PDCM configuration Dn

Table 26. 2nd byte - DnCHIP_TIME

Bit	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	CHIPTIME[1]	CHIPTIME[0]
W								
Reset	0	0	0	0	0	0	0	0

Table 27. 3rd byte - DnSID_R0R1

Bit	7	6	5	4	3	2	1	0
R W	SID_R0[3]	SID_R0[2]	SID_R0[1]	SID_R0[0]	SID_R1[3]	SID_R1[2]	SID_R1[1]	SID_R1[0]
Reset	0	0	0	0	0	0	0	0

Table 28. 4th byte - DnSID_R2R3

Bit	7	6	5	4	3	2	1	0
R W	SID_R2[3]	SID_R2[2]	SID_R2[1]	SID_R2[0]	SID_R3[3]	SID_R3[2]	SID_R3[1]	SID_R3[0]
Reset	0	0	0	0	0	0	0	0

Table 29. PDCM configuration Dn fields description

Field	Description
CHIPTIME[3:0]	DSI responses chip time These bits set the chip duration to use when decoding the current responses from slaves in the DSI bus. 00: 3.0 μs 01: 3.5 μs 10: 4.0 μs 11: 4.5 μs
SID_Rm[3:0]	Source ID These bits set the expected source ID of the DSI slave at address m. These values are used as CRC seeds.

6.1.5.6 Channel clear Dn

Table 30. 2nd byte - DnCLR

Bit	7	6	5	4	3	2	1	0
R W	DnCLR[7]	DnCLR[6]	DnCLR[5]	DnCLR[4]	DnCLR[3]	DnCLR[2]	DnCLR[1]	DnCLR[0]
Reset	0	0	0	0	0	0	0	0

Table 31. Channel clear Dn fields description

Field	Description
DnCLR[7:0]	Channel clear When writing 0xFF to this byte, all the registers of the corresponding channel n are reset to its initial values.

6.1.5.7 NCKPTN

Table 32. 2nd byte - 0xAA

Bit	7	6	5	4	3	2	1	0
R	1	0	1	0	1	0	1	0
W								
Reset	1	0	1	0	1	0	1	0

Table 33. 3rd byte - 0xAA

Bit	7	6	5	4	3	2	1	0
R	1	0	1	0	1	0	1	0
W								
Reset	1	0	1	0	1	0	1	0

Table 34. 4th byte - 0xAA

Bit	7	6	5	4	3	2	1	0
R	1	0	1	0	1	0	1	0
W								
Reset	1	0	1	0	1	0	1	0

Table 35. NCKPTN fields description

Field	Description
0xAA	Inverted pattern check This register and its bytes are meant to check validate the communication with the device.

6.1.5.8 CHKPTN

Table 36. 2nd byte - 0x55

Bit	7	6	5	4	3	2	1	0
R	0	1	0	1	0	1	0	1
W								
Reset	0	1	0	1	0	1	0	1

Table 37. 3rd byte - 0x55

Bit	7	6	5	4	3	2	1	0
R	0	1	0	1	0	1	0	1
W								
Reset	0	1	0	1	0	1	0	1

Table 38. 4th byte - 0x55

Bit	7	6	5	4	3	2	1	0
R	0	1	0	1	0	1	0	1
W								
Reset	0	1	0	1	0	1	0	1

Table 39. CHKPTN fields description

Field	Description
0x55	Pattern check This register and its bytes are meant to check validate the communication with the device.

6.1.5.9 MASKID

Table 40. 2nd byte - MASKID

Bit	7	6	5	4	3	2	1	0
R	MASKID[7]	MASKID[6]	MASKID[5]	MASKID[4]	MASKID[3]	MASKID[2]	MASKID[1]	MASKID[0]
W								
Reset								

Table 41. MASKID fields description

Field	Description
MASKID[7:0]	Mask ID These bits indicate the chip's silicon revision number

6.1.6 Electrical characteristics

Table 42. SPI modules electrical characteristics

Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
V_{IH} V_{IL} V_{HYST}	I/O logic levels (CSB, MOSI, SCK) • Input high-voltage • Input low-voltage • Input hysteresis	2.0 — 0.1	— — 0.35	— 0.9 0.8	V	
C_I	Input capacitance • CSB, MOSI, and SCK	—	—	10	pF	
V_{OL}	Output low voltage • MISO pin = 1.0 mA	0.0	—	0.5	V	
V_{OH}	Output high voltage • MISO pin = -1.0 mA	VCC5 - 0.5	—		V	
I_{MISO}	Output leakage current • MISO pin = 0 V • MISO pin = V_{CC5}	-10 -10	— —	10 10	µA	
I_{PU}	SCK, CSB pull-up current • $V_{OUT} = V_{CC5}$ - 2.0 V	-50	-30	-10	µA	
I_{PD}	MOSI pull-down current • V_{OUT} = 1.0 V	5.0	10	13	µA	

6.2 DSI protocol engine

6.2.1 Block diagram

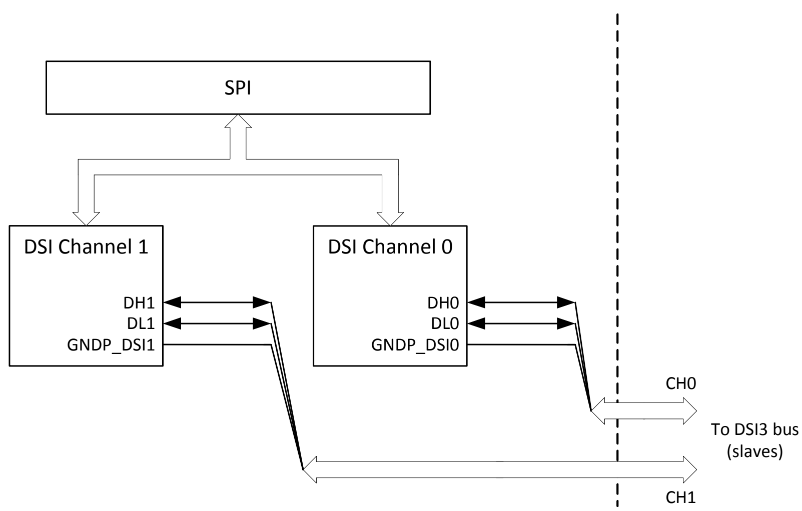


Figure 9. DSI modules pins and block diagram

33SA0528

6.2.2 DSI implementation parameters

6.2.2.1 Bus driver

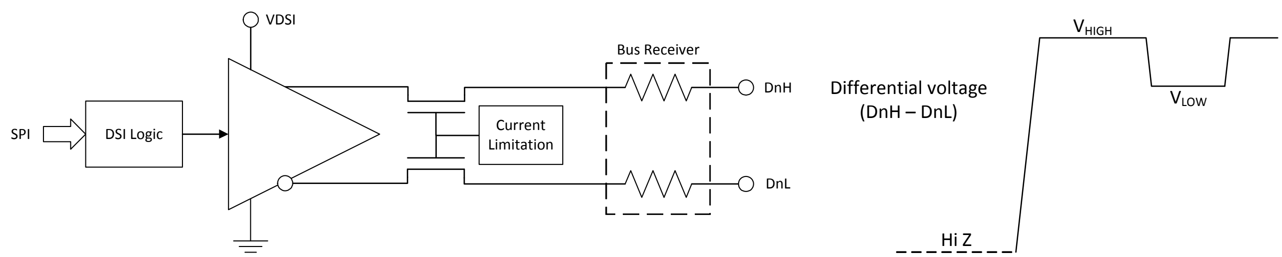


Figure 10. DSI bus driver block diagram

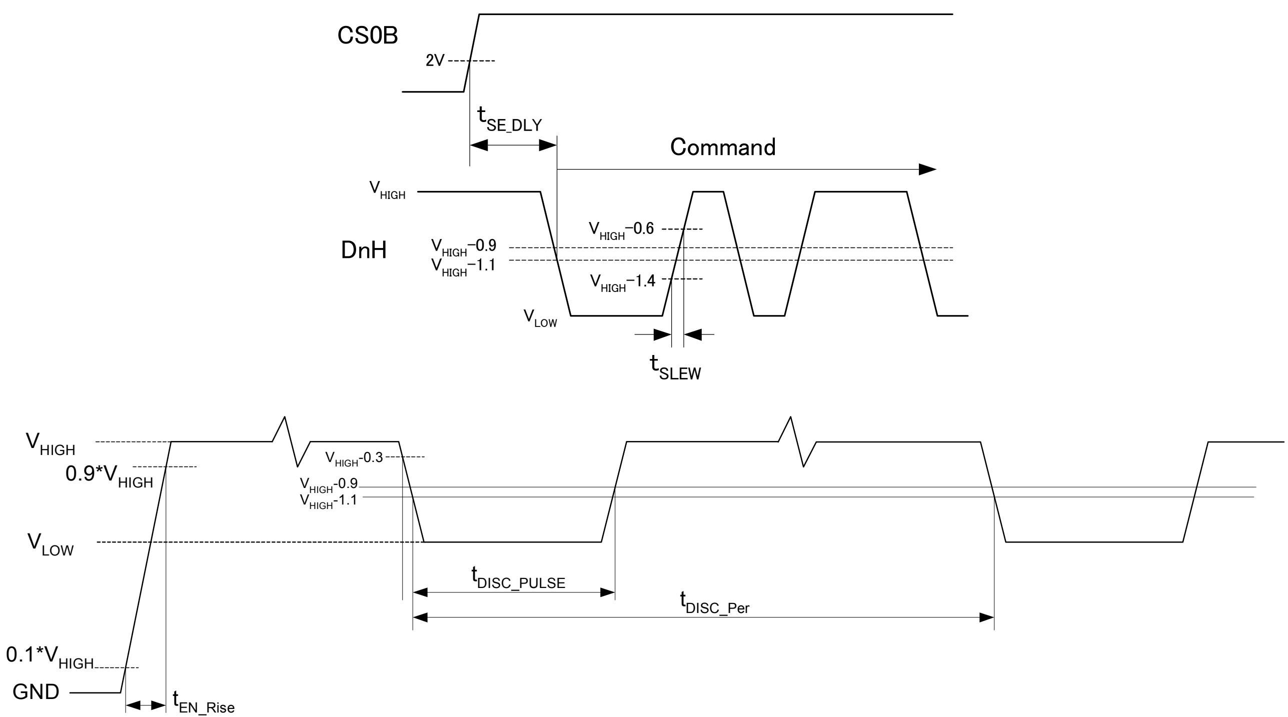


Figure 11. DSI bus voltages timings

Table 43. Bus driver characteristics

Characteristics noted under conditions 9.0 V ≤ V_{DSI} < 9.6 V, 4.8 V < V_{CC5} < 5.25 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted. All parameters not mentioned in this table are compliant with those described in the DSI protocol specification, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
V_{HIGH}	DSI voltage level high (DnH open, DnL open)	7.5	—	—	V	
V_{LOW}	DSI voltage level low (DnH open, DnL open)	V_{HIGH} - 2.2	—	V_{HIGH} - 1.8	V	
V_{HIGH_Drift}	DSI high level voltage drift	-150	—	150	mV	
	Common mode voltage peak to peak during single bit signal	—	—	100	mV	
R_{HIGH}	High-side output resistance	—	3.0	5.4	W	
R_{LOW}	Low-side output resistance	—	3.0	5.4	W	
R_M	Total output resistance (R_{HIGH} + R_{LOW})	—	—	10	W	
D_{RATE}	Communication data rate	—	125	—	kbps	
t_{SE_DLY}	Command start delay (CS0B rising edge to command start edge) • PDCM (DnPDCM_DLY = 0) • CRM	 — —	 — —	 1.5 5.0	µs	
t_{SLEW}	Voltage signal slew rate	2.0	—	6.0	V/µs	
t_{EN_Rise}	Bus enable rising time	—	—	10	µs	
t_{DISC_PULSE}	Self discovery pulse width	15	16	17	µs	
t_{DISC_PER}	Self discovery pulse period	120	125	130	µs	

6.2.2.2 Bus receiver

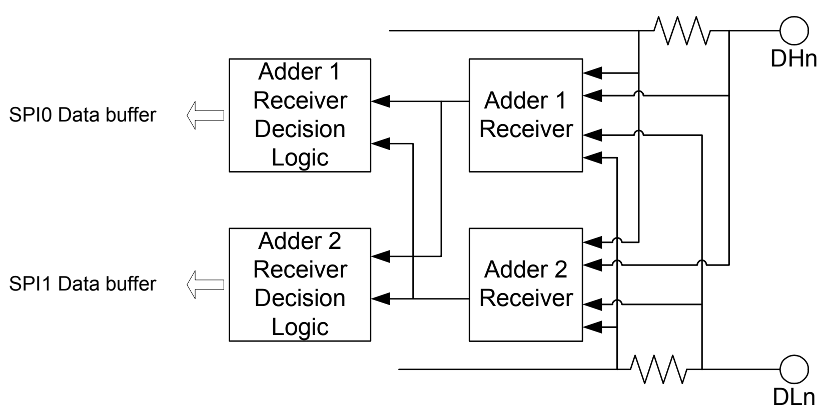


Figure 12. DSI bus receiver block diagram

The bus receiver presents doubled redundancy for safety purposes. It consists of two receivers and two independent decision logics.

- The first decision logic checks data integrity of the first receiver (referring to the second receiver), and transfers this data to SPI0 data buffer.
- The second decision logic checks data integrity of the second receiver (referring to the first receiver), and transfers this data to SPI1 data buffer.

The only case where ER bit is not set is given by satisfying all three conditions below. Any other case sets an ER bit.

- Receiver 1 CRC is OK
- Receiver 2 CRC is OK
- Receiver 1 XOR (bitwise) receiver 2 is OK

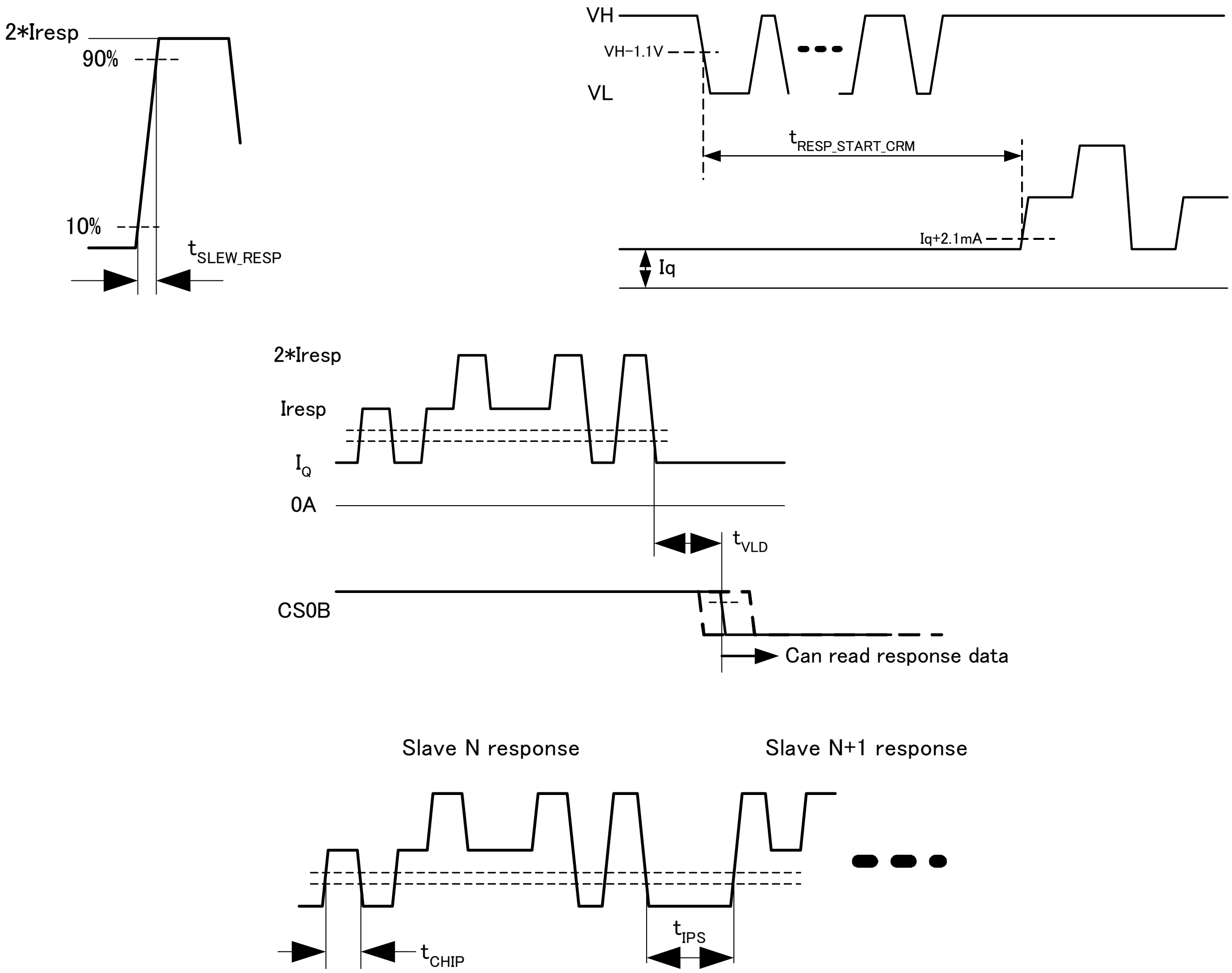


Figure 13. DSI bus currents timings

Table 44. Bus receiver characteristics

Characteristics noted under conditions 9.0 V ≤ V_{DSI} < 9.6 V, 4.8 V < V_{CC5} < 5.25 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted. All parameters not mentioned in this table are compliant with those described in the DSI protocol specification, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
I_{Q_TOTAL}	Total slaves quiescent current	-	-	40	mA	
$I_{RESP\_TH\_LOW\_DnH}$	Response current low threshold (receiver 1)	I_{Q_TOTAL} +5.0	-	I_{Q_TOTAL} +7.0	mA	
$I_{RESP\_TH\_HIGH\_DnH}$	Response current high threshold (receiver 1)	I_{Q_TOTAL} +15	-	I_{Q_TOTAL} +20	mA	
$I_{RESP\_TH\_LOW\_ADDER}$	Response current low threshold (receiver 2)	I_{Q_TOTAL} +5.0	-	I_{Q_TOTAL} +7.0	mA	
$I_{RESP\_TH\_HIGH\_ADDER}$	Response current high threshold (receiver 2)	I_{Q_TOTAL} +15	-	I_{Q_TOTAL} +20	mA	
$t_{RESP\_START\_CRM}$	Response start time in command and response mode	280	295	310	µs	
t_{SLEW_RESP}	Response current slew rate	21	-	45	mA/µs	
t_{CHIP_CRM}	Chip time in command and response mode	4.75	5.0	5.25	µs	

Table 44. Bus receiver characteristics (continued)

Characteristics noted under conditions 9.0 V ≤ V_{DSI} < 9.6 V, 4.8 V < V_{CC5} < 5.25 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted. All parameters not mentioned in this table are compliant with those described in the DSI protocol specification, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
t_{VLD}	Data valid time	-	-	1.0	µs	
t_{IPS}	Inter packet separation	3.0	-	-	chips	

6.2.3 Block logic and operation

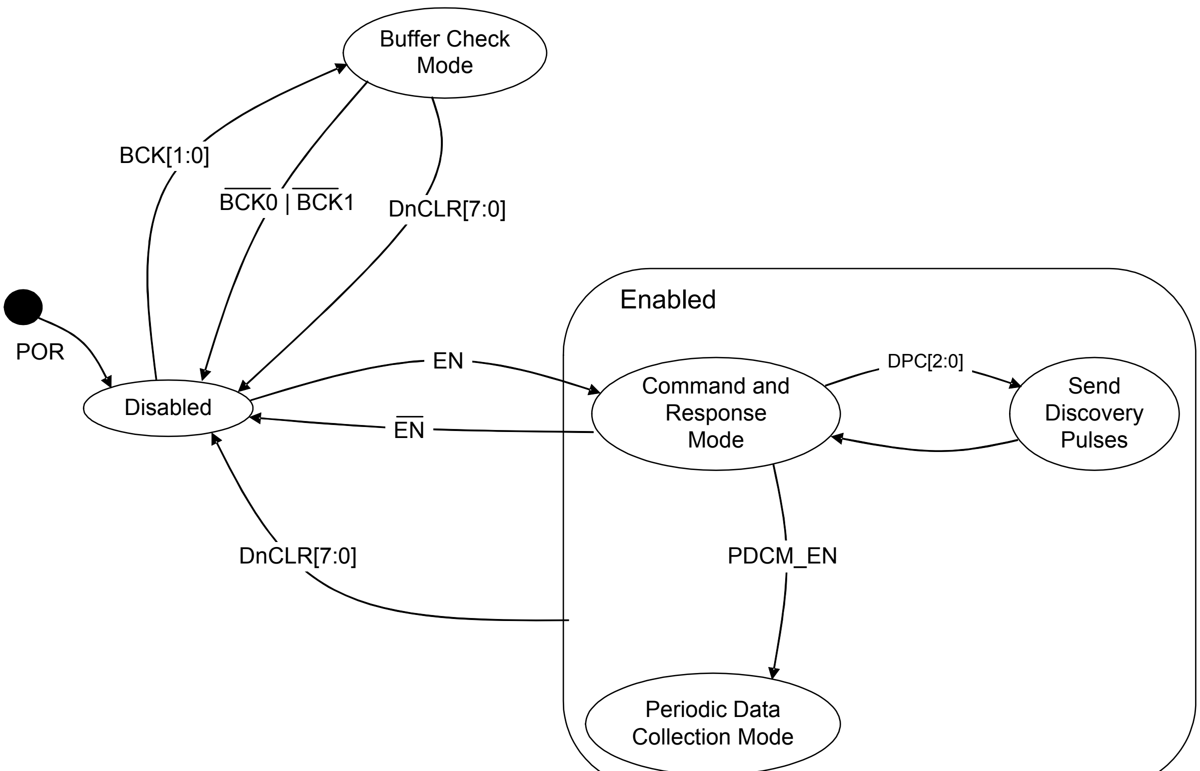


Figure 14. DSI block main states diagram for channel n

There are three states in the DSI protocol engine's logic for each channel: disabled, enabled and buffer check mode. In the disabled state, all SPI data buffers are reset to their initial values and any write access to the Tx buffer is ignored. The enabled state contains two modes, command and response mode, and periodic data collection mode. In command and response mode, the MCU can request the 33SA0528 to transceive any data (Tx/Rx buffers) or DSI discovery pulses to the DSI slaves in the bus. In periodic data collection mode, the DSI master stores and decodes four slaves responses per channel after every broadcast read command is sent through the DSI bus, which happens every 500 µs if in auto mode, or manually each time the DnBRC bit is set.

6.2.3.1 Command and response mode

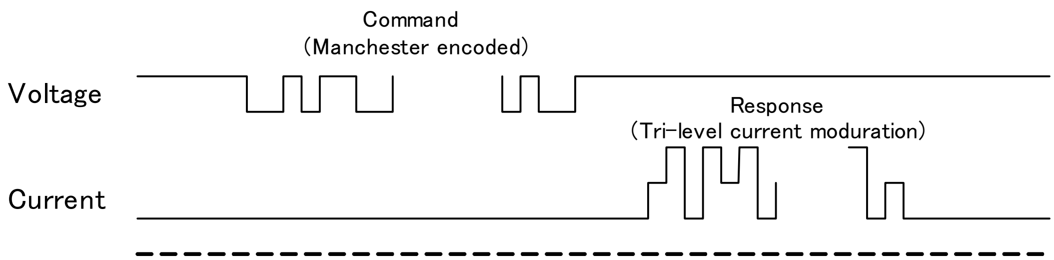


Figure 15. DSI Command and response mode operating principle

In this mode, any data written to the CRM Tx/Rx data buffer registers by the MCU, via SPI0, is outputted through the DSI bus as Manchester encoded voltage pulses, composing a command. The DSI slaves connected to the bus then receive this command and, if applicable, send back their responses following a tri-level current modulation, as detailed in the DSI protocol specification. The response is decoded by the DSI block and stored back to the corresponding CRM Tx/Rx Data Buffer register.

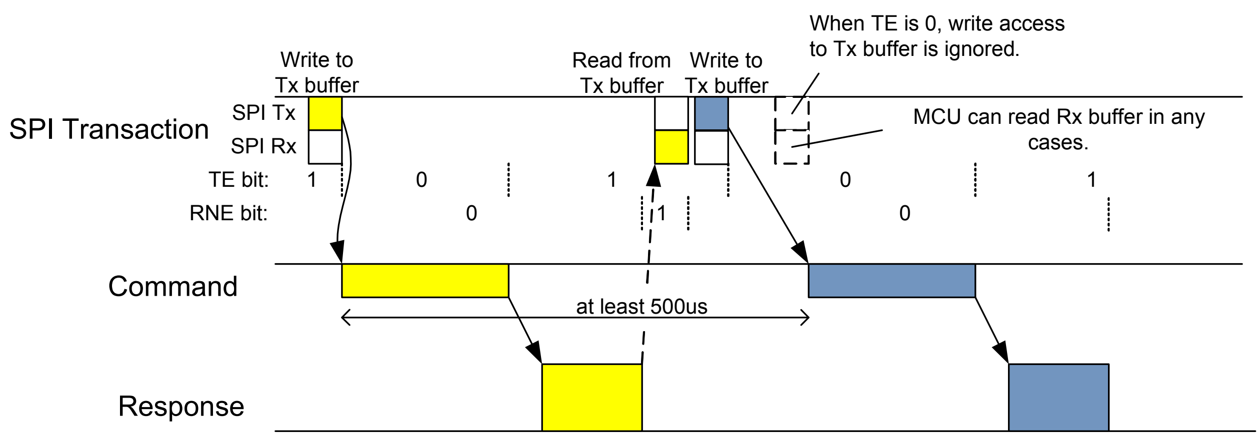


Figure 16. Command and response mode behavior on TE and RNE bits

The DSI voltage command is transmitted through the DSI bus immediately after the MCU completes writing data, via SPI0, to the CRM Tx/Rx data buffer register. This is not valid if the elapsed time from the start of the previous command is less than 500 µs. If the MCU writes data to the CRM Tx buffer when the TE bit is set (TE=1) and 500 µs have not yet elapsed from the start of the previous command, a new command is queued and outputted once this time is concluded. When the TE bit is cleared (TE=0), any MCU write operation to the CRM Tx buffer are ignored. However, the MCU can read the CRM Rx Data Buffer at any time.

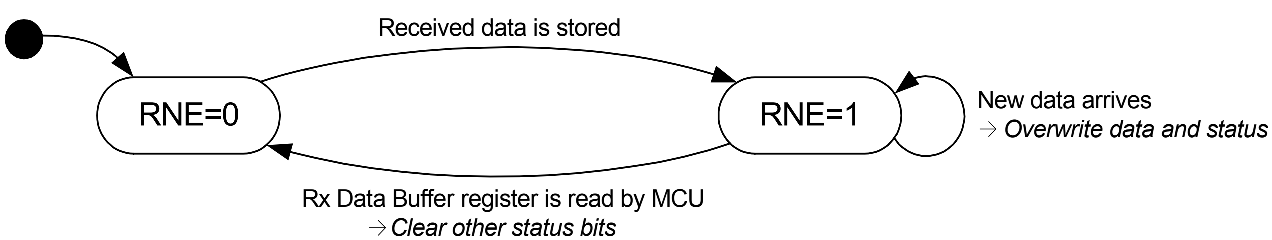


Figure 17. Command and response mode RNE bit behavior