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Power Management Integrated Circuit (PMIC) for i.MX50/53 Families

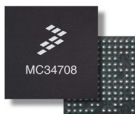
The MC34708 is the Power Management Integrated Circuit (PMIC) designed specifically for use with the Freescale i.MX50 and i.MX53 families. This device is powered by SMARTMOS technology.

Features

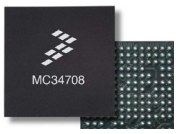
- Six multi-mode buck regulators for direct supply of the processor core, memory, and peripherals
- Boost regulator for USB OTG support
- Eight regulators with internal and external pass devices for thermal budget optimization
- USB/UART/Audio switching for mini-micro USB connector
- 10-bit ADC for monitoring battery and other inputs
- Real time clock and crystal oscillator circuitry with coin cell backup/ charger
- SPI/I^{2}C bus for control and register interface

34708

POWER MANAGEMENT



VK SUFFIX (PB-FREE)
98ASA00312D
206 MAPBGA
8.0 X 8.0 (0.5 MM PITCH)



VM SUFFIX (PB-FREE)
98ASA00299D
206 MAPBGA
13.0 X 13.0 (0.8 MM PITCH)

Applications
Tablets
Smart Mobile Devices
Portable Navigation Devices

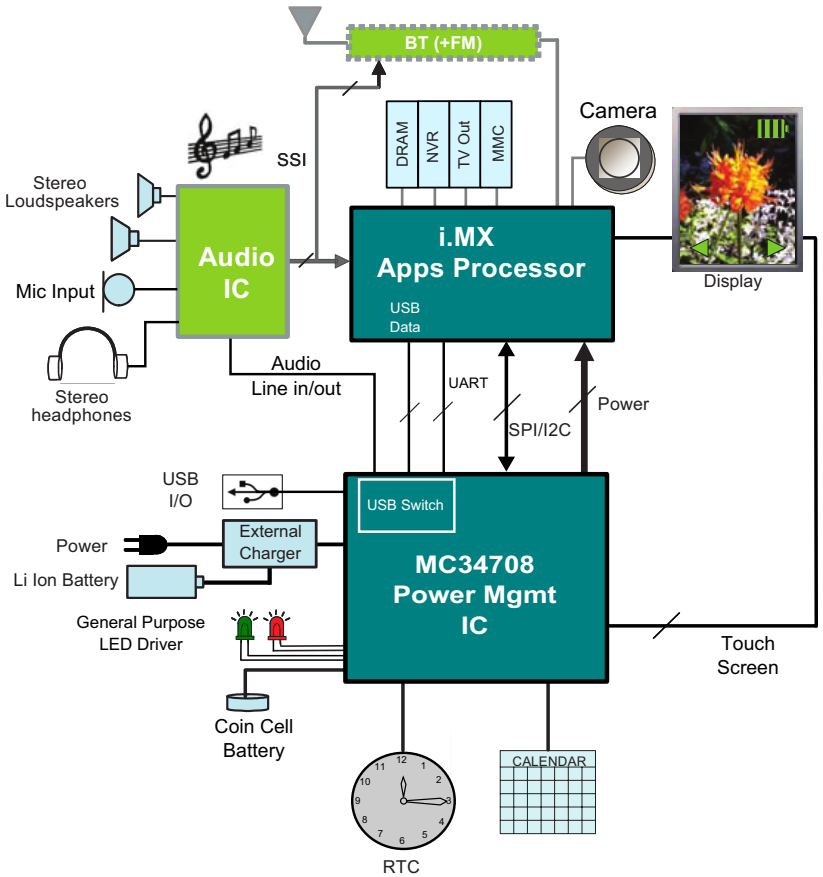


Figure 1. MC34708 Simplified Application Diagram

Table of Contents

1 Orderable Parts

This section describes the part numbers available to be purchased along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.freescale.com and perform a part number search for the following device numbers.

Table 1. Orderable Part Variations

Part Number [1]	Temperature (T_A)	Package
MC34708VK	-40 to 85 °C	206 MAPBGA - 8.0 x 8.0 mm - 0.5 mm pitch
MC34708VM		206 MAPBGA - 13 x 13 mm - 0.8 mm pitch

Notes
1. To Order parts in Tape & Reel, add the R2 suffix to the part number.

2 Part Identification

This section provides an explanation of the part numbers and their alpha numeric breakdown.

2.1 Description

Part numbers for the chips have fields that identify the specific part configuration. You can use the values of these fields to determine the specific part you have received.

2.2 Format and Examples

Part numbers for a given device have the following format, followed by a device example:

Table 2 - Part Numbering - Analog:

MC tt xxx r v PP RR - MC34708VKR2

2.3 Fields

These tables list the possible values for each field in the part number (not all combinations are valid).

Table 2: Part Numbering - Analog

FIELD	DESCRIPTION	VALUES
MC	Product Category	• MC- Qualified Standard • PC- Prototype Device
tt	Temperature Range	• 34 = -40 °C to ≤ 105 °C
xxx	Product Number	• Assigned by Marketing
r	Revision	• (default blank)
v	Variation	• (default blank)
PP	Package Identifier	• Varies by package
RR	Tape and Reel Indicator	• R2 = 13 inch reel hub size

3 Internal Block Diagram

3.1 Simplified Internal Diagram

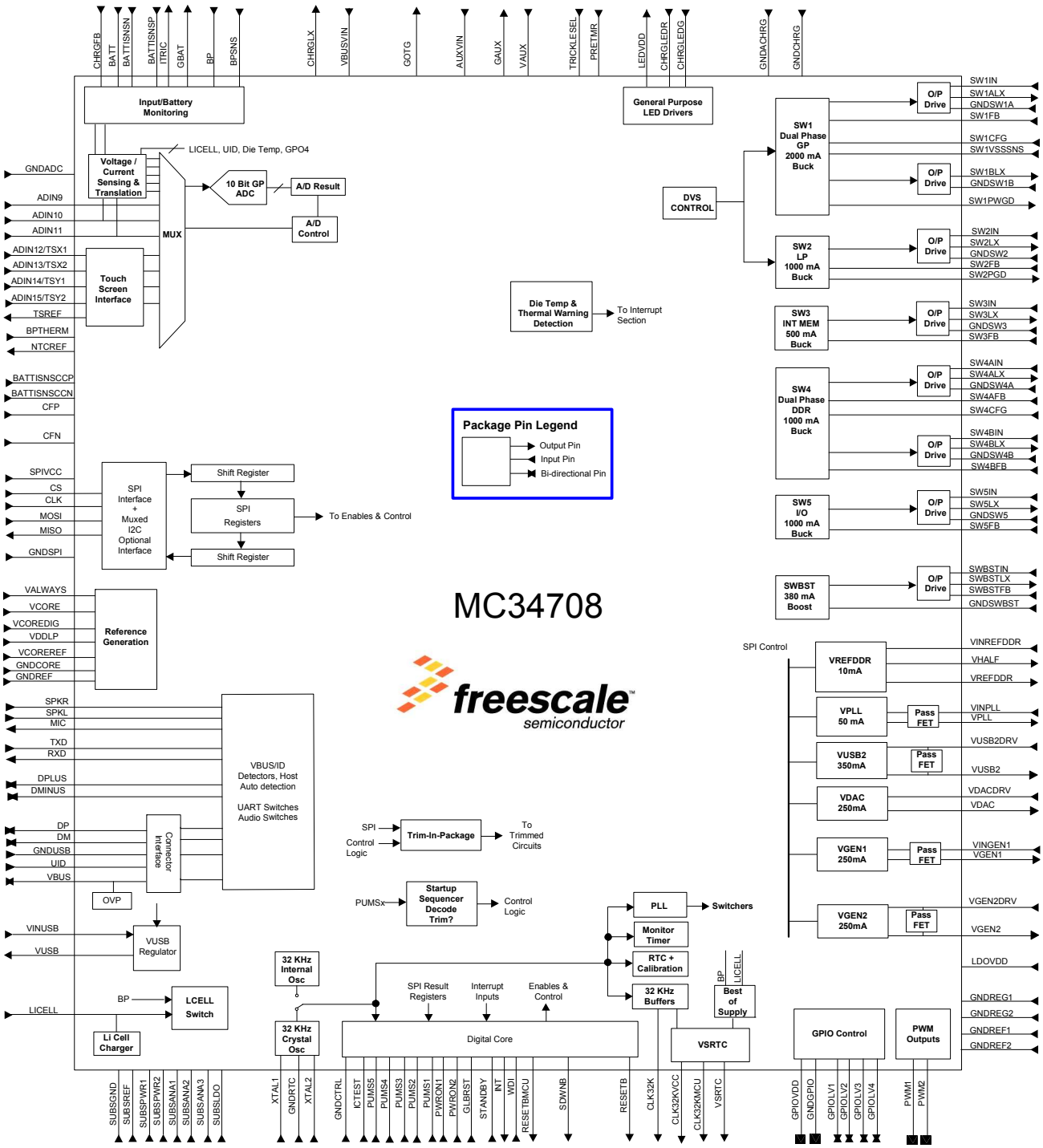


Figure 2. Simplified Internal Block Diagram

4 Pin Connections

4.1 Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A		TRICKLESEL	GNDACHRG	BATT	CFP	BP	VBUSVIN	CHRGLX	GNDCHRG	LEDVDD	LICELL	PWM1	GPIOVDD	PUMS4	
B	AUXVIN	AUXVIN	PRETMR	BPTHERM	CFN	GBAT	VBUSVIN	CHRGLX	GNDCHRG	CHRGLEDG	GPIOLV1	GNDGPIO	PUMS3	PUMS2	SUBSANA2
C	AUXVIN	AUXVIN	SUBSANA3	NTCREF	CHRGFB	BPSNS	VBUSVIN	CHRGLX	GNDCHRG	PWM2	GPIOLV3	PUMS1	GNDSW2	GNDSW2	GNDSW2
D	VAUX	GOTG	GAUX	SDWNB			VBUSVIN	CHRGLX	GNDCHRG	ICTEST	GPIOLV2	PUMS5	SW2LX	SW2LX	SW2LX
E	RESETB	GNDCTRL	PWRON2	INT		BATTISNSCCN	BATTISNSP	ITRIC	SUBSPWR1	CHRGLEDR	GPIOLV0	SW2FB	SW2IN	SW2IN	SW2IN
F	MISO	GNDSPI	MOSI	SPIVCC	RESETBMCU	BATTISNSCCP	BATTISNSN	SUBSPWR1	SUBSPWR1		GNDREF2	SWBSTIN	SWBSTIN	GNDSW3	GNDSW3
G	CLK	CS	VINUSB	RXD	TXD		GLBRST	PWRON1	SUBSPWR1	SW2PWGD	SW3FB	GNDSWBST	GNDSWBST	SW3LX	SW3LX
H	VBUS	VUSB	UID	VALWAYS	SUBSREF	SUBSPWR1	MIC	SUBSPWR1	SUBSPWR1	CLK32KMCU	CLK32KVCC	SWBSTFB	CLK32K	SW3IN	SW3IN
J	DM	SPKR	VCOREDIG	VDDLP	STANDBY	TSY2	TSY1	SUBSPWR1	SUBSPWR1	VDACDRV	VINPLL	VPLL	VSRTC	SWBSTLX	SWBSTLX
K	DP	SPKL	VCORE	TSX1		ADIN10	ADIN9	SUBSPWR1	SUBSPWR1	VHALF	VGEN2	VDAC	GNDREG1	GNDRTC	SUBSLDO
L	DPLUS	GNDCORE	GNDUSB	WDI	TSX2	ADIN11	SUBSPWR1	GNDREF1	SW1VSSSNS	SW1CFG	VINREFDDR	GNDREG2	VUSB2	LDOVDD	XTAL2
M	DMINUS	GNDREF				SW4CFG	SW5FB			SW1FB	SW1PWGD		VGEN1	VUSB2DRV	XTAL1
N	VCOREREF	GNDADC	GNDADC	GNDADC			SW5IN	SW5LX	GNDSW5		SW1IN	SW1IN	SUBSANA1	VINGEN1	VGEN2DRV
P	TSREF	GNDSW4A	GNDADC	GNDADC	SW4BFB	SW4AFB	SW5IN	SW5LX	GNDSW5	GNDSW1A	SW1ALX	SW1IN	SW1BLX	GNDSW1B	VREFDDR
R		SW4ALX	SW4AIN	SW4BIN	SW4BLX	GNDSW4B	SW5IN	SW5LX	GNDSW5	GNDSW1A	SW1ALX	SW1IN	SW1BLX	GNDSW1B	

Legend

- LDOs
- Switching Regulators
- Control Logic
- Misc
- RTC
- Ground
- USB
- ADC
- SPI/I2C
- No Connect
- No Ball

Figure 3. Top View Ballmap

4.2 Pin Definitions

Table 3. MC34708 Pin Definitions

Pin Number	Pin Name	Pin Function	Definition
Charger (Function no longer supported on MC34708)			
A7, B7, C7, D7	VBUSVIN	NC	Charger Not supported. No Connect
B1, B2, C1, C2	AUXVIN	NC	Charger Not supported. No Connect
D1	VAUX	NC	Charger Not supported. No Connect
A8, B8, C8, D8	CHRGLX	NC	Charger Not supported. No Connect
C5	CHRGFB	I	Connect to BATT pin
D2	GOTG	NC	Charger Not supported. No Connect
D3	GAUX	NC	Charger Not supported. No Connect
C6	BPSNS	I	BP sense point
A6	BP	I	1. Application supply point 2. Input supply to the IC core circuitry 3. Application supply voltage sense
B6	GBAT	O	Connect to GND
E8	ITRIC	NC	Charger Not supported. No Connect
E7	BATTISNSP	I	Battery current sensing point.(Optional) If required, connect a 20 mΩ sense resistor between BATTISNSP and BATTISNSN
F7	BATTISNSN	I	Battery current sensing point (Optional) If required, connect a 20 mΩ sense resistor between BATTISNSP and BATTISNSN
A4	BATT	I	1. Battery positive terminal 2. Battery current sensing point 2 3. Battery supply voltage sense
F6	BATTISNSCCP	NC	Coulomb counter Not supported. No Connect
E6	BATTISNSCCN	NC	Coulomb counter Not supported. No Connect
A2	TRICKLESEL	I	Connect to VCOREDIG
B3	PRETMR	I	Connect to Ground
A5	CFP	NC	Coulomb Counter Not supported. No Connect
B5	CFN	NC	Coulomb Counter Not supported. No Connect
A10	LEDVDD	O	LED supply
E10	CHRGLEDR	I	Red LED driver

Table 3. MC34708 Pin Definitions (continued)

Pin Number	Pin Name	Pin Function	Definition
B10	CHRGLEDG	I	Green LED driver
A3	GNDACHRG	GND	Analog ground
A9, B9, C9, D9	GNDCHRG	GND	Ground
C4	NTCREF	NC	Charger Not supported. No Connect
B4	BPTHERM	I	Connect to Ground
IC Core			
K3	VCORE	O	Regulated supply for the IC analog core circuitry
J3	VCOREDIG	O	Regulated supply for the IC digital core circuitry
H4	VALWAYS	O	Always on supply for internal core circuitry
N1	VCOREREF	O	Main bandgap reference
J4	VDDLP	O	VDDLP reference
L2	GNDCORE	GND	Ground for the IC core circuitry
M2	GNDREF	GND	Ground reference for the IC core circuitry
Switching Regulators			
N11, N12, P12, R12	SW1IN	I	SW1 input
P11, R11	SW1ALX	O	SW1A switch node connection
M10	SW1FB	I	SW1 feedback
P10, R10	GNDSW1A	GND	Ground for SW1A
L9	SW1VSSSNS	GND	SW1 sense
M11	SW1PWGD	O	Powergood signal for SW1
P13, R13	SW1BLX	O	SW1B switch node connection
P14, R14	GNDSW1B	GND	Ground for SW1B
L10	SW1CFG	I	SW1A/B mode configuration
E13, E14, E15	SW2IN	I	SW2 input
D13, D14, D15	SW2LX	O	SW2 switch node connection
E12	SW2FB	I	SW2 feedback
C13, C14, C15	GNDSW2	GND	Ground for SW2
G10	SW2PWGD	O	Powergood signal for SW2
H14, H15	SW3IN	I	SW3 input
G14, G15	SW3LX	O	SW3 switch node connection
G11	SW3FB	I	SW3 feedback
F14, F15	GNDSW3	GND	Ground for SW3
F11	GNDREF2	GND	Ground reference for switching regulators
R3	SW4AIN	I	SW4A input

Table 3. MC34708 Pin Definitions (continued)

Pin Number	Pin Name	Pin Function	Definition
R2	SW4ALX	O	SW4A switch node connection
P6	SW4AFB	I	SW4A feedback
P2	GNDSW4A	GND	Ground for SW4A
R4	SW4BIN	I	SW4B input
R5	SW4BLX	O	SW4B switch node connection
P5	SW4BFB	I	SW4B feedback
R6	GNDSW4B	GND	Ground for SW4B
M6	SW4CFG	I	SW4A/B mode configuration
N7, P7, R7	SW5IN	I	SW5 input
N8, P8, R8	SW5LX	O	SW5 output
M7	SW5FB	I	SW5 feedback
N9, P9, R9	GNDSW5	GND	Ground for SW5
L8	GNDREF1	GND	Ground reference for Switching Regulators
F12, F13	SWBSTIN	I	Boost Regulator BP supply
J14, J15	SWBSTLX	O	SWBST switch node connection
H12	SWBSTFB	I	Boost Regulator feedback
G12, G13	GNDSWBST	GND	Ground for boost Regulator
LDO Regulators			
L11	VINREFDDR	I	VREFDDR input supply
P15	VREFDDR	O	VREFDDR regulator output
K10	VHALF	O	Half supply reference for VREFDDR
J11	VINPLL	I	VPLL input supply
J12	VPLL	O	VPLL regulator output
J10	VDACDRV	O	Drive output for VDAC regulator using external PNP device
K12	VDAC	O	VDAC regulator output
L14	LDOVDD	I	Supply pin for VUSB2, VDAC, and VGEN2. Must always be connected to the same supply as the PNP emitter. Recommended to use BP as the LDOVDD supply. See Figure 38 for a typical connection diagram.
M14	VUSB2DRV	I	1. VUSB2 input using internal PMOS FET
		O	2. Drive output for VUSB2 regulator using external PNP device
L13	VUSB2	O	VUSB2 regulator output
N14	VINGEN1	I	VGEN1 input supply
M13	VGEN1	O	VGEN1 regulator output
N15	VGEN2DRV	I	1. VGEN2 input using internal PMOS FET
		O	2. Drive output for VGEN2 regulator using external PNP device
K11	VGEN2	O	VGEN2 regulator output
J13	VSRTC	O	Output regulator for SRTC module on processor
K13	GNDREG1	GND	Ground for regulators 1

Table 3. MC34708 Pin Definitions (continued)

Pin Number	Pin Name	Pin Function	Definition
L12	GNDREG2	GND	Ground for regulators 2
A13	GPIOVDD	I	Supply for GPIO
E11	GPIOLV0	I/O	General purpose input/output 0
B11	GPIOLV1	I/O	General purpose input/output 1
D11	GPIOLV2	I/O	General purpose input/output 2
C11	GPIOLV3	I/O	General purpose input/output 3
A12	PWM1	O	PWM output 1
C10	PWM2	O	PWM output 2
B12	GNDGPIO	-	GPIO ground
Control Logic			
A11	LICELL	I/O	1. Coin cell supply input 2. Coin cell charger output
M15	XTAL1	I	32.768 kHz Oscillator crystal connection 1
L15	XTAL2	I	32.768 kHz Oscillator crystal connection 2
K14	GNDRTC	GND	Ground for the RTC block
H11	CLK32KVCC	I	Supply voltage for 32 kHz buffer
H13	CLK32K	O	32 kHz Clock output for peripherals
H10	CLK32KMCU	O	32 kHz Clock output for processor
E1	RESETB	O	Reset output for peripherals
F5	RESETBMCU	O	Reset output for processor
L4	WDI	I	Watchdog input
J5	STANDBY	I	Standby input signal from processor
E4	INT	O	Interrupt to processor
G8	PWRON1	I	Power on/off button connection 1
E3	PWRON2	I	Power on/off button connection 2
G7	GLBRST	I	Global Reset
C12	PUMS1	I	Power up mode supply setting 1
B14	PUMS2	I	Power up mode supply setting 2
B13	PUMS3	I	Power up mode supply setting 3
A14	PUMS4	I	Power up mode supply setting 4
D12	PUMS5	I	Power up mode supply setting 5
D10	ICTEST	I	Connect to ground for normal mode operation.
E2	GNDCTRL	GND	Ground for control logic
F4	SPIVCC	I	Supply for SPI bus
G2	CS	I	Primary SPI select input
G1	CLK	I	Primary SPI clock input
F3	MOSI	I	Primary SPI write input
F1	MISO	O	Primary SPI read output

Table 3. MC34708 Pin Definitions (continued)

Pin Number	Pin Name	Pin Function	Definition
D4	SDWNB	O	Indication of imminent system shutdown
F2	GNDSPI	GND	Ground for SPI interface
USB [(2)]			
H3	UID	I/O	USB OTG transceiver cable ID
L3	GNDUSB	GND	USB Ground
K1	DP	I/O	USB Data +
J1	DM	I/O	USB Data –
L1	DPLUS	I/O	Processor D+
M1	DMINUS	I/O	Processor D-
G4	RXD	O	UART Receive
G5	TXD	I/O	UART Transmit
H7	MIC	O	Mic output
J2	SPKR	I	Speaker right
K2	SPKL	I	Speaker left
H1	VBUS	I/O	USB transceiver cable interface VBUS & OTG supply output
H2	VUSB	O	USB transceiver regulator output
G3	VINUSB	I	Input option for VUSB; tie to SWBST at top level.
A to D Converter			
K7	ADIN9	I	ADC generic input channel 9
K6	ADIN10	I	ADC generic input channel 10,
L6	ADIN11	I	ADC generic input channel 11
K4	TSX1/ADIN12	I	Touch Screen Interface X1 or ADC generic input channel 12
L5	TSX2/ADIN13	I	Touch Screen Interface X2 or ADC generic input channel 13
J7	TSY1/ADIN14	I	Touch Screen Interface Y1 or ADC generic input channel 14
J6	TSY2/ADIN15	I	Touch Screen Interface Y2 or ADC generic input channel 15
P1	TSREF	O	Touch Screen Reference
N2, N3, N4, P3, P4	GNDADC	GND	Ground for ADC
Thermal Grounds			
H5	SUBSREF	GND	Substrate ground connection for reference circuitry
E9, F8,F9, L7, G9, H6, H8, H9, J8, J9, K8, K9	SUBSPWR1	GND	Substrate ground connection for power devices SW1, SW4, SW5
K15	SUBSLDO	GND	Substrate ground connection for all LDOs
N13	SUBSANA1	GND	Substrate ground connection for analog circuitry of SW1, SW4, SW5
B15	SUBSANA2	GND	Substrate ground connection for analog circuitry of SW2, SW3, SWBST

Table 3. MC34708 Pin Definitions (continued)

Pin Number	Pin Name	Pin Function	Definition
C3	SUBSANA3	GND	Substrate ground connection for analog circuitry

Notes

2. In applications without USB support, leave all USB pins unconnected.

5 General Product Characteristics

5.1 Maximum Ratings

Table 4. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Max.	Unit	Notes
ELECTRICAL RATINGS				
V_{BATT}, V_{BP}, V_{LICELL}	Input Supply Pins • BATT, BP, BPSNS • LICELL	 4.8 4.8	V	
	Input Sense Pins • CHRGFB • BATTISNSP, BATTISNSN	 7.5 5.5	V	
	LED Drivers Pins • CHRGLEDR, CHRGLEDG	 7.5	V	
	IC Core Reference • VCOREREF • VCOREDIG, VDDLP • VCORE • VALWAYS	 1.5 1.65 3.6 7.5	V	
	Switching Regulators Pins • SWxIN, SWxLX, SWBSTFB • SWxFB, SWxPWGD, SWxCFG • SWBSTLX	 5.5 3.6 7.5	V	
	LDO Regulator Pins • VREFDDR, VHALF • VPLL, VGEN1, VINGEN1, VSRTC • VINREFDDR,VDAC, VUSB2, VGEN2, • VINPLL, VDACDRV, VUSB2DRV, VGEN2DRV • LDOVDD	 1.5 2.5 3.6 4.8 5.5	V	
	GPIO Pins • GPIOVDD, GPIOLVx, PWMx	 2.5	V	
	Control Logic Pins • ICTEST • XTAL1, XTAL2 • CLK32KVCC, CLK32K, CLK32KMCU, WDI, STANDBY,INT, PWRON1, PWRON2, GLBRST, PUMSx, SPIVCC, CS, CLK, MOSI, MISO, SDWNB	 1.8 2.5 3.6	V	
	Mini/Micro USB Interface Pins • VBUS input sense pin • VUSB • UID, DP, DM, DPLUS, DMINUS, RXD, TXD, MIC, SPKR, SPKL, VINUSB	 20 3.6 5.5	V	
	ADC Interface Pins • ADINx, TSX1/ADIN12, TSX2/ADIN13, TSY1/ADIN14, TSY2/ADIN15, TSREF	 4.8	V	

Table 4. Maximum Ratings *(continued)*

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Max.	Unit	Notes
V_{ESD}	ESD Ratings		V	
	• Human Body Model All pins	±2000		(3)
	• Charge Device Model All pins	±500		(3)
	• Air Gap Discharge Model for UID, VBUS, DP, and DM pins	±15000		(4)
	• Human Body Model (HBM) for UID, VBUS, DP, and DM pins	±8000		(4)

Notes

3. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).
4. Need external ESD protection diode array to meet IEC1000-4-2 15000 V Air Gap discharge and 8000 V HBM requirements. (CZAP = 150 pF, RZAP = 330 ohm).

5.2 Thermal Characteristics

Table 5. Thermal Ratings

Symbol	Description (Rating)	Min.	Max.	Unit	Notes
THERMAL RATINGS					
T_A	Ambient Operating Temperature Range	-40	85	°C	
T_J	Operating Junction Temperature Range	-40	125	°C	(5)
T_{ST}	Storage Temperature Range	-65	150	°C	
T_{PPRT}	Peak Package Reflow Temperature During Reflow	-	Note 7	°C	(6), (7)
8.0 X 8.0 MM, THERMAL RESISTANCE AND PACKAGE DISSIPATION RATINGS					
$R_{\theta JA}$	Junction to Ambient Natural Convection • Single layer board (1s)	-	93	°C/W	(8), (9)
$R_{\theta JMA}$	Junction to Ambient Natural Convection • Four layer board (2s2p)	-	53	°C/W	(8), (10)
$R_{\theta JMA}$	Junction to Ambient (@200 ft/min.) • Single layer board (1s)	-	80	°C/W	(8), (10)
$R_{\theta JMA}$	Junction to Ambient (@200 ft/min.) • Four layer board (2s2p)	-	49	°C/W	(8), (10)
$R_{\theta JB}$	Junction to Board	-	34	°C/W	(11)
$R_{\theta JC}$	Junction to Case	-	25	°C/W	(12)
θJT	Junction to Package Top • Natural Convection	-	3.0	°C/W	(13)
13 X 13 MM, THERMAL RESISTANCE AND PACKAGE DISSIPATION RATINGS					
$R_{\theta JA}$	Junction to Ambient Natural Convection • Single layer board (1s)	-	57	°C/W	(8), (9)
$R_{\theta JMA}$	Junction to Ambient Natural Convection • Four layer board (2s2p)	-	36	°C/W	(8), (9), (10)

Table 5. Thermal Ratings *(continued)*

Symbol	Description (Rating)	Min.	Max.	Unit	Notes
$R_{\theta JMA}$	Junction to Ambient (@200 ft/min.) • Single layer board (1s)	-	48	°C/W	(8), (10)
$R_{\theta JMA}$	Junction to Ambient (@200 ft/min.) • Four layer board (2s2p)	-	32	°C/W	(8), (10)
$R_{\theta JB}$	Junction to Board	-	22	°C/W	(11)
$R_{\theta JC}$	Junction to Case	-	15	°C/W	(12)
θJT	Junction to Package Top • Natural Convection	-	3.0	°C/W	(13)

Notes

5. Do not operate above 125 °C for extended periods of time. Operation above 150 °C may cause permanent damage to the IC.
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
7. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx), and review parametrics.
8. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
9. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
10. Per JEDEC JESD51-6 with the board horizontal.
11. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
12. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
13. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

5.2.1 Power Dissipation

During operation, the temperature of the die should not exceed the maximum junction temperature. To optimize the thermal management scheme and avoid overheating, the MC34708 PMIC provides a thermal management system. The thermal protection is based on a circuit with a voltage output proportional to the absolute temperature.This voltage can be read out via the ADC for specific temperature readouts, see Channel 3 Die Temperature.

The ADEN SPI bit must be set = 1 to enable the comparators for the thermal monitoring (THERM110, THERM120, THERM125, THERM130, and thermal shutdown). With ADEN = 0 the thermal monitors and thermal shutdown are disabled. Interrupts THERM110, THERM120, THERM125, and THERM130 will be generated when respectively crossing in either direction the thresholds specified in Table 6. The temperature range can be determined by reading the THERMxxxS bits.

Thermal protection is integrated to power off the MC34708 PMIC in case of over dissipation. This thermal protection will act above the maximum junction temperature to avoid any unwanted power downs. The protection is debounced for 8.0 ms in order to suppress any (thermal) noise. This protection should be considered as a fail-safe mechanism and therefore the application design should be dimensioned such that this protection is not tripped under normal conditions. The temperature thresholds and the sense bit assignment are listed in Table 6

Table 6. Thermal Protection Thresholds

Parameter	Min	Typ	Max	Units	Notes
Thermal 110 °C threshold (THERM110)	105	110	115	°C	
Thermal 120 °C threshold (THERM120)	115	120	125	°C	
Thermal 125 °C threshold (THERM125)	120	125	130	°C	
Thermal 130 °C threshold (THERM130)	125	130	135	°C	
Thermal warning hysteresis	2.0	-	4.0	°C	(14)
Thermal protection threshold	130	140	150	°C	

Notes
14. Equivalent to approx. 30 mW min, 60 mW max

The THERM1xx thresholds are debounced by the SPI bits DIE_TEMP_DB[1:0], which are programmable from 100 µs to 4.0 ms (4.0 ms by default), see Table 7. When the die temperature crosses these thresholds, the corresponding sense bit will change, and an interrupt will be generated to notify the software the hardware is reaching its thermal limit.

Table 7. Die Temp Debounce Settings

DIE_TEMP_DB [1:0]	Time	Units
00	0.100	ms
01	1.0	ms
10	2.5	ms
11 (default)	4.0	ms

5.3 Electrical Characteristics

5.3.1 Recommended Operating Conditions

Table 8. Recommended Operating Conditions

Symbol	Description (Rating)	Min.	Max.	Unit	Notes
V_{BP}	Main Input Supply	3.0	4.5	V	
V_{LICELL}	LICELL Backup Battery	1.8	3.6	V	
T_A	Ambient Temperature	-40	85	°C	

5.3.2 General PMIC Specifications

Table 9. Pin Logic Thresholds

Pin Name	Internal Termination (19)	Parameter	Load Condition	Min	Max (22)	Unit	Notes
PWRON1, PWRON2, GLBRST	Pull-up	Input Low	47 kOhm	0.0	0.3	V	(16)
		Input High	1.0 MOhm	1.0	VCOREDIG	V	(16)
STANDBY, WDI	Weak Pull-down	Input Low	-	0.0	0.3	V	(21)
		Input High	-	0.9	3.6	V	(21)
CLK32K	CMOS	Output Low	-100 µA	0.0	0.2	V	
		Output High	100 µA	CLK32KVCC - 0.2	CLK32KVCC	V	
CLK32KMCU	CMOS	Output Low	-100 µA	0.0	0.2	V	
		Output High	100 µA	VSRTC - 0.2	VSRTC	V	
RESETB, RESETBMCU, SDWNB, SW1PWGD, SW2PWGD	Open Drain	Output Low	-2.0 mA	0.0	0.4	V	(20)
		Output High	Open Drain	-	3.6	V	(20)
GPIOLV1,2,3,4	CMOS	Input Low	-	0.0	0.3 * GPIOVDD	V	
		Input High	-	0.7 * GPIOVDD	GPIOVDD + 0.3	V	
		Output Low	-	0.0	0.2	V	
		Output High	-	GPIOVDD - 0.2	GPIOVDD	V	
	Open Drain	Output Low	-2.0 mA	0	0.4	V	
		Output High	Open Drain	-	GPIOVDD + 0.3	V	
PWM1, PWM2	CMOS	Output Low	-	0.0	0.2	V	
		Output High	-	GPIOVDD - 0.2	GPIOVDD	V	
CLK, MOSI		Input Low	-	0.0	0.3 * SPIVCC	V	(15)
		Input High	-	0.7 * SPIVCC	SPIVCC + 0.3	V	(15)
CS	Weak Pull-down	Input Low	-	0.0	0.4	V	(15)
		Input High	-	1.1	SPIVCC + 0.3	V	(15)
CS, MOSI (at Booting for SPI / I^2C decoding)	Weak Pull-down on CS	Input Low	-	0.0	0.3 * VCOREDIG	V	(15), (23)
		Input High	-	0.7 * VCOREDIG	VCOREDIG	V	(15), (23)

Table 9. Pin Logic Thresholds

Pin Name	Internal Termination (19)	Parameter	Load Condition	Min	Max (22)	Unit	Notes
MISO, INT	CMOS	Output Low	-100 µA	0.0	0.2	V	MISO (15) (24)
		Output High	100 µA	SPIVCC - 0.2	SPIVCC	V	MISO (15) (24)
PUMS1,2,3,4,5		Input Low PUMSxS = 0	-	0.0	0.3	V	(17)
		Input High PUMSxS = 1	-	1.0	VCOREDIG	V	(17)
ICTEST		Input Low	-	0.0	0.3	V	(18)
		Input High	-	1.1	1.7	V	(18)
SW1CFG, SW4CFG		Input Low	-	0.0	0.3	V	
		Input Mid	-	1.3	2.0	V	
		Input High	-	2.5	3.1	V	

Notes

15. SPIVCC is typically connected to the output of buck regulator SW5 and set to 1.800 V
16. Input has internal pull-up to VCOREDIG equivalent to 200 kOhm
17. Input state is latched in first phase of cold start, refer to Serial Interfaces for a description of the PUMS configuration
18. Input state is not latched
19. A weak pull-down represents a nominal internal pull-down of 100 nA unless otherwise noted
20. RESETB, RESETBMCU, SDWNB, SW1PWGD, SW2PWGD have open drain outputs, external pull-ups are required
21. SPIVCC needs to remain enabled for proper detection of WDI High to avoid involuntary shutdown
22. The maximum should never exceed the maximum rating of the pin as given in Pin Connections
23. The weak pull-down on CS is disabled if a VIH is detected at startup to avoid extra consumption in I^2C mode
24. The output drive strength is programmable

5.3.3 Current Consumption

The current consumption of the individual blocks is described in detail throughout this specification. For convenience, a summary table follows for standard use cases.

Table 10. Current Consumption Summary (27)

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Mode	Description	Typ	Max	Unit	Notes
RTC / Power cut	All blocks disabled, no main battery attached, coin cell is attached to LICELL (at 25 °C only) • RTC Logic • VSRTC • 32 kHz Oscillator • Clk32KMCU buffer active(10 pF load)	4.0	8.0	µA	
OFF (good battery)	All blocks disabled, main battery attached • Digital Core • RTC Logic • VSRTC • 32 kHz Oscillator • CLK32KMCU buffer active (10 pF load)	20	55	µA	
LPM ON Standby	Low Power Mode (Standby pin asserted and ON_STBY_LP=1) • Digital Core • RTC Logic • VCORE Module • VSRTC • CLK32KMCU/CLK32K active (10 pF load) • 32 kHz Oscillator • I_{REF} • SW1, SW2, SW3, SW4A, SW4B, SW5 in PFM (26),(30) • VDDREF, VPLL, VGEN1, VGEN2, VUSB2, VDAC in low power mode (25),(28) • Mini-USB	340	424	µA	
ON Standby	• Digital Core • RTC Logic • VCORE module • VSRTC • CLK32KMCU/CLK32K active (10 pF load) • 32 kHz Oscillator • Digital • I_{REF} • SW1, SW2, SW3 SW4A, SW4B, SW5 in PFM (26),(30) • VDDREF, VPLL, VGEN1, VGEN2, VUSB2, VDAC on in low power mode (26),(28) • Mini-USB • PLL (for mini USB)	480	561	µA	

Table 10. Current Consumption Summary (27)

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

ON	Typical use case • Digital Core • RTC Logic • VCORE Module • VSRTC CLK32KMCU/CLK32K active (10 pf) • 32 kHz Oscillator • I_{REF} • SW1, SW2, SW3 SW4A, SW4B, SW5 in Apskip SWBST (26),(29),(30) • VDDREF, VPLL, VGEN1, VGEN2, VUSB2, VDAC on in low power mode (25),(28) • Digital • PLL • Mini-USB	1600	3000	µA	

Notes
25. Equivalent to approx. 30 mW min, 60 mW max
26. Current in RTC Mode is from LICELL=2.5 V; in all other modes from BP = 3.6 V.
27. External loads are not included (1)
28. VUSB2, VGEN2 external pass PNPs
29. SWBST in auto mode
30. SW4A output 2.5 V

6 General Description

6.1 Features

Power Generation

- Six Buck Switching Regulators
    - Two Single/Dual Phase Buck Regulators
    - Three Single Phase Buck Regulators
    - PFM/Auto Pulse Skip/PWM Operation Mode
    - Dynamic Voltage Scaling
- 5 V Boost Regulator
    - USB On-the-go Support
- Eight LDO Regulators
    - Two with Selectable Internal or External Pass Devices
    - Five with Embedded Pass Devices
    - One with an External PNP Device

Analog to Digital Converter

- Seven General Purpose Channels
- Internal Dedicated Channels
- Resistive Touchscreen Interface

Auxiliary Circuits

- Mini/Micro USB Switch
    - Bidirectional Audio/Data/UART
    - Accessory Identification Circuit
- General Purpose I/Os
- PWM Outputs
- Two general purpose LED Drivers.

Clocking and Oscillators

- Real Time clock
    - Time and day Counters
    - Time of day Alarm
- 32.768 kHz Crystal Oscillator
- Coin Cell Battery Backup and Charger

Serial Interface

- SPI
- I^2C

6.2 Block Diagram

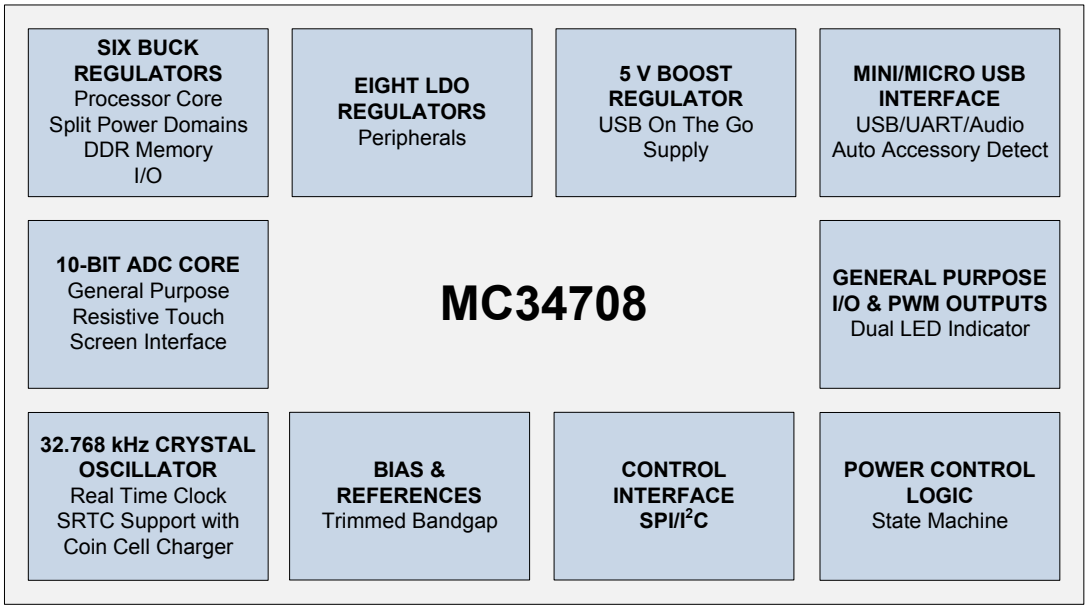


Figure 4. Functional Block Diagram

6.3 Functional Description

The MC34708 Power Management Integrated Circuit (PMIC) represents a complete system power solution in a single package. Designed specifically for use with the Freescale i.MX50/53 families. The MC34708 integrates six multi-mode buck regulators and eight LDO regulators for direct supply of the processor core, memory and peripherals.

The USB switch enables the use of a single, mini or micro USB connector for USB, UART and audio connections, switching the relevant signals to the connector depending on the type of device connected. In addition, the MC34708 also integrates a real time clock, coin cell charger, a 13-channel 10-bit ADC, 5 V USB Boost regulator, two PWM outputs, touch-screen interface, status LED drivers and four GPIOs.

7 Functional Block Description

7.1 Startup Requirements

When power is applied, there is an initial delay of 8.0 ms during which the core circuitry is enabled. The switching and linear regulators are then sequentially enabled in time slot steps of 2.0 ms. This allows the PMIC to limit the inrush current.

The outputs of the switching regulators not enabled are discharged with weak pull-downs on the output to ensure a proper power-up sequence. Any undervoltage detection at BP is masked while the power-up sequencer is running. When the switching regulators are enabled, they will start in PWM mode. After 3.0 ms, the switching regulators will transition to the mode programmed in the SPI register map.

The Power-up mode select pins PUMSx (x = 1, 2, 3, 4, and 5) are used to configure the start-up characteristics of the regulators. Supply enabling and output level options are selected by hardwiring the PUMSx pins. It is recommended to minimize the load during system boot-up by supplying only the essential voltage domains. This allows the start-up transients to be minimized after which the rest of the system power tree can be brought up by software. The PUMSx pins also allow optimization of the supply sequence and default values. Software code can load the required programmable options without any change to hardware.

The state of the PUMSx pins are latched before any of the regulators are enabled, with the exception of VCORE. PUMSx options and start-up configurations are robust to a PCUT event, whether occurring during normal operation or during the 8.0 ms of pre-sequencer initialization, i.e. the system will not end up in an unexpected / undesirable consumption state.

Table 11 shows the initial setup for the voltage level of the switching and linear regulators, and whether they get enabled.

Table 11. Power Up Defaults

i.MX	Reserved	53 LPM	53 DDR2	53 DDR3	53 LVDDR3	53 LVDDR2	50 MDDR	50 LPDDR2	50 LPDDR2	50 MDDR	50 LPDDR2	50 MDDR
PUMS[4:1]	0000-0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
PUMS5=0 VUSB2 VGEN2	Reserved	Ext PNP	Ext PNP	Ext PNP	Ext PNP	Ext PNP	Ext PNP	Ext PNP	Ext PNP	Ext PNP	Ext PNP	Ext PNP
PUMS5=1 VUSB2 VGEN2	Reserved	Internal PMOS	Internal PMOS	Internal PMOS	Internal PMOS	Internal PMOS	Internal PMOS	Internal PMOS	Internal PMOS	Internal PMOS	Internal PMOS	Internal PMOS
SW1A (VDDGP)	Reserved	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1
SW1B (VDDGP)	Reserved	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1
SW2[31] (VCC)	Reserved	1.225	1.3	1.3	1.3	1.3	1.2	1.2	1.2	1.2	1.2	1.2
SW3[31] (VDDA)	Reserved	1.2	1.3	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2
SW4A[31] (DDR/SYS)	Reserved	1.5	1.8	1.5	1.35	1.2	1.8	1.2	3.15	3.15	3.15	3.15
SW4B[31] (DDR/SYS)	Reserved	1.5	1.8	1.5	1.35	1.2	1.8	1.2	1.2	1.8	1.2	1.8
SW5[31] (I/O)	Reserved	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8
SWBST	Reserved	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off
VUSB[32]	Reserved	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3
VUSB2	Reserved	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5

Table 11. Power Up Defaults

i.MX	Reserved	53 LPM	53 DDR2	53 DDR3	53 LVDDR3	53 LVDDR2	50 MDDR	50 LPDDR2	50 LPDDR2	50 MDDR	50 LPDDR2	50 MDDR
VSRTC	Reserved	1.2	1.3	1.3	1.3	1.3	1.2	1.2	1.2	1.2	1.2	1.2
VPLL	Reserved	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8
VREFDDR	Reserved	On	On	On	On	On	On	On	On	On	On	On
VDAC	Reserved	2.775	2.775	2.775	2.775	2.775	2.5	2.5	2.5	2.5	2.5	2.5
VGEN1	Reserved	1.2	1.3	1.3	1.3	1.3	1.2	1.2	1.2	1.2	1.2	1.2
VGEN2	Reserved	2.5	2.5	2.5	2.5	2.5	3.1	3.1	3.1	3.1	2.5	2.5

Notes

31. The SWx node are activated in APS mode when enabled by the startup sequencer.
32. VUSB regulator is only enabled if 5.0 V is present on VBUS. By default VUSB will be supplied by VBUS. SWBST = 5.0 V powers up as does VUSB, regardless of 5.0 V present on UVBUS. By default VUSB is supplied by SWBST.

The power up sequence is shown in Tables 12 and 13. VCOREDIG, VSRTC, and VCORE, are brought up in the pre-sequencer startup.

Table 12. Power Up Sequence i.MX53

Tap x 2.0 ms	PUMS [4:1] = [0101,0110,0111,1000,1001] (i.MX53)
0	SW2 (VCC)
1	VPLL (NVCC_CKIH = 1.8 V)
2	VGEN2 (VDD_REG= 2.5 V, external PNP
3	SW3 (VDDA)
4	SW1A/B (VDDGP)
5	SW4A/B, VREFDDR (DDR/SYS)
6	
7	SW5 (I/O), VGEN1
8	VUSB [33], VUSB2
9	VDAC

Notes:

33. The VUSB regulator is only enabled if 5.0 V is present on the VBUS pin. By default VUSB will be supplied by the VBUS pin.