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Document Number: MC34827
Rev. 2.0, 3/2011

RoHS

Mini or Micro-USB Interface IC

34827

INTERFACE IC

(PB-FREE)
98ASA00050D
20-PIN UTQFN-EP

(PB-FREE)
98ASA00037D
20-PIN UTQFN-EP

The 34827 is a dedicated IC for managing charging and signal multiplexing between a cell phone and its accessory via a 5-pin Mini or Micro-USB connector. An external power source, such as a dedicated AC/DC adapter or a standard USB port, is able to charge the battery in the cell phone via the connector. The 34827 is capable of identifying the type of the external power source and selecting one of two battery charge current levels according to the type. The internal power switch can protect the phone system against 28 V power supply input. The 34827 is also able to multiplex the 5 pins to support UART and High-Speed USB 2.0 data communication, mono/stereo-audio/microphone headset with or without a cord remote control, manufacturing or R/D test cables and other accessories.

To identify what accessory is plugged into the Mini or Micro-USB connector, the 34827 supports various detection mechanisms, including the VBUS detection and ID detection. A high accurate 5-bit ADC is offered to distinguish the 32 levels of ID resistance and to identify the button pressed in a cord remote control while an Audio Type 1 cable is attached. After identifying the accessory attached, the 34827 configures itself to support the accessory and interrupts a host via an I^2C serial bus for further actions. The 34827 is also able to identify some non-supported accessory, such as video cable, Phone-Powered Devices and USB OTG devices. The host controls the 34827 via the I^2C serial bus.

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC34827A2EP/R2	-40 to 85 °C	3.0 mm X 4.0 mm UTQFN-EP
MC34827A1EP/R2		3.0 mm X 3.0 mm UTQFN-EP

Features

- Automatically identifies the power supply type and sets one of two battery-charge-current levels
- Internal power switch protects the phone system against 28 V power supply input
- Supports stereo/mono headset with or without micro phone and remote control
- Supports USB or UART test and R/D cables
- High speed USB2.0 compliant
- Supports 32 ID resistance values with a high-accuracy 5-bit ADC
- I^2C interface with interrupt to the host
- 10 μA quiescent current in Standby mode

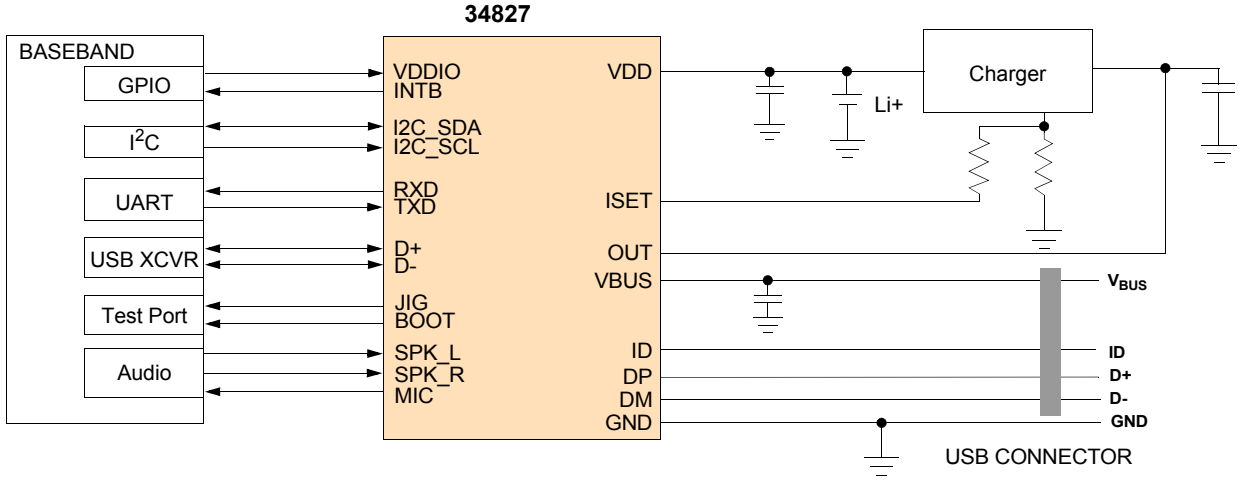


Figure 1. MC34827 Simplified Application Diagram

*This document contains certain information on a product under development. Freescale reserves the right to change or discontinue this product without notice

freescale semiconductor

INTERNAL BLOCK DIAGRAM

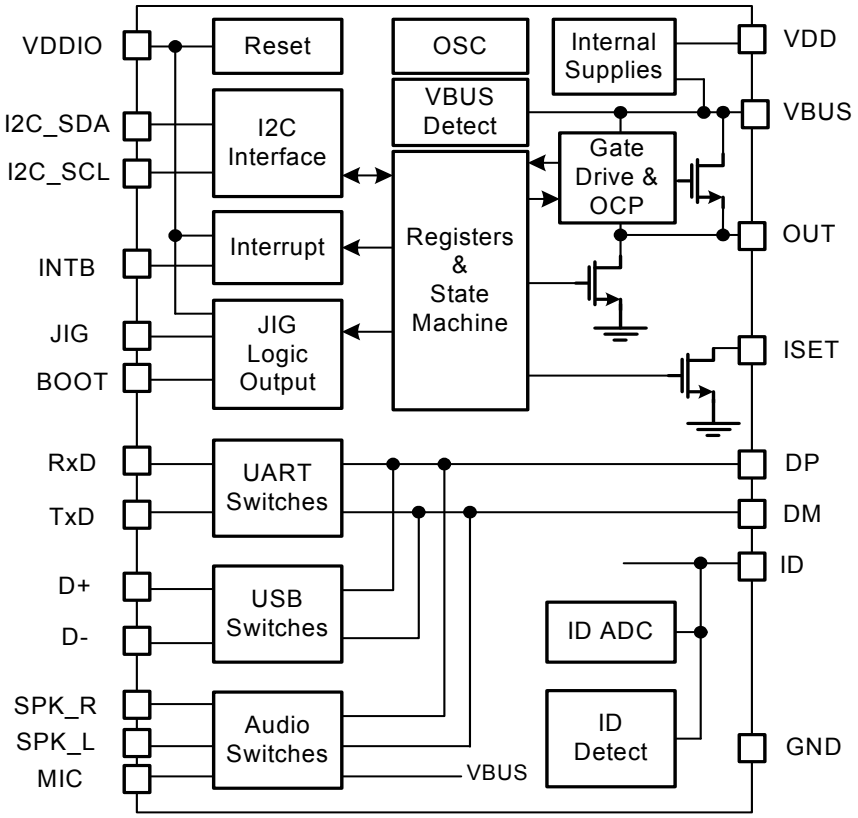
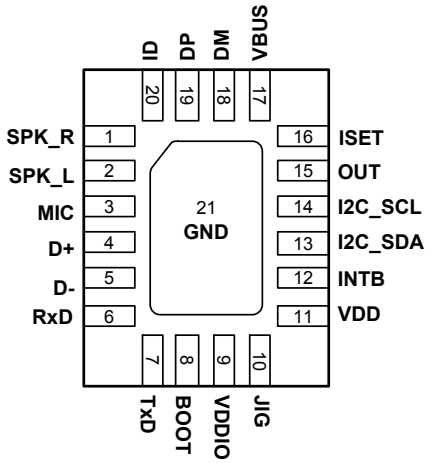
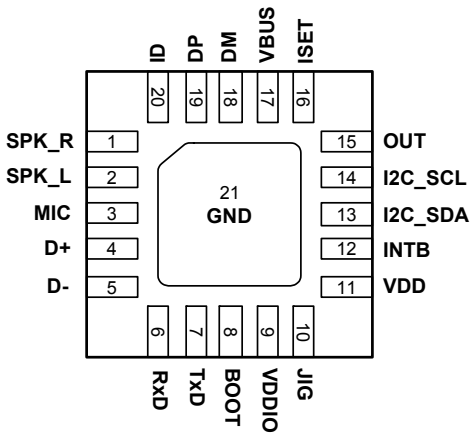


Figure 2. MC34827 Simplified Internal Block Diagram

PIN CONNECTIONS



(A). Pinout of 34827 Using a 3.0 mm X 4.0 mm 20 Pin. UTQFN Package
(Transparent Top View)



(B). Pinout of 34827 Using a 3.0 mm X 3.0 mm 20 Pin. UTQFN Package
(Transparent Top View)

Figure 3. MC34827 Pin Connections

Table 1. MC34827 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 13.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	SPK_R	Input	Speaker right channel	Right channel input of the speaker signals
2	SPK_L	Input	Speaker left channel	Left channel input of the speaker signals
3	MIC	Output	Microphone output	Microphone output to the baseband of the cell phone system
4	D+	IO	D+ of the USB transceiver	D+ line of the USB transceiver
5	D-	IO	D- of the USB transceiver	D- line of the USB transceiver
6	RxD	Output	UART receiver	Receive line of the UART
7	TxD	Input	UART transmitter	Transmit line of the UART
8	BOOT	Output	BOOT indicator	Push-pull output to indicate the boot switch setting of the jig cable
9	VDDIO	Input	IO power supply	IO supply voltage. This is the internal supply voltage for the BOOT and INTB outputs. It can supply the external pull-up voltages for the JIG pin and the I^2C bus outside the 34827. This pin also functions as the hardware reset to the IC.
10	JIG	Output	JIG indicator	Open-drain output to indicate the insertion of a jig cable
11	VDD	Input	Power supply	Supply input
12	INTB	Output	Interrupt output	Push-pull interrupt output
13	I2C_SDA	IO	I^2C Data	Data line of the I^2C interface
14	I2C_SCL	Input	I^2C Clock	Clock line of the I^2C interface
15	OUT	Output	Power output	The output of the power MOSFET pass switch
16	ISET	Output	Charge current setting	Open-drain output to set the charger current
17	VBUS	Input	VBUS power supply	Mini-USB VBUS line

Table 1. MC34827 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 13.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
18	DM	IO	D- of the USB connector	D- line of the mini-USB connector
19	DP	IO	D+ of the USB connector	D+ line of the mini-USB connector
20	ID	Input	ID of the USB connector	ID pin of the mini-USB connector
21	GND	Ground	Ground	Ground

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Input Voltage Range			V
VBUS Pin	V_{BUS}	-0.3 to 28	
OUT Pin	V_{OUT}	-0.3 to 8	
VDD Pin	V_{DD}	-0.3 to 6	
VDDIO Pin(1)	V_{DDIO}	-0.3 to 4.2	
SPK_L, SPK_R, DP and DM Pins		-2.0 to V_{DD}+0.3	
All Other Pins		-0.3 to 5.5	
ESD Voltage (2)	V_{ESD}		V
Air Gap Discharge Model for VBUS, DP, DM, ID Pins(3)		±15000	
Human Body Model (HBM) for VBUS, DP, DM, ID Pins		±8000	
Human Body Model (HBM) for all other pins		±2000	
Machine Model (MM)		±200	
THERMAL RATINGS			
Operating Temperature			°C
Ambient	T_A	-40 to +85	
Junction	T_J	150	
Storage Temperature	T_{STG}	-65 to +150	°C
Thermal Resistance (4)			°C/W
Junction-to-Case	$R_{\theta JC}$	6	
Junction-to-Ambient	$R_{\theta JA}$	45	
Peak Package Reflow Temperature During Reflow (5), (6)	T_{PPRT}	Note 6	°C

Notes

1. The VDDIO pin CANNOT exceed a maximum voltage of 4.2 V, else it will suffer permanent damage.
2. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the Machine Model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
3. Need external ESD protection diode array to meet IEC1000-4-2 15000V air gap discharge requirement (C_{ZAP} = 150 pF, R_{ZAP} = 330 Ω).
4. Device mounted on the Freescale EVB test board per JEDEC DESD51-2.
5. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
6. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.freescale.com, search by part number, e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions V_{DD} = 3.6 V, V_{BUS} = 5.0 V, V_{DDIO} = 3.0 V, -40 °C ≤ T_A ≤ 85 °C (see Figure 1), unless otherwise noted. Typical values noted reflect the approximate parameter means at V_{DD} = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Recommended Operating Voltage Range for VDD Supply Voltage	V_{DD}	2.7	-	5.5	V
VDD Power-on Reset Threshold	V_{VDDPOR}				
Rising edge		-	2.5	2.65	V
Hysteresis		-	100	-	mV
VDD Quiescent Current	I_{VDD}				µA
In Standby mode		-	9.0	12	
In Power Save mode		-	12	18	
When accessory is attached & INT_MASK = '1'		-	125	160	
In Active mode (VDD < VBUS)		-	550	650	
In Active mode (VDD > VBUS)		-	850	1000	
VBUS Supply Voltage	V_{BUS}	2.8	5.0	28	V
VBUS Detection Threshold Voltage	V_{BUS_DET}				
Rising edge		-	2.65	2.80	V
Hysteresis		-	150	-	mV
VBUS Supply Quiescent Current	I_{VBUS}				
In VBUS power mode		-	-	1.2	mA
In Active mode - Dedicated Charger		-	-	1.2	mA
In Active mode - Audio or TTY[7] (VBUS < VDD)		-	-	0.5	µA
VBUS Over-voltage Protection Threshold	V_{BUS_OVP}				
Rising edge		6.8	7.0	7.2	V
Hysteresis		-	150	-	mV
VBUS Over-current Protection	I_{BUS_OCP}				
Triggering threshold (at onset of OTP shutoff)		1.2	1.8	2.2	A
Over-temperature Protection Threshold	T_{OTP}				°C
Rising threshold		115	130	145	
Falling threshold		-	95	-	
VDDIO Supply Voltage	V_{DDIO}	1.65	-	3.6	V
SWITCH					
ISET Open-drain Output MOSFET					
On resistance (loaded by 3.0 mA current)	R_{ISET}	-	-	100	Ω
Leakage current (when the MOSFET is off at 5.0 V bias voltage)	I_{ISET_OFF}	-	-	0.5	µA
OUT Pin Discharge MOSFET[16]					
On resistance (loaded by 3.0 mA current)	R_{OUT_DISC}	-	-	100	Ω
Leakage current (when the MOSFET is off at 5.0 V bias voltage)	I_{OUT_OFF}	-	0.5	-	µA

Notes

7. This is an important specification because when an audio accessory is attached, the VBUS line is connected to the microphone. The quiescent current will affect the bias of the microphone.
8. The OUT pin discharge MOSFET is shown in Figure 20. This MOSFET will be turned on when the power MOSFET is off.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions V_{DD} = 3.6 V, V_{BUS} = 5.0 V, V_{DDIO} = 3.0 V, -40 °C ≤ T_A ≤ 85 °C (see Figure 1), unless otherwise noted. Typical values noted reflect the approximate parameter means at V_{DD} = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Power MOSFET On resistance (when V_{BUS} = 5.0 V, T_A< 50 °C)	R_{PSW}	 -	 200	 250	mΩ
SPK_L and SPK_R Switches On resistance (20 Hz to 470 kHz) Matching between channels On resistance flatness (from -1.2 V to 1.2 V)	 R_{SPK_ON} R_{SPK_ONMCT} R_{SPK_ONFLT}	 - - -	 1.6 0.12 0.01	 3.0 0.25 0.05	Ω
D+ and D- Switches On resistance (0.1 Hz to 240 MHz) Matching between channels On resistance flatness (from 0.0 V to 3.3 V)	 R_{USB_ON} R_{USB_ONMCT} R_{USB_ONFLT}	 - - -	 - 0.1 0.02	 5.0 0.5 0.1	Ω
RxD and TxD Switches On resistance On resistance flatness (from 0.0 V to 3.3 V)	 R_{UART_ON} R_{UART_ONFLT}	 - -	 - -	 60 5.0	Ω
MIC Switches On resistance (at below 2.3 V MIC bias voltage) On resistance flatness (from 1.8 V to 2.3 V)	 R_{MIC_ON} R_{MIC_ONFLT}	 - -	 - -	 100 5.0	Ω
Pull-down Resistors between SPK_L or SPK_R Pins to GND	R_{PD_AUDIO}	-	100	-	kΩ
Signal Voltage Range SPK_L, SPK_R, D+, D-, RxD, TxD, MIC		 -1.5 -0.3	 - -	 1.5 3.6	V
PSRR - From VDD (100 mVrms) to DP/DM Pins [9] 20 Hz to 20 kHz with 32/16 Ω load.	V_{A_PSRR}	 -	 -	 -60	dB
Total Harmonic Distortion[9] 20 Hz to 20 kHz with 32/16 Ω load.	THD	 -	 -	 0.05	%
Crosstalk between Two Channels[9] 20 Hz to 20 kHz with 32/16 Ω load.	V_{A_CT}	 -	 -	 -50	dB
Off-Channel Isolation[9] Less than 1.0 MHz	V_{A_ISO}	 -	 -	 -100	dB
POWER SUPPLY TYPE IDENTIFICATION					
Data Source Voltage Loaded by 0~200 μA	V_{DAT_SRC}	 0.5	 0.6	 0.7	V
Data Source Current	I_{DAT_SRC}	0	-	200	μA
Data Detect Voltage	V_{DAT_REF}	0.3	0.35	0.4	V
Car Kit Detect Voltage	V_{CR_REF}	0.8	0.9	1.0	V
Data Sink Current DM pin is biased between 0.15 to 3.6 V	I_{DAT_SINK}	 65	 100	 135	μA
DP, DM Pin Capacitance	$C_{DP/DM}$	-	8.0	-	pF

Notes

9. Not tested. Guaranteed by design.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions V_{DD} = 3.6 V, V_{BUS} = 5.0 V, V_{DDIO} = 3.0 V, -40 °C ≤ T_A ≤ 85 °C (see Figure 1), unless otherwise noted. Typical values noted reflect the approximate parameter means at V_{DD} = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
DP, DM Pin Impedance	$R_{DP/DM}$				MΩ
All switches are off (Switch_Open = 0)		-	50	-	
ID DETECTION					
ID FLOAT Threshold	V_{FLOAT}				V
Detection threshold		-	2.3	-	
Pull-up Current Source	I_{ID}				μA
When ADC Result is 1xxxx		1.9	2.0	2.1	
When ADC Result is 0xxxx		30.4	32	33.6	
Video Cable Detection					
Detection current	I_{VCBL}	1.0	1.2	1.4	mA
Detection voltage low threshold	V_{VCBL_L}	-	50	-	mV
Detection voltage high threshold	V_{VCBL_H}	-	118	-	mV
LOGIC INPUT AND OUTPUT					
VDDIO Logic Input Threshold					
Input LOW threshold	V_{DDIO_IL}	-	-	0.5	V
Input HIGH threshold	V_{DDIO_IH}	1.5	-	-	V
Push-Pull Logic Output (INTB and BOOT)					V
Output HIGH level (loaded by 1.0 mA current)	V_{OH}	$0.7V_{DDIO}$	-	-	
Output LOW level (loaded by 4.0 mA current)	V_{OL}	-	-	0.4	
Open-Drain Logic Output (JIG)	V_{JIGOL}				V
Output LOW level (loaded by 4.0 mA current)		-	-	0.4	
I^2C INTERFACE					
Low Voltage on I2C_SDA, I2C_SCL Inputs	V_{I2C_IL}	-0.2	-	$0.3V_{DDIO}$	V
High Voltage on I2C_SDA, I2C_SCL Inputs	V_{I2C_IH}	$0.7V_{DDIO}$	-	V_{DDIO}	V
Low Voltage on I2C_SDA Output	V_{I2C_OL}	-	-	0.4	V
Current Load when I2C_SDA Outputs Low Voltage	I_{I2C_OL}	0	-	4.0	mA
Leakage Current on I2C_SDA, I2C_SCL Outputs	I_{I2C_LEAK}	-1.0	-	1.0	μA
Input Capacitance of the I2C_SDA, I2C_SCL Pins(10)	C_{I2CIN}	-	-	8.0	pF

Notes
10. Not tested. Guaranteed by design.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions V_{DD} = 3.6 V, V_{BUS} = 5.0 V, V_{DDIO} = 3.0 V, -40 °C ≤ T_A ≤ 85 °C (see Figure 1), unless otherwise noted. Typical values noted reflect the approximate parameter means at V_{DD} = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER ON AND OFF DELAY					
VDD Power-on Reset Threshold					ms
VDD rising deglitch time	t_{D2}	7.0	8.5	10.2	
VDD falling deglitch time	t_{VDDDGT_F}	1.7	2.5	3.5	
VBUS Detection Threshold Deglitch Time (for Both Rising and Falling Edges)	t_{VBUS_DET}	3.5	4.5	5.7	ms
VBUS Over-voltage Protection					µs
Protection delay(11)	t_{OVPD}	-	-	2.0	
Falling-edge deglitch time(12)	t_{OVPDGT_F}	-	25	-	
VBUS Over-temperature Protection					
MOSFET turning off speed when OTP occurs(13)	t_{OTP_TO}	-	-	0.5	A/µs
Deglitch time	t_{OTP_DGT}	-	15	-	µs
OSCILLATOR					
Oscillation Frequency	f_{OSC}	88	100	112	kHz
SWITCHING DELAY					
t_1 - t_0 (td in Figure 17, Default Value is TD = 0100)	t_d				ms
TD = 0000		-	100	-	
TD = 0001		-	200	-	
TD = 0010		-	300	-	
TD = 0011		-	400	-	
TD = 0100		-	500	-	
...		...	...	...	
TD = 1111		-	1600	-	
t_2 - t_1(Figure 17)	t_{SW}	20	-	-	ms
t_3 - t_2(Figure 17)	t_{SW}	20	-	-	ms
t_4 - t_1(Figure 17)	t_{SW}	100	-	-	ms
t_6 - t_3(Figure 17)	t_{SW}	100	-	-	ms
ID DETECTION					
ID FLOAT Detection Deglitch Time	t_{ID_FLOAT}	-	20	-	ms
Video Cable Detection Time (Video Cable Detection Current Source On Time)	t_{VCBL}	-	20	-	ms
ADC					
ADC Conversion Time	t_{CONV}	-	1.0	-	ms

Notes

11. The protection delay is defined as the interval between VBUS voltage rising above the OVP rising threshold, and the OUT pin voltage dropping below the OVP rising threshold voltage for a VBUS ramp rate of >1.0 V/µs.
12. The OVP deglitch timer is only for the falling edge threshold.
13. Not tested. Guaranteed by design.

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions V_{DD} = 3.6 V, V_{BUS} = 5.0 V, V_{DDIO} = 3.0 V, -40 °C ≤ T_A ≤ 85 °C (see Figure 1), unless otherwise noted. Typical values noted reflect the approximate parameter means at V_{DD} = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
REMOTE CONTROL					
Key Press Comparator Debounce Time	t_{RMTCON_DG}	-	20	-	ms
RESET TIMING					
Device Reset Time	t_{RSTDVC}	-	10	-	µs
VDDIO Logic Input Timing					µs
Rising-edge deglitch time	$t_{VDDIODGT\_R}$	660	875	1130	
Falling-edge deglitch time	$t_{VDDIODGT\_F}$	105	125	150	
VDDIO Reset Timing					µs
VDDIO reset pulse width	$t_{RSTVDDIO}$	150	-	-	
I^2C Reset Timing					ms
I^2C reset pulse width	t_{RSTI2C}	13.5	-	-	
I2C_SDA/I2C_SCL concurrent low time without causing reset	$t_{NRSTI2C}$	-	-	8.8	
I^2C INTERFACE(14)					
SCL Clock Frequency	f_{SCL}	-	-	400	kHz
Bus Free Time between a STOP and START Condition	t_{BUF}	1.3	-	-	µs
Hold Time Repeated START Condition	$t_{HD:STA}$	0.6	-	-	µs
Low Period of SCL Clock	t_{LOW}	1.3	-	-	µs
High Period of SCL Clock	t_{HIGH}	0.6	-	-	µs
Setup Time for a Repeated START condition	$t_{SU:STA}$	0.6	-	-	µs
Data Hold Time	$t_{HD:DAT}$	0	-	-	µs
Data Setup Time	$t_{SU:DAT}$	120	-	-	ns
Rising Time of Both SDA and SCL Signals	t_R	20+0.1C_B	-	-	ns
Falling Time of Both SDA and SCL Signals	t_F	20+0.1C_B	-	-	ns
Setup Time for STOP Condition	$t_{SU:STO}$	0.6	-	-	µs
Input Deglitch Time (for Both Rising and Falling Edges)	t_{DGT}	55	-	300	ns

Notes
14. Not tested. Guaranteed by design.

ELECTRICAL PERFORMANCE CURVES

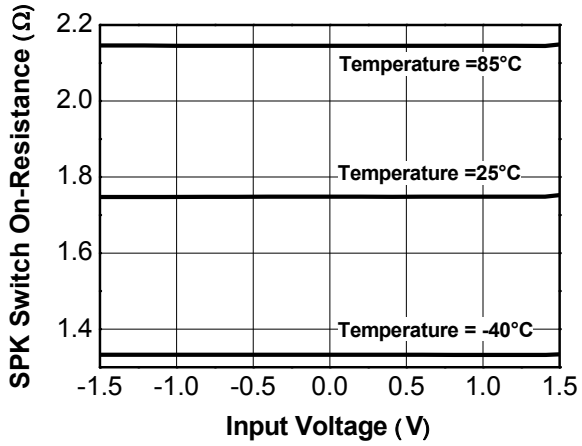


Figure 4. SPK Switch On-resistance vs Input Voltage

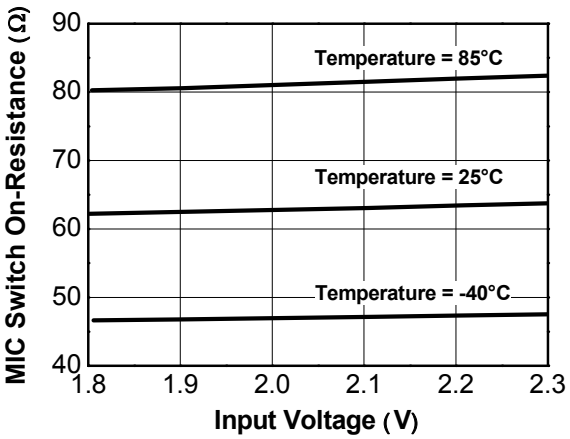


Figure 7. MIC Switch On-resistance vs Input Voltage

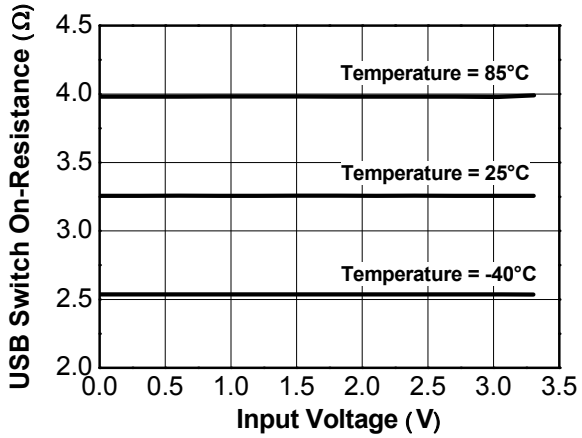


Figure 5. USB Switch On-resistance vs Input Voltage

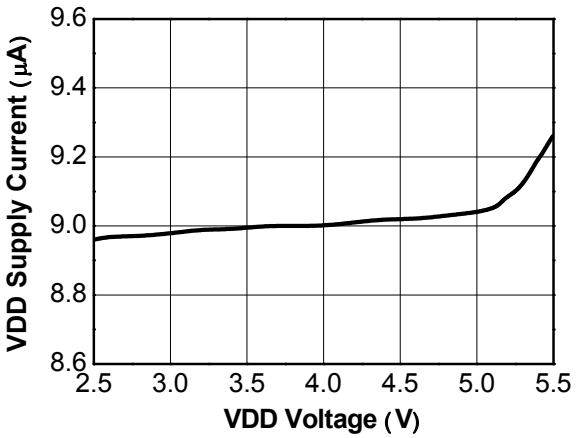


Figure 8. VDD Supply Current vs Supply Voltage In Standby Mode

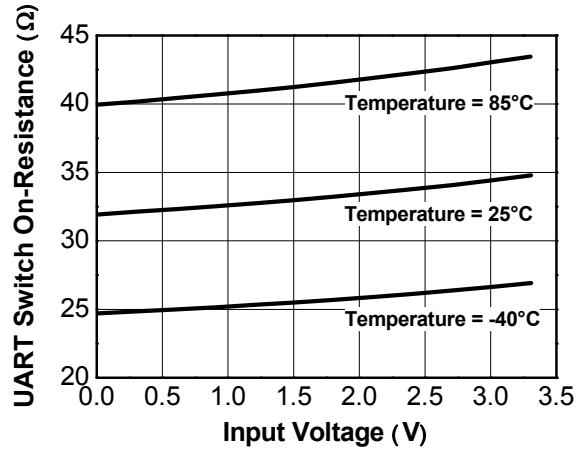


Figure 6. UART Switch On-resistance vs Input Voltage

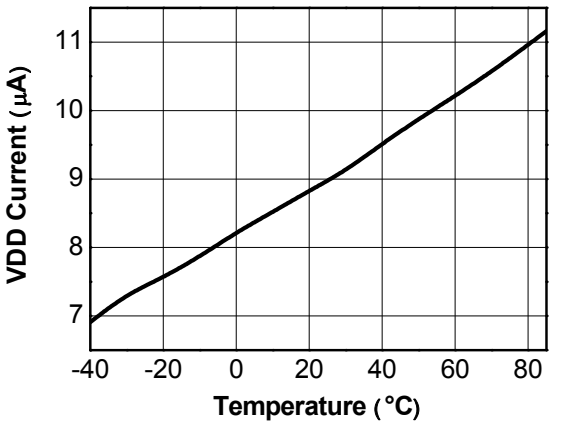


Figure 9. VDD Supply Current vs Temperature In Standby Mode

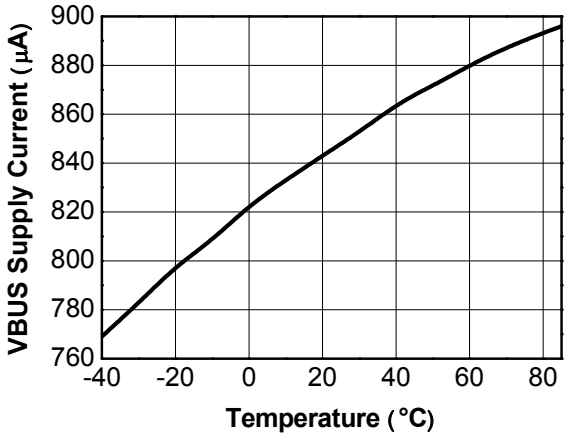


Figure 10. VBUS Supply Current vs Temperature In VBUS Power Mode

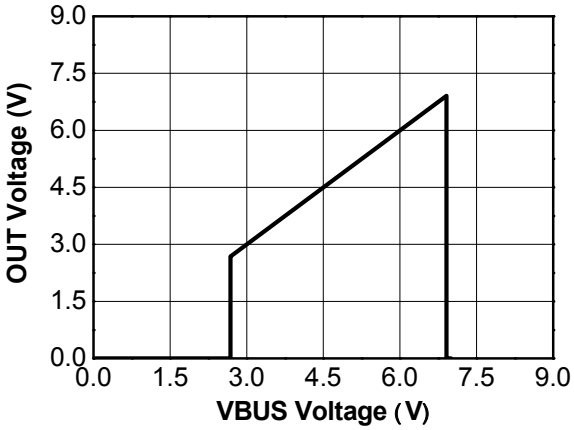


Figure 11. OUT Voltage vs VBUS Voltage

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 34827 is used to identify what is attached to the Mini or Micro-USB connector, configure the signal paths between the phone baseband and the 5-pin connector accordingly, and then inform the baseband of the attachment. It also detects the detachment of accessory and then informs the baseband.

To identify what is plugged into the Mini or Micro-USB connector, the 34827 supports various detection mechanisms, including ID detection and VBUS detection. The detection flow is initiated either by the change of VBUS pin voltage or by the change of ID pin voltage. A high accurate 5-bit ADC is offered to distinguish the 32 levels of ID resistance. Each level of resistance can be assigned to an accessory or a button in a cord remote controller. Some non-supported accessories, such as video cable, Phone-Powered Devices, USB OTG devices and so on, can also be identified. For 34827, the mapping relationship between the ADC values and the types of accessories is fixed and the detailed information is given in section Application Information.

The detachment of accessory is also monitored by both of the ID detector and the VBUS detector.

The host IC can control the 34827 via an I^2C serial bus.

FUNCTIONAL PIN DESCRIPTION

SPEAKER RIGHT CHANNEL (SPK_R)

Right channel of the baseband speaker output.

SPEAKER LEFT CHANNEL (SPK_L)

Left channel of the baseband speaker output.

MICROPHONE OUTPUT (MIC)

Microphone output to the baseband.

D+ OF THE USB TRANSCEIVER (D+)

D+ line of the USB transceiver.

D- OF THE USB TRANSCEIVER (D-)

D- line of the USB transceiver.

UART RECEIVER (RXD)

Receiver line of the UART.

UART TRANSMITTER (TXD)

Transmitter line of the UART.

BOOT INDICATOR (BOOT)

VDDIO referenced push-pull output to indicate the boot switch setting of jig cables.

IO POWER SUPPLY (VDDIO)

Power supply input for the logic IO interface. Generally the IO power supply voltage should be the same as the IO voltage used in the cell phone system. VDDIO is also one of hardware reset input sources. A falling edge at this pin will reset the 34827.

JIG INDICATOR (JIG)

Open-drain output to indicate the insertion of a jig cable.

POWER SUPPLY (VDD)

Power supply input. Bypass to ground with a 1.0 μF capacitor.

INTERRUPT OUTPUT (INTB)

Active low and VDDIO referenced push-pull output. When the 34827 detects a change of external cable status, this pin outputs low voltage to interrupt the baseband. INTB returns to high voltage once all the interrupt bits are read.

DATA LINE OF THE I^2C INTERFACE (I2C_SDA)

Data line of the I^2C interface. I2C_SDA together with I2C_SCL is one of hardware reset input sources.

CLOCK LINE OF THE I^2C INTERFACE(I2C_SCL)

Clock line of the I^2C interface. I2C_SCL together with I2C_SDA is one of hardware reset input sources.

POWER OUTPUT (OUT)

Output of the power MOSFET in the 34827. This pin is connected to a charger. Bypass to ground with a 1.0 μF capacitor.

CHARGE CURRENT SETTING (ISET)

Open-drain output to set the charge current for a charger according to the VBUS power supply type.

VBUS POWER SUPPLY (VBUS)

Mini-USB VBUS input. Bypass this pin to ground with a less than 10nF capacitor. When the attached accessory is an audio kit, this pin is the microphone input to the 34827.

D- OF THE USB CONNECTOR (DM)

D- line of the mini-USB connector.

D+ OF THE USB CONNECTOR (DP)

D+ line of the mini-USB connector.

ID OF THE USB CONNECTOR (ID)

ID pin of the mini-USB connector.

GROUND (GND)

Ground.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

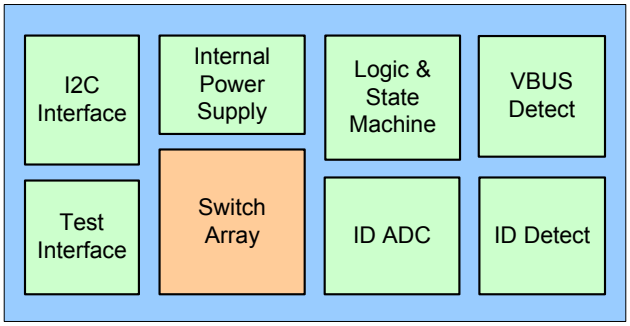


Figure 12. MC34827 Functional Internal Block Diagram

LOGIC AND STATE MACHINE

Internal state machine executes the detection and identification flow and turns on or off the signal switches according to the identification result.

I²C INTERFACE

I²C interface circuit is an I²C slave device. It receives commands and data from an I²C master device and transfers them to internal registers of 34827. It also transfers the data from the registers of 34827 to the I²C master device.

TEST INTERFACE

Test interface connects to a test block of the baseband.

SWITCH ARRAY

Switch array consist of switches for UART, USB and audio signal channels.

INTERNAL POWER SUPPLY

This block outputs power supply for the internal digital IO interface and also outputs high power supply for all internal blocks and for the external battery charger. The input power supplies of the block include VBUS, VDD and VDDIO.

VBUS DETECT

This block detects whether the power supply at VBUS pin is present.

ID ADC

An internal 5-bit ADC measures the resistance at the ID pin. The result is sent to the Logic and State Machine block to determine what accessory is attached.

ID DETECT

This block generates current sources and other signals to the ID pin to help the ID ADC block measure the ID resistance.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

According to the status of the VBUS and VDD power supplies, the 34827 has five operational modes: Power Down mode, VBUS Power mode, Standby mode, Active mode, and Power Save mode. The mode-transition diagram is given in Figure 13. Details about the mode-transition conditions can be found in Figure 14.

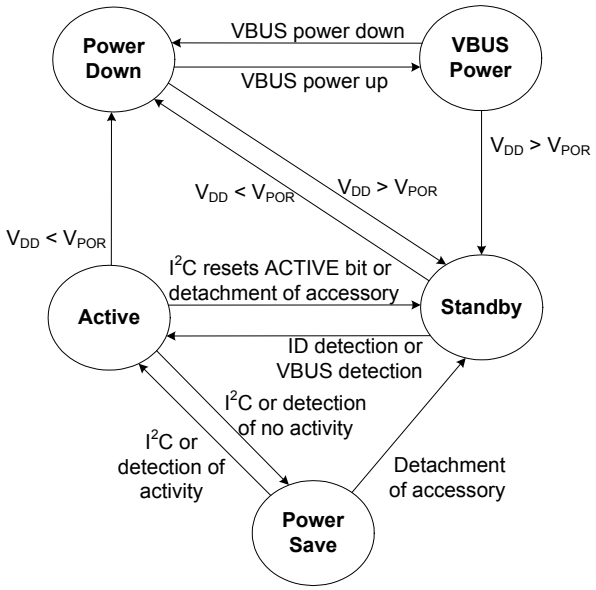


Figure 13. Mode Transition Diagram

POWER DOWN MODE

The Power Down mode is when neither the VDD nor the VBUS is powered. In this mode, the IC does not respond to any accessory attachment except for a power supply. When an external power supply is plugged, the 34827 enters the VBUS Power mode.

VBUS POWER MODE

34827 enters the VBUS Power mode when VBUS is powered but VDD is not. The 34827 supports regular USB port, dedicated charger, USB charger, 5 wire charger, charger on the A/V cable and any other accessory with powered VBUS voltage. In VBUS Power mode, the internal power MOSFET is turned on to power the charger IC, charging the battery in the phone. ISET pin outputs high impedance to select a lower charge current level for the charger IC.

STANDBY MODE

The Standby mode is when the VDD voltage is higher than the POR (Power-On Reset) threshold and no accessory is attached. In this mode only ID detection circuit, I^2C interface, and internal registers are powered in order to minimize the quiescent current of VDD. The ID detection circuit samples the status of ID line in a period which can be programmed by the Device Wake Up bits in Timing Set 1 register (refer to Register Map section for more register information).

In Standby mode, all signal switches and the power MOSFET are turned off. The ISET, JIG pins output high impedance and BOOT pin outputs low logic voltage.

If detecting an accessory attachment, the 34827 moves to the Active mode for further accessory identification.

ACTIVE MODE

The Active mode starts when an accessory is plugged with VDD powered. The 34827 identifies the accessory, configures the signal paths according to the identification result and interrupts the baseband for further actions. Different functions will be enabled according to the identification result. The quiescent current of VDD in Active mode is dependent on the type of attached accessory. The signal switches can also be turned on manually. See more information in section Control Functions.

Mode can be changed from Active to Standby either by accessory detachment or by I^2C programming.

POWER SAVE MODE

The Power Save mode is contributing only for the accessory of Audio Type 1 or TTY. The 34827 enters into

Power Save mode to minimize the operating current when Audio Type 1 or TTY accessory is attached but not used. For example, when the Audio Type 1 accessory is attached and the cell phone is not in audio playing mode, the baseband can move the 34827 to the Power Save mode via the I^2C programming. The 34827 can also automatically switch to Power Save mode when no activity is detected on the SPK_R or SPK_L pins for a period which can be programmed by the Activity Idle Detection Time bits in Timing Set 1 register. The power consumption in Power Save mode approximates that in Standby mode.

The 34827 can quit the Power Save mode to Active mode by I^2C programming or automatically when detecting signal activity. The configuration of the 34827 before switching to the Power Save mode is resumed. The mode can also be changed from Power Save mode directly to Standby mode due to the accessory detachment.

DEVICE MODE REGISTER

The PSAVE bit, ACTIVE bit and RST bit in Device Mode register hold the information of the device operational mode. The RST bit, which is of R/C type, indicates whether a reset has occurred. The RST is set when a Power-on Reset of VDD, or a hardware reset of VDDIO input, or a hardware reset of I^2C inputs occurs, and it will be cleared when it is read by I^2C. The ACTIVE bit and the PSAVE bit together indicate the device mode according to the relationship shown in Table 5. When the device is in VBUS Power mode, registers are not powered up.

The ACTIVE bit and PSAVE bit are of R/W type. The baseband can move the device mode to Standby mode manually by writing 0x00 to the Device Mode register via I^2C. If an accessory is still attached during the operation, the accessory identification flow shown in Figure 14 can be re-started.

Table 5. The Device Modes vs. the Register Bits

PSAVE	ACTIVE	MODE
0	0	Standby
0	1	Active
1	1	Power Save
1	0	Undefined

POWER-UP

The 34827 has four possible power-up scenarios depending on which of the VDD and the VBUS is powered first. The four scenarios correspond to the following four mode transitions (refer to Figure 14):

1. **From Power Down to VBUS Power:** VBUS is powered up when $V_{VDD} < V_{VDDPOR}$ (VDD POR threshold)
2. **From VBUS Power to Standby:** VBUS is already powered when the VDD rises above its POR threshold
3. **From Power Down to Standby:** VDD is powered up when $V_{VBUS} < V_{VBUSPOR}$ (VBUS POR threshold)
4. **From Standby to Active:** VDD is already powered when VBUS rises above its POR threshold

SCENARIO 1: VDD = 0 V AND VBUS IS POWERED UP (POWER DOWN MODE TO VBUS POWER MODE TRANSITION)

If VDD is not powered but the VBUS is powered up to a voltage range between the POR threshold and the OVP threshold, the internal charge pump for the power MOSFET gate driver starts to operate, softly turning on the power MOSFET. The IC is in the VBUS Power mode.

In this case, the ISET outputs high-impedance, all registers are in reset states.

SCENARIO 2: VBUS = HIGH AND VDD IS POWERED UP (VBUS POWER MODE TO STANDBY MODE TRANSITION)

If the VBUS is already powered up, when VDD is powered, the device moves from the VBUS Power mode to the Standby mode and then quickly move to the VBUS detection flow of the Active mode to identify the accessory, as shown in Figure 14.

After VDD is powered up, the 34827 starts up the internal supplies. The POR resets all register bits. The power MOSFET remains on during the reset process.

SCENARIO 3: VBUS = 0 V AND VDD IS POWERED UP (POWER DOWN MODE TO STANDBY MODE TRANSITION)

If no accessory is plugged, when VDD is powered, the 34827 moves from the Power Down mode to the Standby mode. The internal supplies are started up first, and then the whole chip is reset and is ready to accept accessories. When an accessory is attached, the 34827 enters the Active mode. The power MOSFET is off in this case since VBUS = 0 V.

SCENARIO 4: VDD = HIGH AND VBUS IS POWERED UP (STANDBY TO ACTIVE MODE TRANSITION)

This is a normal VBUS detection case.

ACCESSORY IDENTIFICATION

The identification flow chart is shown in Figure 14.

When an accessory with powered VBUS is attached in Power Down mode, the 34827 enters VBUS Power mode. The 34827 will not identify the type of accessory in VBUS Power mode. The ISET pin outputs high-impedance for all accessories, and the power MOSFET is turned on to pass the VBUS voltage to the charger IC to charge the battery. Once the VDD is increased above the POR threshold, the 34827 enters Standby mode to start the identification flow

In the Standby mode, the 34827 monitors both the ID pin and the VBUS pin. If an accessory attachment is detected, the 34827 enters Active mode to start the identification flow. The ID detection state machine will find out what ID resistor is attached and the PSTI circuit will find out what type of power supplies is connected.

An identification conclusion can be drawn when the identification flow is finished. The corresponding bit in the Device Type register is set to indicate the device type, and the ATTACH bit in the Interrupt 1 register is set to inform the baseband; If the attached accessory can't be identified, the Unknown_Atta bit in the Interrupt 2 register will be set.

According to the automatic configuration capability of the 34827 in Active mode, there are three types of accessories:

1. Recognized and supported. Such accessories include: USB port, Dedicated charger, USB charger, A/V charger, 5-wire type 1 and 5-wire type 2 chargers, UART, Audio Type 1 cable, TTY accessory, USB jig cable and UART jig cable. Automatic configurations are supported for those accessories.
2. Recognized but not supported. These accessories can be identified but not supported by 34827, including A/V cable, Phone-Powered Devices, USB OTG accessories and Audio Type 2 cable.
3. Not recognized accessories. These will be identified as Unknown accessories.

The details on the identification flow in Active mode are described as following.

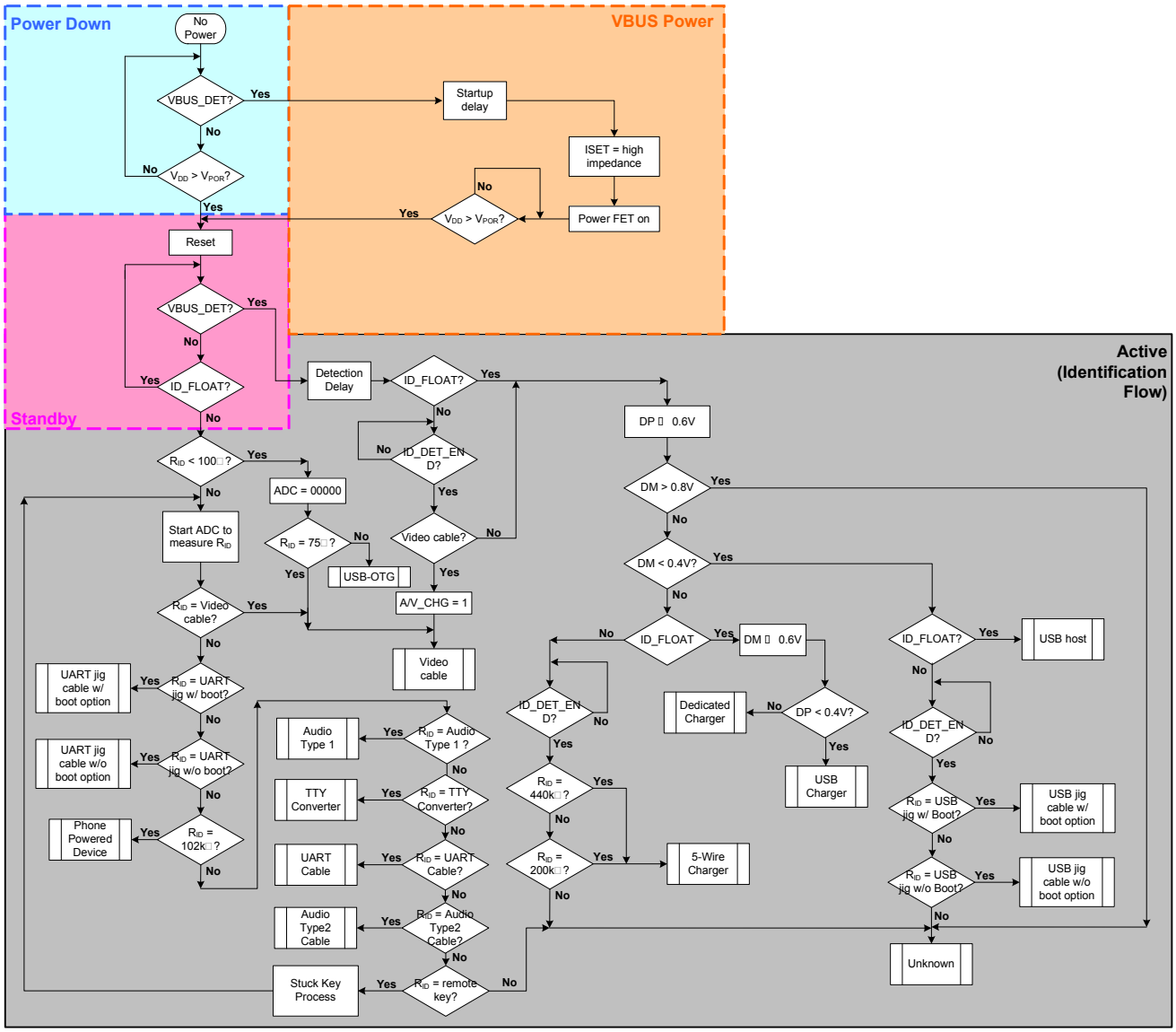


Figure 14. Detailed Accessory Identification Flow Diagram

RID IDENTIFICATION

A comparator monitors the ID pin impedance to ground. When a resistor less than 1.0 MΩ is connected between the ID line and the ground, the ID_FLOAT bit in the FSL Status 1 register will be set to 0; when the resistor is removed, ID_FLOAT bit will be set to 1. A falling-edge of this bit starts the identification flow and a rising-edge of this bit starts the detachment detection flow.

A signal, ID_DET_END, is used to indicate the end of the identification.

ID ADC

After the ID_FLOAT bit is set to 0, the identification flow is started, and an ADC_EN signal is set to enable an ADC conversion. A 5-bit ID ADC is used to measure the ID resistance. The ADC is also used to identify what button is pressed in a cord remote control when the attached accessory is Audio Type 1 cable. The ADC allows 32 levels for the ID resistance measurement and can accurately convert a 1% resistor value to a 5-bit result. The ADC outputs vs. ID resistor values are given in Table 6.

When the conversion completes, an ADC_STATUS bit is set and the ADC result value is sent to the ADC Result register. The ADC_EN signal is cleared automatically after the conversion finishes.

If the ID resistance is below 2.0 kΩ, the ADC Result is set to 00000. If the ID line is floating, the ADC Result is set to 11111.

STUCK KEY IDENTIFICATION

When the ADC conversion is finished and the ADC Result is found to be a value corresponding to a remote control key of Audio Type 1 cable, a stuck key process flow will be initiated to find out whether a remote control key is stuck and to inform the baseband of the stuck key status.

Figure 15 shows the stuck key process flow. If the stuck key is detected to be released within 1.5 s, the flow will return to re-start the ID identification flow; Otherwise, a Stuck_Key Interrupt will be set. When the key is released, a Stuck_Key_RCV Interrupt will be generated and then the identification flow will be re-started to find out the ID resistance of the attached cable.

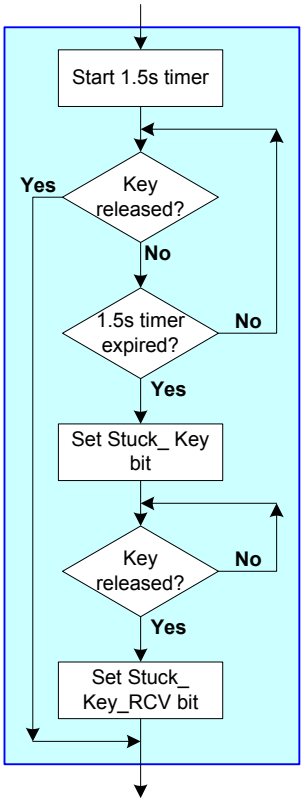


Figure 15. The Stuck Key Process Flow Diagram

Table 6. ADC Output vs. Resistor Values (Unit: kΩ)

ADC Result	R_{ID} (kΩ)	ADC Result	R_{ID} (kΩ)	ADC Result	R_{ID} (kΩ)	ADC Result	R_{ID} (kΩ)
00000	(15)	01000	10.03	10000	40.2	11000	255
00001	2.00	01001	12.03	10001	49.9	11001	301
00010	2.604	01010	14.46	10010	64.9	11010	365
00011	3.208	01011	17.26	10011	80.07	11011	442
00100	4.014	01100	20.5	10100	102	11100	523
00101	4.820	01101	24.07	10101	121	11101	619
00110	6.03	01110	28.7	10110	150	11110	1000
00111	8.03	01111	34.0	10111	200	11111	(16)

Notes:
15. If the ID resistance is below 1.9 kΩ, the ADC Result is set to 00000.
16. If the ID line is floating, the ADC Result is set to 11111

POWER SUPPLY TYPE IDENTIFICATION

The PSTI (Power Supply Type Identification) circuit is used in Active mode to identify the type of the connected power supply. The supported power supply should be compliant with the USB Battery Charging Specification Revision 1.1. The PSTI circuit first detects whether the DP and DM pins are short. If the DP and DM pins are found to be short, the PSTI circuit will continue to find out whether DP and DM are forward short or reverse short. The detection result together with the ID detection result is used to determine what powered accessory is connected.

The PSTI circuit is shown in Figure 16. Its operation is described as follows.

When the 34827 detects that the VBUS_DET bit is set, the PSTI identification flow starts.

1. Wait for a Detection Delay td (programmable in the Time Delay register).
2. During t_D, check to see whether ID_FLOAT = 0. If yes, then wait for the ID_DET_END to be set and check whether the attached is an A/V cable.
3. If the result is an A/V cable, set the A/V_CHG and ATTACH interrupt bits as well as the A/V bit in Device Type register to inform the baseband and finish the identification flow. If not, go to step 4.
4. Enable the PSTI (PSTI_EN set to '1') at t_1. When PSTI_EN rises, the switch SW1 is turned on to drive the data source voltage, V_{DAT_SRC}, to DP line. In the meantime, switch SW2 is turned on so the current source, I_{DAT_SINK}, sinks a current from the DM line. At t_2, the PSTI starts to compare the DM line voltage with references V_{DAT_REF} and V_{CR_REF}. If the DM line voltage stays above V_{DAT_REF} but below V_{CR_REF} for 20 ms continuously before t_4, which means that the DP and DM pins are short, the DP/DM_short signal is set to '1' at t_3, and go to step 5. If the DP and DM are not short, the VBUS detection completes at t_4 and the VBUS_DET_END is set to '1'. Then the state machine will go to step 6 to find out the type of accessory based on the DM voltage.
5. The state machine checks if the ID pin is floating. If the ID pin is not floating at t_3, the PSTI circuit turns off SW1 and SW2 and the VBUS detection completes. The VBUS_DET_END is set to '1' and the state machine goes to step 6. If the ID pin is floating at t_3, the PSTI circuit turns off SW1 and SW2 and then turns on SW3 and SW4 to force V_{DAT_SRC} to the DM pin. If the DP pin is between the two thresholds V_{DAT_REF} and V_{CR_REF} for 20 ms continuously before t_6, it means that the DP and DM pins are reverse short, then the DP/DM_reverse_short is set to '1' at t_5, and the SW3 and SW4 are turned off, VBUS_DET_END is set to '1', and the state machine goes to step 6. If the DP and DM are not reverse short, the VBUS detection completes at t_6, SW3 and SW4 are turned off, the VBUS_DET_END is set to '1', and the state machine goes to step 6.
6. The state machine will make a decision of the attached accessory based on the ID identification and the VBUS identification results.

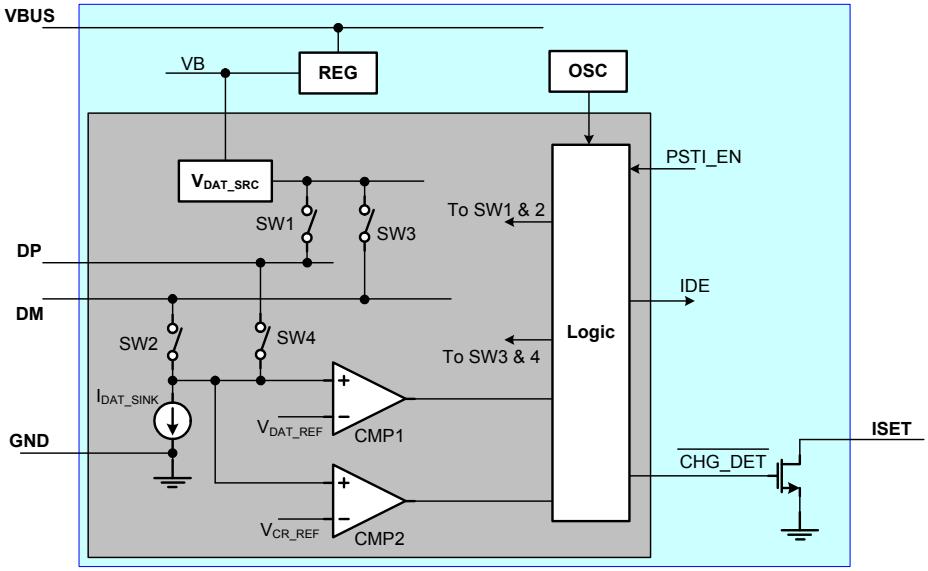


Figure 16. Power Supply Type Identification Circuit Block Diagram

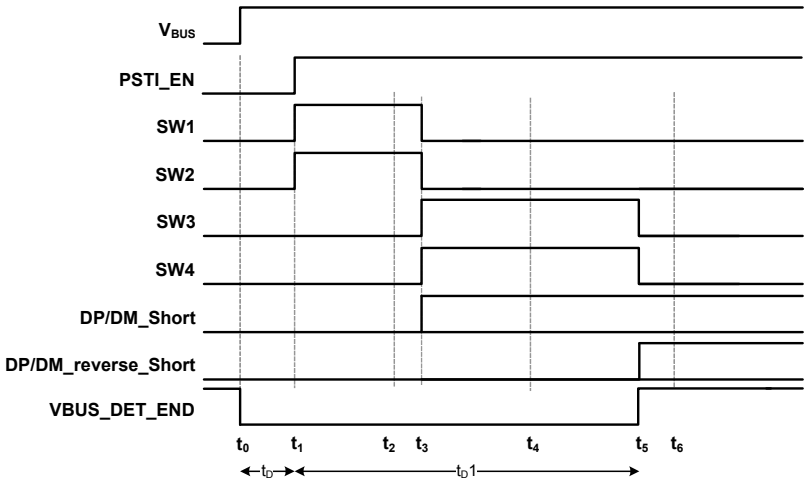


Figure 17. Operating Waveforms for the PSTI Circuit

OPERATION AFTER IDENTIFICATION

The identification process is started when VDD is above POR and the accessory attachment is detected. After the identification process is finished, the operation of the 34827 is determined together by the type of accessory, that is JIG cable or non-JIG cable, the status of power supplies, including the VBUS, VDD and VDDIO, and the Control register values.

If VBUS is powered up and VDD and VDDIO are low, the identification flow is not started. The 34827 is in the VBUS Power mode. The power MOSFET is on and ISET outputs high impedance. The JIG pin outputs high impedance, and the BOOT pin outputs logic low voltage for all accessories.

When VDD increases above POR but VDDIO is still low, the identification flow is started. But the interrupt mask control bit INT_MASK in Control register is in reset state (‘1’) to mask all interrupt outputs. All signal switches are off no matter what type of accessory is attached. This condition happens when the cell phone is not powered up yet. In this condition, if the accessory is found to be a JIG cable, the JIG pin outputs low impedance to enable the PMIC in the cell phone. Then VDDIO rises. Once the VDDIO rises to high, the BOOT pin will output the correct logic voltage and the UART or the USB switches will be turned on according to the type of JIG cable.

When the VDDIO is started up, the INT_MASK bit is still in reset state ‘1’, and the INTB output stays low. If the accessory is not a JIG cable, when the VDD and VDDIO are both powered up, the signal switches remains off until the INT_MASK is written to ‘0’ by I^2C.

The behaviors of INTB and signal switches during such transition and other important control functions are described below in detail.

CONTROL FUNCTIONS

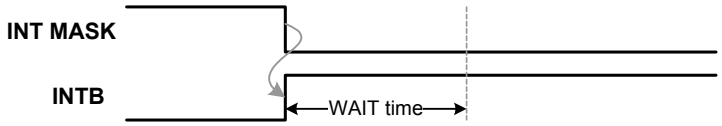
The 34827 contains registers which hold control and status information. The register map and the description of each register can be found in Register Map section. The details about some important control bits are described as follows.

INTERRUPT MASK (INT_MASK)

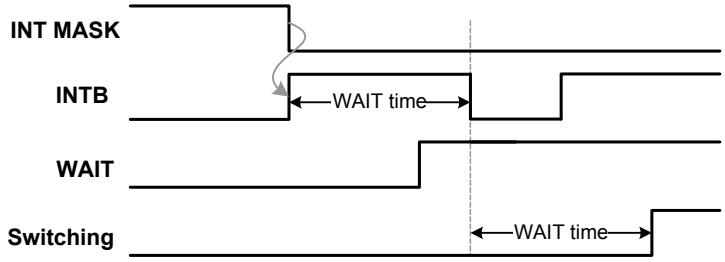
The INT_MASK bit masks all interrupt outputs to the host. When the INT_MASK bit is ‘1’, the INTB output is forced to low, and the corresponding interrupt bit can be still set when an interrupt event happens, but the host should not read the interrupt registers when INT_MASK = 1. When INT_MASK bit is set to ‘0’, the INTB output is allowed to send an interrupt, if any, to the host after a delay as shown in Figure 18. The delay is a WAIT time programmed by the Switching Wait bits in Timing Set 2 register. During the delay time, the INTB outputs a high voltage, and the host is not allowed to read the interrupt registers.

Figure 18 illustrates the switching behavior when the INT_MASK is set to ‘0’. Figure (A) shows the case that no interrupt bit is already set. In this case, the INTB outputs high when INT_MASK bit is set to zero. Figure (B) shows the case that an interrupt bit is already set due to attachment of an accessory and WAIT = 1 when the first delay time expires. In this case, INTB outputs high voltage during the first delay time and then outputs low voltage when the delay time expires. Once the INTB outputs low voltage after the delay time, the 34827 waits for a second WAIT time before turning on the signal switches. The baseband should read the interrupt registers via the I^2C, and since all the interrupt bits are of R/C type, the interrupt bits will be cleared after being read and then the INTB output returns to high. Figure (C)

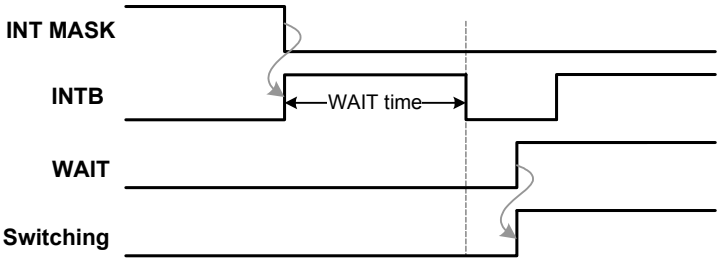
shows the case that an interrupt bit is already set due to attachment of an accessory and WAIT = 0 when the first delay time expires. In this case, INTB outputs high voltage in the first delay time and then outputs low voltage after the first delay time expires. The signal switches are not turned on until the WAIT bit is written to '1' by I^2C. When the baseband reads the interrupt registers via the I^2C, the interrupt bits are cleared and the INTB output returns to high.



(A). No accessory attached when the INT_MASK is reset to zero



(B). An accessory is already attached when the INT_MASK is reset to zero and WAIT bit = 1 when the first wait time expires.

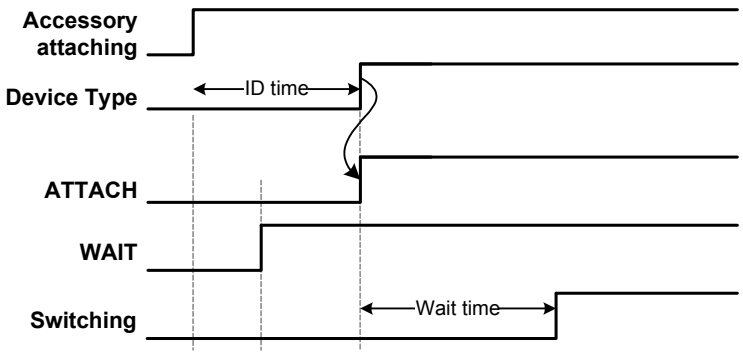


(C). An accessory is already attached when the INT_MASK is reset to zero and the WAIT bit = 0 when the first wait time expires.

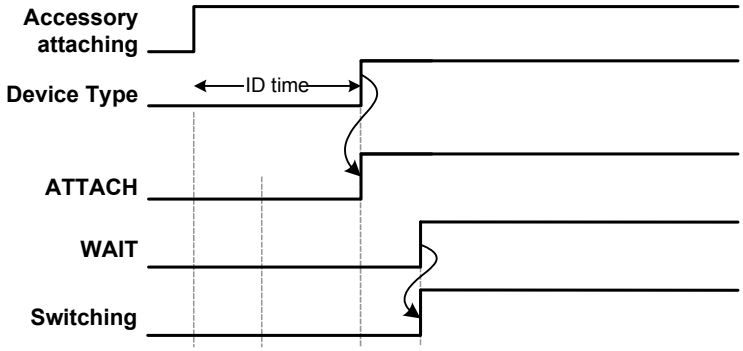
Figure 18. Operating Waveforms of the INT_MASK Bit

TIMING OF THE SWITCHING ACTION (WAIT BIT)

If the INT_MASK bit is already set to '0' before an accessory is attached, the INTB outputs low voltage once an interrupt bit is set and the following timing of the switching action is controlled by the WAIT bit in the Control register. If the WAIT bit is '1' when the Attach interrupt bit is set and INTB outputs low voltage, the 34827 waits for a WAIT time before turning on the switches. The WAIT time is programmed by the Switching Wait bits in the Timing Set 2 register. If the WAIT bit is '0' when the Attach interrupt is generated, the 34827 will not turn on the switches until the WAIT bit is set to '1' by I^2C. Both cases are shown in the Figure 19.



(A). WAIT = 1 when the ATTACH interrupt is generated. (VDDIO is high and INT_MASK = 1.)



(B). WAIT = 0 when the ATTACH interrupt is generated. (VDDIO is high and INT_MASK = 1.)

Figure 19. Operating Waveforms of the WAIT Bit

AUTOMATIC SWITCHING OR MANUAL SWITCHING (SWITCH_OPEN & MANUAL S/W BITS)

When a supported accessory is identified, the default behavior of 34827 is to automatically turn on the corresponding signal switches. The user can also choose to turn on optional signal switches manually. How to turn on the switches is controlled by the Manual S/W bit and the Switch_Open bits in the Control register.

If the Switch_Open bit is '0', all switches are off, including the power MOSFET.

If Manual S/W = 1, which is its reset value, the switches to be turned on and the outputs of ISET, JIG and BOOT pins are determined automatically by the Device Mode register, that is the identification result. If Manual S/W = 0, the switches to be turned on and the outputs of ISET, JIG and BOOT pins are determined by the values of the Manual S/W register. The relationship between the values of the Manual S/W register and the switches to be turned on can be found in Register Map section.

The values of Switch_Open and Manual S/W bits will not affect the identification flow and the timing of signal switching action of the 34827. The difference between Manual S/W = 1 and Manual S/W = 0 is what switches are turned on and what the ISET, JIG and BOOT pins output when an accessory is attached. In both way, no switches are turned on in Standby mode. If the Manual S/W bit is changed from '1' to '0' while an accessory is attached, the already automatically turned on switches will be turned off, the switches selected manually will be turned on, and the status of the ISET, JIG and BOOT pins will be determined by the corresponding bit value in the Manual S/W 2 register. However, writing Manual S/W bit back to '1' in Active mode will not change the switches status and the outputs.

RAW DATA (RAW DATA BIT)

The RAW DATA bit functions only when the accessory is Audio Type 1, which supports the remote control key. The RAW DATA bit determines whether to report the ID pin resistance change to the baseband when any key is pressed. When RAW DATA = 1, the ADC is enabled only when an ID line event is detected, such as when a key is pressed. In this case, the interrupt bits KP, LKP or LKR and the corresponding button bits in Button 1 and Button 2 registers will be set accordingly. Detailed behavior information when RAW DATA = 1 can be found in section Audio Device Type 1 -- Audio with or without the Remote Control. When RAW DATA = 0, the ADC is enabled periodically to calculate the ID line resistance. Any change of ADC Result will set the ADC_Change interrupt bit to inform the baseband. Then the baseband can read the ADC Result via I^2C. The KP, LKP or LKR and the button bits will not set when RAW DATA = 0.

The period of ADC conversion is determined by the Device Wake-up bits in the Timing Set 1 register. All other behaviors of Audio Type 1 and other accessories will not be affected by the RAW DATA bit.

POWER SAVE MODE (AUTOPSAVE BIT)

The 34827 supports the Power Save mode when the accessory is Audio Type 1 or TTY to reduce the power consumption. The default behavior of 34827 is to enter the Power Save mode automatically if no signal activity is detected within a programmable time which is controlled by the Activity Idle Detection Time bits in the Time Delay register. The default delay time is 10s. Once the signal activity is detected, the 34827 will quit the Power Save mode and enter the Active mode immediately. In the Power Save mode, the SPK_R/SPK_L to DP/DM switches and the VBUS to MIC switch all keep on. Remote control key pressing in Power Save mode can be responded as in the Active mode.

If the AutoPSAVE bit in FSL Control register is set to ‘0’, the 34827 will not enter Power Save mode automatically. Under this condition, the baseband can control the mode transition manually by writing the PSAVE bit when the accessory is Audio Type 1 or TTY. If the PSAVE is set to ‘0’, the 34827 keeps in Active mode; if the PSAVE is set to ‘1’, the 34827 keeps in Power Save mode even if the audio signal is applied at SPK_R and SPK_L pins.

If the Manual S/W is set to ‘0’ for Audio Type 1 or TTY, the 34827 has the same mode transition behavior as when the Manual S/W is in default value ‘1’.

NORMAL OPERATION SETTING OF THE CONTROL BITS

After the VDD and VDDIO are powered up, the 34827 is normally configured to turn on the switches automatically after the attached accessory is identified. Thus the INT_MASK bit must be set to ‘0’, the WAIT bit is normally set to ‘1’, the Manual S/W bit is set to ‘1’, the RAW Data bit is set to ‘1’ and the Switch_Open bit is set to ‘1’. This is the normal setting of these control bits for the normal operation.

ANALOG AND DIGITAL SWITCHES

The signal switches in the 34827 are shown in Figure 20.

These switches are controlled by the identification result when the Manual S/W = 1 and by the Manual S/W registers when the Manual S/W = 0 in Active mode. The Switch_Open bit overrides the switch configuration. When the Switch_Open bit is 0, all switches, including the power MOSFET, are turned off.

The switches for the SPK_L and SPK_R are capable of passing signals of ±1.5 V, referencing to GND pin voltage. The SPK_L and SPK_R pins are pulled down to ground via a 100 kΩ resistor respectively, as shown in Figure 20.

When the switches are configured automatically by the identification result, the configuration of the switches vs. the device type is shown in Table 7.

When detachment of an accessory is detected, the 34827 will return to the Standby mode. In the Standby mode, no matter Manual S/W = 1 or Manual S/W = 0, all signal switches and the power MOSFET are off in the Standby mode except for the OUT-to-ground FET SW10. The OUT-to-ground FET is turned on whenever the FET_ON bit is ‘0’. The ISET and JIG pins output high-impedance and BOOT pin outputs low logic voltage in the Standby mode