Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

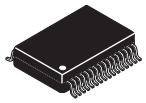
ɛscale Semiconductor
Technical Data

Document Number: MC34903_4_5
Rev. 4.0, 10/2013

System Basis Chip with CAN High Speed and LIN Interface

34903/4/5
Industrial

SYSTEM BASIS CHIP



EK Suffix (Pb-free)
98ASA10556D
32-PIN SOIC

The 34903/4/5 is the second generation family of the System Basis Chip (SBC). It combines several features and enhances present module designs. The device works as an advanced power management unit for the MCU with additional integrated circuits such as sensors and CAN transceivers. It has a built-in enhanced high-speed CAN interface (ISO11898-2 and -5) with local and bus failure diagnostics, protection, and fail-safe operation modes. The SBC may include zero or one LIN 2.1 interface with LIN output pin switches. It includes up to four wake-up input pins that can also be configured as output drivers for flexibility. This device is powered by SMARTMOS technology.

This device implements multiple Low-power (LP) modes, with very low-current consumption. In addition, the device is part of a family concept where pin compatibility adds versatility to module design.

The 34903/4/5 also implements an innovative and advanced fail-safe state machine and concept solution.

Features

- Voltage regulator for MCU, 5.0 or 3.3 V, part number selectable, with possibility of usage external PNP to extend current capability and share power dissipation
- Voltage, current, and temperature protection
- Extremely low quiescent current in LP modes
- Fully-protected embedded 5.0 V regulator for the CAN driver
- Multiple undervoltage detections to address various MCU specifications and system operation modes (i.e. cranking)
- Auxiliary 5.0 or 3.3 V SPI configurable regulator, for additional ICs, with overcurrent detection and undervoltage protection
- MUX output pin for device internal analog signal monitoring and power supply monitoring
- Advanced SPI, MCU, ECU power supply, and critical pins diagnostics and monitoring.
- Multiple wake-up sources in LP modes: CAN or LIN bus, I/O transition, automatic timer, SPI message, and V_{DD} overcurrent detection.
- ISO11898-5 high-speed CAN interface compatibility for baud rates of 40 kb/s to 1.0 Mb/s
- Scalable product family of devices ranging from 0 to 1 LIN, compatible to J2602-2 and LIN 2.1

Applications

- Industrial process control
- Automation
- Motor control
- Robotics

TABLE OF CONTENTS

SIMPLIFIED APPLICATION DIAGRAMS

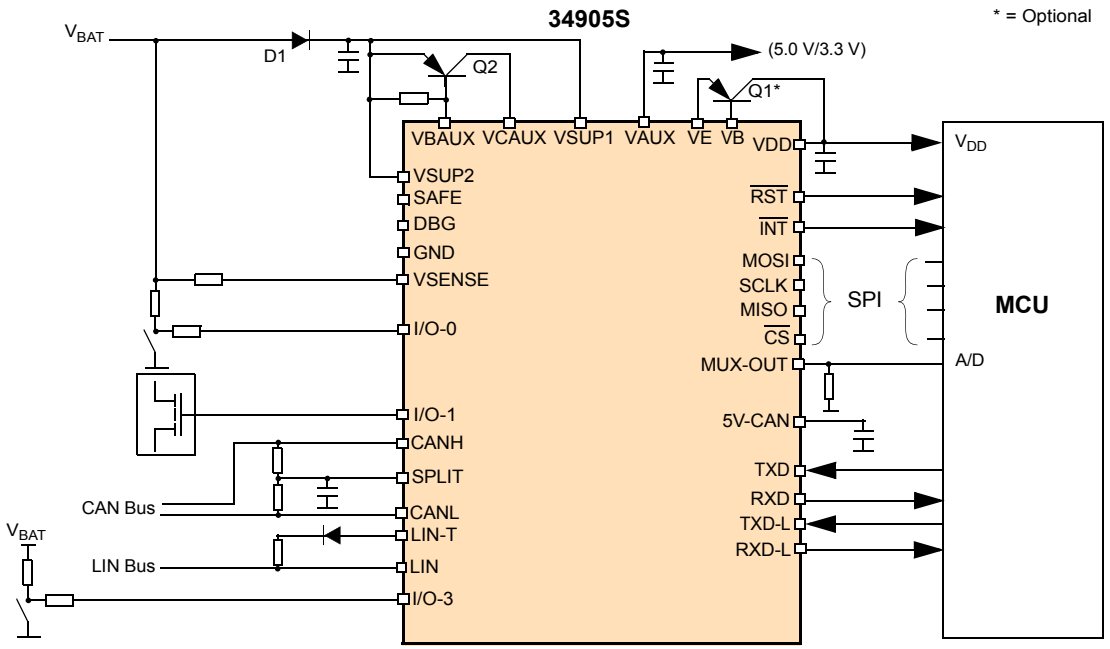


Figure 1. 34905S Simplified Application Diagram

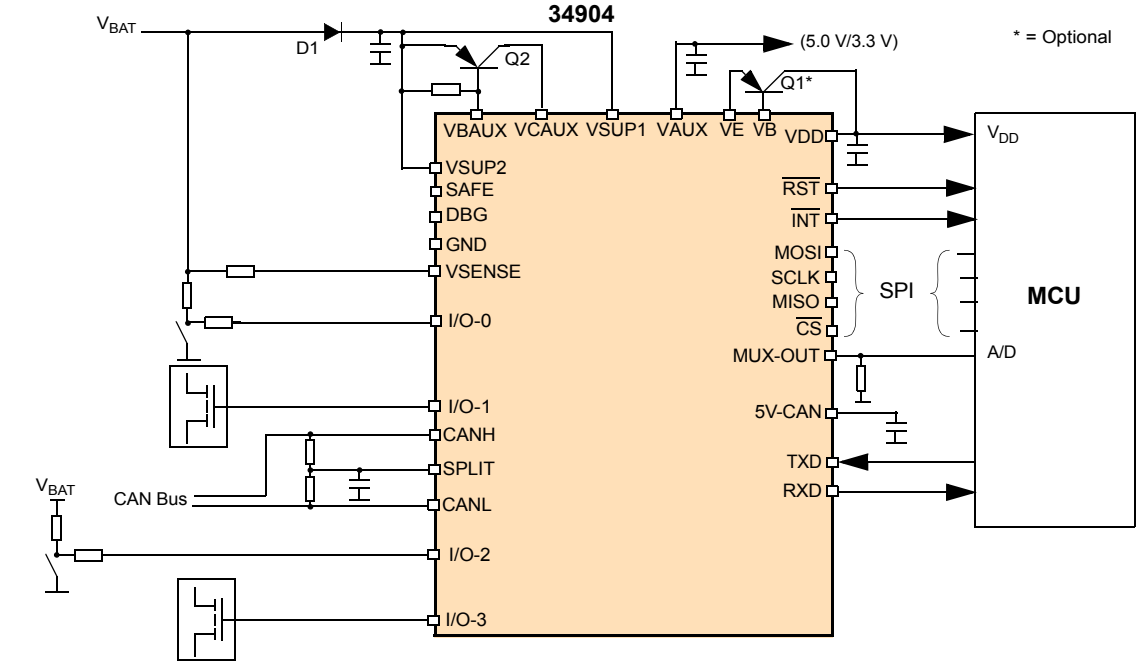


Figure 2. 34904 Simplified Application Diagram

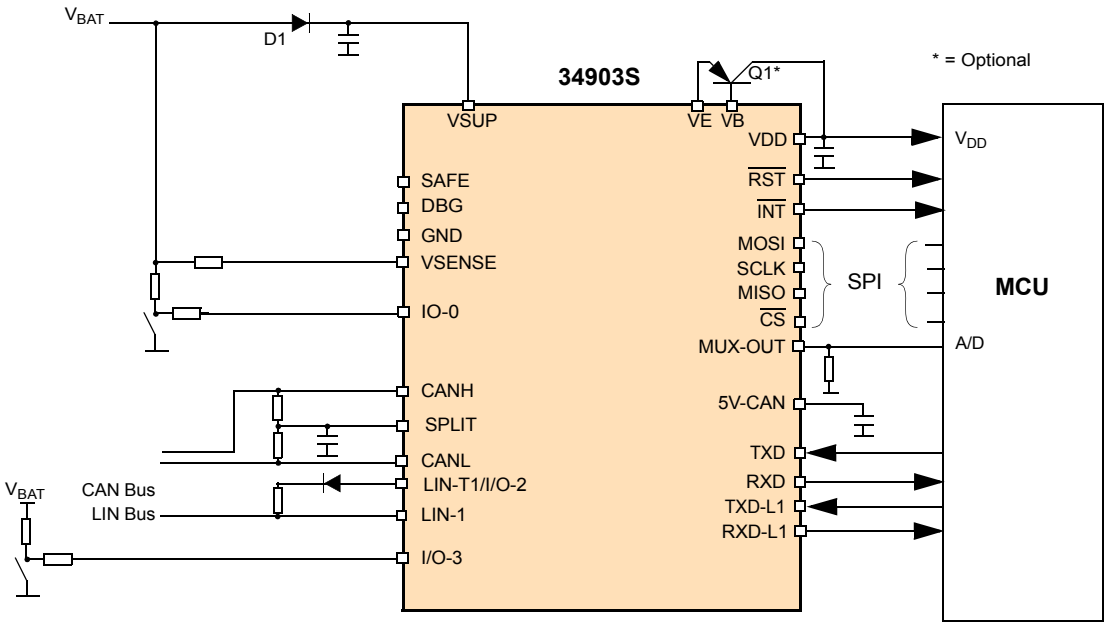


Figure 3. 34903S Simplified Application Diagram

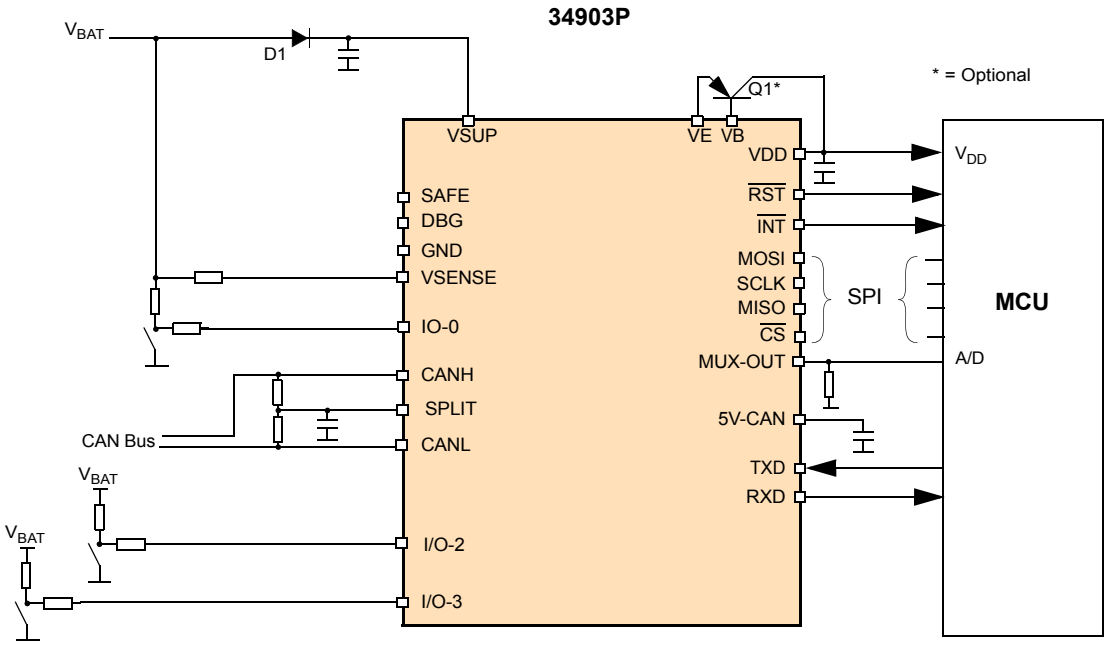


Figure 4. 34903P Simplified Application Diagram

DEVICE VARIATIONS

Table 1. MC34905 Device Variations - (All devices rated at T_A = -40 TO 125 °C)

Freescale Part Number	Version	V_{DD} Output Voltage	LIN Interface(s)	Wake-up Input / LIN Master Termination	Package	V_{AUX}	V_{SENSE}	MUX
MC34905S (Single LIN)								
MC34905CS3EK/R2	C	3.3 V	1	3 Wake-up + 1 LIN terms or 4 Wake-up + no LIN terms	SOIC 32 pin exposed pad	Yes	Yes	Yes
MC34905CS5EK/R2	C	5.0 V						

Table 2. MC34904 Device Variations - (All devices rated at T_A = -40 TO 125 °C)

Freescale Part Number	Version	V_{DD} Output Voltage	LIN Interface(s)	Wake-up Input / LIN Master Termination	Package	V_{AUX}	V_{SENSE}	MUX
MC34904								
MC34904C3EK/R2	C	3.3 V	0	4 Wake-up	SOIC 32 pin exposed pad	Yes	Yes	Yes
MC34904C5EK/R2	C	5.0 V						

Table 3. MC34903 Device Variations - (All devices rated at T_A = -40 TO 125 °C)

Freescale Part Number	Version	V_{DD} Output Voltage	LIN Interface(s)	Wake-up Input / LIN Master Termination	Package	V_{AUX}	V_{SENSE}	MUX
MC34903S (Single LIN)								
MC34903CS3EK/R2	C	3.3 V	1	2 Wake-up + 1 LIN terms or 3 Wake-up + no LIN terms	SOIC 32 pin exposed pad	No	Yes	Yes
MC34903CS5EK/R2	C	5.0 V						
MC34903P								
MC34903CP5EK/R2	C	5.0 V	0	3 Wake-up	SOIC 32 pin exposed pad	No	Yes	Yes
MC34903CP3EK/R2		3.3 V						

INTERNAL BLOCK DIAGRAMS

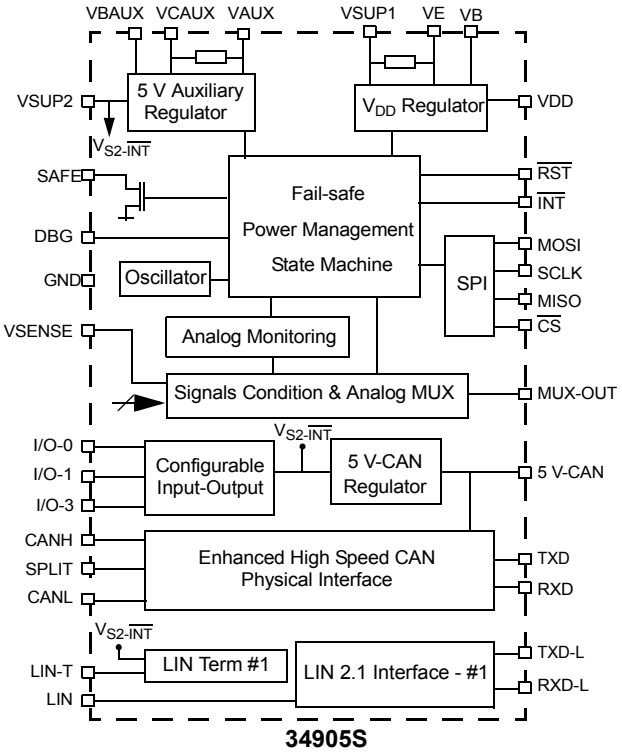


Figure 5. 34905 Internal Block Diagram

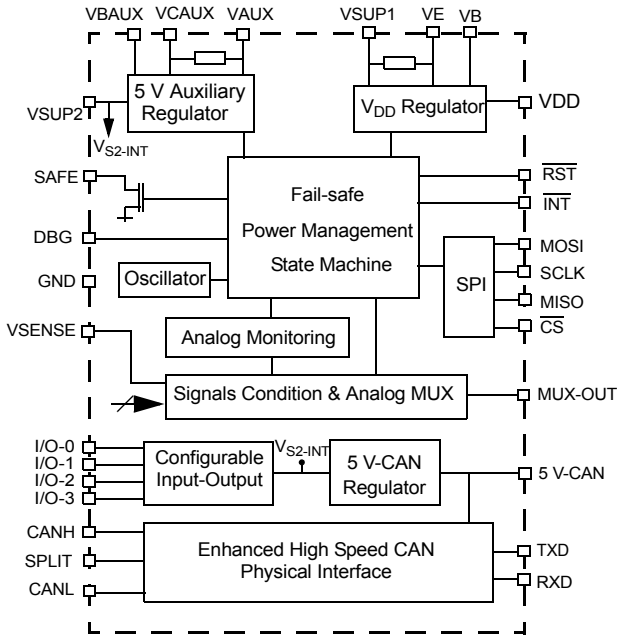


Figure 6. 34904 Internal Block Diagram

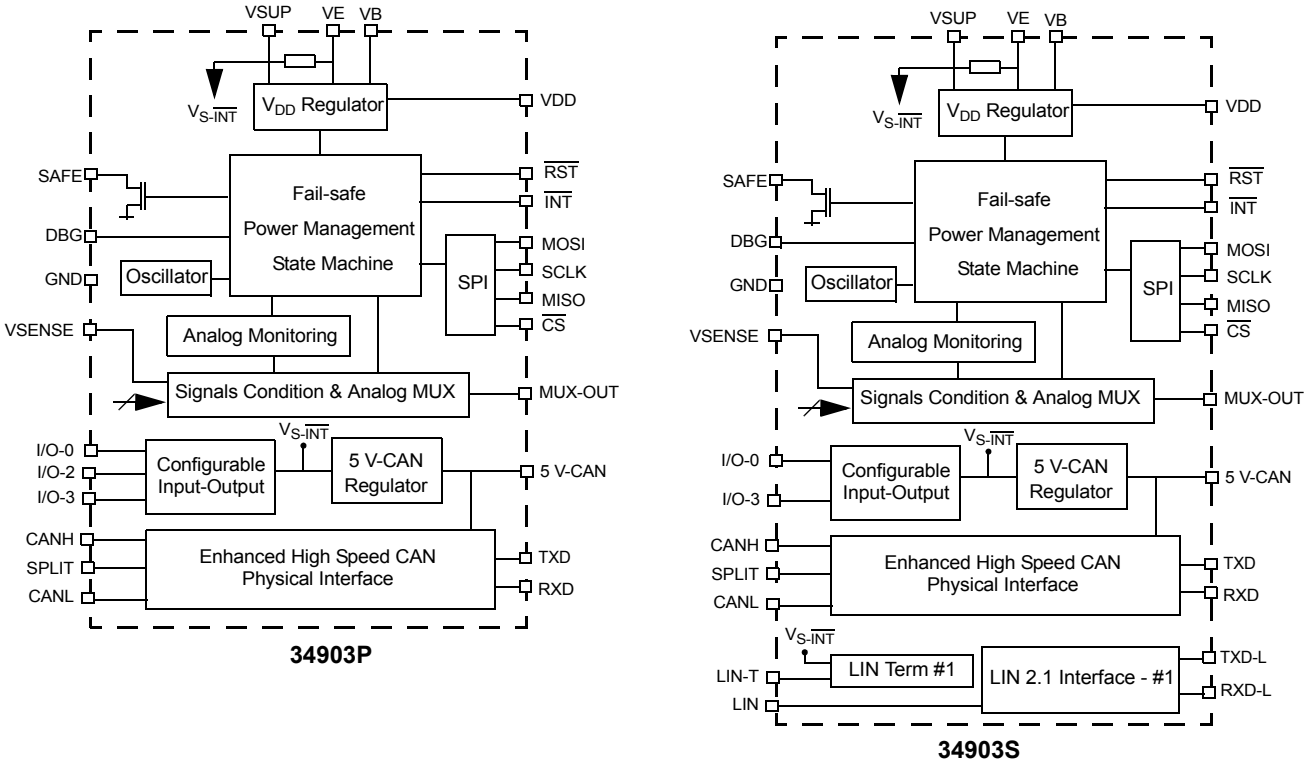
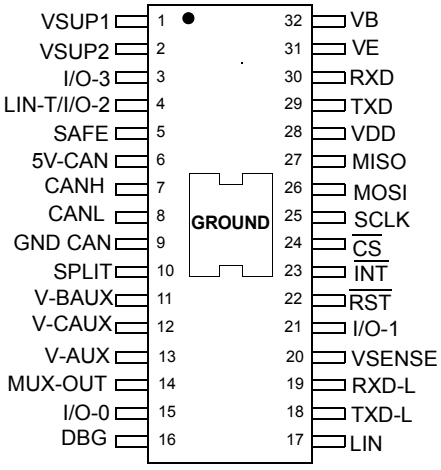


Figure 7. 34903 Internal Block Diagram

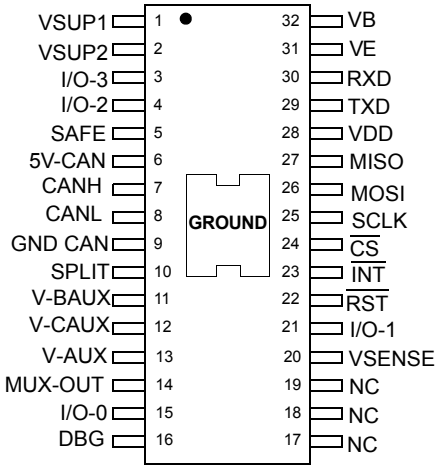
PIN CONNECTIONS

MC34905S



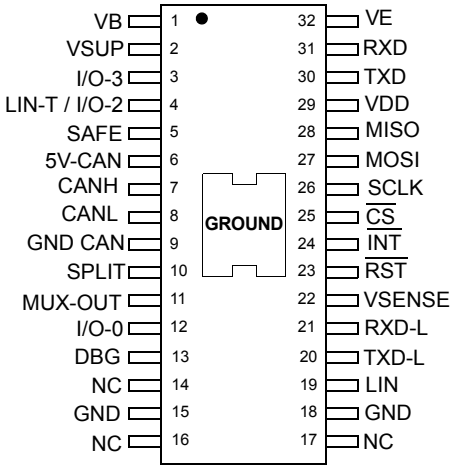
GND - LEAD FRAME
32 pin exposed package

MC34904



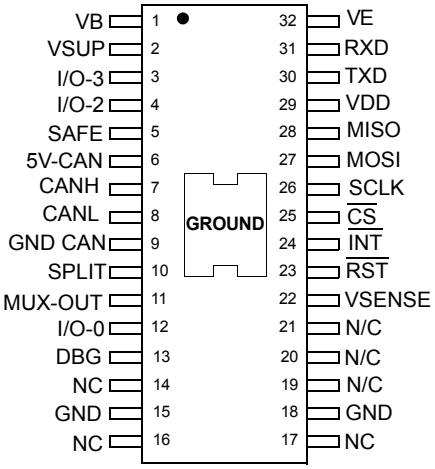
GND - LEAD FRAME
32 pin exposed package

MC34903S



GND - LEAD FRAME
32 pin exposed package

MC34903P



GND - LEAD FRAME
32 pin exposed package

Note: MC34905D, MC34905S, MC34904 and MC34903 are footprint compatible,

Figure 8. MC34905S, MC34904 and MC34903 Pin Connections

PIN DEFINITIONS

A functional description of each pin can be found in the Functional Pin Description section beginning on page 31.

Table 4. 34903/4/5 Pin Definitions

32 Pin 34905S	32 Pin 34904	32 Pin 34903S	32 Pin 34903P	Pin Name	Pin Function	Formal Name	Definition
N/A	17, 18, 19	N/A	N/A	N/C	No Connect	-	Connect to GND.
N/A	N/A	14, 16, 17	14, 16, 17, 19-21	N/C	No Connect		**Do NOT connect the N/C pins to GND. Leave these pins Open**.
1	1	2	2	VSUP/1	Power	Battery Voltage Supply 1	Supply input for the device internal supplies, power on reset circuitry and the V_{DD} regulator. VSUP and VSUP1 supplies are internally connected on part number MC34903BDEK and MC34903BSEK
2	2	N/A	N/A	VSUP2	Power	Battery Voltage Supply 2	Supply input for 5 V-CAN regulator, V_{AUX} regulator, I/O and LIN pins. VSUP1 and VSUP2 supplies are internally connected on part number MC34903BDEK and MC34903BSEK
3	3	3	3	I/O-3	Output or Input/ Output	LIN Termination 2 or Input/Output 3	Configurable pin as an input or HS output, for connection to external circuitry (switched or small load). The input can be used as a programmable Wake-up input in (LP) mode. When used as a HS, no overtemperature protection is implemented. A basic short to GND protection function, based on switch drain-source overvoltage detection, is available.
4	4	4	4	LIN-T1 or LIN-T or I/O-2	Output or Input/ Output	LIN Termination 1 or Input/Output 2	Configurable pin as an input or HS output, for connection to external circuitry (switched or small load). The input can be used as a programmable Wake-up input in (LP) mode. When used as a HS, no overtemperature protection is implemented. A basic short to GND protection function, based on switch drain-source overvoltage detection, is available.
5	5	5	5	SAFE	Output	Safe Output (Active LOW)	Output of the safe circuitry. The pin is asserted LOW if a fault event occurs (e.g.: software watchdog is not triggered, V_{DD} low, issue on the $\overline{RST}$ pin, etc.). Open drain structure.
6	6	6	6	5 V-CAN	Output	5V-CAN	Output voltage for the embedded CAN interface. A capacitor must be connected to this pin.
7	7	7	7	CANH	Output	CAN High	CAN high output.
8	8	8	8	CANL	Output	CAN Low	CAN low output.
9	9	9	9	GND-CAN	Ground	GND-CAN	Power GND of the embedded CAN interface
10	10	10	10	SPLIT	Output	SPLIT Output	Output pin for connection to the middle point of the split CAN termination
11	11	N/A	N/A	VBAUX	Output	VB Auxiliary	Output pin for external path PNP transistor base
12	12	N/A	N/A	VCAUX	Output	VCOLLECT OR Auxiliary	Output pin for external path PNP transistor collector
13	13	N/A	N/A	VAUX	Output	VOUT Auxiliary	Output pin for the auxiliary voltage.
14	14	11	11	MUX-OUT	Output	Multiplex Output	Multiplexed output to be connected to an MCU A/D input. Selection of the analog parameter available at MUX-OUT is done via the SPI. A switchable internal pull-down resistor is integrated for V_{DD} current sense measurements.

Table 4. 34903/4/5 Pin Definitions (continued)

32 Pin 34905S	32 Pin 34904	32 Pin 34903S	32 Pin 34903P	Pin Name	Pin Function	Formal Name	Definition
15	15	12	12	I/O-0	Input/ Output	Input/Output 0	Configurable pin as an input or output, for connection to external circuitry (switched or small load). The voltage level can be read by the SPI and via the MUX output pin. The input can be used as a programmable Wake-up input in LP mode. In LP, when used as an output, the High Side (HS) or Low Side (LS) can be activated for a cyclic sense function.
16	16	13	13	DBG	Input	Debug	Input to activate the Debug mode. In Debug mode, no watchdog refresh is necessary. Outside of Debug mode, connection of a resistor between DBG and GND allows the selection of Safe mode functionality.
N/A	N/A	15, 18	15, 18	GND	Ground	Ground	Ground of the IC.
17	N/A	19	N/A	LIN	Input/ Output	LIN bus	LIN bus input output connected to the LIN bus.
18	N/A	20	N/A	TXD-L	Input	LIN Transmit Data	LIN bus transmit data input. Includes an internal pull-up resistor to VDD.
19	N/A	21	N/A	RXD-L	Output	LIN Receive Data	LIN bus receive data output.
20	20	22	22	VSENSE	Input	Sense input	Direct battery voltage input sense. A serial resistor is required to limit the input current during high voltage transients.
21	21	N/A	N/A	I/O-1	Input/ Output	Input Output 1	Configurable pin as an input or output, for connection to external circuitry (switched or small load). The voltage level can be read by the SPI and the MUX output pin. The input can be used as a programmable Wake-up input in (LP) mode. It can be used in association with I/O-0 for a cyclic sense function in (LP) mode.
22	22	23	23	$\overline{RST}$	Output	Reset Output (Active LOW)	This is the device reset output whose main function is to reset the MCU. This pin has an internal pull-up to VDD. The reset input voltage is also monitored in order to detect external reset and safe conditions.
23	23	24	24	$\overline{INT}$	Output	Interrupt Output (Active LOW)	This output is asserted low when an enabled interrupt condition occurs. This pin is an open drain structure with an internal pull up resistor to VDD.
24	24	25	25	$\overline{CS}$	Input	Chip Select (Active LOW)	Chip select pin for the SPI. When the $\overline{CS}$ is low, the device is selected. In (LP) mode with V_{DD} ON, a transition on $\overline{CS}$ is a Wake-up condition
25	25	26	26	SCLK	Input	Serial Data Clock	Clock input for the Serial Peripheral Interface (SPI) of the device
26	26	27	27	MOSI	Input	Master Out/ Slave In	SPI data received by the device
27	27	28	28	MISO	Output	Master In/ Slave Out	SPI data sent to the MCU. When the $\overline{CS}$ is high, MISO is high-impedance
28	28	29	29	VDD	Output	Voltage Digital Drain	5.0 or 3.3 V output pin of the main regulator for the Microcontroller supply.
29	29	30	30	TXD	Input	Transmit Data	CAN bus transmit data input. Internal pull-up to VDD
30	30	31	31	RXD	Output	Receive Data	CAN bus receive data output
31	31	32	32	VE		Voltage Emitter	Connection to the external PNP path transistor. This is an intermediate current supply source for the V_{DD} regulator

Table 4. 34903/4/5 Pin Definitions (continued)

32 Pin 34905S	32 Pin 34904	32 Pin 34903S	32 Pin 34903P	Pin Name	Pin Function	Formal Name	Definition
32	32	1	1	VB	Output	Voltage Base	Base output pin for connection to the external PNP pass transistor
EX PAD	EX PAD	EX PAD	EX PAD	GND	Ground	Ground	Ground

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 5. Maximum Ratings

All voltages are referenced to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS[1]			
Supply Voltage at VSUP/1 and VSUP2 Normal Operation (DC) Transient Conditions (Load Dump)	 $V_{SUP1/2}$ $V_{SUP1/2TR}$	 -0.3 to 28 -0.3 to 40	V
DC voltage on LIN/1 Normal Operation (DC) Transient Conditions (Load Dump)	 V_{BUSLIN} $V_{BUSLINTR}$	 -28 to 28 -28 to 40	V
DC voltage on CANL, CANH, SPLIT Normal Operation (DC) Transient Conditions (Load Dump)	 V_{BUS} V_{BUSTR}	 -28 to 28 -32 to 40	V
DC Voltage at SAFE Normal Operation (DC) Transient Conditions (Load Dump)	 V_{SAFE} V_{SAFETR}	 -0.3 to 28 -0.3 to 40	V
DC Voltage at I/O-0, I/O-1, I/O-2, I/O-3 (LIN-T Pins) Normal Operation (DC) Transient Conditions (Load Dump)	 $V_{I/O}$ $V_{I/OTR}$	 -0.3 to 28 -0.3 to 40	V
DC voltage on TXD-L, TXD-L1, RXD-L, RXD-L1	V_{DIGLIN}	-0.3 to V_{DD} +0.3	V
DC voltage on TXD, RXD[3]	V_{DIG}	-0.3 to V_{DD} +0.3	V
DC Voltage at $\overline{INT}$	$V_{\overline{INT}}$	-0.3 to 10	V
DC Voltage at $\overline{RST}$	$V_{\overline{RST}}$	-0.3 to V_{DD} +0.3	V
DC Voltage at MOSI, MSIO, SCLK and $\overline{CS}$	$V_{\overline{RST}}$	-0.3 to V_{DD} +0.3	V
DC Voltage at MUX-OUT	V_{MUX}	-0.3 to V_{DD} +0.3	V
DC Voltage at DBG	V_{DBG}	-0.3 to 10	V
Continuous current on CANH and CANL	ILH	200	mA
DC voltage at VDD, 5V-CAN, VAUX, VCAUX	V_{REG}	-0.3 to 5.5	V
DC voltage at VBASE[2] and VBAUX	V_{REG}	-0.3 to 40	V
DC voltage at VE[3]	VE	-0.3 to 40	V
DC voltage at VSENSE	V_{SENSE}	-28 to 40	V

Notes

1. The voltage on non-VSUP pins should never exceed the V_{SUP} voltage at any time or permanent damage to the device may occur.
2. If the voltage delta between VSUP/1/2 and VBASE is greater than 6.0 V, the external V_{DD} ballast current sharing functionality may be damaged.
3. Potential Electrical Over Stress (EOS) damage may occur if RXD is in contact with VE while the device is ON.

Table 5. Maximum Ratings *(continued)*

All voltages are referenced to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ESD Capability			V
AECQ100[4]			
Human Body Model - JESD22/A114 (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω)			
CANH and CANL. LIN1 Pins versus all GND pins	V_{ESD1-1}	±8000	
all other Pins including CANH and CANL	V_{ESD1-2}	±2000	
Charge Device Model - JESD22/C101 (C_{ZAP} = 4.0 pF)			
Corner Pins (Pins 1, 16, 17, and 32)	V_{ESD2-1}	±750	
All other Pins (Pins 2-15, 18-31)	V_{ESD2-2}	±500	
Tested per IEC 61000-4-2 (C_{ZAP} = 150 pF, R_{ZAP} = 330 Ω)			
Device unpowered, CANH and CANL pin without capacitor, versus GND	V_{ESD3-1}	±15000	
Device unpowered, LIN, LIN1 pin, versus GND	V_{ESD3-2}	±15000	
Device unpowered, VS1/VS2 (100 nF to GND), versus GND	V_{ESD3-3}	±15000	
Tested per specific OEM EMC requirements for CAN and LIN with additional capacitor on VSUP/1/2 pins (See Typical Applications on page 85)			
CANH, CANL without bus filter	V_{ESD4-1}	±9000	
LIN, LIN1 with and without bus filter	V_{ESD4-2}	±12000	
I/O with external components (22 k - 10 nF)	V_{ESD4-3}	±7000	
THERMAL RATINGS			
Junction temperature[5]	T_J	150	°C
Ambient temperature	T_A	-40 to 125	°C
Storage temperature	T_{ST}	-50 to 150	°C
THERMAL RESISTANCE			
Thermal resistance junction to ambient[8]	$R_{\theta JA}$	50[8]	°C/W
Peak package reflow temperature during reflow[6], [7]	T_{PPRT}	Note 7	°C

Notes

4. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Charge Device Model (CDM), and Robotic (C_{ZAP} = 4.0 pF).
5. To achieve high reliability over 10 years of continuous operation, the device's continuous operating junction temperature should not exceed 125 °C.
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
7. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC34xxxD enter 34xxx), and review parametrics.
8. This parameter was measured according to Figure 9:

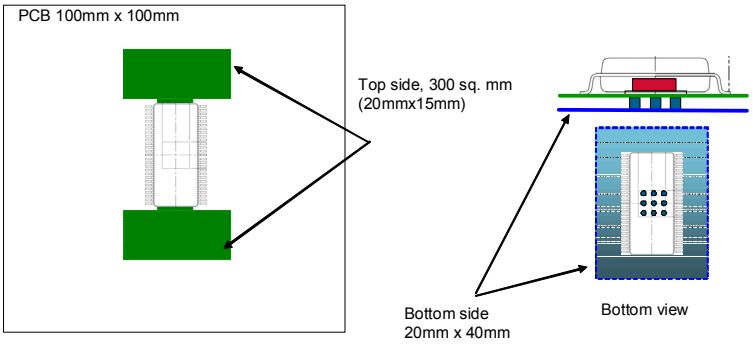


Figure 9. PCB with Top and Bottom Layer Dissipation Area (Dual Layer)

STATIC ELECTRICAL CHARACTERISTICS

Table 6. Static Electrical Characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Nominal DC Voltage Range[9]	V_{SUP1}/V_{SUP2}	5.5	-	28	V
Extended DC Low Voltage Range[10]	V_{SUP1}/V_{SUP2}	4.0	-	5.5	V
Undervoltage Detector Thresholds, at the VSUP/1 pin, Low threshold (VSUP/1 ramp down) High threshold (VSUP/1 ramp up) Hysteresis Note: function not active in LP mode	V_{S1_LOW}	 5.5 - 0.2	 6.0 - 0.35	 6.5 6.6 0.5	V
Undervoltage Detector Thresholds, at the VSUP2 pin: Low threshold (VSUP2 ramp down) High threshold (VSUP2 ramp up) Hysteresis Note: function not active in LP modes	V_{S2_LOW}	 5.5 - 0.2	 6.0 - 0.35	 6.5 6.6 0.5	V
V_{SUP} Overvoltage Detector Thresholds, at the VSUP/1 pin: Not active in LP modes	V_{S_HIGH}	16.5	17	18.5	V
Battery loss detection threshold, at the VSUP/1 pin.	BATFAIL	2.0	2.8	4.0	V
VSUP/1 to turn V_{DD} ON, VSUP/1 rising	$V_{SUP-TH1}$	-	4.1	4.5	V
VSUP/1 to turn V_{DD} ON, hysteresis (Guaranteed by design)	$V_{SUP-TH1HYST}$	150	180		mV
Supply current[11], [12] - from VSUP/1 - from VSUP2, (5V-CAN V_{AUX}, I/O OFF)	I_{SUP1}	 - -	 2.0 0.05	 4.0 0.85	mA
Supply current, I_{SUP1} + I_{SUP2}, Normal mode, V_{DD} ON - 5 V-CAN OFF, V_{AUX} OFF - 5 V-CAN ON, CAN interface in Sleep mode, V_{AUX} OFF - 5 V-CAN OFF, Vaux ON - 5 V-CAN ON, CAN interface in TXD/RXD mode, V_{AUX} OFF, I/O-x disabled	I_{SUP1+2}	 - - - -	 2.8 - - -	 4.5 5.0 5.5 8.0	mA
LP mode V_{DD} OFF. Wake-up from CAN, I/O-x inputs V_{SUP} ≤ 18 V, -40 to 25 °C V_{SUP} ≤ 18 V, 125 °C	I_{LPM_OFF}	 - -	 15 -	 35 50	µA
LP mode V_{DD} ON (5.0 V) with V_{DD} undervoltage and V_{DD} overcurrent monitoring, Wake-up from CAN, I/O-x inputs V_{SUP} ≤ 18 V, -40 to 25 °C, I_{DD} = 1.0 µA V_{SUP} ≤ 18 V, -40 to 25 °C, I_{DD} = 100 µA V_{SUP} ≤ 18 V, 125 °C, I_{DD} = 100 µA	I_{LPM_ON}	 - -	 20 40 -	 - 65 85	µA
LP mode, additional current for oscillator (used for: cyclic sense, forced Wake-up, and in LP V_{DD} ON mode cyclic interruption and watchdog) V_{SUP} ≤ 18 V, -40 to 125 °C	I_{OSC}	 -	 5.0	 9.0	µA
Debug mode DBG voltage range	V_{DBG}	8.0	-	10	V

Notes

9. All parameters in spec (ex: V_{DD} regulator tolerance).
10. Device functional, some parameters could be out of spec. V_{DD} is active, device is not in Reset mode if the lowest V_{DD} undervoltage reset threshold is selected (approx. 3.4 V). CAN and I/Os are not operational.
11. In Run mode, CAN interface in Sleep mode, 5 V-CAN and V_{AUX} turned OFF. I_{OUT} at V_{DD} < 50 mA. Ballast: turned OFF or not connected.
12. VSUP1 and VSUP2 supplies are internally connected on part number MC34903BDEK and MC34903BSEK. Therefore, I_{SUP1} and I_{SUP2} cannot be measured individually.

Table 6. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
V_{DD} VOLTAGE REGULATOR, VDD PIN					
Output Voltage					V
V_{DD} = 5.0 V, V_{SUP} 5.5 to 28 V, I_{OUT} 0 to 150 mA	$V_{OUT-5.0}$	4.9	5.0	5.1	
V_{DD} = 3.3 V, V_{SUP} 5.5 to 28 V, I_{OUT} 0 to 150 mA	$V_{OUT-3.3}$	3.234	3.3	3.4	
Drop voltage without external PNP pass transistor(13)	V_{DROP}				mV
V_{DD} = 5.0 V, I_{OUT} = 100 mA		-	330	450	
V_{DD} = 5.0 V, I_{OUT} = 150 mA		-	-	500	
Drop voltage with external transistor(13)	V_{DROP-B}				mV
I_{OUT} = 200 mA ($I\_{BALLAST}$ + $I\_{INTERNAL}$)		-	350	500	
VSUP/1 to maintain V_{DD} within $V_{OUT-3.3}$ specified voltage range	$V_{SUP1-3.3}$				V
V_{DD} = 3.3 V, I_{OUT} = 150 mA		4.0	-	-	
V_{DD} = 3.3 V, I_{OUT} = 200 mA, external transistor implemented		4.0	-	-	
External ballast versus internal current ratio ($I\_{BALLAST}$ = K x Internal current)	K	1.5	2.0	2.5	
Output Current limitation, without external transistor	I_{LIM}	150	350	550	mA
Temperature pre-warning (Guaranteed by design)	T_{PW}	-	140	-	°C
Thermal shutdown (Guaranteed by design)	T_{SD}	160	-	-	°C
Range of decoupling capacitor (Guaranteed by design)(14)	C_{EXT}	4.7	-	100	µF
LP mode V_{DD} ON, I_{OUT} ≤ 50 mA (time limited)	V_{DDLP}				V
V_{DD} = 5.0 V, 5.6 V ≤ V_{SUP} ≤ 28 V		4.75	5.0	5.25	
V_{DD} = 3.3 V, 5.6 V ≤ V_{SUP} ≤ 28 V		3.135	3.3	3.465	
LP mode V_{DD} ON, dynamic output current capability (Limited duration. Ref. to device description).	$L_{P-IOUTDC}$	-	-	50	mA
LP V_{DD} ON mode:	L_{P-ITH}				mA
Overcurrent Wake-up threshold.		1.0	3.0	-	
Hysteresis		0.1	1.0	-	
LP mode V_{DD} ON, drop voltage, at I_{OUT} = 30 mA (Limited duration. Ref. to device description) (13)	$L_{P-VDROP}$	-	200	400	mV
LP mode V_{DD} ON, min V_{SUP} operation (Below this value, a V_{DD}, undervoltage reset may occur)	$L_{P-MINVS}$	5.5	-	-	V
V_{DD} when V_{SUP} < $V_{SUP-TH1}$, at I_V_{DD} ≤ 10 µA (Guaranteed by design)	V_{DD_OFF}	-	-	0.3	V
V_{DD} when V_{SUP} ≥ $V_{SUP-TH1}$, at I_V_{DD} ≤ 40 mA (Guaranteed with parameter $V_{SUP-TH1}$	$V_{DD\_START\ UP}$	3.0	-	-	V

Notes

13. For 3.3 V V_{DD} devices, the drop-out voltage test condition leads to a V_{SUP} below the min V_{SUP} threshold (4.0 V). As a result, the dropout voltage parameter cannot be specified.
14. The regulator is stable without an external capacitor. Usage of an external capacitor is recommended for AC performance.

Table 6. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE REGULATOR FOR CAN INTERFACE SUPPLY, 5.0 V-CAN PIN					
Output voltage, $V_{SUP/2}$ = 5.5 to 40 V I_{OUT} 0 to 160 mA	$5V_{-C\ OUT}$	4.75	5.0	5.25	V
Output Current limitation (15)	$5V_{-C\ ILIM}$	160	280	-	mA
Undervoltage threshold	$5V_{-C\ UV}$	4.1	4.5	4.7	V
Thermal shutdown (Guaranteed by design)	$5V_{-CTS}$	160	-	-	°C
External capacitance (Guaranteed by design)	$C_{EXT-CAN}$	1.0	-	100	µF
V AUXILIARY OUTPUT, 5.0 AND 3.3 V SELECTABLE PIN VB-AUX, VC-AUX, VAUX					
VAUX output voltage V_{AUX} = 5.0 V, V_{SUP} = V_{SUP2} 5.5 to 40 V, I_{OUT} 0 to 150 mA V_{AUX} = 3.3 V, V_{SUP} = V_{SUP2} 5.5 to 40 V, I_{OUT} 0 to 150 mA	V_{AUX}	4.75 3.135	5.0 3.3	5.25 3.465	V
VAUX undervoltage detector (VAUX configured to 5.0 V) Low Threshold Hysteresis VAUX undervoltage detector (VAUX configured to 3.3 V, default value)	$V_{AUX-UVTH}$	4.2 0.06 2.75	4.5 - 3.0	4.70 0.12 3.135	V
VAUX overcurrent threshold detector V_{AUX} set to 3.3 V V_{AUX} set to 5.0 V	$V_{AUX-ILIM}$	250 230	360 330	450 430	mA
External capacitance (Guaranteed by design)	$V_{AUX\ CAP}$	2.2	-	100	µF
UNDERVOLTAGE RESET AND RESET FUNCTION, $\overline{RST}$ PIN					
V_{DD} undervoltage threshold down - 90% V_{DD} (V_{DD} 5.0 V)(16), (18) V_{DD} undervoltage threshold up - 90% V_{DD} (V_{DD} 5.0 V) V_{DD} undervoltage threshold down - 90% V_{DD} (V_{DD} 3.3 V)(16), (18) V_{DD} undervoltage threshold up - 90% V_{DD} (V_{DD} 3.3 V)	$V_{RST-TH1}$	4.5 - 2.75 -	4.65 - 3.0 -	4.85 4.90 3.135 3.135	V
V_{DD} undervoltage reset threshold down - 70% V_{DD} (V_{DD} 5.0 V)(17), (18)	$V_{RST-TH2-5}$	2.95	3.2	3.45	V
Hysteresis for threshold 90% V_{DD}, 5.0 V device for threshold 70% V_{DD}, 5.0 V device Hysteresis 3.3 V V_{DD} for threshold 90% V_{DD}, 3.3 V device	$V_{RST-HYST}$	20 10 10	- - -	150 150 150	mV
V_{DD} undervoltage reset threshold down - LP V_{DD} ON mode (Note: device change to Normal Request mode). V_{DD} 5.0 V (Note: device change to Normal Request mode). V_{DD} 3.3 V	V_{RST-LP}	4.0 2.75	4.5 3.0	4.85 3.135	V

Notes
15. Current limitation will be reported by setting a flag.
16. Generate a Reset or an $\overline{INT}$. SPI programmable
17. Generate a Reset
18. In Non-LP modes

Table 6. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
UNDERVOLTAGE RESET AND RESET FUNCTION, $\overline{RST}$ PIN (CONTINUED)					
Reset V_{OL} @ 1.5 mA, V_{SUP} 5.5 to 28 V	V_{OL}	-	300	500	mV
Current limitation, Reset activated, V_{RESET} = 0.9 x V_{DD}	$I_{RESET\ LOW}$	2.5	7.0	10	mA
Pull-up resistor (to VDD pin)	$R_{PULL-UP}$	8.0	11	15	kΩ
V_{SUP} to guaranteed reset low level(19)	$V_{SUP-RSTL}$	2.5	-	-	V
Reset input threshold	$V_{RST-VTH}$				V
Low threshold, V_{DD} = 5.0 V		1.5	1.9	2.2	
High threshold, V_{DD} = 5.0 V		2.5	3.0	3.5	
Low threshold, V_{DD} = 3.3 V		0.99	1.17	1.32	
High threshold, V_{DD} = 3.3 V		1.65	2.0	2.31	
Reset input hysteresis	V_{HYST}	0.5	1.0	1.5	V
I/O PINS WHEN FUNCTION SELECTED IS OUTPUT					
I/O-0 HS switch drop @ I = -12 mA, V_{SUP} = 10.5 V	$V_{I/O-0\ HSDRP}$	-	0.5	1.4	V
I/O-2 and I/O-3 HS switch drop @ I = -20 mA, V_{SUP} = 10.5 V	$V_{I/O-2-3\ HSDRP}$	-	0.5	1.4	V
I/O-1, HS switch drop @ I = -400 µA, V_{SUP} = 10.5 V	$V_{I/O-1\ HSDRP}$	-	0.4	1.4	V
I/O-0, I/O-1 LS switch drop @ I = 400 µA, V_{SUP} = 10.5 V	$V_{I/O-01\ LSDRP}$	-	0.4	1.4	V
Leakage current, I/O-x ≤ V_{SUP}	I_{I/O_LEAK}	-	0.1	3.0	µA
I/O PINS WHEN FUNCTION SELECTED IS INPUT					
Negative threshold	V_{I/O_NTH}	1.4	2.0	2.9	V
Positive threshold	V_{I/O_PTH}	2.1	3.0	3.8	V
Hysteresis	V_{I/O_HYST}	0.2	1.0	1.4	V
Input current, I/O ≤ VSUP/2	I_{I/O_IN}	-5.0	1.0	5.0	µA
I/O-0 and I/O-1 input resistor. I/O-0 (or I/O-1) selected in register, 2.0 V < $V_{I/O-X}$ <16 V (Guaranteed by design).	$R_{I/O-X}$	-	100	-	kΩ
VSENSE INPUT					
VSENSE undervoltage threshold (Not active in LP modes)	V_{SENSE_TH}				V
Low Threshold		8.1	8.6	9.0	
High threshold		-	-	9.1	
Hysteresis		0.1	0.25	0.5	
Input resistor to GND. In all modes except in LP modes. (Guaranteed by design).	R_{VSENSE}	-	125	-	kΩ

Notes

19. Reset must be kept low

Table 6. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
ANALOG MUX OUTPUT					
Output Voltage Range, with external resistor to GND >2.0 kΩ	V_{OUT_MAX}	0.0	-	V_{DD} - 0.5	V
Internal pull-down resistor for regulator output current sense	R_{MI}	0.8	1.9	2.8	kΩ
External capacitor at MUX OUTPUT[20] (Guaranteed by design)	C_{MUX}	-	-	1.0	nF
Chip temperature sensor coefficient (Guaranteed by design and device characterization)	$TEMP_{-COEFF}$				mv/°C
V_{DD} = 5.0 V		20	21	22	
V_{DD} = 3.3 V		13.2	13.9	14.6	
Chip temperature: MUX-OUT voltage	V_{TEMP}				V
V_{DD} = 5.0 V, T_A = 125 °C		3.6	3.75	3.9	
V_{DD} = 3.3 V, T_A = 125 °C		2.45	2.58	2.65	
Chip temperature: MUX-OUT voltage (guaranteed by design and characterization)	$V_{TEMP(GD)}$				V
T_A = -40 °C, V_{DD} = 5.0 V		0.12	0.30	0.48	
T_A = 25 °C, V_{DD} = 5.0 V		1.5	1.65	1.8	
T_A = -40 °C, V_{DD} = 3.3 V		0.07	0.19	0.3	
T_A = 25 °C, V_{DD} = 3.3 V		1.08	1.14	1.2	
Gain for V_{SENSE}, with external 1.0 k 1% resistor	V_{SENSE} GAIN				
V_{DD} = 5.0 V		5.42	5.48	5.54	
V_{DD} = 3.3 V		8.1	8.2	8.3	
Offset for V_{SENSE}, with external 1.0 k 1% resistor	V_{SENSE} OFFSET	-20	-	20	mV
Divider ratio for $V_{SUP/1}$	$V_{SUP/1}$ RATIO				
V_{DD} = 5.0 V		5.335	5.5	5.665	
V_{DD} = 3.3 V		7.95	8.18	8.45	
Attenuation/Gain ratio for I/O-0 and I/O-1 actual voltage:	VI/O RATIO				
V_{DD} = 5.0 V, I/O = 16 V (Attenuation, MUX-OUT register bit 3 set to 1)		3.8	4.0	4.2	
V_{DD} = 5.0 V, (Gain, MUX-OUT register bit 3 set to 0)		-	2.0	-	
V_{DD} = 3.3 V, I/O = 16 V (Attenuation, MUX-OUT register bit 3 set to 1)		5.6	5.8	6.2	
V_{DD} = 3.3 V, (Gain, MUX-OUT register bit 3 set to 0)		-	1.3	-	
Internal reference voltage	V_{REF}				V
V_{DD} = 5.0 V		2.45	2.5	2.55	
V_{DD} = 3.3 V		1.64	1.67	1.7	
Current ratio between VDD output & I_{OUT} at MUX-OUT (I_{OUT} at MUX-OUT = I_{DD} out / I_{DD_RATIO})	I_{DD_RATIO}				
At I_{OUT} = 50 mA		80	97	115	
$I_{\_OUT}$ from 25 to 150 mA		62.5	97	117	
SAFE OUTPUT					
SAFE low level, at I = 500 µA	V_{OL}	0.0	0.2	1.0	V
Safe leakage current (V_{DD} low, or device unpowered). V_{SAFE} 0 to 28 V.	$I_{SAFE-IN}$	-	0.0	1.0	µA

Notes

20. When C is higher than CMUX, a serial resistor must be inserted

Table 6. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INTERRUPT					
Output low voltage, I_{OUT} = 1.5 mA	V_{OL}	-	0.2	1.0	V
Pull-up resistor	R_{PU}	6.5	10	14	kΩ
Output high level in LP V_{DD} ON mode (Guaranteed by design)	$V_{OH-LPVDDON}$	3.9	4.3		V
Leakage current $\overline{INT}$ voltage = 10 V (to allow high-voltage on MCU $\overline{INT}$ pin)	V_{MAX}	-	35	100	µA
Sink current, $V_{\overline{INT}}$ > 5.0 V, $\overline{INT}$ low state	I_{SINK}	2.5	6.0	10	mA
MISO, MOSI, SCLK, $\overline{CS}$ PINS					
Output low voltage, I_{OUT} = 1.5 mA (MISO)	V_{OL}	-	-	1.0	V
Output high voltage, I_{OUT} = -0.25 mA (MISO)	V_{OH}	V_{DD} -0.9	-		V
Input low voltage (MOSI, SCLK,$\overline{CS}$)	V_{IL}	-	-	0.3 x V_{DD}	V
Input high voltage (MOSI, SCLK,$\overline{CS}$)	V_{IH}	0.7 x V_{DD}	-	-	V
Tri-state leakage current (MISO)	I_{HZ}	-2.0	-	2.0	µA
Pull-up current ($\overline{CS}$)	I_{PU}	200	370	500	µA
CAN LOGIC INPUT PINS (TXD)					
High Level Input Voltage	V_{IH}	0.7 x V_{DD}	-	V_{DD} + 0.3	V
Low Level Input Voltage	V_{IL}	-0.3	-	0.3 x V_{DD}	V
Pull-up Current, TXD, V_{IN} = 0 V V_{DD} =5.0 V V_{DD} =3.3 V	I_{PDWN}	 -850 -500	 -650 -250	 -200 -175	µA
CAN DATA OUTPUT PINS (RXD)					
Low Level Output Voltage I_{RXD} = 5.0 mA	$VOUT_{LOW}$	0.0	-	0.3 x V_{DD}	V
High Level Output Voltage I_{RX} = -3.0 mA	$VOUT_{HIGH}$	0.7 x V_{DD}	-	V_{DD}	V
High Level Output Current V_{RXD} = V_{DD} - 0.4 V	$IOUT_{HIGH}$	2.5	5.0	9.0	mA
Low Level Input Current V_{RXD} = 0.4 V	$IOUT_{LOW}$	2.5	5.0	9.0	mA

Table 6. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CAN OUTPUT PINS (CANH, CANL)					
Bus pins common mode voltage for full functionality	V_{COM}	-12	-	12	V
Differential input voltage threshold	$V_{CANH-VCANL}$	500	-	900	mV
Differential input hysteresis	$V_{DIFF-HYST}$	50	-	-	mV
Input resistance	R_{IN}	5.0	-	50	kΩ
Differential input resistance	$R_{IN-DIFF}$	10	-	100	kΩ
Input resistance matching	$R_{IN-MATCH}$	-3.0	0.0	3.0	%
CANH output voltage (45 Ω < R_{BUS} < 65 Ω)	V_{CANH}				V
TXD dominant state		2.75	3.5	4.5	
TXD recessive state		2.0	2.5	3.0	
CANL output voltage (45 Ω < R_{BUS} < 65 Ω)	V_{CANL}				V
TXD dominant state		0.5	1.5	2.25	
TXD recessive state		2.0	2.5	3.0	
Differential output voltage (45 Ω < R_{BUS} < 65 Ω)	V_{OH}-V_{OL}				V
TXD dominant state		1.5	2.0	3.0	
TXD recessive state		-0.5	0.0	0.05	
CAN H output current capability - Dominant state	I_{CANH}	-	-	-30	mA
CAN L output current capability - Dominant state	I_{CANL}	30	-	-	mA
CANL overcurrent detection - Error reported in register	$I_{CANL-OC}$	75	120	195	mA
CANH overcurrent detection - Error reported in register	$I_{CANH-OC}$	-195	-120	-75	mA
CANH, CANL input resistance to GND, device supplied, CAN in Sleep mode, V_CANH, V_CANL from 0 to 5.0 V	$R_{INSLEEP}$	5.0	-	50	kΩ
CANL, CANH output voltage in LP V_{DD} OFF and LP V_{DD} ON modes	V_{CANLP}	-0.1	0.0	0.1	V
CANH, CANL input current, VCANH, VCANL = 0 to 5.0 V, device unpowered (VSUP, VDD, 5V-CAN: open).[21]	I_{CAN-UN_SUP1}	-	3.0	10	µA
CANH, CANL input current, VCANH, VCANL = -2.0 to 7.0 V, device unpowered (VSUP, VDD, 5V-CAN: open).[21]	I_{CAN-UN_SUP2}	-	-	250	µA
Differential voltage for recessive bit detection in LP mode[22]	$V_{DIFF-R-LP}$	-	-	0.4	V
Differential voltage for dominant bit detection in LP mode[22]	$V_{DIFF-D-LP}$	1.15	-	-	V
CANH AND CANL DIAGNOSTIC INFORMATION					
CANL to GND detection threshold	V_{LG}	1.6	1.75	2.0	V
CANH to GND detection threshold	V_{HG}	1.6	1.75	2.0	V
CANL to VBAT detection threshold, $V_{SUP/1}$ and V_{SUP2} > 8.0 V	V_{LVB}	-	V_{SUP} -2.0	-	V
CANH to VBAT detection threshold, $V_{SUP/1}$ and V_{SUP2} > 8.0 V	V_{HVB}	-	V_{SUP} -2.0	-	V
CANL to VDD detection threshold	V_{L5}	4.0	V_{DD} -0.43	-	V
CANH to VDD detection threshold	V_{H5}	4.0	V_{DD} -0.43	-	V

Notes

21. VSUP, VDD, 5V-CAN: shorted to GND, or connected to GND via a 47 k resistor instances are guaranteed by design and device characterization.
22. Guaranteed by design and device characterization.

Table 6. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPLIT					
Output voltage Loaded condition I_{SPLIT} = ±500 µA Unloaded condition Rmeasure > 1.0 MΩ	V_{SPLIT}	 0.3 x V_{DD} 0.45 x V_{DD}	 0.5 x V_{DD} 0.5 x V_{DD}	 0.7 x V_{DD} 0.55 x V_{DD}	V
Leakage current -12 V < V_{SPLIT} < +12 V -22 to -12 V < V_{SPLIT} < +12 to +35 V	I_{LSPLIT}	 - -	 0.0 -	 5.0 200	µA
LIN TERMINALS (LIN-T/1)					
LIN-T1 HS switch drop @ I = -20 mA, V_{SUP} > 10.5 V	V_{LT_HSDRP}	-	1.0	1.4	V
LIN1 34903D/5D PIN - LIN 34903S/5S PIN (Parameters guaranteed for $V_{SUP/1}$, V_{SUP2} 7.0 V ≤ V_{SUP} ≤ 18 V)					
Operating Voltage Range	V_{BAT}	8.0	-	18	V
Supply Voltage Range	V_{SUP}	7.0	-	18	V
Current Limitation for Driver Dominant State Driver ON, V_{BUS} = 18 V	I_{BUS_LIM}	 40	 90	 200	mA
Input Leakage Current at the receiver Driver off; V_{BUS} = 0 V; V_{BAT} = 12 V	$I_{BUS\_PAS\_DOM}$	 -1.0	 -	 -	mA
Leakage Output Current to GND Driver Off; 8.0 V < V_{BAT} < 18 V; 8.0 V < V_{BUS} < 18 V; V_{BUS} ≥ V_{BAT}	$I_{BUS\_PAS\_REC}$	 -	 -	 20	µA
Control unit disconnected from ground (Loss of local ground must not affect communication in the residual network) GND_{DEVICE} = V_{SUP}; V_{BAT} = 12 V; 0 < V_{BUS} < 18 V (Guaranteed by design)	$I_{BUS\_NO\_GND}$	 -1.0	 -	 1.0	mA
V_{BAT} Disconnected; V_{SUP_DEVICE} = GND; 0 < V_{BUS} < 18 V (Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition). (Guaranteed by design)	I_{BUSNO_BAT}	 -	 -	 100	µA
Receiver Dominant State	V_{BUSDOM}	 -	 -	 0.4	V_{SUP}
Receiver Recessive State	V_{BUSREC}	 0.6	 -	 -	V_{SUP}
Receiver Threshold Center (V_{TH_DOM} + V_{TH_REC})/2	V_{BUS_CNT}	 0.475	 0.5	 0.525	V_{SUP}
Receiver Threshold Hysteresis (V_{TH_REC} - V_{TH_DOM})	V_{HYS}	 -	 -	 0.175	V_{SUP}
LIN Wake-up threshold from LP V_{DD} ON or LP V_{DD} OFF mode	V_{BUSWU}	-	5.3	5.8	V
LIN Pull-up Resistor to V_{SUP}	R_{SLAVE}	20	30	60	kΩ
Overtemperature Shutdown (Guaranteed by design)	T_{LINSD}	140	160	180	°C
Overtemperature Shutdown Hysteresis (Guaranteed by design)	T_{LINSD_HYS}	-	10	-	°C

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 7. Dynamic Electrical Characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI TIMING					
SPI Operation Frequency (MISO cap = 50 pF)	FREQ	0.25	-	4.0	MHz
SCLK Clock Period	t_{PCLK}	250	-	N/A	ns
SCLK Clock High Time	t_{WSCLKH}	125	-	N/A	ns
SCLK Clock Low Time	t_{WSCLKL}	125	-	N/A	ns
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK "C" version All others	t_{LEAD}	 30 550	 - -	 N/A N/A	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$	t_{LAG}	30	-	N/A	ns
MOSI to Falling Edge of SCLK	t_{SISU}	30	-	N/A	ns
Falling Edge of SCLK to MOSI	t_{SIH}	30	-	N/A	ns
MISO Rise Time (CL = 50 pF)	t_{RSO}	-	-	30	ns
MISO Fall Time (CL = 50 pF)	t_{FSO}	-	-	30	ns
Time from Falling to MISO Low-impedance Time from Rising to MISO High-impedance	t_{SOEN} t_{SODIS}	- -	- -	30 30	ns
Time from Rising Edge of SCLK to MISO Data Valid	t_{VALID}	-	-	30	ns
Delay between falling and rising edge on $\overline{CS}$ "C" version All others	$t_{\overline{CS}LOW}$	 1.0 5.5	 - -	 N/A N/A	µs
$\overline{CS}$ Chip Select Low Timeout Detection	$t_{\overline{CS}\text{-}TO}$	2.5	-	-	ms
SUPPLY, VOLTAGE REGULATOR, RESET					
V_{SUP} undervoltage detector threshold deglitcher	$t_{VS\_LOW1/2\_DGLT}$	30	50	100	µs
Rise time at turn ON. V_{DD} from 1.0 to 4.5 µV. 2.2 µF at the VDD pin.	$t_{RISE\text{-}ON}$	50	250	800	µs
Deglitcher time to set $\overline{RST}$ pin low	$t_{RST\text{-}DGLT}$	20	30	40	µs
RESET PULSE DURATION					
V_{DD} undervoltage (SPI selectable) short, default at power on when BATFAIL bit set medium medium long long	$t_{RST\text{-}PULSE}$	 0.9 4.0 8.5 17	 1.0 5.0 10 20	 1.4 6.5 12 24	ms
Watchdog reset	$t_{RST\text{-}WD}$	0.9	1.0	1.4	ms
I/O INPUT					
Deglitcher time (Guaranteed by design)	t_{IODT}	19	30	41	µs
VSENSE INPUT					
Undervoltage deglitcher time	t_{BFT}	30	-	100	µs

Table 7. Dynamic Electrical Characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INTERRUPT					
$\overline{INT}$ pulse duration (refer to SPI for selection. Guaranteed by design)	$t_{\overline{INT}\text{-PULSE}}$				µs
short (25 to 125 °C)		20	25	35	
short (-40 °C)		20	25	40	
long (25 to 125 °C)		90	100	130	
long (-40 °C)		90	100	140	
STATE DIGRAM TIMINGS					
Delay for SPI Timer A, Timer B or Timer C write command after entering Normal mode (No command should occur within t_{D_NM}. t_{D_NM} delay definition: from $\overline{CS}$ rising edge of "Go to Normal mode (i.e. 0x5A00)" command to $\overline{CS}$ falling edge of "Timer write" command)	t_{D_NM}	60	-	-	µs
Tolerance for: watchdog period in all modes, FWU delay, Cyclic sense period and active time, Cyclic Interrupt period, LP mode overcurrent (unless otherwise noted)[26]	$t_{TIMING\text{-}ACC}$	-10	-	10	%
CAN DYNAMIC CHARACTERISTICS					
TXD Dominant State Timeout	t_{DOUT}	300	600	1000	µs
Bus dominant clamping detection	t_{DOM}	300	600	1000	µs
Propagation loop delay TXD to RXD, recessive to dominant (Fast slew rate)	t_{LRD}	60	120	210	ns
Propagation delay TXD to CAN, recessive to dominant	t_{TRD}	-	70	110	ns
Propagation delay CAN to RXD, recessive to dominant	t_{RRD}	-	45	140	ns
Propagation loop delay TXD to RXD, dominant to recessive (Fast slew rate)	t_{LDR}	100	120	200	ns
Propagation delay TXD to CAN, dominant to recessive	t_{TDR}	-	75	150	ns
Propagation delay CAN to RXD, dominant to recessive	t_{RDR}	-	50	140	ns
Loop time TXD to RXD, Medium Slew Rate (Selected by SPI)	$t_{LOOP\text{-}MSL}$				ns
Recessive to Dominant		-	200	-	
Dominant to Recessive		-	200	-	
Loop time TXD to RXD, Slow Slew Rate (Selected by SPI)	$t_{LOOP\text{-}SSL}$				ns
Recessive to Dominant		-	300	-	
Dominant to Recessive		-	300	-	
CAN Wake-up filter time, single dominant pulse detection[23] (See Figure 31)	$t_{CAN\text{-}WU1\text{-}F}$	0.5	2.0	5.0	µs
CAN Wake-up filter time, 3 dominant pulses detection[24]	$t_{CAN\text{-}WU3\text{-}F}$	300	-	-	ns
CAN Wake-up filter time, 3 dominant pulses detection timeout[25] (See Figure 32)	$t_{CAN\text{-}WU3\text{-}TO}$	-	-	120	µs

Notes

23. No Wake-up for single pulse shorter than $t_{CAN\text{-}WU1}$ min. Wake-up for single pulse longer than $t_{CAN\text{-}WU1}$ max.
24. Each pulse should be greater than $t_{CAN\text{-}WU3\text{-}F}$ min. Guaranteed by design, and device characterization.
25. The 3 pulses should occur within $t_{CAN\text{-}WU3\text{-}TO}$. Guaranteed by design, and device characterization.
26. Guaranteed by design.

Table 7. Dynamic Electrical Characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR NORMAL SLEW RATE - 20.0 KBIT/SEC ACCORDING TO LIN PHYSICAL LAYER SPECIFICATION **BUS LOAD R_{BUS} AND C_{BUS} 1.0 NF / 1.0 KΩ, 6.8 NF / 660 Ω, 10 NF / 500 Ω. SEE Figure 14, PAGE 28.**					
Duty Cycle 1: $TH_{REC(MAX)}$ = 0.744 * V_{SUP} $TH_{DOM(MAX)}$ = 0.581 * V_{SUP} D1 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT}), t_{BIT} = 50 µs, 7.0 V ≤ V_{SUP} ≤ 18 V	D1	0.396	-	-	
Duty Cycle 2: $TH_{REC(MIN)}$ = 0.422 * V_{SUP} $TH_{DOM(MIN)}$ = 0.284 * V_{SUP} D2 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT}), t_{BIT} = 50 µs, 7.6 V ≤ V_{SUP} ≤ 18 V	D2	-	-	0.581	
LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR SLOW SLEW RATE - 10.4 KBIT/SEC ACCORDING TO LIN PHYSICAL LAYER SPECIFICATION **BUS LOAD R_{BUS} AND C_{BUS} 1.0 NF / 1.0 KΩ, 6.8 NF / 660 Ω, 10 NF / 500 Ω. MEASUREMENT THRESHOLDS. SEE Figure 15, PAGE 29.**					
Duty Cycle 3: $TH_{REC(MAX)}$ = 0.778 * V_{SUP} $TH_{DOM(MAX)}$ = 0.616 * V_{SUP} D3 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT}), t_{BIT} = 96 µs, 7.0 V ≤ V_{SUP} ≤ 18 V	D3	0.417	-	-	
Duty Cycle 4: $TH_{REC(MIN)}$ = 0.389 * V_{SUP} $TH_{DOM(MIN)}$ = 0.251 * V_{SUP} D4 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT}), t_{BIT} = 96 µs, 7.6 V ≤ V_{SUP} ≤ 18 V	D4	-	-	0.590	
LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR FAST SLEW RATE					
LIN Fast Slew Rate (Programming Mode)	SR_{FAST}	-	20	-	V/µs
LIN PHYSICAL LAYER: CHARACTERISTICS AND WAKE-UP TIMINGS **V_{SUP} FROM 7.0 TO 18 V, BUS LOAD R_{BUS} AND C_{BUS} 1.0 NF / 1.0 KΩ, 6.8 NF / 660 Ω, 10 NF / 500 Ω. SEE Figure 14, PAGE 28.**					
Propagation Delay and Symmetry (See Figure 14, page 27 and Figure 15, page 29)					µs
Propagation Delay of Receiver, t_{REC_PD} = MAX (t_{REC_PDR}, t_{REC_PDF})	t_{REC_PD}	-	4.2	6.0	
Symmetry of Receiver Propagation Delay, t_{REC_PDF} - t_{REC_PDR}	t_{REC_SYM}	-2.0	-	2.0	
Bus Wake-up Deglitcher (LP V_{DD} OFF and LP V_{DD} ON modes) (See Figure 16, page 28 for LP V_{DD} OFF mode and Figure 17, page 29 for LP mode)	t_{PROPWL}	42	70	95	µs
Bus Wake-up Event Reported					µs
From LP V_{DD} OFF mode	$t_{WAKE\_LPVDD\ OFF}$	-	-	1500	
From LP V_{DD} ON mode	$t_{WAKE\_LPVDD\ ON}$	1.0	-	12	
TXD Permanent Dominant State Delay (Guaranteed by design)	t_{TXDDOM}	0.65	1.0	1.35	s