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NXP Semiconductors
Technical Data

Document Number: MC33912
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LIN system basis chip with dc motor pre-driver and current sense

33912

SYSTEM BASIS CHIP WITH LIN 2ND GENERATION

AC SUFFIX (Pb-FREE)
98ASH70029A
32-PIN LQFP

The 33912G5/BAC is a Serial Peripheral Interface (SPI) controlled System Basis Chip (SBC), combining many frequently used functions in an MCU based system, plus a Local Interconnect Network (LIN) transceiver. The 33912 has a 5.0 V, 50 mA/60 mA low dropout regulator with full protection and reporting features. The device provides full SPI readable diagnostics and a selectable timing watchdog for detecting errant operation. The LIN Protocol Specification 2.0 and 2.1 compliant LIN transceiver has waveshaping circuitry which can be disabled for higher data rates.

Two 50 mA/60 mA high-side switches and two 150 mA/160 mA low-side switches with output protection are available. All outputs can be pulse-width modulated (PWM). Four high voltage inputs are available for use in contact monitoring, or as external wake-up inputs. These inputs can be used as high voltage Analog Inputs. The voltage on these pins is divided by a selectable ratio and available via an analog multiplexer.

The 33912 has three main operating modes: Normal (all functions available), Sleep (V_{DD} off, wake-up via LIN, wake-up inputs (L1-L4), cyclic sense and forced wake-up), and Stop (V_{DD} on with limited current capability, wake-up via $\overline{CS}$, LIN bus, wake-up inputs, cyclic sense, forced wake-up and external reset).

The 33912 is compatible with LIN Protocol Specification 2.0, 2.1, and SAEJ2602-2. This device is powered using SMARTMOS technology.

Features

- Full-duplex SPI interface at frequencies up to 4.0 MHz
- LIN transceiver capable of up to 100 kbps with wave shaping
- Current sense module
- Four high voltage analog/logic Inputs
- Configurable window watchdog
- Switched/protected 5.0 V output (used for Hall sensors)
- Two 50 mA high-side and two 150 mA/160 mA low-side protected switches
- 5.0 V low drop regulator with fault detection and low voltage reset (LVR) circuitry

Applications

- Door module: window
- Lift, mirror, door lock, seat control switch
- Seat position motors, occupancy sensor
- Rain and light sensor, light control, sun roof
- Wiper, turning light, cruise control
- Climate: small motors, control panel
- Engine control: sensors, small motors

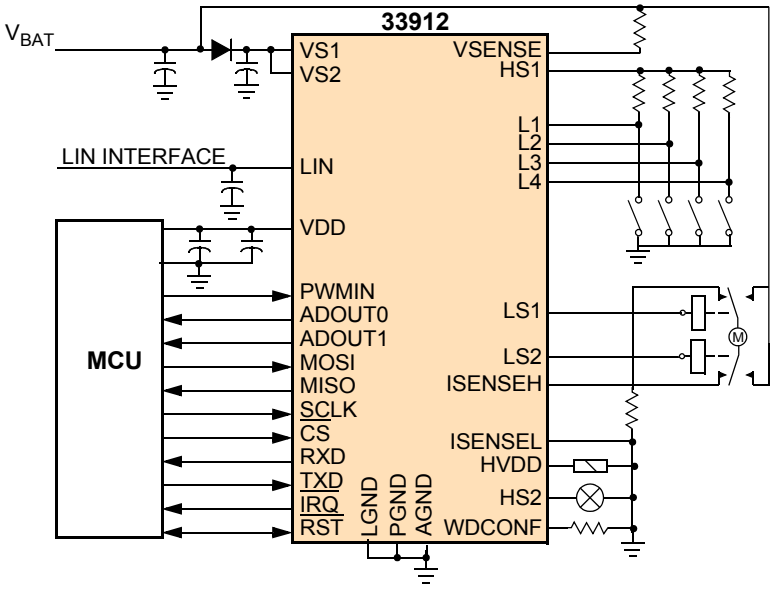


Figure 1. 33912 simplified application diagram

1 Orderable parts

The 33912G5 data sheet is within MC33912G5 product specifications, Pages 3 to 52
The 33912BAC data sheet is within MC33912BAC product specifications, Pages 53 to 103

Table 1. Orderable part variations

Part number [1]	Temperature (T_A)	Package	Generation	Changes
MC33912G5AC	-40 to 125 °C	32-LQFP	2.5	1. Increase ESD Gun IEC61000-4-2 (gun test contact with 150 pF, 330 ohm test conditions) performance to achieve ±6.0 kV min on the LIN pin. 2. Immunity against ISO7637 pulse 3b 3. Reduce EMC emission level on LIN 4. Improve EMC immunity against RF - target new specification including 3x68pF 5. Comply with J2602 conformance test
MC34912G5AC	-40 to 85 °C			
MC33912BAC	-40 to 125 °C		2.0	Initial release
MC34912BAC	-40 to 85 °C			

Notes
1. To order parts in Tape & Reel, add the R2 suffix to the part number.

2 MC33912G5 product specifications, Pages 3 to 52

3 Internal block diagram

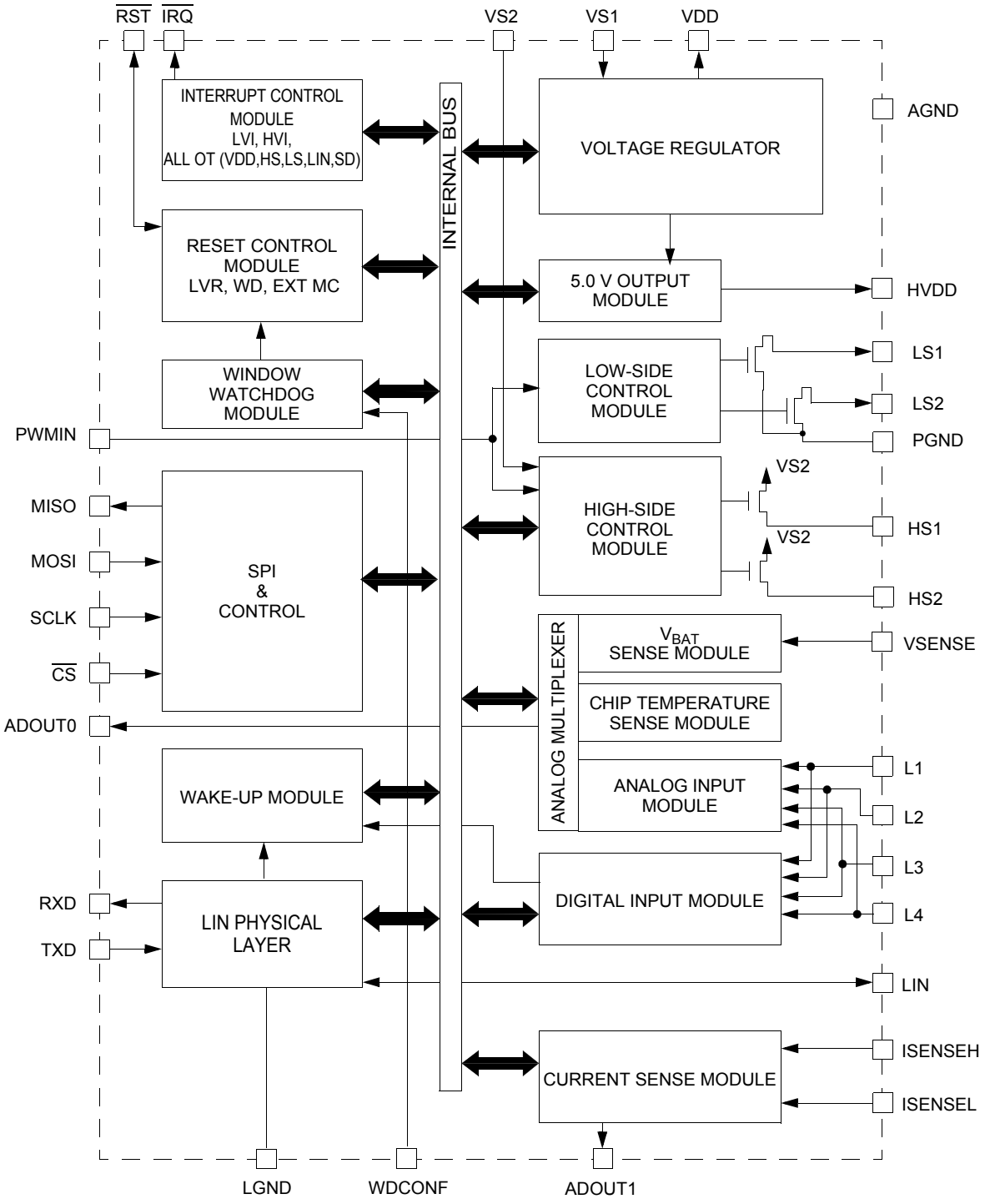


Figure 2. 33912 simplified internal block diagram

4 Pin connections

4.1 Pinout diagram

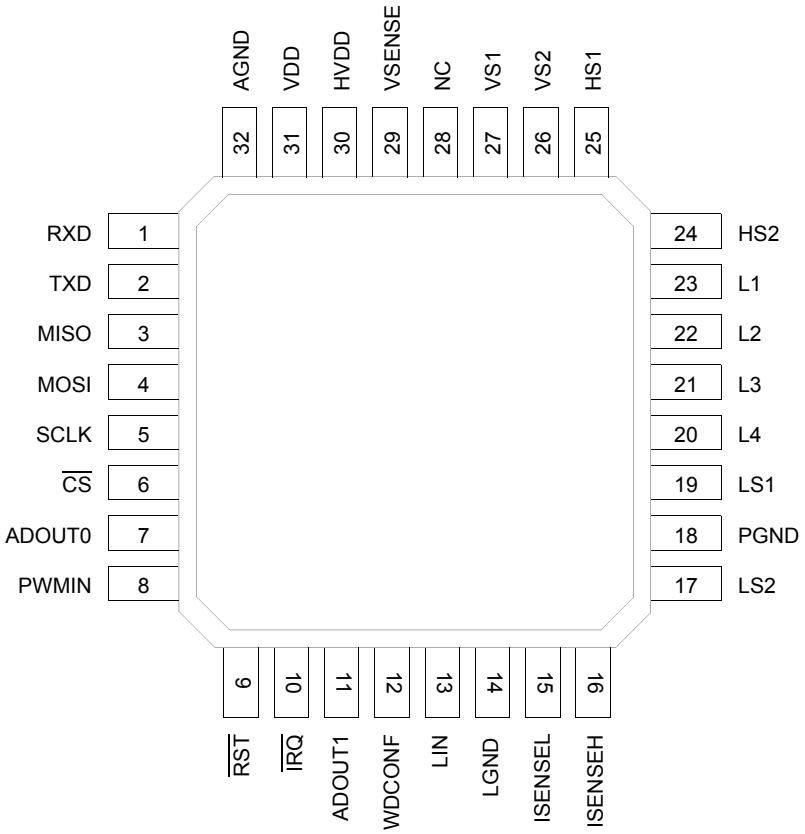


Figure 3. 33912 pin connections

A functional description of each pin can be found in the Functional pin description section beginning on page 23.

Table 2. 33912 pin definitions

Pin	Pin name	Formal name	Definition
1	RXD	Receiver Output	This pin is the receiver output of the LIN interface which reports the state of the bus voltage to the MCU interface.
2	TXD	Transmitter Input	This pin is the transmitter input of the LIN interface which controls the state of the bus output.
3	MISO	SPI Output	SPI (Serial Peripheral Interface) data output. When $\overline{CS}$ is high, pin is in the high-impedance state.
4	MOSI	SPI Input	SPI (Serial Peripheral Interface) data input.
5	SCLK	SPI Clock	SPI (Serial Peripheral Interface) clock Input.
6	CS	SPI Chip Select	SPI (Serial Peripheral Interface) chip select input pin. $\overline{CS}$ is active low.
7	ADOUT0	Analog Output Pin 0	Analog Multiplexer Output.
8	PWMIN	PWM Input	High-side and Low-side Pulse Width Modulation Input.
9	RST	Internal Reset I/O	Bidirectional Reset I/O pin - driven low when any internal reset source is asserted. $\overline{RST}$ is active low.

Table 2. 33912 pin definitions (continued)

Pin	Pin name	Formal name	Definition
10	IRQ	Internal Interrupt Output	Interrupt output pin, indicating wake-up events from Stop mode or events from Normal and Normal request modes. IRQ is active low.
11	ADOUT1	Analog Output Pin 1	Current sense analog output.
12	WDCONF	Watchdog Configuration Pin	This input pin is for configuration of the watchdog period and allows the disabling of the watchdog.
13	LIN	LIN Bus	This pin represents the single-wire bus transmitter and receiver.
14	LGND	LIN Ground Pin	This pin is the device LIN ground connection. It is internally connected to the PGND pin.
15 16	ISENSEL ISENSEH	Current Sense Pins	Current Sense differential inputs.
17 19	LS2 LS1	Low-side Outputs	Relay drivers low-side outputs.
18	PGND	Power Ground Pin	This pin is the device low-side ground connection. It is internally connected to the LGND pin.
20 21 22 23	L4 L3 L2 L1	Wake-up Inputs	These pins are the wake-up capable digital inputs[2]. In addition, all Lx inputs can be sensed analog via the analog multiplexer.
24 25	HS2 HS1	High-side Outputs	High-side switch outputs.
26 27	VS2 VS1	Power Supply Pin	These pins are device battery level power supply pins. VS2 is supplying the HSx drivers while VS1 supplies the remaining blocks.[3]
28	NC	Not Connected	This pin can be left open or connected to any potential ground or power supply.
29	VSENSE	Voltage Sense Pin	Battery voltage sense input.[4]
30	HVDD	Hall Sensor Supply Output	+5.0 V switchable supply output pin.[5]
31	VDD	Voltage Regulator Output	+5.0 V main voltage regulator output pin.[6]
32	AGND	Analog Ground Pin	This pin is the device analog ground connection.

Notes

2. When used as digital input, a series 33 kΩ resistor must be used to protect against automotive transients.
3. Reverse battery protection series diodes must be used externally to protect the internal circuitry.
4. This pin can be connected directly to the battery line for voltage measurements. The pin is self protected against reverse battery connections. It is strongly recommended to connect a 10 kΩ resistor in series with this pin for protection purposes.
5. External capacitor (1.0 µF < C < 10 µF; 0.1 Ω < ESR < 5.0 Ω) required.
6. External capacitor (2.0 µF < C < 100 µF; 0.1 Ω < ESR < 10 Ω) required.

5 Electrical characteristics

5.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings				
$V_{SUP(SS)}$ $V_{SUP(PK)}$	Supply Voltage at VS1 and VS2 • Normal Operation (DC) • Transient Conditions (load dump)	 -0.3 to 27 -0.3 to 40	V	
V_{DD}	Supply Voltage at VDD	-0.3 to 5.5	V	
V_{IN} $V_{IN(IRQ)}$	Input / Output Pins Voltage • $\overline{CS}$, $\overline{RST}$, SCLK, PWMIN, ADOUT0, ADOUT1, MOSI, MISO, TXD, RXD, HVDD • Interrupt Pin ($\overline{IRQ}$)	-0.3 to V_{DD} +0.3 -0.3 to 11	V	(7) (8)
V_{HS}	HS1 and HS2 Pin Voltage (DC)	-0.3 to V_{SUP} +0.3	V	
V_{LS}	LS1 and LS2 Pin Voltage (DC)	-0.3 to 45	V	
V_{LxDC} V_{LxTR}	L1, L2, L3 and L4 Pin Voltage • Normal Operation with a series 33 k resistor (DC) • Transient input voltage with external component (according to ISO7637-2) (See Figure 5, page 19)	-18 to 40 ±100	V	
V_{ISENSE}	ISENSEH and ISENSEL Pin Voltage (DC)	-0.3 to 40	V	
V_{VSENSE}	VSENSE Pin Voltage (DC)	-27 to 40	V	
V_{BUSDC} V_{BUSTR}	LIN Pin Voltage • Normal Operation (DC) • Transient input voltage with external component (according to ISO7637-2) (See Figure 4, page 19)	-18 to 40 -150 to 100	V	
I_{VDD}	VDD output current	Internally Limited	A	

Notes

7. Exceeding voltage limits on specified pins may cause a malfunction or permanent damage to the device.
8. Extended voltage range for programming purpose only.

Table 3. Maximum ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
	ESD Capability • AECQ100 • Human Body Model - JESD22/A114 (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω)			
V_{ESD1-1} V_{ESD1-2} V_{ESD1-3}	• LIN Pin • L1, L2, L3, and L4 • all other Pins	±8.0k ±6.0k ±2000		
	• Charge Device Model - JESD22/C101 (C_{ZAP} = 4.0 pF)			
V_{ESD2-1} V_{ESD2-2}	• Corner Pins (Pins 1, 8, 9, 16, 17, 24, 25 and 32) • All other Pins (Pins 2-7, 10-15, 18-23, 26-31)	±750 ±500		
	• According to LIN Conformance Test Specification / LIN EMC Test Specification, August 2004 (C_{ZAP} = 150 pF, R_{ZAP} = 330 Ω)		V	
	• Contact Discharge, Unpowered			
V_{ESD3-1} V_{ESD3-2} V_{ESD3-3} V_{ESD3-4}	• LIN pin with 220 pF • LIN pin without capacitor • VS1/VS2 (100 nF to ground) • Lx inputs (33 kΩ serial resistor)	±20k ±11k >±12k ±6000		
	• According to IEC 61000-4-2 (C_{ZAP} = 150 pF, R_{ZAP} = 330 Ω)			
	• Unpowered			
V_{ESD4-1} V_{ESD4-2} V_{ESD4-3}	• LIN pin with 220 pF and without capacitor • VS1/VS2 (100 nF to ground) • Lx inputs (33 kΩ serial resistor)	±8000 ±8000 ±8000		
Thermal ratings				
T_A	Operating Ambient Temperature 33912 34912	 -40 to 125 -40 to 85	°C	(9)
T_J	Operating Junction Temperature	-40 to 150	°C	
T_{STG}	Storage Temperature	-55 to 150	°C	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient Natural Convection, Single Layer board (1s) Natural Convection, Four Layer board (2s2p)	 85 56	°C/W	 (9), (10) (9), (11)
$R_{\theta JC}$	Thermal Resistance, Junction to Case	23	°C/W	(12)
T_{PPRT}	Peak Package Reflow Temperature During Reflow	Note 14	°C	(13), (14)

Notes

9. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
10. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
11. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
12. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
13. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
14. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.NXP.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

5.2 Static electrical characteristics

Table 4. Static electrical characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Supply voltage range (VS1, VS2)						
V_{SUP}	Nominal Operating Voltage	5.5	–	18	V	
V_{SUPOP}	Functional Operating Voltage	–	–	27	V	(15)
V_{SUPLD}	Load Dump	–	–	40	V	
Supply current range (V_{SUP} = 13.5 V)						
I_{RUN}	Normal Mode (I_{OUT} at V_{DD} = 10 mA), LIN Recessive State	–	4.5	10	mA	(16)
I_{STOP}	Stop Mode, VDD ON with I_{OUT} = 100 µA, LIN Recessive State • 5.5 V < V_{SUP} < 12 V • V_{SUP} = 13.5 V • 13.5 V < V_{SUP} < 18 V	 – – –	 47 62 180	 80 90 400	µA	(16), (17), (18), (19)
I_{SLEEP}	Sleep Mode, VDD OFF, LIN Recessive State • 5.5 V < V_{SUP} < 12 V • V_{SUP} = 13.5 V • 13.5 V ≤ V_{SUP} < 18 V	 – – –	 27 33 160	 35 48 300	µA	(16), (18)
I_{CYCLIC}	Cyclic Sense Supply Current Adder	–	10	–	µA	(20)
Supply under/overvoltage detections						
$V_{BATFAIL}$ $V_{BATFAIL\_HYS}$	Power-On Reset (BATFAIL) • Threshold (measured on VS1) • Hysteresis (measured on VS1)	 1.5 –	 3.0 0.9	 3.9 –	V	(21), (20)
V_{SUV} V_{SUV_HYS}	V_{SUP} Undervoltage Detection (VSUV Flag) (Normal and Normal Request Modes, Interrupt Generated) • Threshold (measured on VS1) • Hysteresis (measured on VS1)	 5.55 –	 6.0 0.2	 6.6 –	V	
V_{SOV} V_{SOV_HYS}	V_{SUP} Overvoltage Detection (VSOV Flag) (Normal and Normal Request Modes, Interrupt Generated) • Threshold (measured on VS1) • Hysteresis (measured on VS1)	 18 –	 19.25 1.0	 20.5 –	V	

Notes

15. Device is fully functional. All features are operating.
16. Total current (I_{VS1} + I_{VS2}) measured at GND pins excluding all loads, cyclic sense disabled.
17. Total I_{DD} current (including loads) below 100 µA.
18. Stop and Sleep Modes current increases if V_{SUP} exceeds13.5 V.
19. This parameter is guaranteed after 90 ms.
20. This parameter is guaranteed by process monitoring but not production tested.
21. The Flag is set during power up sequence. To clear the flag, a SPI read must be performed.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Voltage regulator (22) (VDD)						
V_{DDRUN}	Normal Mode Output Voltage • 1.0 mA < I_{VDD} < 50 mA; 5.5 V < V_{SUP} < 27 V	4.75	5.00	5.25	V	
I_{VDDRUN}	Normal Mode Output Current Limitation	60	110	200	mA	
V_{DDDROP}	Dropout Voltage • I_{VDD} = 50 mA	–	0.1	0.25	V	(23)
V_{DDSTOP}	Stop Mode Output Voltage • I_{VDD} < 5.0 mA	4.75	5.0	5.25	V	
$I_{VDDSTOP}$	Stop Mode Output Current Limitation	6.0	13	36	mA	
LR_{RUN} LR_{STOP}	Line Regulation • Normal Mode, 5.5 V < V_{SUP} < 18 V; I_{VDD} = 10 mA • Stop Mode, 5.5 V < V_{SUP} < 18 V; I_{VDD} = 1.0 mA	– –	– –	25 25	mV	
LD_{RUN} LD_{STOP}	Load Regulation • Normal Mode, 1.0 mA < I_{VDD} < 50 mA • Stop Mode, 0.1 mA < I_{VDD} < 5.0 mA	– –	– –	80 50	mV	
T_{PRE}	Overtemperature Prewarning (Junction) • Interrupt generated, VDDOT Bit Set	90	115	140	°C	(24)
T_{PRE_HYS}	Overtemperature Prewarning Hysteresis	–	13	–	°C	(24)
T_{SD}	Overtemperature Shutdown Temperature (Junction)	150	170	190	°C	(24)
T_{SD_HYS}	Overtemperature Shutdown Hysteresis	–	13	–	°C	(24)
Hall sensor supply output (25) (HVDD)						
H_{VDDACC}	V_{DD} Voltage matching H_{VDDACC} = (HVDD-VDD) / VDD * 100% • I_{HVDD} = 15 mA	-2.0	–	2.0	%	
I_{HVDD}	Current Limitation	20	35	50	mA	
$H_{VDDDROP}$	Dropout Voltage • I_{HVDD} = 15 mA; I_{VDD} = 5.0 mA	–	160	300	mV	
LR_{HVDD}	Line Regulation • I_{HVDD} = 5.0 mA; I_{VDD} = 5.0 mA	–	–	40	mV	
LD_{HVDD}	Load Regulation • 1.0 mA > I_{HVDD} > 15 mA; I_{VDD} = 5.0 mA	–	–	20	mV	

Notes

22. Specification with external capacitor 2.0 µF < C < 100 µF and 100 mΩ ≤ ESR ≤ 10 Ω.
23. Measured when voltage has dropped 250 mV below its nominal Value (5.0 V).
24. This parameter is guaranteed by process monitoring but not production tested.
25. Specification with external capacitor 1.0 µF < C < 10 µF and 100 mΩ ≤ ESR ≤ 10 Ω.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
$\overline{RST}$ input/output pin ($\overline{RST}$)						
$V_{\overline{RST}TH}$	VDD Low Voltage Reset Threshold	4.3	4.5	4.7	V	
V_{OL}	Low-state Output Voltage • I_{OUT} = 1.5 mA; 3.5 V ≤ V_{SUP} ≤ 27 V	0.0	–	0.9	V	
I_{OH}	High-state Output Current (0 V < V_{OUT} < 3.5 V)	-150	-250	-350	µA	
I_{PD_MAX}	Pull-down Current Limitation (internally limited) V_{OUT} = V_{DD}	1.5	–	8.0	mA	
V_{IL}	Low-state Input Voltage	-0.3	–	0.3 x V_{DD}	V	
V_{IH}	High-state Input Voltage	0.7 x V_{DD}	–	V_{DD} +0.3	V	
MISO SPI output pin (MISO)						
V_{OL}	Low-state Output Voltage • I_{OUT} = 1.5 mA	0.0	–	1.0	V	
V_{OH}	High-state Output Voltage • I_{OUT} = -250 µA	V_{DD} -0.9	–	V_{DD}	V	
$I_{TRIMISO}$	Tri-state Leakage Current • 0 V ≤ V_{MISO} ≤ V_{DD}	-10	–	10	µA	
SPI input pins (MOSI, SCLK, $\overline{CS}$)						
V_{IL}	Low-state Input Voltage	-0.3	–	0.3 x V_{DD}	V	
V_{IH}	High-state Input Voltage	0.7 x V_{DD}	–	V_{DD} +0.3	V	
I_{IN}	MOSI, SCLK Input Current • 0 V ≤ V_{IN} ≤ V_{DD}	-10	–	10	µA	
$I_{PU\overline{CS}}$	$\overline{CS}$ Pull-up Current • 0 V < V_{IN} < 3.5 V	10	20	30	µA	
Interrupt output pin ($\overline{IRQ}$)						
V_{OL}	Low-state Output Voltage • I_{OUT} = 1.5 mA	0.0	–	0.8	V	
V_{OH}	High-state Output Voltage • I_{OUT} = -250 µA	V_{DD} -0.8	–	V_{DD}	V	
I_{OUT}	Leakage Current • V_{DD} ≤ V_{OUT} ≤ 10 V	–	–	2.0	mA	
Pulse width modulation input pin (PWMIN)						
V_{IL}	Low-state Input Voltage	-0.3	–	0.3 x V_{DD}	V	
V_{IH}	High-state Input Voltage	0.7 x V_{DD}	–	V_{DD} +0.3	V	
$I_{PUPWMIN}$	Pull-up current • 0 V < V_{IN} < 3.5 V	10	20	30	µA	

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
High-side outputs HS1 and HS2 Pins (HS1, HS2)						
$R_{DS(on)}$	Output Drain-to-Source On Resistance • T_J = 25 °C, I_{LOAD} = 50 mA; V_{SUP} > 9.0 V • T_J = 150 °C, I_{LOAD} = 50 mA; V_{SUP} > 9.0 V • T_J = 150 °C, I_{LOAD} = 30 mA; 5.5 V < V_{SUP} < 9.0 V	 – – –	 – – –	 7.0 10 14	Ω	(26)
I_{LIMHSX}	Output Current Limitation • 0 V < V_{OUT} < V_{SUP} - 2.0 V	60	90	250	mA	(27)
I_{OLHSX}	Open Load Current Detection	–	5.0	7.5	mA	(28)
I_{LEAK}	Leakage Current • -0.2 V < V_{HSX} < V_{S2} + 0.2 V	–	–	10	µA	
V_{THSC}	Short-circuit Detection Threshold • 5.5 V < V_{SUP} < 27 V	V_{SUP} -2.0	–	–	V	(29)
T_{HSSD}	Overtemperature Shutdown	140	160	180	°C	(30), (34)
T_{HSSD_HYS}	Overtemperature Shutdown Hysteresis	–	10	–	°C	(34)
Low-side outputs LS1 and LS2 Pins (LS1, LS2)						
$R_{DS(on)}$	Output Drain-to-Source On Resistance • T_J = 25 °C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V • T_J = 125 °C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V • T_J = 125 °C, I_{LOAD} = 120 mA, 5.5 V < V_{SUP} < 9.0 V	 – – –	 – – –	 2.5 4.5 10	Ω	
I_{LIMLSX}	Output Current Limitation • 2.0 V < V_{OUT} < V_{SUP}	160	275	350	mA	(31)
I_{OLLSX}	Open Load Current Detection	–	7.5	12	mA	(32)
I_{LEAK}	Leakage Current • -0.2 V < V_{OUT} < VS1	–	–	10	µA	
V_{CLAMP}	Active Output Energy Clamp • I_{OUT} = 150 mA	V_{SUP} +2.0	–	V_{SUP} +5.0	V	
V_{THSC}	Short-circuit Detection Threshold • 5.5 V < V_{SUP} < 27 V	2.0	–	–	V	(29)
T_{LSSD}	Overtemperature Shutdown	140	160	180	°C	(33), (34)
T_{LSSD_HYS}	Overtemperature Shutdown Hysteresis	–	10	–	°C	

Notes

26. This parameter is production tested up to T_A = 125 °C, and guaranteed by process monitoring up to T_J = 150 °C.
27. When overcurrent occurs, the corresponding high-side stays ON with limited current capability and the HSxCL flag is set in the HSSR.
28. When open load occurs, the flag (HSxOP) is set in the HSSR.
29. HS and LS automatically shutdown if HSOT or LSOT occurs or if the HVSE flag is enabled and an overvoltage occurs.
30. When overtemperature shutdown occurs, both high-sides are turned off. All flags in HSSR are set.
31. When overcurrent occurs, the corresponding low-side stays ON with limited current capability and the LSxCL flag is set in the LSSR.
32. When open load occurs, the flag (LSxOP) is set in the LSSR.
33. When overtemperature shutdown occurs, both low-sides are turned off. All flags in LSSR are set.
34. Guaranteed by characterization but not production tested

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
L1, L2, L3 and L4 input pins (L1, L2, L3, L4)						
V_{THL}	Low Detection Threshold • 5.5 V < V_{SUP} < 27 V	2.0	2.5	3.0	V	(35)
V_{THH}	High Detection Threshold • 5.5 V < V_{SUP} < 27 V	3.0	3.5	4.0	V	(35)
V_{HYS}	Hysteresis • 5.5 V < V_{SUP} < 27 V	0.4	0.8	1.4	V	(35)
I_{IN}	Input Current • -0.2 V < V_{IN} < VS1	-10	–	10	µA	(36)
R_{LXIN}	Analog Input Impedance	800	1300	2000	kΩ	(37)
$RATIO_{LX}$	Analog Input Divider Ratio ($RATIO_{Lx}$ = V_{Lx} / V_{ADOUT0}) • LXDS (Lx Divider Select) = 0 • LXDS (Lx Divider Select) = 1	 0.95 3.42	 1.0 3.6	 1.05 3.78		
$V_{RATIOLx-OFFSET}$	Analog Output offset Ratio • LXDS (Lx Divider Select) = 0 • LXDS (Lx Divider Select) = 1	 -80 -22	 6.0 2.0	 80 22	mV	
$LX_{MATCHING}$	Analog Inputs Matching • LXDS (Lx Divider Select) = 0 • LXDS (Lx Divider Select) = 1	 96 96	 100 100	 104 104	%	
Window watchdog configuration pin (WDCONF)(38)						
R_{EXT}	External Resistor Range	20	–	200	kΩ	
WD_{ACC}	Watchdog Period Accuracy with External Resistor (Excluding Resistor Accuracy)	-15	–	15	%	(39)
Analog multiplexer						
V_{ADOUT0_TEMP}	Temperature Sense Analog Output Voltage • T_A = -40 °C • T_A = 25 °C • T_A = 125 °C	 2.0 2.8 3.6	 - 3.0 -	 2.8 3.6 4.6	V	
V_{ADOUT0_25}	Temperature Sense Analog Output Voltage per characterization • T_A = 25 °C	3.1	3.15	3.2	V	(40)
S_{TTOV}	Internal Chip Temperature Sense Gain	9.0	10.5	12	mV/K	
S_{TTOV_3T}	Internal Chip Temperature Sense Gain per characterization at 3 temperatures. See Figure 16, Temperature sense gain	9.9	10.2	10.5	mV/K	(40)
$RATIO_{VSENSE}$	VSENSE Input Divider Ratio ($RATIO_{VSENSE}$ = V_{VSENSE} / V_{ADOUT0}) • 5.5 V < V_{SUP} < 27 V	5.0	5.25	5.5		
$RATIO_{VSENSECZ}$	VSENSE Input Divider Ratio (RATIOVSENSE=V_{SENSE}/V_{ADOUT0}) per characterization • 5.5 <V_{SUP}< 27 V	5.15	5.25	5.35		(40)

Notes

35. The unused Lx pins must be connected to ground.
36. Analog multiplexer input disconnected from Lx input pin.
37. Analog multiplexer input connected to Lx input pin.
38. For V_{SUP} 4.7 V to 18 V
39. Watchdog timing period calculation formula: t_{PWD} [ms] = [0.466 * (R_{EXT} - 20)] + 10 with (R_{EXT} in kΩ)
40. These limits have been defined after laboratory characterization on 3 lots and 30 samples. These tighten limits could not be guaranteed by production test.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Analog multiplexer (continued)						
$OFFSET_{VSENSE}$	VSENSE Output Related Offset	-30	-10	30	mV	
$OFFSET_{VSENSE\_CZ}$	V_{SENSE} Output Related Offset per characterization	-30	-12.6	0	mV	(41)
Analog outputs (ADOUT0 and ADOUT1)						
V_{OUT_MAX}	Maximum Output Voltage • -5.0 mA < I_O < 5.0 mA	V_{DD} -0.35	–	V_{DD}	V	
V_{OUT_MIN}	Minimum Output Voltage • -5.0 mA < I_O < 5.0 mA	0.0	–	0.35	V	
Current sense amplifier (ISENSEH, ISENSEL)						
G	Gain • CSGS (Current Sense Gain Select) = 0 • CSGS (Current Sense Gain Select) = 1	 29 14	 30 14.5	 31 15		
DIFF	Differential Input Impedance • CSGS (Current Sense Gain Select) = 0 • CSGS (Current Sense Gain Select) = 1	 2.0 5.0	 10 20	 30 50	kΩ	
CM	Common Mode Input Impedance • CSGS (Current Sense Gain Select) = 0 • CSGS (Current Sense Gain Select) = 1	 100 100	 – –	 200 200	kΩ	
V_{IN}	ISENSEH, ISENSEL Input Voltage Range	-0.2	–	3.0	V	
V_{IN_OFFSET}	Input Offset Voltage • CSAZ (Current Sense Auto Zero) = 0 • CSAZ (Current Sense Auto Zero) = 1	 -15 -2.0	 – –	 15 2.0	mV	
RxD output pin (LIN physical layer) (RxD)						
V_{OL}	Low-state Output Voltage • I_{OUT} = 1.5 mA	0.0	–	0.8	V	
V_{OH}	High-state Output Voltage • I_{OUT} = -250 µA	V_{DD} -0.8	–	V_{DD}	V	
TXD input pin (LIN physical layer) (TXD)						
V_{IL}	Low-state Input Voltage	-0.3	–	0.3 x V_{DD}	V	
V_{IH}	High-state Input Voltage	0.7 x V_{DD}	–	V_{DD} +0.3	V	
I_{PUIN}	Pin Pull-up Current, 0 V < V_{IN} < 3.5 V	10	20	30	µA	
LIN physical layer with J2602 feature enabled (bit DIS_J2602 = 0)						
$V_{TH\_UNDER\_VOLTAGE}$	LIN Undervoltage threshold • Positive and Negative threshold (V_{THP}, V_{THN})	5.0	-	6.0	V	
V_{J2602_DEG}	Hysteresis (V_{THP} - V_{THN})	-	400	-	mV	

Notes

41. These limits have been defined after laboratory characterization on 3 lots and 30 samples. These tighten limits could not be guaranteed by production test.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
LIN physical layer, transceiver (LIN)(42)						
V_{BAT}	Operating Voltage Range	8.0	-	18	V	
V_{SUP}	Supply Voltage Range	7.0	-	18	V	
$V_{SUP\_NON\_OP}$	Voltage Range within which the device is not destroyed	-0.3	-	40	V	
I_{BUS_LIM}	Current Limitation for Driver Dominant State • Driver ON, V_{BUS} = 18 V	40	90	200	mA	
$I_{BUS\_PAS\_DOM}$	Input Leakage Current at the receiver • Driver off; V_{BUS} = 0 V; V_{BAT} = 12 V	-1.0	–	–	mA	
$I_{BUS\_PAS\_REC}$	Leakage Output Current to GND • Driver Off; 8.0 V < V_{BAT} < 18 V; 8.0 V < V_{BUS} < 18 V; V_{BUS} ≥ V_{BAT}	–	–	20	µA	
$I_{BUS\_NO\_GND}$	Control unit disconnected from ground • GND_{DEVICE} = V_{SUP}; V_{BAT} = 12 V; 0 < V_{BUS} < 18 V	-1.0	–	1.0	mA	(43)
I_{BUSNO_BAT}	V_{BAT} Disconnected; V_{SUP_DEVICE} = GND; 0 V < V_{BUS} < 18 V	–	–	100	µA	(44)
V_{BUSDOM}	Receiver Dominant State	–	–	0.4	V_{SUP}	
V_{BUSREC}	Receiver Recessive State	0.6	–	–	V_{SUP}	
V_{BUS_CNT}	Receiver Threshold Center • (V_{TH_DOM} + V_{TH_REC})/2	0.475	0.5	0.525	V_{SUP}	
V_{HYS}	Receiver Threshold Hysteresis • (V_{TH_REC} - V_{TH_DOM})	–	–	0.175	V_{SUP}	
$V_{SERDIODE}$	Voltage Drop at the serial Diode in pull-up path	0.4		1.0	V	
V_{SHIFT_BAT}	VBAT_SHIFT	0		11.5%	V_{BAT}	
V_{SHIFT_GND}	GND_SHIFT	0		11.5%	V_{BAT}	
V_{BUSWU}	LIN Wake-up threshold from Stop or Sleep mode		5.3	5.8	V	(45)
R_{SLAVE}	LIN Pull-up Resistor to V_{SUP}	20	30	60	kΩ	
T_{LINSD}	Overtemperature Shutdown	140	160	180	°C	(46)
T_{LINSD_HYS}	Overtemperature Shutdown Hysteresis	–	10	–	°C	

Notes

42. Parameters guaranteed for 7.0 V ≤ V_{SUP} ≤ 18 V.
43. Loss of local ground must not affect communication in the residual network.
44. Node has to sustain the current which can flow under this condition. Bus must remain operational under this condition.
45. This parameter is 100% tested on an Automatic Tester. However, since it has not been monitored during reliability stresses, NXP does not guarantee this parameter during the product's life time.
46. When overtemperature shutdown occurs, the LIN bus goes in recessive state and the flag LINOT in LINSR is set.

5.3 Dynamic electrical characteristics

Table 5. Dynamic electrical characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
SPI interface timing (see Figure 13, page 22)						
f_{SPIOP}	SPI Operating Frequency	–	–	4.0	MHz	
t_{PSCLK}	SCLK Clock Period	250	–	N/A	ns	
t_{WSCLKH}	SCLK Clock High Time	110	–	N/A	ns	(47)
t_{WSCLKL}	SCLK Clock Low Time	110	–	N/A	ns	(47)
t_{LEAD}	Falling Edge of $\overline{CS}$ to Rising Edge of SCLK	100	–	N/A	ns	(47)
t_{LAG}	Falling Edge of SCLK to $\overline{CS}$ Rising Edge	100	–	N/A	ns	(47)
t_{SISU}	MOSI to Falling Edge of SCLK	40	–	N/A	ns	(47)
t_{SIH}	Falling Edge of SCLK to MOSI	40	–	N/A	ns	(47)
t_{RSO}	MISO Rise Time • C_L = 220 pF	–	40	–	ns	(47)
t_{FSO}	MISO Fall Time • C_L = 220 pF	–	40	–	ns	(47)
t_{SOEN} t_{SODIS}	Time from Falling or Rising Edges of $\overline{CS}$ to: - MISO Low-impedance - MISO High-impedance	 0.0 0.0	 – –	 50 50	ns	(47)
t_{VALID}	Time from Rising Edge of SCLK to MISO Data Valid • 0.2 x V_{DD} ≤ MISO ≥ 0.8 x V_{DD}, C_L = 100 pF	0.0	–	75	ns	(47)
$\overline{RST}$ output pin						
$t_{\overline{RST}}$	Reset Low-level Duration After V_{DD} High (see Figure 12, page 22)	0.65	1.0	1.35	ms	
$t_{\overline{RSTDF}}$	Reset Deglitch Filter Time	350	480	900	ns	
Window watchdog configuration pin (WDCONF)						
t_{PWD}	Watchdog Time Period • External Resistor R_{EXT} = 20 kΩ (1%) • External Resistor R_{EXT} = 200 kΩ (1%) • Without External Resistor R_{EXT} (WDCONF Pin Open)	 8.5 79 110	 10 94 150	 11.5 108 205	ms	(48)
Current sense amplifier(47)						
CMR	Common Mode Rejection Ratio	70	–	–	dB	
SVR	Supply Voltage Rejection Ratio	60	–	–	dB	(49)
GBP	Gain Bandwidth Product	0.75	3.0	–	MHz	
SR	Output Slew-Rate	0.5	–	–	V/µs	

Notes

47. This parameter is guaranteed by process monitoring but not production tested.
48. Watchdog timing period calculation formula: t_{PWD} [ms] = [0.466 * (R_{EXT} - 20)] + 10 with (R_{EXT} in kΩ)
49. Analog Outputs are supplied by V_{DD} and from 100 Hz to 4.0 kHz

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
L1, L2, L3 and L4 inputs						
t_{WUF}	Lx Filter Time Deglitcher	8.0	20	38	µs	(50)
State machine timing						
t_{STOP}	Delay Between $\overline{CS}$ LOW-to-HIGH Transition (at End of SPI Stop Command) and Stop Mode Activation	–	–	5.0	µs	(50)
t_{NRTOUT}	Normal Request Mode Timeout (see Figure 12, page 22)	110	150	205	ms	
T_{ON}	Cyclic Sense ON Time from Stop and Sleep mode	130	200	270	µs	(51)
	Cyclic Sense Accuracy	-35		+35	%	(50)
t_{S-ON}	Delay Between the SPI Command and HS/LS Turn On • 9.0 V < V_{SUP} < 27 V	–	–	10	µs	(52)
t_{S-OFF}	Delay Between the SPI Command and HS/LS Turn Off • 9.0 V < V_{SUP} < 27 V	–	–	10	µs	(52)
t_{SNR2N}	Delay Between Normal Request and Normal mode After a Watchdog Trigger Command (Normal Request Mode)	–	–	10	µs	(50)
$t_{WU\overline{CS}}$ t_{WUSPI}	Delay Between $\overline{CS}$ Wake-up ($\overline{CS}$ LOW to HIGH) in Stop mode and: • Normal Request mode, VDD ON and $\overline{RST}$ HIGH • First Accepted SPI Command	9.0 90	15 —	80 N/A	µs	
$t_{2\overline{CS}}$	Minimum Time Between Rising and Falling Edge on the $\overline{CS}$	4.0	—	—	µs	
J2602 deglitcher						
t_{J2602_DEG}	V_{SUP} Deglitcher • (DIS_J2602 = 0)	35	50	70	µs	(53)
LIN physical layer: driver characteristics for normal slew rate - 20.0 kbit/sec according to lin physical layer specification (54), (55)						
D1	Duty Cycle 1: • $TH_{REC(MAX)}$ = 0.744 * V_{SUP} • $TH_{DOM(MAX)}$ = 0.581 * V_{SUP} • D1 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT}), t_{BIT} = 50 µs, 7.0 V ≤ V_{SUP} ≤ 18 V	0.396	—	—		
D2	Duty Cycle 2: • $TH_{REC(MIN)}$ = 0.422 * V_{SUP} • $TH_{DOM(MIN)}$ = 0.284 * V_{SUP} • D2 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT}), t_{BIT} = 50 µs, 7.6 V ≤ V_{SUP} ≤ 18 V	—	—	0.581		

Notes

50. This parameter is guaranteed by process monitoring but not production tested.
51. This parameter is 100% tested on an Automatic Tester. However, since it has not been monitored during reliability stresses, NXP does not guarantee this parameter during the product's life time.
52. Delay between turn on or off command (rising edge on $\overline{CS}$) and HS or LS ON or OFF, excluding rise or fall time due to external load.
53. This parameter has not been monitoring during operating life test.
54. Bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter.
55. See Figure 7, page 20.

Table 5. Dynamic electrical characteristics (continued)

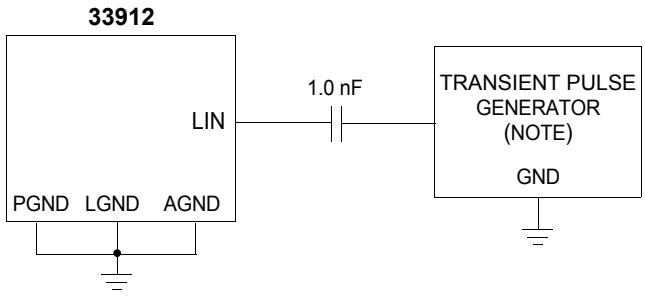
Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
LIN physical layer: driver characteristics for slow slew rate - 10.4 kbit/sec according to lin physical layer specification						(56), (57)
D3	Duty Cycle 3: • $TH_{REC(MAX)}$ = 0.778 * V_{SUP} • $TH_{DOM(MAX)}$ = 0.616 * V_{SUP} • D3 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT}), t_{BIT} = 96 µs, 7.0 V ≤ V_{SUP} ≤ 18 V	0.417	—	—		
D4	Duty Cycle 4: • $TH_{REC(MIN)}$ = 0.389 * V_{SUP} • $TH_{DOM(MIN)}$ = 0.251 * V_{SUP} • D4 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT}), t_{BIT} = 96 µs, 7.6 V ≤ V_{SUP} ≤ 18 V	—	—	0.590		
LIN physical layer: driver characteristics for fast slew rate						
SR_{FAST}	LIN Fast Slew Rate (Programming mode)	—	20	—	V/µs	
LIN physical layer: characteristics and wake-up timings						(58)
t_{REC_PD} t_{REC_SYM}	Propagation Delay and Symmetry • Propagation Delay of Receiver, t_{REC_PD} = MAX (t_{REC_PDR}, t_{REC_PDF}) • Symmetry of Receiver Propagation Delay, t_{REC_PDF} - t_{REC_PDR}	— -2.0	4.2 —	6.0 2.0	µs	(59)
t_{PROPWL}	Bus Wake-up Deglitcher (Sleep and Stop modes)	42	70	95	µs	(60), (64) (61)
t_{WAKE_SLEEP} t_{WAKE_STOP}	Bus Wake-Up Event Reported • From Sleep Mode • From Stop Mode	— 9.0	— 27	1500 35	µs	(62) (63)
t_{TXDDOM}	TXD Permanent Dominant State Delay	0.65	1.0	1.35	s	
Pulse width modulation input pin (PWMIN)						
f_{PWMIN}	PWMIN pin • Max. frequency to drive HS and LS output pins	-	10	-	kHz	(64)

Notes

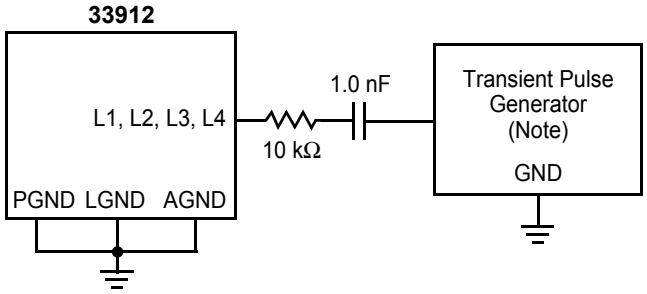
56. Bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 6, page 20.
57. See Figure 8, page 20.
58. V_{SUP} from 7.0 to 18 V, bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 6, page 20.
59. See Figure 9, page 21
60. See Figure 10, page 21 for Sleep and Figure 11, page 21 for Stop mode.
61. This parameter is tested on automatic tester but has not been monitoring during operating life test.
62. The measurement is done with 1.0 µF capacitor and 0mA current load on V_{DD}. The value takes into account the delay to charge the capacitor. The delay is measured between the bus wake-up threshold (V_{BUSWU}) rising edge of the LIN bus and when V_{DD} reaches 3.0 V. See Figure 10, page 21. The delay depends of the load and capacitor on V_{DD}.
63. In Stop mode, the delay is measured between the bus wake-up threshold (V_{BUSWU}) and the falling edge of the $\overline{IRQ}$ pin. See Figure 11, page 21.
64. This parameter is guaranteed by process monitoring but not production tested.

5.4 Timing diagrams



Note Waveform per ISO 7637-2. Test Pulses 1, 2, 3a, 3b.

Figure 4. Test circuit for transient test pulses (LIN)



Note Waveform per ISO 7637-2. Test Pulses 1, 2, 3a, 3b,.

Figure 5. Test circuit for transient test pulses (Lx)

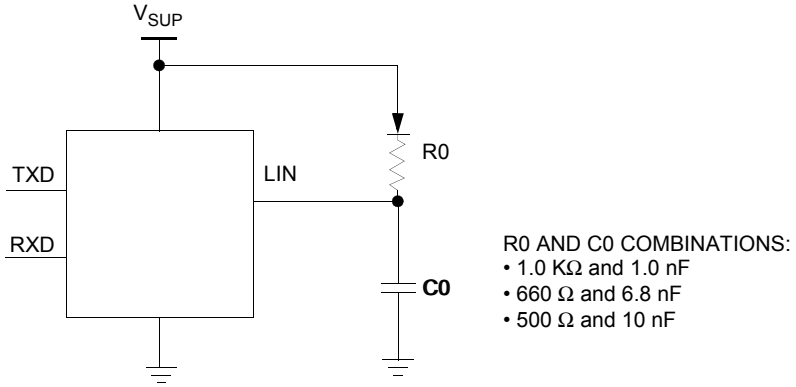


Figure 6. Test circuit for LIN timing measurements

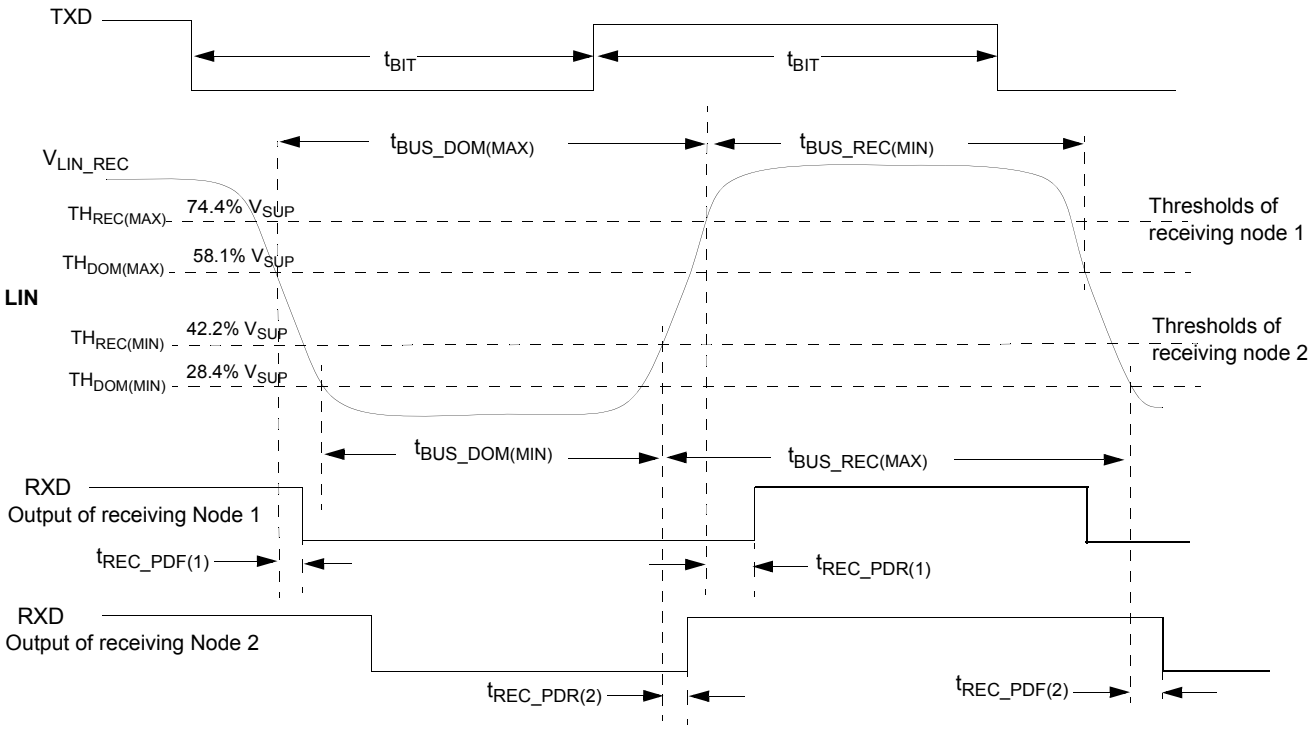


Figure 7. LIN timing measurements for normal slew rate

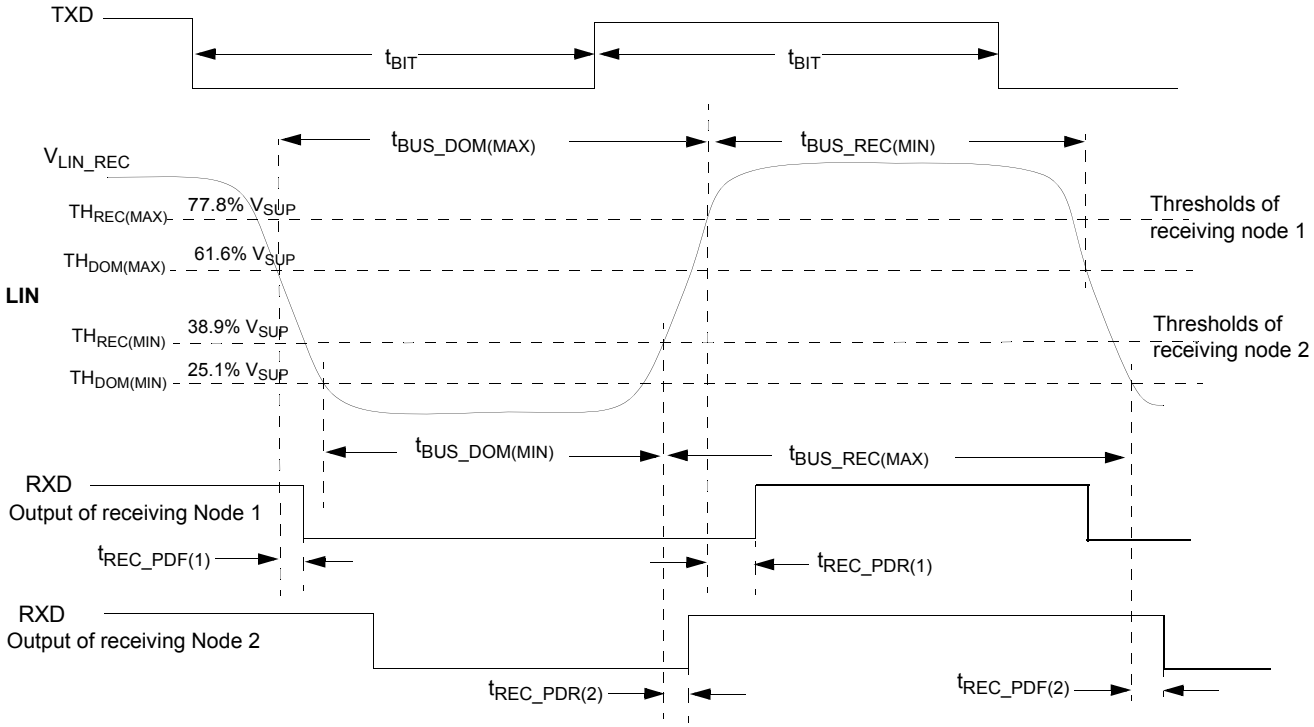


Figure 8. LIN timing measurements for slow slew rate

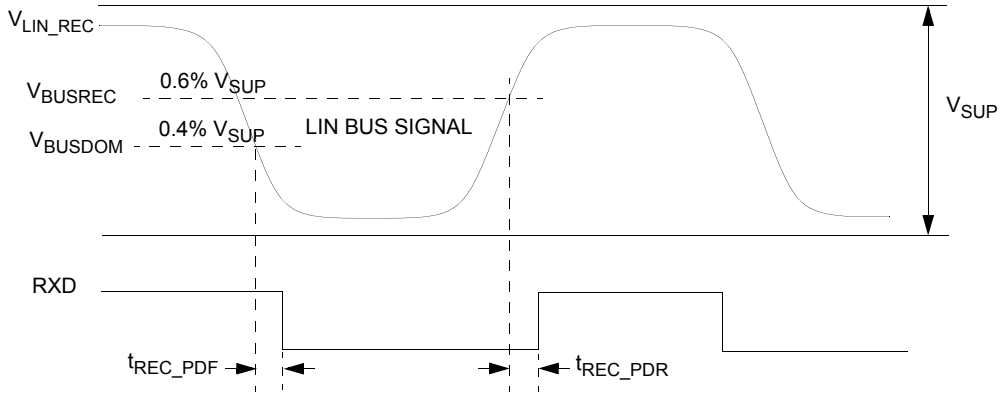


Figure 9. LIN receiver timing

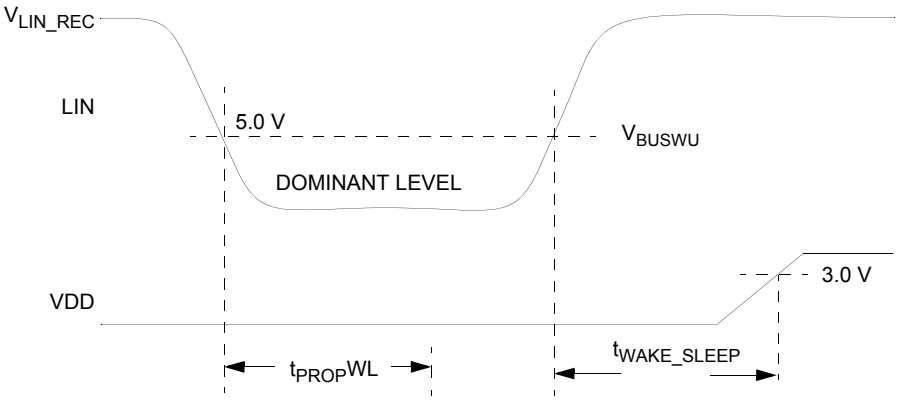


Figure 10. LIN wake-up sleep mode timing

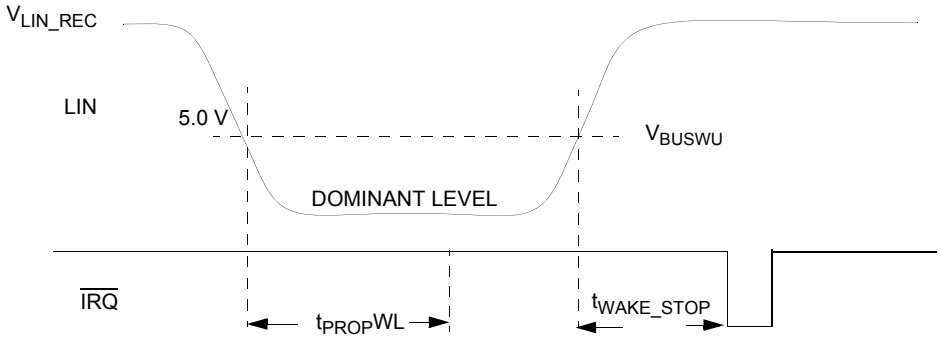


Figure 11. LIN wake-up stop mode timing

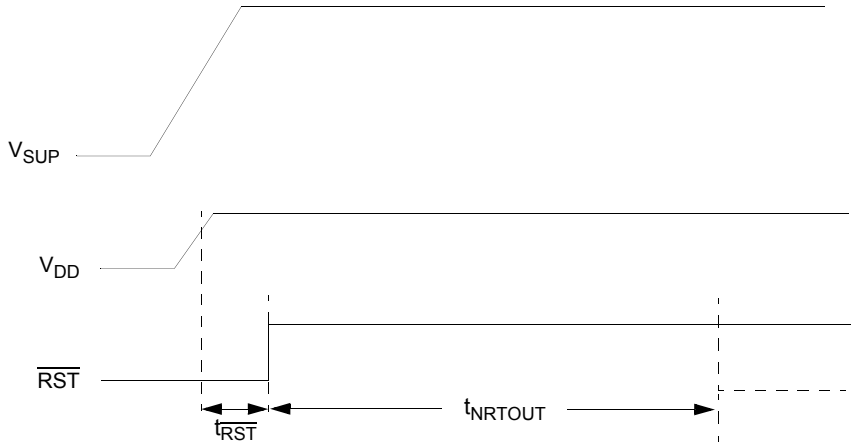


Figure 12. Power on reset and normal request timeout timing

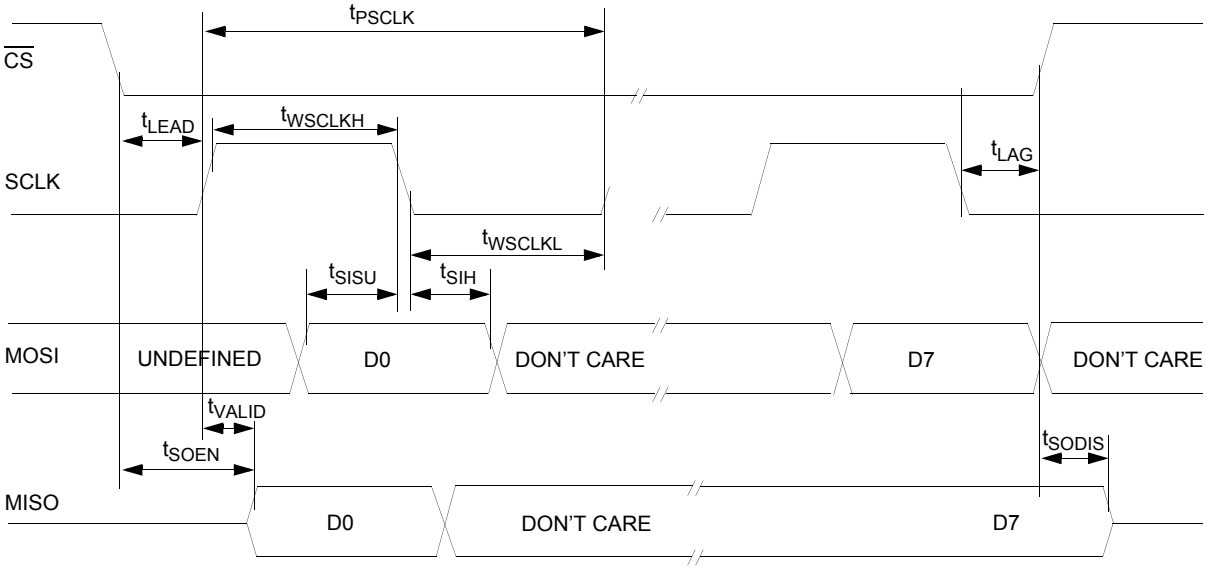


Figure 13. SPI timing characteristics

6 Functional description

6.1 Introduction

The 33912 was designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 33912 is well suited to perform relay control in applications such as a window lift, sunroof, etc. via the LIN bus. Power switches are provided on the device configured as high-side and low-side outputs. Other ports are also provided, which include a current and voltage sense port, a Hall Sensor port supply, and four wake-up capable pins. An internal voltage regulator provides power to a MCU device.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables this device to be compatible with 3-wire bus systems, where one wire is used for communication, one for battery, and one for ground.

6.2 Functional pin description

See Figure 1, 33912 simplified application diagram, page 1, for a graphic representation of the various pins referred to in the following paragraphs. Also, see the pin diagram on page 5 for a description of the pin locations in the package.

6.2.1 Receiver output pin (RXD)

The RXD pin is a digital output. It is the receiver output of the LIN interface and reports the state of the bus voltage: RXD Low when LIN bus is dominant, RXD High when LIN bus is recessive.

6.2.2 Transmitter input pin (TXD)

The TXD pin is a digital input. It is the transmitter input of the LIN interface and controls the state of the bus output (dominant when TXD is Low, recessive when TXD is High). This pin has an internal pull-up to force recessive state in case the input is left floating.

6.2.3 Lin bus pin (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is compliant to the LIN bus specification 2.0, 2.1, and SAE J2602-2. The LIN interface is only active during Normal Mode. See Table 6, Operating modes overview.

6.2.4 Serial data clock pin (SCLK)

The SCLK pin is the SPI clock input. MISO data changes on the positive transition of the SCLK. MOSI is sampled on the negative edge of the SCLK.

6.2.5 Master out slave in pin (MOSI)

The MOSI digital pin receives SPI data from the MCU. This data input is sampled on the negative edge of SCLK.

6.2.6 Master in slave out pin (MISO)

The MISO pin sends data to a SPI-enabled MCU. It is a digital tri-state output used to shift serial data to the microcontroller. Data on this output pin changes on the positive edge of the SCLK. When $\overline{CS}$ is High, this pin remains in the high-impedance state.

6.2.7 Chip select pin ($\overline{CS}$)

$\overline{CS}$ is an active low digital input. It must remain low during a valid SPI communication and allow for several devices to be connected in the same SPI bus without contention. A rising edge on $\overline{CS}$ signals the end of the transmission and the moment the data shifted in is latched. A valid transmission must consist of 8 bits only. While in STOP mode, a low-to-high level transition on this pin generates a wake-up condition for the 33912.

6.2.8 Analog multiplexer pin (ADOUT0)

The ADOUT0 pin can be configured via the SPI to allow the MCU A/D converter to read the several inputs of the Analog Multiplexer, including the VSENSE, L1, L2, L3, L4 input voltages, and the internal junction temperature.

6.2.9 Current sense amplifier pin (ADOUT1)

The ADOUT1 pin is an analog interface to the MCU A/D converter. It allows the MCU to read the output of the current sense amplifier.

6.2.10 PWM input control pin (PWMIN)

This digital input can control the high-sides and low-sides drivers in Normal Request and Normal mode. To enable PWM control, the MCU must perform a write operation to the High-side Control register (HSCR) or the Low-side Control register (LSCR). This pin has an internal 20 μA current pull-up.

6.2.11 Reset pin ($\overline{\text{RST}}$)

This bidirectional pin is used to reset the MCU in case the 33912 detects a reset condition, or to inform the 33912 the MCU has just been reset. After release of the $\overline{\text{RST}}$ pin, Normal Request mode is entered.

The $\overline{\text{RST}}$ pin is an active low filtered input and output formed by a weak pull-up and a switchable pull-down structure which allows this pin to be shorted either to V_{DD} or to GND during software development, without the risk of destroying the driver.

6.2.12 Interrupt pin ($\overline{\text{IRQ}}$)

The $\overline{\text{IRQ}}$ pin is a digital output used to signal events or faults to the MCU while in Normal and Normal Request mode or to signal a wake-up from Stop mode. This active low output transitions to high only after the interrupt is acknowledged by a SPI read of the respective status bits.

6.2.13 Watchdog configuration pin (WDCONF)

The WDCONF pin is the configuration pin for the internal watchdog. A resistor can be connected to this pin to configure the window watchdog period. When connected directly to ground, the watchdog is disabled. When this pin is left open, the watchdog period is fixed to its lower precision internal default value (150 ms typical).

6.2.14 Ground connection pins (AGND, PGND, LGND)

The AGND, PGND, and LGND pins are the Analog and Power ground pins. The AGND pin is the ground reference of the voltage regulator and the current sense module. The PGND and LGND pins are used for high current load return as in the relay-drivers and LIN interface pin.

Note: PGND, AGND, And LGND pins must be connected together.

6.2.15 Current sense amplifier input pins (ISENSEH and ISENSEL)

The ISENSEH and ISENSEL pins are the input pins of a ground compatible differential amplifier designed to be used to sense the voltage drop over a shunt resistor. The main purpose of this amplifier is to implement accurate current sensors. The gain of the differential amplifier can be set by the SPI.

6.2.16 Low-side pins (LS1 and LS2)

LS1 and LS2 are the low-side driver outputs. Those outputs are short-circuit protected and include active clamp circuitry to drive inductive loads. Due to the energy clamp voltage on this pin, it can raise above the battery level when switched off. The switches are controlled through the SPI and can be configured to respond to a signal applied to the PWMIN input pin. Both low-side switches are protected against overheating. In case of VS1 disconnection and the low-sides are still supplied by V_{BAT} through a load, both low-sides has a VDS voltage equal to the clamping value, as stated in the specification.

6.2.17 Digital/analog pins (L1, L2, L3, and L4)

The Lx pins are multi purpose inputs. They can be used as digital inputs, which can be sampled by reading the SPI and used for wake-up when 33912 is in Low-power mode or used as analog inputs for the analog multiplexer. When used to sense voltage outside the module, a 33 kΩ series resistor must be used on each input.

When used as wake-up inputs L1-L4 can be configured to operate in cyclic-sense mode. In this mode one or both of the high-side switches are configured to be periodically turned on and sample the wake-up inputs. If a state change is detected between two cycles a wake-up is initiated. The 33912 can also wake-up from Stop or Sleep by a simple state change on L1-L4.

When used as analog inputs, the voltage present on the Lx pins is scaled down by an selectable internal voltage divider and can be routed to the ADOUT0 output through the analog multiplexer. When an Lx input is not selected in the analog multiplexer, the voltage divider is disconnected from this input.

Note: If an Lx input is selected in the analog multiplexer, it is disabled as a digital input and remains disabled in Low-power mode. No wake-up feature is available in this condition.

6.2.18 High-side output pins (HS1 and HS2)

These two high-side switches are able to drive loads such as relays or lamps. Their structures are connected to the VS2 supply pin. The pins are short-circuit protected and both outputs are also protected against overheating. HS1 and HS2 are controlled by the SPI and can respond to a signal applied to the PWMIN input pin. HS1 and HS2 outputs can also be used during low-power mode for the cyclic-sense of the wake inputs.

6.2.19 Power supply pins (VS1 and VS2)

Those are the battery level voltage supply pins. In an application, VS1 and VS2 pins must be protected against reverse battery connection and negative transient voltages with external components. These pins sustain standard automotive voltage conditions such as a load dump at 40 V. The high-side switches (HS1 and HS2) are supplied by the VS2 pin. All other internal blocks are supplied by the VS1 pin.

6.2.20 Voltage sense pin (VSENSE)

This input can be connected directly to the battery line. It is protected against battery reverse connection. The voltage present in this input is scaled down by an internal voltage divider, and can be routed to the ADOUT0 output pin and used by the MCU to read the battery voltage. The ESD structure on this pin allows for excursion up to +40 V and down to -27 V, allowing this pin to be connected directly to the battery line. It is strongly recommended to connect a 10 kΩ resistor in series with this pin for protection purposes.

6.2.21 Hall sensor switchable supply pin (HVDD)

This pin provides a switchable supply for external hall sensors. While in Normal mode, this current limited output can be controlled through the SPI. The HVDD pin needs to be connected to an external capacitor to stabilize the regulated output voltage.

6.2.22 +5.0 V main regulator output pin (VDD)

An external capacitor has to be placed on the VDD pin to stabilize the regulated output voltage. The VDD pin is intended to supply a microcontroller. The pin is current limited against shorts to GND and overtemperature protected. During Stop mode, the voltage regulator does not operate with its full drive capabilities and the output current is limited. During Sleep mode, the regulator output is completely shutdown.