Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

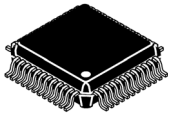
NXP Semiconductors
Advance Information

Document Number: MC34FS6407-08
Rev. 3.0, 7/2016

Power system basis chip with high speed can transceiver

FS6407
FS6408

POWER SYSTEM BASIS CHIP



AE SUFFIX (PB-FREE)
98ASA00173D
48-PIN LQFP-EP

The FS6407/FS6408 SMARTMOS devices area multi-output, power supply, integrated circuit, including HSCAN transceiver, dedicated to the industrial market.

Multiple switching and linear voltage regulators, including low-power mode (32 μA) are available with various wake-up capabilities. An advanced power management scheme is implemented to maintain high efficiency over wide input voltages (down to 2.7 V) and wide output current ranges (up to 1.5 A).

The FS6407/FS6408 include enhanced safety features, with multiple fail-safe outputs, becoming a full part of a safety oriented system partitioning, to reach a high integrity safety level.

The built-in enhanced high-speed CAN interface fulfills the ISO11898-2 and -5 standards.

Features

- Highly flexible SMPS pre-regulator, allowing two topologies: non-inverting buck-boost and standard buck
- Switching mode power supply (SMPS) dedicated to MCU core supply, from 1.2 V to 3.3 V delivering up to 1.5 A
- Multiple wake-up sources in low-power mode: CAN and/or IOs
- Six configurable I/Os
- Linear voltage regulator dedicated to auxiliary functions, or to a sensor supply (V_{CCA} tracker or independent), 5.0 V or 3.3 V
- Linear voltage regulator dedicated to MCU A/D reference voltage or I/Os supply (V_{CCA}), 5.0 V or 3.3 V

Applications

- Automation (PLC, robotics)
- Building control (lift)
- Transportation (mobile machine, military)
- Medical (Infusion pump, stairs)

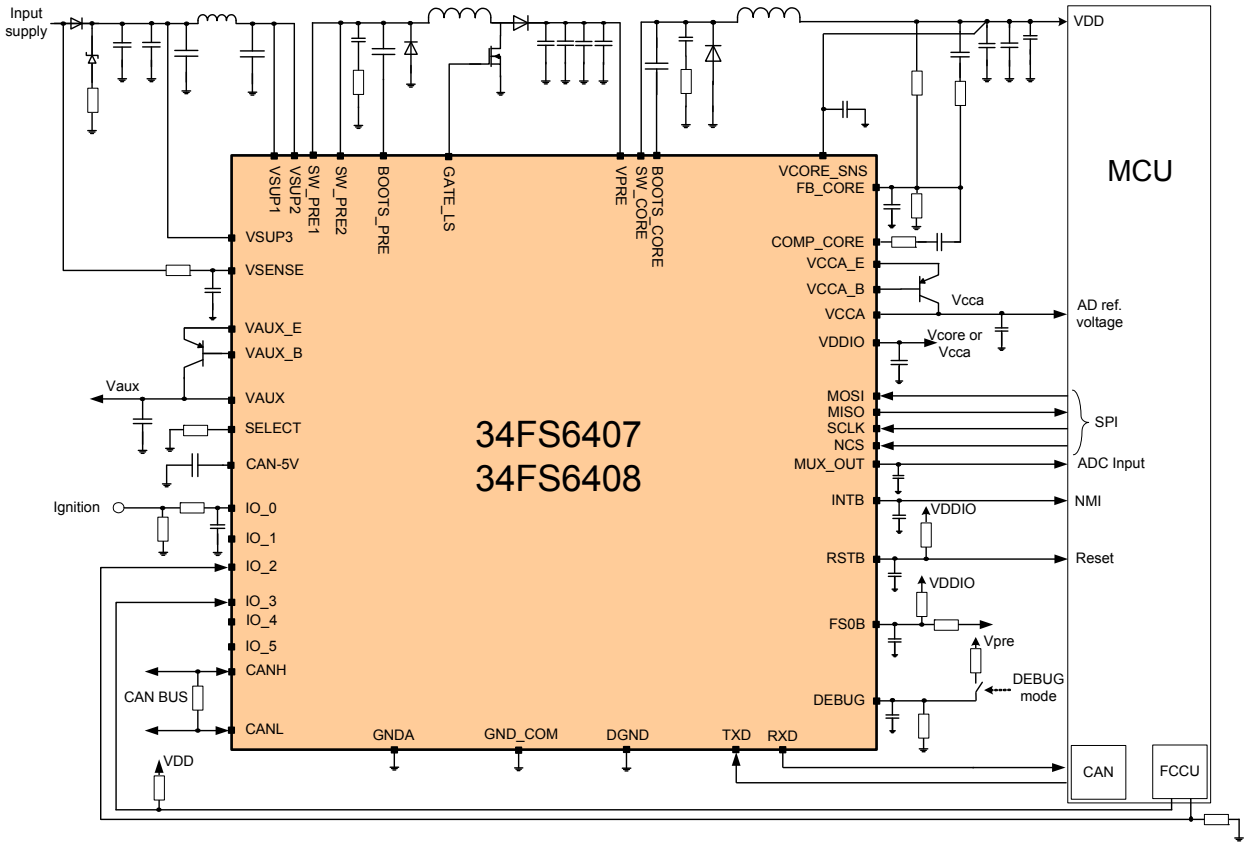


Figure 1. FS6407/FS6408 simplified application diagram - buck boost configuration

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

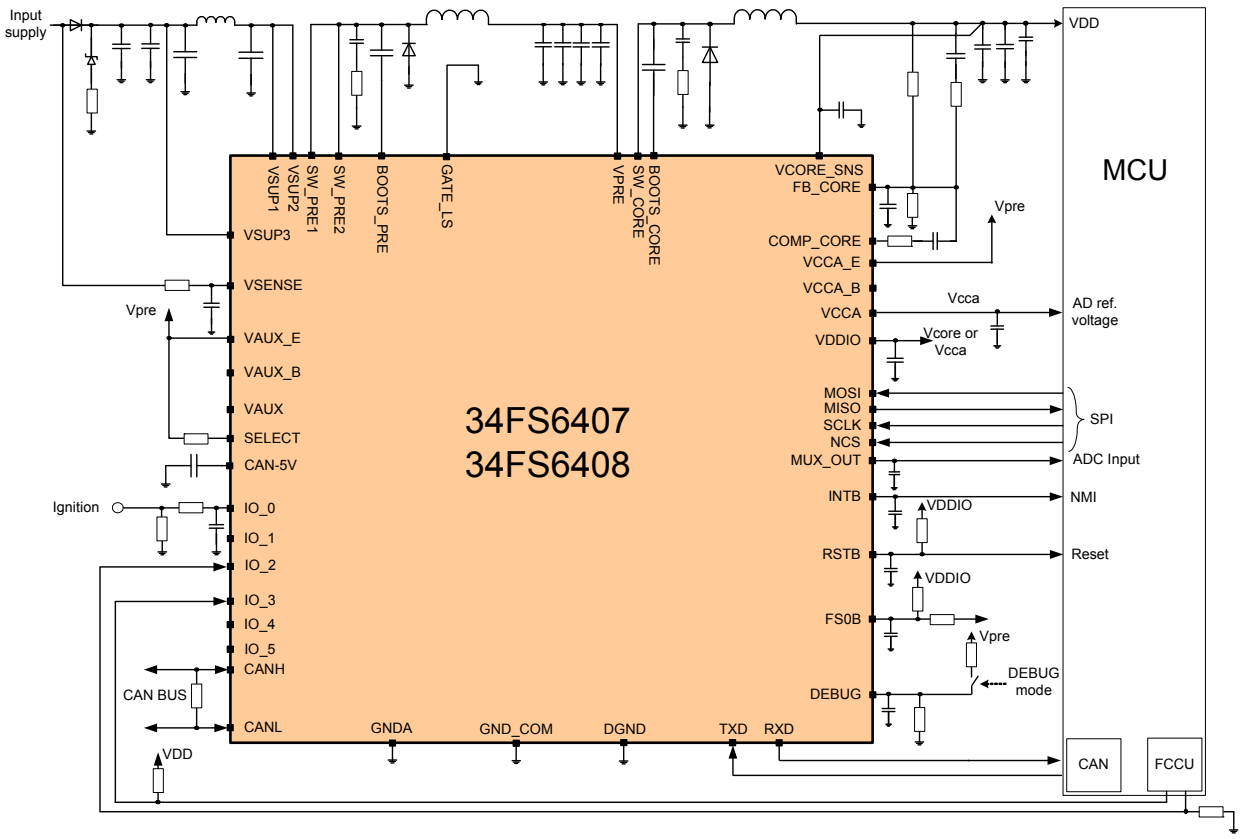


Figure 2. Simplified application diagram - buck configuration, V_{AUX} not used, V_{CCA} = 100 mA

1 Orderable parts

Table 1. Orderable part variations

Part number	Temperature (T_A)	Package	CAN	Vcore	Notes
MC34FS6407NAE	-40 °C to 125 °C	48-pin LQFP exposed pad	1	0.8 A	(1)
MC34FS6408NAE				1.5 A	

Notes

1. To order parts in Tape & Reel, add the R2 suffix to the part number.

2 Internal block diagram

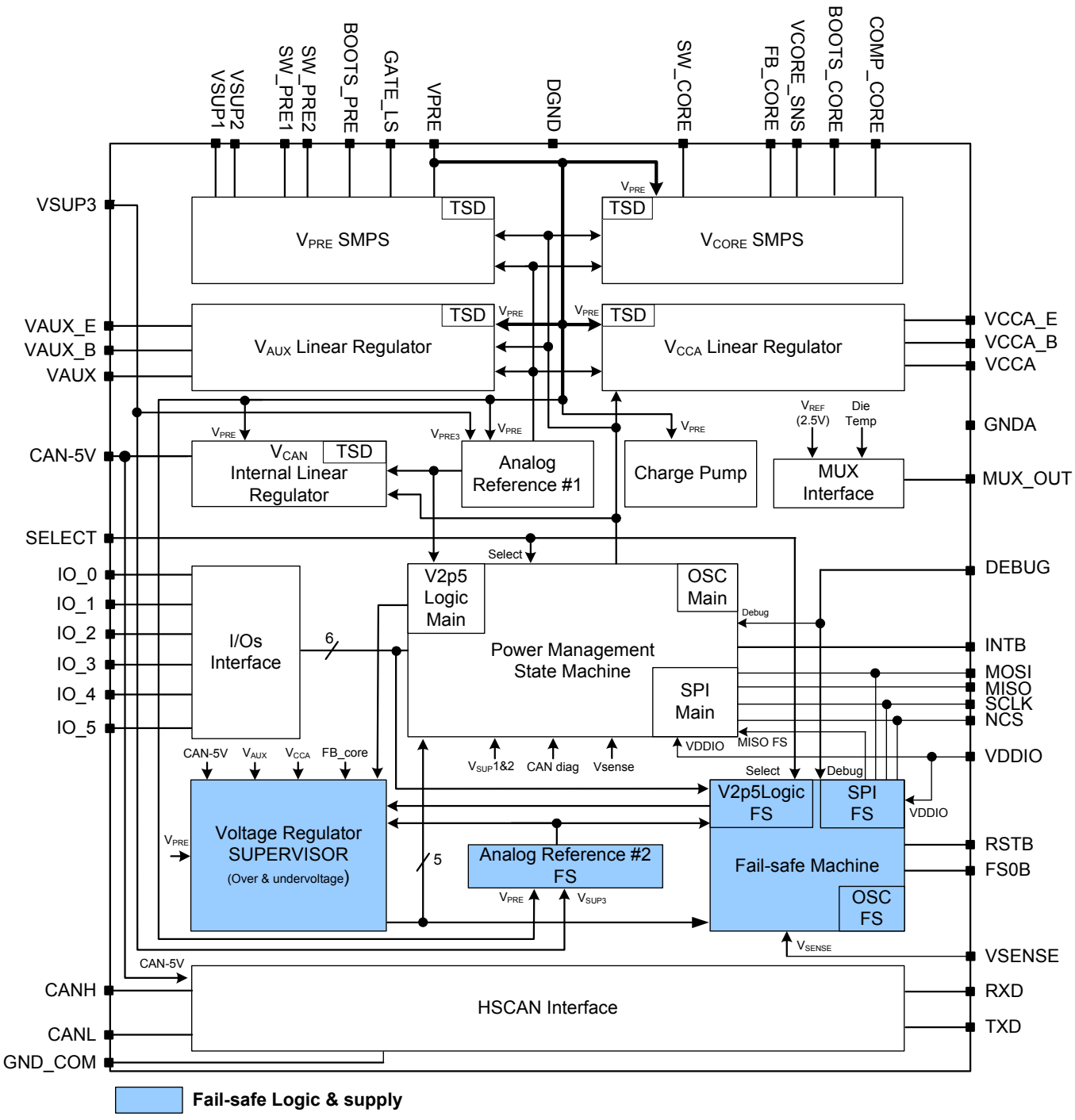


Figure 3. FS6407/FS6408 simplified internal block diagram

3 Pin connections

3.1 Pinout diagram for FS6407/FS6408

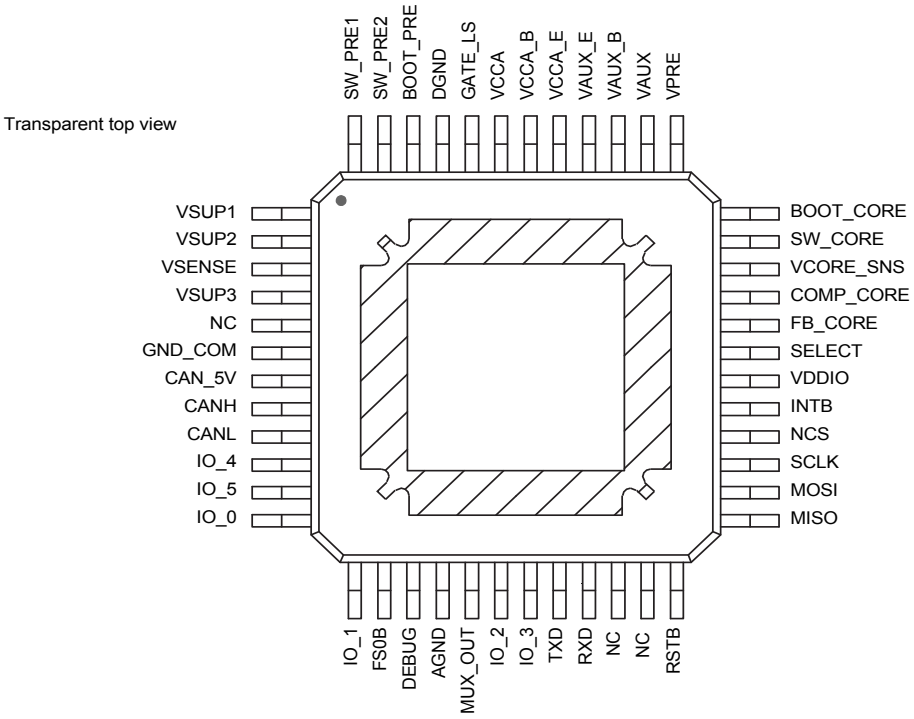


Figure 4. FS6407/FS6408 pinout

3.2 Pin definitions

A functional description of each pin can be found in the functional pin description section beginning on page 22.

Table 2. FS6407/FS6408 pin definition

Pin Number	Pin Name	Type	Definition
1	VSUP1	A_IN	Power supply of the device. An external reverse battery protection diode in series is mandatory
2	VSUP2	A_IN	Second power supply. Protected by the external reverse battery protection diode used for VSUP1. VSUP1 and VSUP2 must be connected together externally.
3	VSENSE	A_IN	Sensing of the battery voltage. Must be connected prior to the reverse battery protection diode.
4	VSUP3	A_IN	Third power supply dedicated to the device supply. Protected by the external reverse battery protection diode used for VSUP1. Must be connected between the reverse protection diode and the input PI filter.
5, 22, 23	NC	N/A	Not connected. Pins must be left open.
6	GND_COM	GND	Dedicated ground for CAN
7	CAN_5V	A_OUT	Output voltage for the embedded CAN interface
8	CANH	A_IN/OUT	HSCAN output High
9	CANL	A_IN/OUT	HSCAN output Low

Table 2. FS6407/FS6408 pin definition (continued)

Pin Number	Pin Name	Type	Definition
10 11	IO_4:5	D_IN A_OUT	Can be used as digital input (load dump proof) with wake-up capability or as an output gate driver **Digital input**: Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes. **Wake-up capability:** Can be selectable to wake-up on a rising or falling edge, or on a transition **Output gate driver:** Can drive a logic level low-side NMOS transistor. Controlled by the SPI.
12 13	IO_0:1	A_IN D_IN	Can be used as analog or digital input (load dump proof) with wake-up capability (selectable) **Analog input**: Pin status can be read through the MUX output pin **Digital input:** Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes **Wake-up capability:** Can be selectable to wake-up on a rising or falling edge, or on a transition **Rk:** For safety purposes, IO_1 can also be used to monitor the middle point of a redundant resistor bridge connected on V_{CORE} (in parallel to the one used to set the Vcore voltage).
14	FS0B	D_OUT	Output of the safety block (active low). The pin is asserted low at start-up and when a fault condition is detected. Open drain structure.
15	DEBUG	D_IN	Debug mode entry input
16	AGND	GROUND	Analog ground connection
17	MUX_OUT	A_OUT	Multiplexed output to be connected to an MCU ADC input. Selection of the analog parameter is available at MUX-OUT through the SPI.
18 19	IO_2:3	D_IN	Digital input pin with wake-up capability (logic level compatible) **Digital INPUT**: Pin status can be read through the SPI. Can be used to monitor error signals from MCU for safety purposes. **Wake-up capability:** Can be selectable to wake-up on a rising or falling edge, or on a transition.
20	TXD	D_IN	Transceiver input from the MCU which controls the state of the HSCAN bus. Internal pull-up to VDDIO. Internal pull-up to VDDIO.
21	RXD	D_OUT	Receiver output which reports the state of the HSCAN bus to the MCU
24	RSTB	D_OUT	This output is asserted low when the safety block reports a failure. The main function is to reset the MCU. Reset input voltage is also monitored in order to detect external reset and fault condition. Open drain structure.
25	MISO	D_OUT	SPI bus. Master Input Slave Output
26	MOSI	D_IN	SPI bus. Master Output Slave Input
27	SCLK	D_IN	SPI Bus. Serial clock
28	NCS	D_IN	No Chip Select (Active low)
29	INTB	D_OUT	This output pin generates a low pulse when an Interrupt condition occurs. Pulse duration is configurable. Internal pull-up to VDDIO.
30	VDDIO	A_IN	Input voltage for MISO output buffer. Allows voltage compatibility with MCU I/Os.
31	SELECT	D_IN	Hardware selection pin for VAUX and VCCA output voltages
32	FB_CORE	A_IN	VCORE voltage feedback. Input of the error amplifier.
33	COMP_CORE	A_IN	Compensation network. Output of the error amplifier.
34	VCORE_SNS	A_IN	VCORE output voltage sense
35	SW_CORE	A_IN	VCORE switching point
36	BOOT_CORE	A_IN/OUT	Bootstrap capacitor for VCORE internal NMOS gate drive
37	VPRE	A_OUT	VPRE output voltage
38	VAUX	A_OUT	VAUX output voltage. External PNP ballast transistor. Collector connection
39	VAUX_B	A_OUT	VAUX voltage regulator. External PNP ballast transistor. Base connection
40	VAUX_E	A_OUT	VAUX voltage regulator. External PNP ballast transistor. Emitter connection
41	VCCA_E	A_OUT	VCCA voltage regulator. External PNP ballast transistor. Emitter connection
42	VCCA_B	A_OUT	VCCA voltage regulator. External PNP ballast transistor. Base connection

Table 2. FS6407/FS6408 pin definition (continued)

Pin Number	Pin Name	Type	Definition
43	VCCA	A_OUT	VCCA output voltage. External PNP ballast transistor. Collector connection
44	GATE_LS	A_OUT	Low-side MOSFET gate drive for “Non-inverting Buck-boost” configuration
45	DGND	GROUND	Digital ground connection
46	BOOT_PRE	A_IN/OUT	Bootstrap capacitor for the VPRE internal NMOS gate drive
47	SW_PRE2	A_IN	Second pre-regulator switching point
48	SW_PRE1	A_IN	First pre-regulator switching point

4 General product characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings				
$V_{SUP1/2/3}$	DC Voltage at Power Supply Pins	-1.0 to 40	V	(2)
V_{SENSE}	DC Voltage at Battery Sense Pin	-14 to 40	V	
$V_{SW1,2}$	DC Voltage at SW_PRE1 and SW_PRE2 Pins	-1.0 to 40	V	
V_{PRE}	DC Voltage at VPRE Pin	-0.3 to 8	V	
V_{GATE_LS}	DC Voltage at Gate_LS pin	-0.3 to 8	V	
V_{BOOT_PRE}	DC Voltage at BOOT_PRE pin	-1.0 to 50	V	
V_{SW_CORE}	DC Voltage at SW_CORE pin	-1.0 to 8.0	V	
V_{CORE_SNS}	DC Voltage at VCORE_SNS pin	0.0 to 8.0	V	
V_{BOOT_CORE}	DC Voltage at BOOT_CORE pin	0.0 to 15	V	
V_{FB_CORE}	DC Voltage at FB_CORE pin	-0.3 to 2.5	V	
V_{COMP_CORE}	DC Voltage at COMP_CORE pin	-0.3 to 2.5	V	
$V_{AUX\_E,B}$	DC Voltage at VAUX_E, VAUX_B pin	-0.3 to 40	V	
V_{AUX}	DC Voltage at VAUX pin	-2.0 to 40	V	
$V_{CCA\_B,E}$	DC Voltage at VCCA_B, VCCA_E pin	-0.3 to 8.0	V	
V_{CCA}	DC Voltage at VCCA pin	-0.3 to 8.0	V	
V_{DDIO}	DC Voltage at VDDIO	-0.3 to 8.0	V	
V_{FS0}	DC Voltage at FS0B (with ext R mandatory)	-0.3 to 40	V	
V_{DEBUG}	DC Voltage at DEBUG	-0.3 to 40	V	
$V_{IO\_0,1,4,5}$	DC Voltage at IO_0:1; 4:5 (with ext R = 5.1 kΩ in series mandatory)	-0.3 to 40	V	
V_{DIG}	DC Voltage at INTB, RSTB, MISO, MOSI, NCS, SCLK, MUX_OUT, RXD, TXD, IO_2, IO_3	-0.3 to V_{DDIO}+0.3	V	
V_{SELECT}	DC Voltage at SELECT	-0.3 to 8.0	V	
V_{BUS_CAN}	DC Voltage on CANL, CANH	-27 to 40	V	
V_{CAN_5V}	DC Voltage on CAN_5 V	-0.3 to 8.0	V	
$I\_IO_{0,\ 1,\ 4,\ 5}$	IOs Maximum Current Capability(IO_0, IO_1, IO_4, IO_5)	-5.0 to 5.0	mA	

Notes

2. All V_{SUPS} ($V_{SUP1/2/3}$) must be connected to the same supply (Figure 49)

Table 3. Maximum ratings (continued)

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
	ESD Voltage			
	Human Body Model (JESD22/A114) - 100 pF, 1.5 kΩ			
$V_{ESD-HBM1}$	• All pins (ESD Class 2)	±2.0	kV	
$V_{ESD-HBM2}$	• VSUP1,VSUP2, VSUP3, VSENSE, VAUX, IO_0:1, IO_4:5,FS0B, DEBUG (ESD Class 3A)	±4.0	kV	
$V_{ESD-HBM3}$	• CANH, CANL (ESD Class 3A)	±6.0	kV	
	Charge Device Model (JESD22/C101):			
$V_{ESD-CDM1}$	• All Pins (ESD Class 2)	±500	V	
$V_{ESD-CDM2}$	• Corner Pins (ESD Class 2)	±750	V	
	System level ESD (Gun Test)			(3)
	• VSUP1, VSUP2, VSUP3, VSENSE, VAUX, IO_0:1, IO_4:5, FS0B			
$V_{ESD-GUN1}$	330 Ω / 150 pF Unpowered According to IEC61000-4-2:	±8.0	kV	
$V_{ESD-GUN2}$	330 Ω / 150 pF Unpowered According to OEM CAN, FLexray Conformance	±8.0	kV	
$V_{ESD-GUN3}$	2.0 kΩ / 150 pF Unpowered According to ISO10605.2008	±8.0	kV	
$V_{ESD-GUN4}$	2.0 kΩ / 330 pF Powered According to ISO10605.2008	±8.0	kV	
	• CANH, CANL			
$V_{ESD-GUN5}$	330 Ω / 150 pF Unpowered According to IEC61000-4-2:	±15.0	kV	
$V_{ESD-GUN6}$	330 Ω / 150 pF Unpowered According to OEM CAN, FLexray Conformance	±12.0	kV	
$V_{ESD-GUN7}$	2.0 kΩ / 150 pF Unpowered According to ISO10605.2008	±15.0	kV	
$V_{ESD-GUN8}$	2.0 kΩ / 330 pF Powered According to ISO10605.2008	±15.0	kV	
Thermal ratings				
T_A	Ambient Temperature	-40 to 125	°C	
T_J	Junction Temperature	-40 to 150	°C	
T_{STG}	Storage Temperature	-55 to 150	°C	
Thermal resistance				
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	30	°C/W	(4)
$R_{\theta JCTOP}$	Thermal Resistance Junction to Case Top	24.2	°C/W	(5)
$R_{\theta JCBOTTOM}$	Thermal Resistance Junction to Case Bottom	0.9	°C/W	(6)

Notes

3. Compared to AGND.
4. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC - 883 Method 1012.1).
6. Thermal resistance between the die and the solder par on the bottom of the packaged based on simulation without any interface resistance.

4.2 Static electrical characteristics

Table 4. Operating range

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Power supply						
I_{SUP123}	Power Supply Current in Normal Mode (V_{SUP} > $V_{SUP\_UV\_7}$)	2.0	–	13.0	mA	
I_{SUP3}	Power Supply Current for VSUP3 in Normal Mode (V_{SUP} > $V_{SUP\_UV\_7}$)	–	3.5	5.0	mA	
I_{SUP_LPOFF1}	Power Supply Current in LPOFF (V_{SUP} = 14 V at T_A = 25 °C)	–	32	–	µA	
I_{SUP_LPOFF2}	Power Supply Current in LPOFF (V_{SUP} = 18 V at T_A = 80 °C)	–	42	60	µA	
V_{SNS_UV}	Power Supply Undervoltage Warning	–	8.5	–	V	
$V_{SNS\_UV\_HYST}$	Power Supply Undervoltage Warning Hysteresis	0.1	–	–	V	
$V_{SUP\_UV\_7}$	Power Supply Undervoltage Lockout (power-up)	7.0	–	8.0	V	
$V_{SUP\_UV\_5}$	Power Supply Undervoltage Lockout (power-up)	–	–	5.6	V	
$V_{SUP\_UV\_L}$	Power Supply Undervoltage Lockout (falling - Boost config.)	–	–	2.7	V	
$V_{SUP\_UV\_L\_B}$	Power Supply Undervoltage Lockout (falling - Buck config.)	–	–	4.6	V	(7)
$V_{SUP\_UV\_HYST}$	Power Supply Undervoltage Lockout Hysteresis	–	0.1	–	V	(8)
V_{PRE} voltage pre-regulator						
V_{PRE}	V_{PRE} Output Voltage • Buck mode (V_{SUP} > $V_{SUP\_UV\_7}$) • Buck mode ($V_{SUP\_UV\_7}$ ≥ V_{SUP} ≥ 4.6 V) • Boost mode (V_{SUP} ≥ 2.7 V)	6.25 $V_{PRE\_UV\_4P3}$ 6.0	– V_{SUP} - R_{DSON_PRE} * I_{PRE} –	6.75 – 7.0	V	
I_{PRE}	V_{PRE} Maximum Output Current Capability • Buck or Boost with V_{SUP} > $V_{SUP\_UV\_7}$ • Buck with $V_{SUP\_UV\_7}$ ≥ V_{SUP} ≥ 4.6 V • Boost with $V_{SUP\_UV\_7}$ ≥ V_{SUP} ≥ 6.0 V • Boost with 6.0 V ≥ V_{SUP} ≥ 4.0 V • Boost with 4.0 V ≥ V_{SUP} ≥ 2.7 V	 – 0.5 – 1.0 0.3	 – – – – –	 1.7 1.7 1.7 – –	A	(8)
I_{PRE_LPOFF}	V_{PRE} Maximum Output Current Capability in LPOFF at low V_{SUP} voltage • Buck with $V_{SUP\_UV\_7}$ ≥ V_{SUP} ≥ 4.6 V • Boost with $V_{SUP\_UV\_7}$ ≥ V_{SUP} ≥ 6.0 V • Boost with 6.0 V ≥ V_{SUP} ≥ 4.0 V • Boost with 4.0 V ≥ V_{SUP} ≥ 2.7 V	 0.05 1.7 1.0 0.3	 – – – –	 – – – –	A	(8)
I_{PRE_LIM}	V_{PRE} Output Current Limitation	3.5	–	–	A	
I_{PRE_OC}	V_{PRE} Overcurrent Detection Threshold (in buck mode only)	5.0	–	–	A	
V_{PRE_UV}	V_{PRE} Undervoltage Detection Threshold (Falling)	5.5	–	6.0	V	

Notes

7. $V_{SUP\_UV\_L\_B}$ = $V_{PRE\_UV\_4P3}$ + R_{DSON_PRE} * I_{PRE}
8. Guaranteed by design

Table 4. Operating range (continued)

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{PRE} voltage pre-regulator (continued)						
$V_{PRE\_UV\_HYST}$	V_{PRE} Undervoltage Hysteresis	0.05	–	0.15	V	(9)
$V_{PRE\_UV\_4P3}$	V_{PRE} Shut-off Threshold (Falling - buck and buck/boost)	4.2	–	4.5	V	
$V_{PRE\_UV\_4P3\_HYST}$	V_{PRE} Shut-off Hysteresis	0.05	–	0.15	V	(9)
R_{DSON_PRE}	V_{PRE} Pass Transistor On Resistance	–	–	200	mΩ	
L_{IR_VPRE}	V_{PRE} Line Regulation	–	20	–	mV	(9)
LOR_{VPRE_BUCK}	V_{PRE} Load Regulation for C_{OUT} = 57 µF • I_{PRE} from 50 mA to 2.0 A - Buck mode	–	100	–	mV	(9)
LOR_{VPRE_BOOST}	V_{PRE} Load Regulation for C_{OUT} = 57 µF • I_{PRE} from 50 mA to 2.0 A - Boost mode	–	500	–	mV	(9)
$V_{PRE\_LL\_H}$ $V_{PRE\_LL\_L}$	V_{PRE} Pulse Skipping Thresholds	– –	200 180	– –	mV	
T_{WARN_PRE}	V_{PRE} Thermal Warning Threshold	–	105	–	°C	
T_{SD_PRE}	V_{PRE} Thermal Shutdown Threshold	160	–	–	°C	
$T_{SD\_PRE\_HYST}$	V_{PRE} Thermal Shutdown Hysteresis	–	10	–	°C	(9)
$V_{G\_LS\_OH}$	LS Gate Driver High Output Voltage (I_{OUT} = 50 mA)	V_{PRE}-1	–	V_{PRE}	V	
$V_{G\_LS\_OL}$	LS Gate driver Low Level (I_{OUT} = 50 mA)	–	–	0.5	V	
V_{core} voltage regulator						
V_{CORE_FB}	V_{CORE} Feedback Input Voltage	0.784	0.8	0.816	V	
I_{CORE}	V_{CORE} Output Current Capability in Normal Mode • FS6407N • FS6408N	 – –	 – –	 0.8 1.5	A	
I_{CORE_LIM}	V_{CORE} Output Current Limitation • FS6407N • FS6408N	 1 1.8	 – –	 2 3.5	A	
R_{DSON_CORE}	V_{CORE} Pass Transistor On Resistance	–	–	200	mΩ	
$LOR_{VCORE\_1.2}$	V_{CORE} Transient Load regulation - 1.2 V range	-60	–	60	mV	(9), (10)
$LOR_{VCORE\_3.3}$	V_{CORE} Transient Load regulation - 3.3 V range	-100	–	100	mV	(9), (10)
$V_{CORE\_LL\_H}$ $V_{CORE\_LL\_L}$	V_{CORE} Pulse Skipping Thresholds	– –	180 160	– –	mV	
T_{WARN_CORE}	V_{CORE} Thermal Warning Threshold	–	105	–	°C	
T_{SD_CORE}	V_{CORE} Thermal Shutdown Threshold	160	–	–	°C	
$T_{SD\_CORE\_HYST}$	V_{CORE} Thermal Shutdown Hysteresis	–	10	–	°C	(9)

Notes

9. Guaranteed by design
10. C_{OUT} = 40 µF, I_{CORE} = 10 mA to 1.5 A, $dI_{CORE}/dt \leq 2.0$ A/µs

Table 4. Operating range (continued)

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{CCA} voltage regulator						
V_{CCA}	V_{CCA} Output Voltage • 5.0 V config. with Internal ballast at 100 mA • 5.0 V config with external ballast at 200 mA • 5.0 V config with external ballast at 300 mA • 3.3 V config with Internal ballast at 100 mA • 3.3 V config with external ballast at 200 mA • 3.3 V config with external ballast at 300 mA	 4.95 4.9 4.85 3.2505 3.234 3.201	 5.0 5.0 5.0 3.3 3.3 3.3	 5.05 5.1 5.15 3.3495 3.366 3.399	V	(11)
I_{CCA_IN}	V_{CCA} Output Current (int. MOSFET)	–	–	100	mA	
I_{CCA_OUT}	V_{CCA} Output Current (external PNP)	–	–	300	mA	
$I_{CCA\_LIM\_INT}$	V_{CCA} Output Current Limitation (int. MOSFET)	100	–	675	mA	
$I_{CCA\_LIM\_OUT}$	V_{CCA} Output Current Limitation (external PNP)	300	–	675	mA	
$I_{CCA\_LIM\_FB}$	V_{CCA} Output Current Limitation Foldback	80	–	200	mA	
$V_{CCA\_LIM\_FB}$	V_{CCA} Output Voltage Foldback Threshold	0.5	–	1.1	V	
$V_{CCA\_LIM\_HYST}$	V_{CCA} Output Voltage Foldback Hysteresis	0.03	–	0.3	V	
$I_{CCA\_BASE\_SC}$ $I_{CCA\_BASE\_SK}$	V_{CCA} Base Current Capability	– 20	– –	30 –	mA	
T_{WARN_CCA}	V_{CCA} Thermal Warning Threshold (int. MOSFET only)	–	105	–	°C	
TSD_{CCA}	V_{CCA} Thermal Shutdown Threshold (int. MOSFET only)	160	–	–	°C	
TSD_{CCA_HYST}	V_{CCA} Thermal Shutdown Hysteresis	–	10	–	°C	(12)
$LORT_{VCCA}$	V_{CCA} Transient Load Regulation • I_{CCA} = 10 mA to 100 mA (internal MOSFET) • I_{CCA} = 10 mA to 300 mA (external ballast)	–	–	1.0	%	(12)

Notes

11. External PNP gain within 150 to 450
12. Guaranteed by design.

Table 4. Operating range (continued)

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Vaux voltage regulator						
V_{AUX_5}	V_{AUX} Output Voltage (5.0 V configuration)	4.85	5.0	5.15	V	
V_{AUX_33}	V_{AUX} Output Voltage (3.3 V configuration)	3.2	3.3	3.4	V	
V_{AUX_TRK}	V_{AUX} Tracking Error (V_{AUX_5} and V_{AUX_33})	-15	–	+15	mV	
I_{AUX_OUT}	V_{AUX} Output Current	–	–	300	mA	
I_{AUX_LIM}	V_{AUX} Output Current Limitation	300	–	700	mA	
$I_{AUX\_LIM\_FB}$	V_{AUX} Output Current Limitation Foldback	100	–	530	mA	
$V_{AUX\_LIM\_FB}$	V_{AUX} Output Voltage Foldback Threshold	0.5	–	1.1	V	
$V_{AUX\_LIM\_HYST}$	V_{AUX} Output Voltage Foldback Hysteresis	0.03	–	0.3	V	
$I_{AUX\_BASE\_SC}$ $I_{AUX\_BASE\_SK}$	V_{AUX} Base Current Capability	– 7.0	– –	-7.0 –	mA	
TSD_{AUX}	V_{AUX} Thermal Shutdown Threshold	160	–	–	°C	
TSD_{AUX_HYST}	V_{AUX} Thermal Shutdown Hysteresis	–	10	–	°C	(13)
LOR_{VAUX}	V_{AUX} Static Load Regulation (I_{AUX_OUT} = 10 mA to 300 mA)	–	15	–	mV	(13)
$LORT_{VAUX}$	V_{AUX} Transient Load Regulation • I_{AUX_OUT} = 10 mA to 300 mA	–	–	1.0	%	(13)
CAN_5V voltage regulator						
V_{CAN}	V_{CAN} Output Voltage V_{SUP} > 6.0 V in Buck mode V_{SUP} > $V_{SUP\_UV\_L}$ in Boost mode	4.8	5.0	5.2	V	
I_{CAN_OUT}	V_{CAN} Output Current	–	–	100	mA	
I_{CAN_LIM}	V_{CAN} Output Current Limitation	100	–	250	mA	
TSD_{CAN}	V_{CAN} Thermal Shutdown Threshold	160	–	–	°C	
TSD_{CAN_HYST}	V_{CAN} Thermal Shutdown Hysteresis	–	10	–	°C	(13)
V_{CAN_UV}	V_{CAN} Undervoltage Detection Threshold	4.25	–	4.8	V	
$V_{CAN\_UV\_HYST}$	V_{CAN} Undervoltage Hysteresis	0.07	–	0.22	V	
V_{CAN_OV}	V_{CAN} Overvoltage Detection Threshold	5.2	–	5.55	V	
$V_{CAN\_OV\_HYST}$	V_{CAN} Overvoltage Hysteresis	0.07	–	0.22	V	
LOR_{VCAN}	V_{CAN} Load Regulation (from 0 to 50 mA)	–	100	–	mV	(13)

Notes
13. Guaranteed by design.

Table 4. Operating range (continued)

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Fail-safe machine voltage supervisor						
V_{PRE_OV}	V_{PRE} Overvoltage Detection Threshold	7.2	–	8.0	V	
$V_{PRE\_OV\_HYST}$	V_{PRE} Overvoltage Hysteresis	–	0.1	–	V	(14)
$V_{CORE\_FB\_UV}$	V_{CORE} FB Undervoltage Detection Threshold	0.67	–	0.773	V	
$V_{CORE\_FB\_UV\_D}$	V_{CORE} FB Undervoltage Detection Threshold - Degraded mode	0.45	–	0.58	V	
$V_{CORE\_FB\_UV\_HYST}$	V_{CORE} FB Undervoltage Hysteresis	10	–	27	mV	(14)
$V_{CORE\_FB\_OV}$	V_{CORE} FB Overvoltage Detection Threshold	0.84	–	0.905	V	
$V_{CORE\_FB\_OV\_HYST}$	V_{CORE} FB Overvoltage Hysteresis	10	–	30	mV	(14)
$V_{CORE\_FB\_DRIFT}$	V_{CORE_FB} Drift versus IO_1	50	100	150	mV	
I_{PD_CORE}	V_{CORE} Internal Pull-down Current (active when $V_{COR\ E}$ is enabled)	5.0	12	25	mA	
$V_{CCA\_UV\_5}$	V_{CCA} Undervoltage Detection Threshold (5.0 V config)	4.5	–	4.75	V	
$V_{CCA\_UV\_5D}$	V_{CCA} Undervoltage Detection Threshold (Degraded 5.0 V)	3.0	–	3.2	V	
$V_{CCA\_UV\_33}$	V_{CCA} Undervoltage Detection Threshold (3.3 V config)	3.0	–	3.2	V	
$V_{CCA\_UV\_HYST}$	V_{CCA} Undervoltage Hysteresis	–	0.07	–	V	(14)
$V_{CCA\_OV\_5}$	V_{CCA} Overvoltage Detection Threshold (5.0 V config)	5.25	–	5.5	V	
$V_{CCA\_OV\_33}$	V_{CCA} Overvoltage Detection Threshold (3.3 V config)	3.4	–	3.6	V	
$V_{CCA\_OV\_HYST}$	V_{CCA} Overvoltage Hysteresis	–	0.15	–	V	(14)
R_{PD_CCA}	V_{CCA} Internal Pull-down Resistor (active when V_{CCA} is disabled)	50	–	160	Ω	
$V_{AUX\_UV\_5}$	V_{AUX} Undervoltage Detection Threshold (5.0 V config)	4.5	–	4.75	V	
$V_{AUX\_UV\_5D}$	V_{AUX} Undervoltage Detection Threshold (Degraded 5.0 V)	3.0	–	3.2	V	
$V_{AUX\_UV\_33}$	V_{AUX} Undervoltage Detection Threshold (3.3 V config)	3.0	–	3.2	V	
$V_{AUX\_UV\_HYST}$	V_{AUX} Undervoltage Hysteresis	–	0.07	–	V	(14)
$V_{AUX\_OV\_5}$	V_{AUX} Overvoltage Detection Threshold (5.0 V config)	5.25	–	5.5	V	
$V_{AUX\_OV\_33}$	V_{AUX} Overvoltage Detection Threshold (3.3 V config)	3.4	–	3.6	V	
$V_{AUX\_OV\_HYST}$	V_{AUX} Overvoltage Hysteresis	–	0.07	–	V	(14)
R_{PD_AUX}	V_{AUX} Internal Pull-down Resistor (active when V_{AUX} is disabled)	50	–	170	Ω	

Notes

14. Guaranteed by design.

Table 4. Operating range (continued)

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Fail-safe outputs						
V_{RSTB_OL}	Reset Low Output Level (I_RSTB = 2.0 mA and 2.0 V < V_{SUP} < 40 V)	–	–	0.5	V	(15)
I_{RSTB_LIM}	Reset Output Current Limitation	12	–	25	mA	
V_{RSTB_IL}	External Reset Detection Threshold (falling)	1.0	–	–	V	
V_{RSTB_IH}	External Reset Detection Threshold (rising)	–	–	2.0	V	
$V_{RSTB\_IN\_HYST}$	External Reset Input Hysteresis	0.2	–	–	V	
V_{FS0B_OL}	FS0B Low Output Level (I_FS0b = 2.0 mA)	–	–	0.5	V	
I_{FS0B_LK}	FS0B Input Current Leakage (V_{FS0B} = 28 V)	–	–	1.0	µA	
I_{FS0B_LIM}	FS0B Output Current Limitation	6.0	–	12	mA	
Digital input						
V_{IO_IH}	Digital High Input voltage level (IO_0:1, IO_4:5) • Min Limit = 2.7 V at V_{SUP} = 40 V	2.6	–	–	V	
V_{IO23_IH}	Digital High Input voltage level (IO_2, IO_3)	2.0	–	–	V	
V_{IO_IL}	Digital Low Input voltage Level (IO_0:1; IO_4:5)	–	–	2.1	V	
V_{IO_HYST}	Input Voltage Hysteresis (IO_0:1, IO_4:5)	50	120	500	mV	(16)
V_{IO23_IL}	Digital Low Input voltage Level (IO_2, IO_3)	–	–	0.9	V	
V_{IO23_HYST}	Input Voltage Hysteresis (IO_2, IO_3)	200	450	700	mV	(16)
$I_{IO\_IN\_0:1}$	Input Current for IO_0:1	-5.0	–	100	µA	
$I_{IO\_IN\_1}$	Input Current for IO_1 when used for FB_Core monitoring	-1.0	–	1.0	µA	
$I_{IO\_IN\_2:5}$	Input Current for IO_2:5	-5.0	–	5.0	µA	
$I_{IO\_IN\_LPOFF}$	Input Current for IO_0:5 in LPOFF	-1.0	–	1.0	µA	
Output gate driver						
V_{IO_OH}	High Output Level at I_{IO_OUT} = -2.5 mA	V_{PRE} - 1.5	–	V_{PRE}	V	
V_{IO_OL}	Low Output Level at I_{IO_OUT} = +2.5 mA	0.0	–	1.0	V	
$V_{IO\_OUT\_SK}$ $V_{IO\_OUT\_SC}$	Output Current Capability	2.5 –	– –	– -2.5	mA	
Analog multiplexer						
V_{AMUX_REF1}	Internal Voltage Reference with 6.0 V < V_{SUP} < 19 V	2.475	2.5	2.525	V	
V_{AMUX_REF2}	Internal Voltage Reference with $V_{SUP} \leq$ 6.0 V or $V_{SUP} \geq$ 19 V	2.468	2.5	2.532	V	
$V_{AMUX\_TP\_CO}$	Internal Temperature sensor coefficient	–	9.9	–	mV/°C	(16)
V_{AMUX_TP}	Temperature Sensor MUX_OUT output voltage (at T_J=165°C)	2.08	2.15	2.22	V	

Notes

15. For V_{SUP} < 2.0 V, all supplies are already off and external pull-up on RSTB (e.g V_{CORE} or V_{CCA}) pulls the line down.
16. Guaranteed by design.

Table 4. Operating range (continued)

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Interrupt						
V_{INTB_OL}	Low Output Level (I_{INT} = 2.5 mA)	–	–	0.5	V	
R_{PU_INT}	Internal Pull-up Resistor (connected to VDDIO)	–	10	–	KΩ	
I_{INT_LK}	Input Leakage Current	–	–	1	µA	
CAN transceiver						
CAN logic input pin (TXD)						
V_{TXD_IH}	TXD High Input Threshold	0.7 x V_{DDIO}	–	–	V	
V_{TXD_IL}	TXD Low Input Threshold	–	–	0.3 x V_{DDIO}	V	
$TXD_{PULL-UP}$	TXD Main Device Pull-up	20	33	50	KΩ	
TXD_{LK}	TXD Input Leakage Current, V_{TXD} = V_{DDIO}	-1.0	–	1.0	µA	
CAN logic output pin (RXD)						
V_{RXD_OL1}	Low Level Output Voltage (I_{RXD} = 250 µA)	–	–	0.4	V	
V_{RXD_OL2}	Low Level Output Voltage (I_{RXD} = 1.5 mA)	–	–	0.9	V	
$VOUT_{HIGH}$	High Level Output Voltage (I_{RXD} = -250 µA, V_{DDIO} = 3.0 V to 5.5 V)	V_{DDIO} - 0.4V	–	–	V	
CAN Output pins (CANH, CANL)						
$V_{DIFF\_COM\_MODE}$	Differential Input Comparator Common Mode Range	-12	–	12	V	
$V_{IN\_DIFF\_SLEEP}$	Differential Input Voltage Threshold in Sleep Mode	0.5	–	0.9	V	
V_{IN_HYST}	Differential Input Hysteresis (in TX, RX mode)	50	–	–	mV	
R_{IN_CHCL}	CANH, CANL Input Resistance	5.0	–	50	kΩ	
R_{IN_DIFF}	CAN Differential Input Resistance	10	–	100	kΩ	
R_{IN_MATCH}	Input Resistance Matching	-3.0	–	3.0	%	
V_{CANH}	CANH Output Voltage (45 Ω < R_{BUS} < 65 Ω) • TX dominant state • TX recessive state	 2.75 2.0	 – 2.5	 4.5 3.0	V	
V_{CANL}	CANL Output Voltage (45 Ω < R_{BUS} < 65 Ω) • TX dominant state • TX recessive state	 0.5 2.0	 – 2.5	 2.25 3.0	V	
V_{CAN_SYM}	CAN dominant voltage symmetry (V_{CANL} + V_{CANH})	4.5	5	5.5	V	
V_{OH}-V_{OL}	Differential Output Voltage • TX dominant state (45 Ω < R_{BUS} < 65 Ω) • TX recessive state	 1.5 -50	 2.0 0.0	 3.0 50	 V mV	
$I_{CANL-SK}$	CANL Sink Current Under Short-circuit Condition (V_{CANL} ≤ 12 V, CANL driver ON, TXD low)	40	–	100	mA	
$I_{CANH-SC}$	CANH Source Current Under Short-circuit Condition (V_{CANH} = -2.0 V, CANH driver ON, TXD low)	-100	–	-40	mA	
$R_{INSLEEP}$	CANH, CANL Input Resistance Device Supplied and in CAN Sleep Mode	5.0	–	50	kΩ	

Table 4. Operating range (continued)

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
CAN output pins (CANH, CANL) (continued)						
V_{CANLP}	CANL, CANH Output Voltage in Sleep Modes. No termination load.	-0.1	0.0	0.1	V	
I_{CAN}	CANH, CANL Input Current, Device Unsupplied, (V_{CANH}, V_{CANL} =5.0V) • V_{SUP} and V_{CAN} connected to GND • V_{SUP} and V_{CAN} connected to GND via 47k resistor	 -10 -10	 – –	 10 10	 µA µA	(17)
T_{OT}	Overtemperature Detection	160	–	–	°C	
T_{HYST}	Overtemperature Hysteresis	–	–	20	°C	
Digital interface						
$MISO_H$	High Output Level on MISO (I_{MISO} = 1.5 mA)	V_{DDIO} - 0.4	–	–	V	
$MISO_L$	Low Output Level on MISO (I_{MISO} = 2.0 mA)	–	–	0.4	V	
I_{MISO}	Tri-state Leakage Current (V_{DDIO} = 5.0 V)	-5.0	–	5.0	µA	
V_{DDIO}	Supply Voltage for MISO Output Buffer	3.0	–	5.5	V	
IV_{DDIO}	Current consumption on VDDIO	–	1.0	3.0	mA	
SPI_{LK}	SCLK, NCS, MOSI Input Current	-1.0	–	1.0	µA	
V_{SPI_IH}	SCLK, NCS, MOSI High Input Threshold	2.0	–	–	V	
R_{SPI}	NCS, MOSI Internal Pull-up (pull-up to VDDIO)	200	400	800	KΩ	
V_{SPI_IL}	SCLK, NCS, MOSI Low Input Threshold	–	–	0.8	V	
Debug						
V_{DEBUG_IL}	Low Input Voltage Threshold	2.1	2.35	2.6	V	
V_{DEBUG_IH}	High Input Voltage Threshold	4.35	4.6	4.97	V	
I_{DEBUG_LK}	Input Leakage Current	-10	–	10	µA	

Notes

17. Guaranteed by design and characterization.

4.3 Dynamic electrical characteristics

Table 5. Dynamic electrical characteristics

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Digital interface timing						
f_{SPI}	SPI Operation Frequency (50% DC)	0.5	–	8.0	MHz	
t_{MISO_TRANS}	MISO Transition Speed, 20 - 80% • V_{DDIO} = 5.0 V, C_{LOAD} = 50 pF • V_{DDIO} = 5.0 V, C_{LOAD} = 150 pF	 5.0 5.0	 – –	 30 50	ns	
t_{CLH}	Minimum Time SCLK = HIGH	62	–	–	ns	
t_{CLL}	Minimum Time SCLK = LOW	62	–	–	ns	
t_{PCLD}	Propagation Delay (SCLK to data at 10% of MISO rising edge)	–	–	30	ns	
t_{CSDV}	NCS = LOW to Data at MISO Active	–	–	75	ns	
t_{SCLCH}	SCLK Low Before NCS Low (setup time SCLK to NCS change H/L)	75	–	–	ns	
t_{HCLCL}	SCLK Change L/H after NCS = low	75	–	–	ns	
t_{SCLD}	SDI Input Setup Time (SCLK change H/L after MOSI data valid)	40	–	–	ns	
t_{HCLD}	SDI Input Hold Time (MOSI data hold after SCLK change H/L)	40	–	–	ns	
t_{SCLCL}	SCLK Low Before NCS High	100	–	–	ns	
t_{HCLCH}	SCLK High After NCS High	100	–	–	ns	
t_{PCHD}	NCS L/H to MISO at High-impedance	–	–	75	ns	
t_{ONNCS}	NCS Min. High Time	500	–	–	ns	
t_{NCS_MIN}	NCS Filter Time	10	–	40	ns	

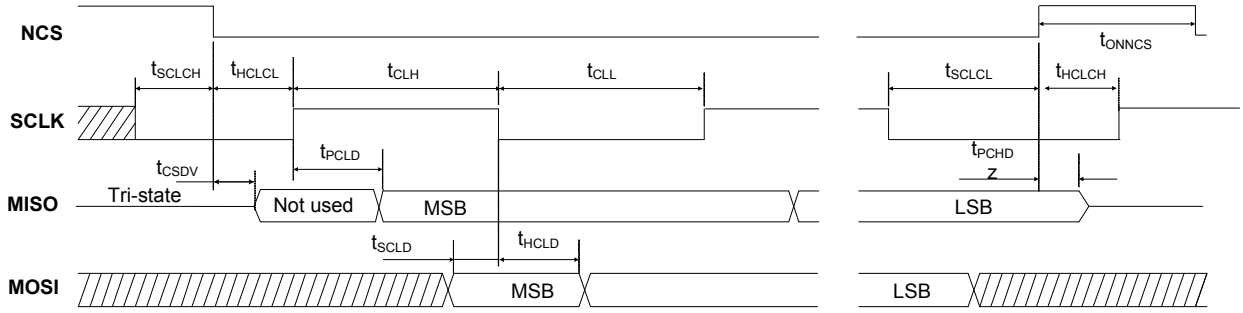


Figure 5. SPI timing diagram

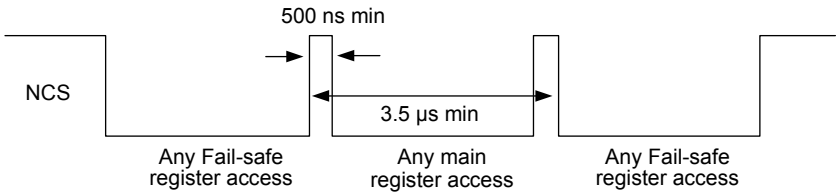


Figure 6. Register access restriction

Table 5. Dynamic electrical characteristics (continued)

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
CAN dynamic characteristics						
t_{DOUT}	TXD Dominant State Timeout	0.8	–	5.0	ms	
t_{DOM}	Bus Dominant Clamping Detection	0.8	–	5.0	ms	
t_{LOOP}	Propagation Loop Delay TXD to RXD • R_{LOAD} = 120 Ω, C between CANH and CANL = 100 pF, C at RxD < 15 pF	–	–	255	ns	
t_{1PWU}	Single Pulse Wake-up Time	0.5	–	5.0	µs	
t_{3PWU}	Multiple Pulse Wake-up Time	0.5	–	1.0	µs	
t_{3PTO1}	Multiple Pulse Wake-up Timeout (120 µs bit selection)	100	120	–	µs	
t_{3PTO2}	Multiple Pulse Wake-up Timeout (360 µs bit selection)	330	360	–	µs	
t_{CAN_READY}	Delay to Enable CAN by SPI Command (NCS rising edge) to CAN to Transmit (device in normal mode and CAN interface in TX/RX mode)	–	–	100	µs	(18)
Fail-safe state machine						
OSC_{FSSM}	Oscillator	405	–	495	kHz	
CLK_{FS_MIN}	Fail-safe Oscillator Monitoring	150	–	–	kHz	
t_{IC_ERR}	IO_0:5 Filter Time	4.0	–	20	µs	
t_{ACK_FS}	Acknowledgement Counter (used for IC error handling IO_1 and IO_5)	7.0	–	9.7	ms	
$t_{\_DFS\_RECOVERY}$	IO_0 Filter Time to Recover from Deep Reset and Fail State	0.8	–	1.3	ms	
$t_{IO1\_DRIFT\_MON}$	IO_1 filter time	1.0	–	2.0	ms	
Fail-safe output						
t_{RSTB_FB}	RSTB Feedback Filter Time	8.0	–	15	µs	
t_{FSOB_FB}	FS0B Feedback Filter Time	8.0	–	15	µs	
t_{RSTB_BLK}	RSTB Feedback Blanking Time	180	–	320	µs	
t_{FSOB_BLK}	FS0B Feedback Blanking Time	180	–	320	µs	
t_{RSTB_POR}	Reset Delay Time (after a Power On Reset or from LPOFF)	12	15.9	23.6	ms	(19)
t_{RSTB_LG}	Reset Duration (long pulse)	8.0	–	10	ms	
t_{RSTB_ST}	Reset duration (short pulse)	1.0	–	1.3	ms	
t_{RSTB_IN}	External Reset Delay time	8.0	–	15	µs	
t_{DIAG_SC}	Fail-safe Output Diagnostic Counter (FS0B)	550	–	800	µs	
VSUP voltage supply						
C_{SUP}	Minimum capacitor on Vsup	44	–	–	µF	

Notes

18. For proper CAN operation, TXD must be set to high level before CAN enable by SPI, and must remain high for at least T_{CAN_READY}.
19. This timing is not guaranteed in case of fault during startup phase (after Power On Reset of from LPOFF)

Table 5. Dynamic electrical characteristics (continued)

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{PRE} voltage pre-regulator						
f_{SW_PRE}	V_{PRE} Switching Frequency	412	437.5	465	kHz	
t_{SW_PRE}	V_{SW_PRE} On and Off Switching Time	–	–	30	ns	(20)
t_{PRE_SOFT}	V_{PRE} Soft Start Duration ($C_{OUT} \leq$ 100 µF)	500	–	700	µs	
$t_{PRE\_BLK\_LIM}$	V_{PRE} Current Limitation Blanking Time	200	–	600	ns	
t_{IPRE_OC}	V_{PRE} Overcurrent Filtering Time	30	–	120	ns	(20)
t_{PRE_UV}	V_{PRE} Undervoltage Filtering Time	20	–	40	µs	
$t_{PRE\_UV\_4p3}$	Vpre Shut-off Filtering Time	3.0	–	7.0	µs	
$d_{IPRE/DT}$	V_{PRE} Load Regulation Variation	–	–	25	A/ms	(20)
t_{PRE_WARN}	V_{PRE} Thermal Warning Filtering Time	30	–	40	µs	
t_{PRE_TSD}	V_{PRE} Thermal Detection Filtering Time	1.0	–	3.0	µs	
$t_{LS\_RISE/FALL}$	LS Gate Voltage Switching Time (I_{OUT} = 300 mA)	–	–	50	ns	
V_{sense} voltage regulator						
t_{VSNS_UV}	V_{SNS} Undervoltage Filtering Time	1.0	–	3.0	µs	
V_{core} voltage regulator						
$t_{CORE\_BLK\_LIM}$	V_{CORE} Current Limitation Blanking Time	20	–	40	ns	
f_{SW_CORE}	V_{CORE} Switching Frequency	2.20	2.34	2.49	MHz	
t_{SW_CORE}	V_{SW_CORE} On and Off Switching Time	6.0	–	12	ns	
V_{CORE_SOFT}	V_{CORE} Soft Start (C_{OUT} = 100 µF max)	–	–	10	V/ms	
t_{CORE_WARN}	V_{CORE} Thermal Warning Filtering Time	30	–	40	µs	
t_{CORE_TSD}	V_{CORE} Thermal Detection Filtering Time	1.0	–	3.0	µs	
V_{cca} voltage regulator						
t_{CCA_LIM}	V_{CCA} Output Current Limitation Filter Time	1.0	–	3.0	µs	
$t_{CCA\_LIM\_OFF1}$ $t_{CCA\_LIM\_OFF2}$	V_{CCA} Output Current Limitation Duration	10 50	– –	– –	ms	
t_{CCA_WARN}	V_{CCA} Thermal Warning Filtering Time	30	–	40	µs	
t_{CCA_TSD}	V_{CCA} Thermal Detection Filter Time (int. MOSFET)	1.0	–	3.0	µs	
dI_{LOAD}/dt	V_{CCA} Load Transient	–	2.0	–	A/ms	(20)
V_{CCA_SOFT}	V_{CCA} Soft Start (5.0 V and 3.3 V)	–	–	50	V/ms	

Notes

20. Guaranteed by characterization.

Table 5. Dynamic electrical characteristics (continued)

T_{CASE} = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP\_UV\_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{aux} voltage regulator						
t_{AUX_LIM}	V_{AUX} Output Current Limitation Filter Time	1.0	–	3.0	µs	
$t_{AUX\_LIM\_OFF1}$ $t_{AUX\_LIM\_OFF2}$	V_{AUX} Output Current Limitation Duration	10 50	– –	– –	ms	
t_{AUX_TSD}	V_{AUX} Thermal Detection Filter Time	1.0	–	3.0	µs	
dI_{AUX}/dt	V_{AUX} Load Transient	–	2.0	–	A/ms	(21)
V_{AUX_SOFT}	V_{AUX} Soft Start (5.0 V and 3.3 V)	–	–	50	V/ms	
CAN_5V voltage regulator						
t_{CAN_LIM}	Output Current Limitation Filter Time	2.0	–	4.0	µs	
t_{CAN_TSD}	V_{CAN} Thermal Detection Filter Time	1.0	–	3.0	µs	
t_{CAN_UV}	V_{CAN} Undervoltage Filtering Time	4.0	–	7.0	µs	
t_{CAN_OV}	V_{CAN} Overvoltage Filtering Time	100	–	200	µs	
dI_{CAN}/dt	V_{CAN} Load Transient	–	100	–	A/ms	(21)
Fail-safe machine voltage supervisor						
t_{PRE_OV}	V_{PRE} Overvoltage Filtering Time	128	–	234	µs	
t_{CORE_UV}	V_{CORE} FB Undervoltage Filtering Time	4.0	–	10	µs	
t_{CORE_OV}	V_{CORE} FB Overvoltage Filtering Time	128	–	234	µs	
t_{CCA_UV}	V_{CCA} Undervoltage Filtering Time	4.0	–	10	µs	
t_{CCA_OV}	V_{CCA} Overvoltage Filtering Time	128	–	234	µs	
t_{AUX_UV}	V_{AUX} Undervoltage Filtering Time	4.0	–	10	µs	
t_{AUX_OV}	V_{AUX} Overvoltage Filtering Time	128	–	234	µs	
Digital input - multi-purpose IOS						
F_{IO_IN}	Digital Input Frequency Range	0.0	–	100	kHz	
Analog multiplexer						
t_{MUX_READY}	SPI Selection to Data Ready to be Sampled on Mux_out • V_{DDIO} = 5.0 V, C_{MUX_OUT} = 1.0 nF	–	–	10	µs	
Interrupt						
t_{INTB_LG}	INTB Pulse Duration (long)	90	100	–	µs	
t_{INTB_ST}	INTB Pulse Duration (short)	20	25	–	µs	
Functional sate machine						
t_{WU_GEN}	General Wake-up Signal Deglitch Time (for any wu signal on IOs)	60	70	80	µs	

Notes

21. Guaranteed by characterization.

5 Functional pin description

5.1 Introduction

The FS6407/FS6408 is the third generation of the System Basis Chip, combining:

- High efficiency switching voltage regulator for MCU, and linear voltage regulators for integrated CAN interface, external ICs such as sensors, and accurate reference voltage for A to D converters.
- Built-in enhanced high-speed CAN interface (ISO11898-2 and -5), with local and bus failure diagnostic, protection, and Fail-safe operation mode.
- Low-power mode, with ultra low-current consumption.
- Various wake-up capabilities.
- Enhanced safety features with multiple fail-safe outputs and scheme to support SIL applications.

5.2 Power supplies (VSUP1, VSUP2, VSUP3)

VSUP1 and VSUP2 are the inputs pins for internal supply dedicated to SMPS regulators. VSUP3 is the input pin for internal voltage reference. VSUP1, 2, and 3 are robust against ISO7637 pulses. VSUP1,2, and 3 must be connected to the same supply (Figure 49).

5.3 VSENSE input (VSENSE)

This pin must be connected to the battery line (before the reverse battery protection diode), via a serial resistor. It incorporates a threshold detector to sense the battery voltage, and provide a battery early warning. It also includes a resistor divider to measure the VSENSE voltage via the MUX-OUT pin. VSENSE pin is robust against ISO7637 pulses.

5.4 Pre-regulator (VPRE)

A highly flexible SMPS pre-regulator is implemented in the FS6407/FS6408. It can be configured as a “non-inverting buck-boost converter” (Figure 24) or “standard buck converter” (Figure 23), depending on the external configuration (connection of pin GATE_LS). The configuration is detected automatically during start-up sequence.

The SMPS pre-regulator is working in current mode control and the compensation network is fully integrated in the device. The high-side switching MOSFET is also integrated to make the current control easier. The pre-regulator delivers a typical output voltage of 6.5 V, which is used internally. Current limitation, overcurrent, overvoltage, and undervoltage detectors are provided. VPRE is enabled by default.

5.5 VCORE output (from 1.2 V to 3.3 V range)

The VCORE block is an SMPS regulator. The voltage regulator is a step down DC-DC converter operating in voltage control mode. The output voltage is configurable from 1.2 V to 3.3 V range thanks to an external resistor divider connected between VCORE and the feedback pin (FB_CORE) (as example in Figure 1, Figure 2, and Figure 49).

The stability of the converter is done externally, by using the COMP_CORE pin. Current limitation, overvoltage, and undervoltage detectors are provided. VCORE can be turned ON or OFF via a SPI command, however it is not recommended to turn OFF VCORE by SPI when VCORE is configured safety critical (both overvoltage and undervoltage have an impact on RSTB and FS0B). VCORE overvoltage information disables VCORE. Diagnostics are reported in the dedicated register and generate an Interrupt. VCORE is enabled by default.

5.6 VCCA output, 5.0 V or 3.3 V selectable

The VCCA voltage regulator is used to provide an accurate voltage output (5.0 V, 3.3 V) selectable through an external resistor connected to the SELECT pin.

The VCCA output voltage regulator can be configured using an internal transistor delivering very good accuracy (±1.0% for 5.0 V configuration and ±1.5% for 3.3 V configuration), with a limited current capability (100 mA) for an analog to digital converter, or with an external PNP transistor, giving higher current capability (up to 300 mA) with lower output voltage accuracy (±3.0% for 300 mA) when using a local supply.

Current limitation, overvoltage, and undervoltage detectors are provided. VCCA can be turned ON or OFF via a SPI command, however it is not recommended to turn OFF VCCA by SPI when VCCA is configured safety critical (both overvoltage and undervoltage have an impact on RSTB and FS0B). VCCA overcurrent (with the use of external PNP only) and overvoltage information disables VCCA. Diagnostics are reported in the dedicated register and generate an Interrupt. VCCA is enabled by default.

5.7 VAUX output, 5.0 V or 3.3 V selectable

The VAUX pin provides an auxiliary output voltage (5.0 V, 3.3 V) selectable through an external resistor connected to SELECT pin. It uses an external PNP ballast transistor for flexibility and power dissipation constraints. The VAUX output voltage regulator can be used as “auxiliary supply” (local supply) or “sensor supply” (external supply) with the possibility to be configured as a tracking regulator following VCCA.

Current limitation, overvoltage, and undervoltage detectors are provided. VAUX can be turned ON or OFF via a SPI command, however it is not recommended to turn OFF VAUX by the SPI when VAUX is configured safety critical (both overvoltage and undervoltage have an impact on RSTB and FS0B). VAUX overcurrent and overvoltage information disables V_{AUX}, reported in the dedicated register, and generates an Interrupt. V_{AUX} is enabled by default.

5.8 SELECT input (VCCA, VAUX voltage configuration)

VCCA and VAUX output voltage configurations are set by connecting an external resistor between the SELECT pin and Ground. According to the value of this resistor, the voltage of VCCA and VAUX are configured after each Power On Reset, and after a wake-up event when device is in LPOFF. Information latches until the next hardware configuration read. Regulator voltage values can be read on the dedicated register via the SPI.

Table 6. V_{CCA}/V_{AUX} voltage selection (Figure 50)

V_{CCA}(V)	V_{AUX}(V)	R Select	Recommended value
3.3	3.3	<7.0 KΩ	5.1 KΩ ±5.0%
5.0	5.0	10.8 << 13.2 KΩ	12 KΩ ±5.0%
3.3	5.0	21.6 << 26.2 KΩ	24 KΩ ±5.0%
5.0	3.3	45.9 << 56.1 KΩ	51 KΩ ±5.0%

When VAUX is not used, the output VCCA voltage configuration is set using an external resistor connected between the SELECT and the VPRE pin.

Table 7. V_{CCA} voltage selection (V_{AUX} not used, Figure 51, Figure 52)

V_{CCA}(V)	R Select	Recommended Value
3.3	<7.0 KΩ	5.1 KΩ ±5.0%
	21.6 << 26.2 KΩ	24 KΩ ±5.0%
5.0	10.8 << 13.2 KΩ	12 KΩ ±5.0%
	45.9 << 56.1 KΩ	51 KΩ ±5.0%

5.9 CAN_5V voltage regulator

The CAN_5V voltage regulator is a linear regulator dedicated to the internal HSCAN interface. An external capacitor is required. Current limitation, overvoltage, and undervoltage detectors are provided. If the internal CAN transceiver is not used, the CAN_5V regulator can supply an external load (CAN_5V voltage regulator). CAN_5V is enabled by default.

5.10 Interrupt (INTB)

The INTB output pin generates a low pulse when an Interrupt condition occurs. The INTB behavior as well as the pulse duration are set through the SPI during INIT phase. INTB has an internal pull-up resistor connected to VDDIO.

5.11 CANH, CANL, TXD, RXD

These are the pins of the high speed CAN physical interface. The CAN transceivers provides the physical interface between the CAN protocol controller of an MCU and the physical dual wires CAN bus. The CAN interface is connected to the MCU via the RXD and TXD pins.

5.11.1 TXD

TXD is the device input pin to control the CAN bus level. TXD is a digital input with an internal pull-up resistor connected to VDDIO. In the application, this pin is connected to the microcontroller transmit pin.

In Normal mode, when TXD is high or floating, the CANH and CANL drivers are OFF, setting the bus in a recessive state. When TXD is low, the CANH and CANL drivers are activated and the bus is set to a dominant state. TXD has a built-in timing protection that disables the bus when TXD is dominant for more than T_{DOUT}. In LPOFF mode, VDDIO is OFF, pulling down this pin to GND.

5.11.2 RXD

RXD is the bus output level report pin. In the application, this pin is connected to the microcontroller receive pin. In Normal mode, RXD is a push-pull structure. When the bus is in a recessive state, RXD is high. When the bus is dominant, RXD is low. In LPOFF mode, this pin is in high-impedance state.

5.11.3 CANH and CANL

These are the CAN bus pins. CANL is a low-side driver to GND, and CANH is a high-side driver to CAN_5V. In Normal mode and TXD high, the CANH and CANL drivers are OFF, and the voltage at CANH and CANL is approximately 2.5 V, provided by the internal bus biasing circuitry. When TXD is low, CANL is pulled to GND and CANH to CAN_5V, creating a differential voltage on the CAN bus.

In LPOFF mode, the CANH and CANL drivers are OFF, and these pins are pulled down to GND via the device R_{IN_CHCL} resistors. CANH and CANL have integrated ESD protection and extremely high robustness versus external disturbance, such as EMC and electrical transients. These pins have current limitation and thermal protection.

5.12 Multiplexer output MUX_OUT

The MUX_OUT pin (Figure 7) delivers analog voltage to the MCU ADC input. The voltage to be delivered to MUX_OUT is selected via the SPI, from one of the following parameters:

- Internal 2.5 V reference
- Die temperature sensor T(°C) = (V_{AMUX} - V_{AMUX_TP}) / $V_{AMUX\_TP\_CO}$ + 165

Voltage range at MUX_OUT is from GND to VDDIO (3.3 V or 5.0 V)

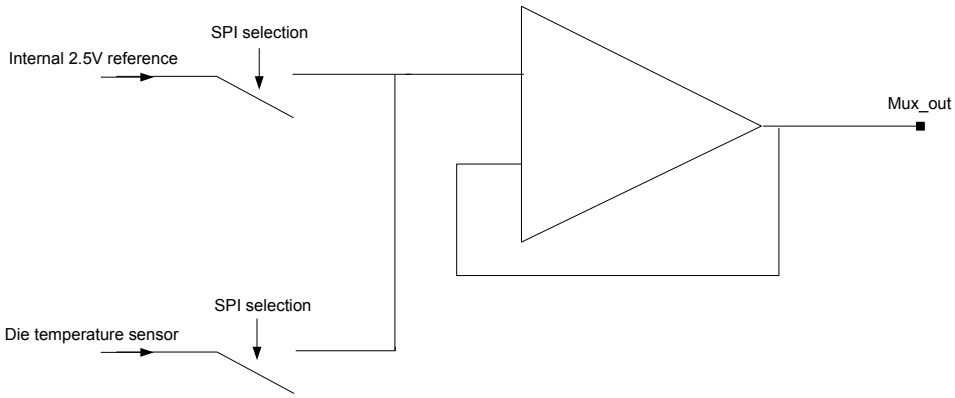


Figure 7. Simplified analog multiplexer block diagram

5.13 I/O pins (I/O_0:I/O_5)

The FS6407/FS6408 includes six multi-purpose I/Os (I/O_0 to I/O_5). I/O_0, I/O_1, I/O_4, and I/O_5 are robust against ISO7637 pulses. An external serial resistor must be connected to those pins to limit the current during ISO pulses.

Table 8. I/Os configuration

I/0 number	Digital input	Wake-up capability	Output gate driver
IO_0	X	X	
IO_1	X	X	
IO_2	X	X	
IO_3	X	X	
IO_4	X	X	X
IO_5	X	X	X

- IO_0:1 are selectable as follows:
  Analog input (load dump proof) sent to the MCU through the MUX_OUT pin. Wake-up input on the rising or falling edge or based on the previous state. Digital input (logic level) sent to the MCU through the SPI. **Safety purpose**: Digital input (logic level) to perform an IC error monitoring (both IO_0 AND IO_1 are used if configured as safety inputs, see Figure 9).
- IO_1 is also selectable as follow:
  Safety purpose: FB_Core using a second resistor bridge (R3/R4 duplicated) connected to IO_1, to detect external resistor drift and trigger when FB_Core - IO_1 > ±150 mV max.
- IO_2:3 are selectable as follows:
  Digital input (logic level) sent to the MCU through the SPI. Wake-up input (logic level) on the rising or falling edge or based on the previous state. **Safety purpose**: Digital input (logic level) to monitor MCU error signals (both IO_2 AND IO_3 are used if configured as safety inputs). Only bi-stable protocol is available.
  When IO_2:3 are used as safety inputs to monitor FCCU error outputs from the NXP MCU, the monitoring is active only when the Fail-safe sate machine is in “normal WD running” state (Figure 11) and all the phases except the “Normal Phase” are considered as an Error.