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Three phase field effect transistor pre-driver

The 34GD3000 is a field effect transistor (FET) pre-drivers designed for three phase motor control and similar applications. The integrated circuit (IC) uses SMARTMOS technology.

The IC contains three high-side FET pre-drivers and three low-side FET pre-drivers. Three external bootstrap capacitors provide gate charge to the high-side FETs.

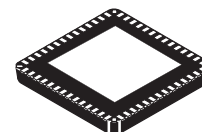
The IC interfaces to a MCU via six direct input control signals, an SPI port for device setup and asynchronous reset, enable and interrupt signals. Both 5.0 V and 3.3 V logic level inputs are accepted and 5.0 V logic level outputs are provided.

Features

- Extended supply voltage operating range: 6.0 V to 60 V
- Wide dead time range (50 ns to 12 μ s) programmable via the SPI port
- Gate drive capability of 1.0 A to 2.5 A
- Charge pump ensures sufficient external FET drive at low supply voltages
- Device protection against reverse charge-injection from C_{GD} and C_{GS} of external FETS
- Integrated overcurrent, desaturation, and phase fault-detection
- Immunity against positive or negative transient voltage spikes on the gate driver
- Current shoot-through protection built into dead time control
- Supports direct 3.3 V and 5.0 V logic interface to MCUs
- Integrated current sensing amplifier
- Device configuration and diagnostics through the SPI

34GD3000
Industrial

THREE PHASE PRE-DRIVER



EP SUFFIX (Pb-FREE)
98ASA00654D
56-PIN QFN

Applications

- 12 V - 48 V 3-phase brushless DC (BLDC) motors and permanent magnet synchronous motors (PMSM)
- Pool pumps, hospital beds, electric scooters
- Industrial robotics, pumps and fans
- Portable power tools, commercial fans/blowers
- Small kitchen appliances

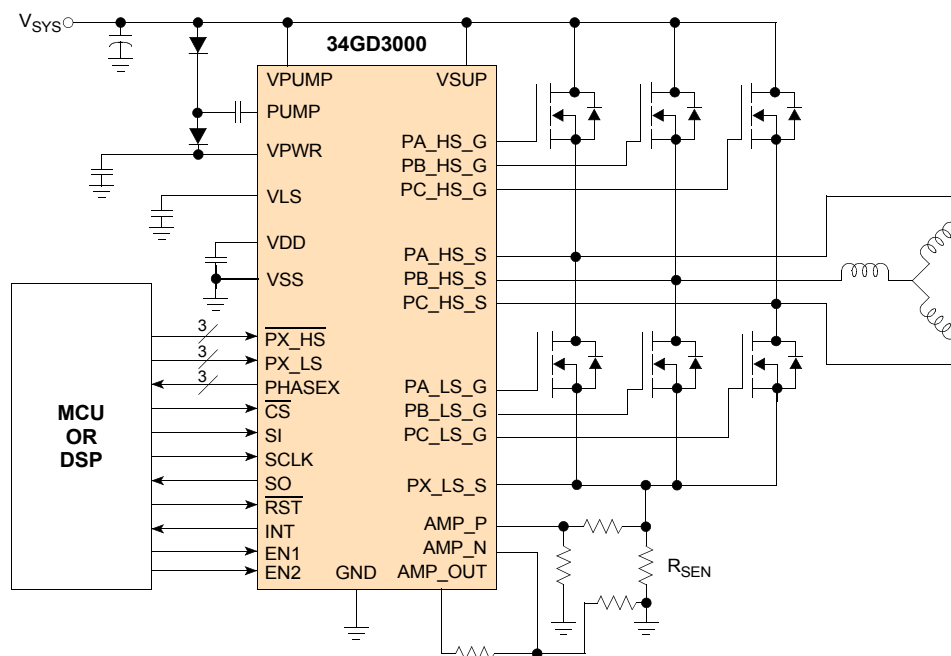


Figure 1. 34GD3000 simplified application diagram

* This document contains certain information on a new product. Specifications and information herein are subject to change without notice.

1 Orderable parts

Table 1. Orderable part variations

Part number ⁽¹⁾	Temperature (T _A)	Package
MC34GD3000EP	-20 °C to 105 °C	56 Pin QFN

Notes

1. To order parts in tape & reel, add the R2 suffix to the part number.

2 Internal block diagram

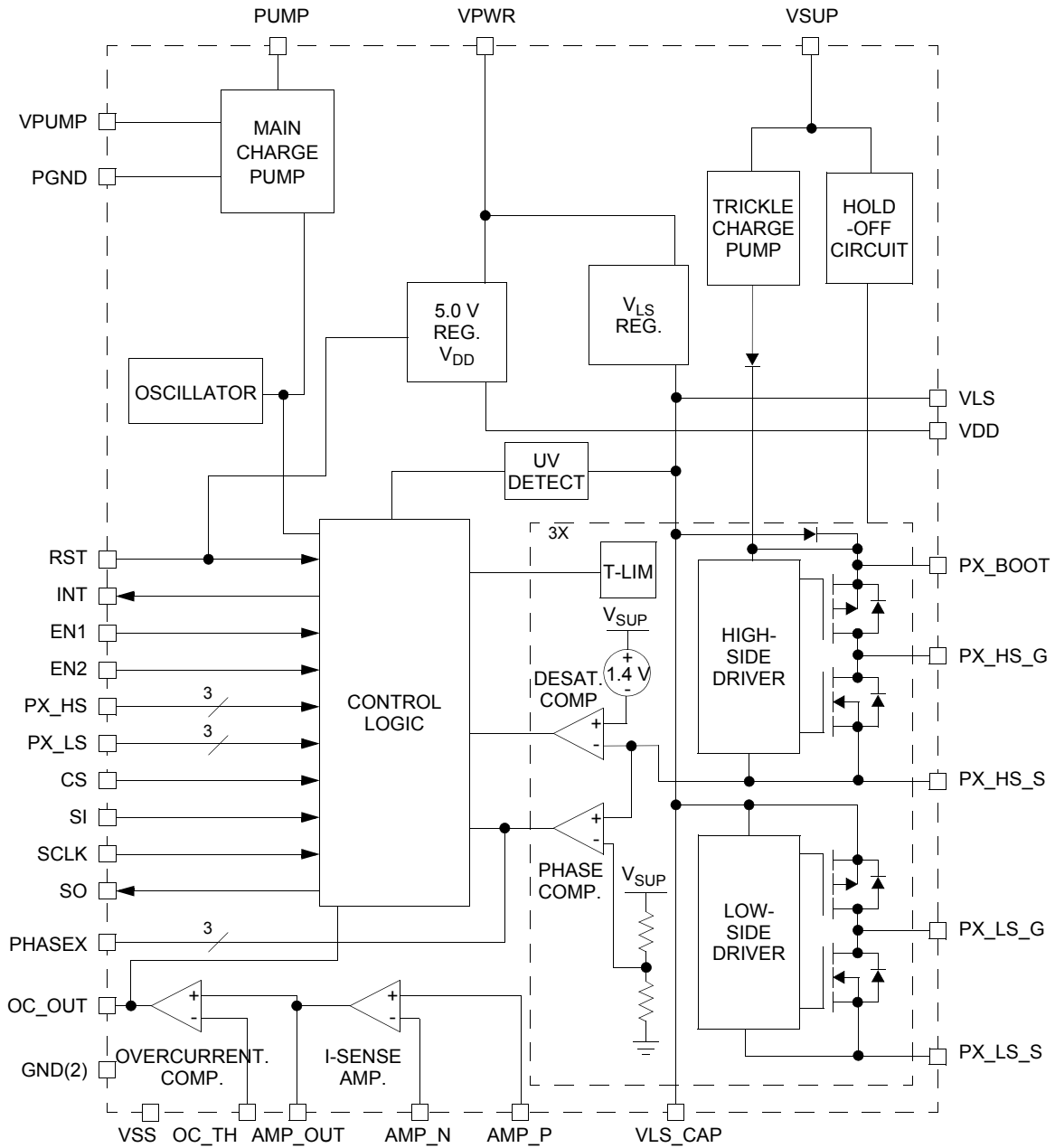


Figure 2. 34GD3000 simplified internal block diagram

3 Pin connections

Transparent
Top View

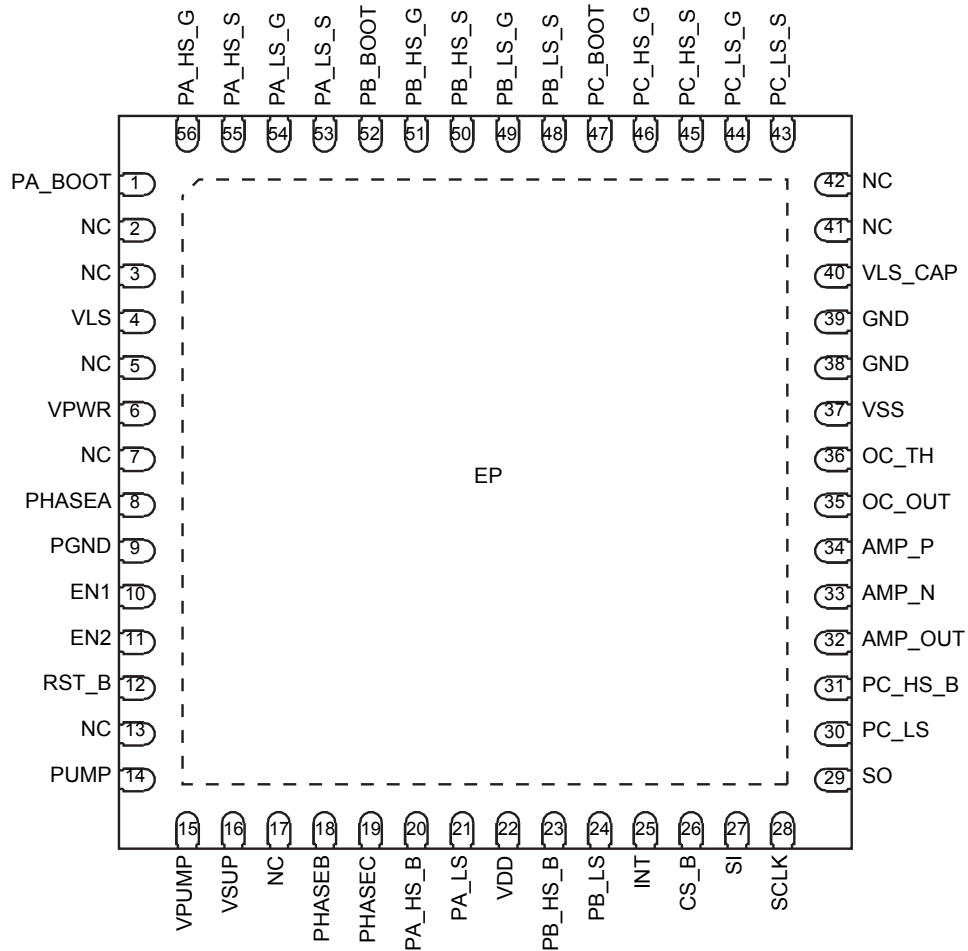


Figure 3. 34GD3000 pin connections

A functional description of each pin can be found in the [Functional pin description](#) section beginning on [page 20](#).

Table 2. 34GD3000 pin definitions

Pin	Pin name	Pin function	Formal name	Definition
1	PA_BOOT	Analog input	Phase A bootstrap	Bootstrap capacitor for Phase A
2, 3, 5, 7, 13, 17, 41, 42	NC	No connect		No connection
4	VLS	Analog output	VLS regulator	VLS regulator output; power supply for the gate drives
6	VPWR	Power input	Voltage power	Power supply input for gate drives
8	PHASEA	Digital output	Phase A	Totem pole output of Phase A comparator; this output is low when the voltage on PA_HS_S (source of high-side FET) is less than 50% of V_{SUP}
9	PGND	Ground	Power ground	Power ground for charge pump
10	EN1	Digital input	Enable 1	Logic signal input must be high (ANDed with EN2) to enable any gate drive output.
11	EN2	Digital input	Enable 2	Logic signal input must be high (ANDed with EN1) to enable any gate drive output

Table 2. 34GD3000 pin definitions

Pin	Pin name	Pin function	Formal name	Definition
12	RST_B	Digital input	Reset	Reset input
14	PUMP	Power drive out	Pump	Charge pump output
15	VPUMP	Power input	Voltage pump	Charge pump supply
16	VSUP	Analog input	Supply voltage	Supply voltage to the load. This pin is to be connected to the common drains of the external high-side FETs
18	PHASEB	Digital output	Phase B	Totem pole output of Phase B comparator. This output is low when the voltage on PB_HS_S (source of high-side FET) is less than 50% of V_{SUP}
19	PHASEC	Digital output	Phase C	Totem pole output of Phase C comparator. This output is low when the voltage on PC_HS_S (source of high-side FET) is less than 50% of V_{SUP}
20	PA_HS_B	Digital input	Phase A high-side	Active low input logic signal enables the high-side driver for Phase A
21	PA_LS	Digital input	Phase A low-side	Active high input logic signal enables the low-side driver for Phase A
22	VDD	Analog output	VDD regulator	VDD regulator output capacitor connection
23	PB_HS_B	Digital input	Phase B high-side	Active low input logic signal enables the high-side driver for Phase B
24	PB_LS	Digital input	Phase B low-side	Active high input logic signal enables the low-side driver for Phase B
25	INT	Digital output	Interrupt	Interrupt pin output
26	CS_B	Digital input	Chip select	Chip select input. It frames SPI commands and enables SPI port
27	SI	Digital input	Serial in	Input data for SPI port. Clocked on the falling edge of SCLK, MSB first
28	SCLK	Digital input	Serial clock	Clock for SPI port and typically is 3.0 MHz
29	SO	Digital output	Serial Out	Output data for SPI port. Tri-state until CS becomes low
30	PC_LS	Digital Input	Phase C low-side	Active high input logic signal enables the low-side driver for Phase C
31	PC_HS_B	Digital input	Phase C high-side	Active low input logic signal enables the high-side driver for Phase C
32	AMP_OUT	Analog output	Amplifier output	Output of the current-sensing amplifier
33	AMP_N	Analog input	Amplifier invert	Inverting input of the current-sensing amplifier
34	AMP_P	Analog input	Amplifier non-invert	Non-inverting input of the current-sensing amplifier
35	OC_OUT	Digital output	Overcurrent out	Totem pole digital output of the overcurrent comparator
36	OC_TH	Analog input	Overcurrent threshold	Threshold of the overcurrent detector
37	VSS	Ground	Voltage source supply	Ground reference for logic interface and power supplies
38, 39	GND	Ground	Ground	Substrate and ESD reference, connect to VSS
40	VLS_CAP	Analog output	VLS regulator output capacitor	VLS Regulator connection for additional output capacitor, providing low impedance supply source for low-side gate drive
43	PC_LS_S	Power input	Phase C Low-side Source	Source connection for Phase C low-side FET
44	PC_LS_G	Power Output	Phase C low-side gate drive	Gate drive output for Phase C low-side
45	PC_HS_S	Power input	Phase C high-side source	Source connection for Phase C high-side FET
46	PC_HS_G	Power output	Phase C high-side gate drive	Gate drive for output Phase C high-side FET
47	PC_BOOT	Analog input	Phase C bootstrap	Bootstrap capacitor for Phase C

Table 2. 34GD3000 pin definitions

Pin	Pin name	Pin function	Formal name	Definition
48	PB_LS_S	Power input	Phase B low-side source	Source connection for Phase B low-side FET
49	PB_LS_G	Power output	Phase B low-side gate drive	Gate drive for output Phase B low-side
50	PB_HS_S	Power input	Phase B high-side source	Source connection for Phase B high-side FET
51	PB_HS_G	Power output	Phase B high-side gate drive	Gate drive for output Phase B high-side
52	PB_BOOT	Analog input	Phase B bootstrap	Bootstrap capacitor for Phase B
53	PA_LS_S	Power input	Phase A low-side source	Source connection for Phase A low-side FET
54	PA_LS_G	Power output	Phase A low-side gate drive	Gate drive for output Phase A low-side
55	PA_HS_S	Power input	Phase A high-side source	Source connection for Phase A high-side FET
56	PA_HS_G	Power output	Phase A high-side gate drive	Gate drive for output Phase A high-side
	EP	Ground	Exposed pad	Device performs as specified with the exposed pad un-terminated (floating) however, it is recommended the exposed pad be terminated to pin 29 (VSS) and system ground

4 Electrical characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to V_{SS} unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings				
V_{SUP}	VSUP supply voltage <ul style="list-style-type: none"> Normal operation (steady-state) Transient survival 	60 -1.5 to 80	V	(2)
V_{PWR}	VPWR supply voltage <ul style="list-style-type: none"> Normal operation (steady-state) Transient survival 	58 -1.5 to 80	V	(2)
V_{PUMP}	Charge pump (PUMP, VPUMP)	-0.3 to 40	V	
V_{LS}	VLS regulator outputs (VLS, VLS_CAP)	-0.3 to 18	V	
V_{DD}	Logic supply voltage	-0.3 to 7.0	V	
V_{OUT}	Logic output (INT, SO, PHASEA, PHASEB, PHASEC, OC_OUT)	-0.3 to 7.0	V	(3)
V_{IN}	Logic input pin voltage (EN1, EN2, Px_HS, Px_LS, SI, SCLK, CS, RST) 10 mA	-0.3 to 7.0	V	
V_{IN_A}	Amplifier input voltage <ul style="list-style-type: none"> (both inputs-GND), (AMP_P - GND) or (AMP_N - GND) 6.0 mA source or sink 	-7.0 to 7.0	V	
V_{OC}	Overcurrent comparator threshold 10 mA	-0.3 to 7.0	V	
V_{BOOT} V_{HS_G} V_{LS_G}	Driver output voltage <ul style="list-style-type: none"> High-side bootstrap (PA_BOOT, PB_BOOT, PC_BOOT) High-side (PA_HS_G, PB_HS_G, PC_HS_G) Low-side (PA_LS_G, PB_LS_G, PC_LS_G) 	75 75 16	V	(4)
V_{HS_G} V_{HS_S} V_{LS_G} V_{LS_S}	Driver voltage transient survival <ul style="list-style-type: none"> High-side (PA_HS_G, PB_HS_G, PC_HS_G, PA_HS_S, PB_HS_S, PC_HS_S) Low-side (PA_LS_G, PB_LS_G, PC_LS_G, PA_LS_S, PB_LS_S, PC_LS_S) 	-7.0 to 75.0 -7.0 to 75.0 -7.0 to 18.0 -7.0 to 7.0	V	(5)
V_{ESD}	ESD voltage <ul style="list-style-type: none"> Human body model - HBM (All pins except for the pins listed below) Pins: PA_Boot, PA_HS_S, PA_HS_G, PB_Boot, PB_HS_S, PB_HS_G, PC_Boot, PC_HS_S, PC_HS_G, VPWR Charge device model - CDM Corner pins All other pins 	±2000 ±1000 ±750 ±300	V	(6)

Notes

- The device can withstand a voltage transient as defined by ISO7637 with peak voltage of 80 V.
- Short-circuit proof, the device is not be damaged or induce unexpected behavior due to shorts to external sources within this range.
- This voltage should not be applied without also taking voltage at HS_S and voltage at PX_LS_S into account.
- Actual operational limitations may differ from survivability limits. The $V_{LS} - V_{LS_S}$ differential and the $V_{BOOT} - V_{HS_S}$ differential must be greater than 3.0 V to insure the output gate drive maintains a commanded OFF condition on the output.
- ESD testing is performed in accordance with the human body model (HBM) ($C_{ZAP} = 100$ pF, $R_{ZAP} = 1500$ Ω) and the charge device model (CDM), robotic ($C_{ZAP} = 4.0$ pF).

Table 3. Maximum ratings (continued)

All voltages are with respect to V_{SS} unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Thermal ratings				
T_{STG}	Storage temperature	-55 to +150	°C	
T_J	Operating junction temperature	-40 to +150	°C	(7)
$R_{\theta JC}$	Thermal resistance • Junction-to-case	1.5	°C/W	(8)
T_{SOLDER}	Soldering temperature	Note 10	°C	(9)

Notes

7. In order to meet or exceed the expected reliability performance level over 10 years of continuous operation, the user must take measures to guarantee the device's *average* junction temperature does not exceed 125 °C. The device's maximum junction temperature remains as specified in the data sheet.
8. Case is considered EP - pin 55 under the body of the device. The actual power dissipation of the device is dependent on the operating mode, the heat transfer characteristics of the board and layout and the operating voltage. See [Figure 22](#) and [Figure 23](#) for examples of power dissipation profiles of two common configurations. Operation above the maximum operating junction temperature results in a reduction in reliability leading to malfunction or permanent damage to the device.
9. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
10. NXP's package reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For peak package reflow temperature and moisture sensitivity levels (MSL), Go to www.nxp.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxx enter 33xxx), and review parametrics.

4.2 Static electrical characteristics

Table 4. Static electrical characteristics

Characteristics noted under conditions $8.0\text{ V} \leq V_{PWR} = V_{SUP} \leq 48\text{ V}$, $-20\text{ }^\circ\text{C} \leq T_A \leq 105\text{ }^\circ\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^\circ\text{C}$ under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power inputs						
V_{PWR_ST}	VPWR supply voltage startup threshold	–	6.0	8.0	V	(11)
I_{SUP}	VSUP supply current, $V_{PWR} = V_{SUP} = 48\text{ V}$ <ul style="list-style-type: none"> RST and ENABLE = 5.0 V No output loads on gate drive pins, no PWM No output loads on gate drive pins, 20 kHz, 50% duty cycle 	– –	1.0 –	– 10	mA	
I_{PWR_ON}	VPWR supply current, $V_{PWR} = V_{SUP} = 48\text{ V}$ <ul style="list-style-type: none"> RST and ENABLE = 5.0 V No output loads on gate drive pins, no PWM, outputs initialized Output loads = 620 nC per FET, 20 kHz PWM 	– –	11 –	20 95	mA	(12)
I_{SUP} I_{PWR}	Sleep state supply current, RST = 0 V <ul style="list-style-type: none"> $V_{SUP} = 48\text{ V}$ $V_{PWR} = 48\text{ V}$ 	– –	14 56	30 110	μA	
V_{GATESS}	Sleep state output gate voltage <ul style="list-style-type: none"> IG < 100 μA 	–	–	1.3	V	
V_{Boot}	Trickle charge pump (bootstrap voltage) <ul style="list-style-type: none"> $V_{SUP} = 14\text{ V}$ 	22	28	32	V	
V_F	Bootstrap diode forward voltage at 10 mA	–	–	1.2	V	

VDD internal regulator

V_{DD}	V_{DD} output voltage, $V_{PWR} = 8.0\text{ V}$ to 48 V, C = 0.47 μF <ul style="list-style-type: none"> External load $I_{DD_EXT} = 0\text{ mA}$ to 1.0 mA 	4.5	–	5.5	V	(13)
I_{DD}	Internal V_{DD} supply current, $V_{DD} = 5.5\text{ V}$, no external load	–	–	12	mA	

VLS regulator

I_{PEAK}	Peak output current, $V_{PWR} = 16\text{ V}$, $V_{LS} = 10\text{ V}$	350	600	800	mA	
V_{LS}	Linear regulator output voltage, $I_{VLS} = 0\text{ mA}$ to 60 mA, $V_{PWR} > V_{LS} + 2.0\text{ V}$	13.5	15	17	V	(14)
V_{THVLS}	VLS disable threshold ⁽¹⁵⁾	7.5	8.0	8.5	V	

Notes

- Operation with the charge pump is recommended when minimum system voltage could be less than 14 V. V_{PWR} must exceed this threshold in order for the charge pump and V_{DD} regulator to startup and drive V_{PWR} to > 8.0 V. Once V_{PWR} exceeds 8.0 V, the circuits continues to operate even if system voltage drops below 6.0 V.
- This parameter is guaranteed by design. It is not production tested.
- Minimum external capacitor for stable V_{DD} operation is 0.47 μF .
- Recommended external capacitor for the V_{LS} regulator is 2.2 μF low ESR at each pin VLS and VLS_CAP.
- When V_{LS} is less than this value, the outputs are disabled and holdoff circuits are active. Recovery requires initialization when V_{LS} rises above this threshold again. A filter delay of approximately 700 ns on the comparator output eliminates responses to spurious transients on V_{LS} .

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions $8.0\text{ V} \leq V_{PWR} = V_{SUP} \leq 48\text{ V}$, $-20\text{ }^\circ\text{C} \leq T_A \leq 105\text{ }^\circ\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^\circ\text{C}$ under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Charge pump						
$R_{DS(on)_HS}$ $R_{DS(on)_LS}$ V_{THREG}	Charge pump • High-side switch on resistance • Low-side switch on resistance • Regulation threshold difference	– – 250	6.0 5.0 500	10 9.4 900	Ω Ω mV	(16), (18)
V_{CP}	Charge pump output voltage • $I_{OUT} = 40\text{ mA}$, $6.0\text{ V} < V_{SYS} < 8.0\text{ V}$ • $I_{OUT} = 40\text{ mA}$, $V_{SYS} \geq 8.0\text{ V}$	8.5 12	9.5 –	– –	V	(17), (18)
Gate drive						
$R_{DS(on)_H_SRC}$	High-side driver on resistance (sourcing) • $V_{PWR} = V_{SUP} = 16\text{ V}$, $-20\text{ }^\circ\text{C} \leq T_A \leq 25\text{ }^\circ\text{C}$ • $V_{PWR} = V_{SUP} = 16\text{ V}$, $25\text{ }^\circ\text{C} < T_A \leq 105\text{ }^\circ\text{C}$	– –	– –	6.0 8.5	Ω	
$R_{DS(on)_H_SINK}$	High-side driver on resistance (sinking) • $V_{PWR} = V_{SUP} = 16\text{ V}$	–	–	3.0	Ω	
I_{HS_INJ}	High-side current injection allowed without malfunction	–	–	0.5	A	(18), (19)
$R_{DS(on)_L_SRC}$	Low-side driver on resistance (sourcing) • $V_{PWR} = V_{SUP} = 16\text{ V}$, $-20\text{ }^\circ\text{C} \leq T_A \leq 25\text{ }^\circ\text{C}$ • $V_{PWR} = V_{SUP} = 16\text{ V}$, $25\text{ }^\circ\text{C} < T_A \leq 105\text{ }^\circ\text{C}$	– –	– –	6.0 8.5	Ω	
$R_{DS(on)_L_SINK}$	Low-side driver on-resistance (sinking) • $V_{PWR} = V_{SUP} = 16\text{ V}$	–	–	3.0	Ω	
I_{LS_INJ}	Low-side current injection allowed without malfunction	–	–	0.5	A	(18), (19)
V_{GS_H} V_{GS_L}	Gate source voltage, $V_{PWR} = V_{SUP} = 48\text{ V}$ • High-side, $I_{GATE} = 0$ • Low-side, $I_{GATE} = 0$	13 13	14.8 15.4	16.5 17	V	(20)
$V_{HS_G_HOLD}$	Reverse high-side gate holding voltage Gate output holding current = $2.0\text{ }\mu\text{A}$ Gate output holding current = $5.0\text{ }\mu\text{A}$, $V_{SUP} < 26\text{ V}$ Gate output holding current = $5.0\text{ }\mu\text{A}$, $V_{SUP} < 48\text{ V}$	– – –	10 10 –	15 15 15	V	(21)

Notes

- When V_{LS} is this amount below the normal V_{LS} linear regulation threshold, the charge pump is enabled.
- V_{SYS} is the system voltage on the input to the charge pump. Recommended external components: $1.0\text{ }\mu\text{F}$ MLC, MUR 120 diode.
- This parameter is a design characteristic, not production tested.
- Current injection only occurs during output switch transitions. The IC is immune to specified injected currents for a duration of approximately $1.0\text{ }\mu\text{s}$ after an output switch transition. $1.0\text{ }\mu\text{s}$ is sufficient for all intended applications of this IC.
- If a slightly higher gate voltage is required, larger bootstrap capacitors are required. At high duty cycles, the bootstrap voltage may not recover completely, leading to a higher output on-resistance. This effect can be minimized by using low ESR capacitors for the bootstrap and the VLS capacitors.
- High-side gate holding voltage is the voltage between the gate and source of the high-side FET when held in an on condition. The trickle charge pump supplies bias and holding current for the high-side FET gate driver and output to maintain voltages after bootstrap events. This parameter is a design characteristic, not production tested.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions $8.0\text{ V} \leq V_{PWR} = V_{SUP} \leq 48\text{ V}$, $-20\text{ }^\circ\text{C} \leq T_A \leq 105\text{ }^\circ\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^\circ\text{C}$ under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Overcurrent comparator						
V_{CM}	Common mode input range	2.0	–	$V_{DD}-0.02$	V	(23)
V_{OS_OC}	Input offset voltage	-50	–	50	mV	
V_{OC_HYST}	Overcurrent comparator threshold hysteresis	50		300	mV	(22)
V_{OH} V_{OL}	Output voltage • High Level at $I_{OH} = -500\text{ }\mu\text{A}$ • Low Level at $I_{OL} = 500\text{ }\mu\text{A}$	$0.85 V_{DD}$ –	– –	V_{DD} 0.5	V	
hold off circuit						
I_{HOLD}	Hold off current (at each GATE pin) • $3.0\text{ V} < V_{SUP} < 48\text{ V}$, $V_{GATE} = 1.0\text{ V}$	10	–	300	μA	(24)
Phase comparator						
V_{IH_TH}	High level input voltage threshold	$0.5 V_{SUP}$	–	$0.65 V_{SUP}$	V	
V_{IL_TH}	Low level input voltage threshold	$0.3 V_{SUP}$	–	$0.45 V_{SUP}$	V	
V_{OH}	High level output voltage at $I_{OH} = -500\text{ }\mu\text{A}$	$0.85 V_{DD}$	–	V_{DD}	V	
V_{OL}	Low level output voltage at $I_{OL} = 500\text{ }\mu\text{A}$	–	–	0.5	V	
R_{IN}	High-side source input resistance	–	40	–	$\text{k}\Omega$	(22), (27)
Desaturation detector						
V_{DES_TH}	Desaturation detector threshold	1.2	1.4	1.6	V	(25)
Current sense amplifier						
R_S	Recommended external series resistor (see Figure 9)	–	1.0	–	$\text{k}\Omega$	
R_{FB}	Recommended external feedback resistor (see Figure 9) • Limited by the output voltage dynamic range	5.0	–	15	$\text{k}\Omega$	(28)
V_{ID}	Maximum input differential voltage (see Figure 9) • $V_{ID} = V_{AMP_P} - V_{AMP_N}$	-800	–	800	mV	
V_{CM}	Input common mode range	-0.5	–	3.0	V	(22), (26)
V_{OS}	Input offset voltage • $R_S = 1.0\text{ k}\Omega$, $V_{CM} = 0.0\text{ V}$	-15	–	15	mV	
$\delta V_{OS}/\delta T$	Input offset voltage drift	–	-10	–	$\mu\text{V}/^\circ\text{C}$	(22)

Notes

22. This parameter is a design characteristic, not production tested.
23. As long as one input is in the common mode range there is no phase inversion on the output.
24. The hold off circuit is designed to operate over the full operating range of V_{SUP} . The specification indicates the conditions used in production test. Hold off is activated at V_{POR} or V_{THVLS} .
25. Desaturation is measured as the voltage drop below V_{SUP} , thus the threshold is compared to the drain-source voltage of the external high-side FET. See [Figure 5](#).
26. As long as one input is within V_{CM} the output is guaranteed to have the correct phase. Exceeding the common mode rails on one input does not cause a phase inversion on the output.
27. Input resistance is impedance from the high-side source and is referenced to V_{SS} . Approximate tolerance is $\pm 20\%$.
28. The current sense amplifier is unity gain stable with a phase margin of approximately 45° . See [Figure 10](#).

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions $8.0\text{ V} \leq V_{\text{PWR}} = V_{\text{SUP}} \leq 48\text{ V}$, $-20\text{ }^\circ\text{C} \leq T_{\text{A}} \leq 105\text{ }^\circ\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_{\text{A}} = 25\text{ }^\circ\text{C}$ under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Current sense amplifier (continued)						
I_{b}	Input bias current • $V_{\text{CM}} = 2.0\text{ V}$	-200	–	+200	nA	
I_{OS}	Input offset current • $I_{\text{OS}} = I_{\text{AMP_P}} - I_{\text{AMP_N}}$	-80	–	+80	nA	
$\delta I_{\text{OS}}/\delta T$	Input offset current drift	–	40	–	pA/°C	(29)
V_{OH} V_{OL}	Output voltage • High level with $R_{\text{LOAD}} = 10\text{ k}\Omega$ to V_{SS} • Low level with $R_{\text{LOAD}} = 10\text{ k}\Omega$ to V_{DD}	$V_{\text{DD}}-0.2$ –	– –	V_{DD} 0.2	V	
R_{I}	Differential input resistance	1.0	–	–	M Ω	
I_{SC}	Output short-circuit current	5.0	–	–	mA	
C_{I}	Common mode input capacitance at 10 kHz	–	–	10	pF	(29), (30)
CMRR	Common mode rejection ratio at DC • $\text{CMRR} = 20 \cdot \log((V_{\text{OUT_DIFF}}/V_{\text{IN_DIFF}}) \cdot (V_{\text{IN_CM}}/V_{\text{OUT_CM}}))$	60	80	–	dB	
A_{OL}	Large signal open loop voltage gain (DC)	–	78	–	dB	(29), (30)
NL	Nonlinearity • $R_{\text{L}} = 1.0\text{ k}\Omega$, $C_{\text{L}} = 500\text{ pF}$, $0.3 < V_{\text{O}} < 4.8\text{ V}$, Gain = 5.0 to 15	-1.0	–	+1.0	%	(29), (30)

Supervisory and control circuits

V_{IH} V_{IL}	Logic inputs (Px_LS, Px_HS, EN1, EN2) • High level input voltage threshold • Low level input voltage threshold	2.1 –	– –	– 0.9	V	(32)
V_{IH} V_{IL}	Logic inputs (SI, SCLK, CS) • High level input voltage threshold • Low level input voltage threshold	2.1 –	– –	– 0.9	V	(31), (32)
V_{IHYS}	Input logic threshold hysteresis • Inputs Px_LS, SI, SCLK, CS, Px_HS, EN1, EN2	100	250	450	mV	(31)
I_{INPD}	Input pull-down current, (Px_LS, SI, SCLK, EN1, EN2) • $0.3 V_{\text{DD}} \leq V_{\text{IN}} \leq V_{\text{DD}}$	8.0	–	18	μA	

Notes

29. This parameter is a design characteristic, not production tested.
30. Without considering any offsets such as input offset voltage, internal mismatch and assuming no tolerance error in external resistors.
31. This parameter is guaranteed by design, not production tested.
32. Logic threshold voltages derived relative to a 3.3 V 10% system.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions $8.0\text{ V} \leq V_{\text{PWR}} = V_{\text{SUP}} \leq 48\text{ V}$, $-20\text{ }^\circ\text{C} \leq T_{\text{A}} \leq 105\text{ }^\circ\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_{\text{A}} = 25\text{ }^\circ\text{C}$ under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Supervisory and control circuits (continued)						
I_{INPU}	Input pull-up current, (CS, Px_HS) • $0 \leq V_{\text{IN}} \leq 0.7 V_{\text{DD}}$	10	–	25	μA	(34)
C_{IN}	Input capacitance • $0.0\text{ V} \leq V_{\text{IN}} \leq 5.5\text{ V}$	–	15	–	pF	(33)
$V_{\text{TH_RST}}$	RST threshold	1.0	–	2.1	V	(35)
R_{RST}	RST pull-down resistance • $0.3 V_{\text{DD}} \leq V_{\text{IN}} \leq V_{\text{DD}}$	40	60	85	$\text{k}\Omega$	
V_{POR}	Power-off rst threshold, (V_{DD} falling)	3.4	4.0	4.5	V	
V_{SOH}	SO high level output voltage • $I_{\text{OH}} = 1.0\text{ mA}$	$0.9 V_{\text{DD}}$	–	–	V	
V_{SOL}	SO low level output voltage • $I_{\text{OL}} = 1.0\text{ mA}$	–	–	$0.1 V_{\text{DD}}$	V	
$I_{\text{SO_LEAK_T}}$	SO tri-state leakage current • $\text{CS} = 0.7 V_{\text{DD}}$, $0.3 V_{\text{DD}} \leq V_{\text{SO}} \leq 0.7 V_{\text{DD}}$	-1.0	–	1.0	μA	
$C_{\text{SO_T}}$	SO tri-state capacitance • $0.0\text{ V} \leq V_{\text{IN}} \leq 5.5\text{ V}$	–	15	–	pF	(33), (36)
V_{OH}	INT high level output voltage • $I_{\text{OH}} = -500\text{ }\mu\text{A}$	$0.85 V_{\text{DD}}$	–	V_{DD}	V	
V_{OL}	INT low level output voltage • $I_{\text{OL}} = 500\text{ }\mu\text{A}$	–	–	0.5	V	

Thermal warning

T_{WARN}	Thermal warning temperature	150	170	185	$^\circ\text{C}$	(33), (37)
T_{HYST}	Thermal hysteresis	8.0	10	12	$^\circ\text{C}$	(33)

Notes

33. This parameter is guaranteed by design, not production tested.
34. Pull-up circuits does not allow back biasing of V_{DD} .
35. There are two elements in the RST circuit: 1) one generally lower threshold enables the internal regulator; 2) the second removes the reset from the internal logic.
36. This parameter applies to the OFF state (tri-stated) condition of SO is guaranteed by design but is not production tested.
37. The thermal warning circuit does not force IC shutdown above this temperature. It is possible to set a bit in the MASK register to generate an interrupt when overtemperature is detected, and the status bit always indicates if any of the three individual thermal warning circuits in the IC sense a fault.

4.3 Dynamic electrical characteristics

Table 5. Dynamic electrical characteristics

Characteristics noted under conditions $8.0\text{ V} \leq V_{\text{PWR}} = V_{\text{SUP}} \leq 48\text{ V}$, $-20\text{ }^\circ\text{C} \leq T_{\text{A}} \leq 105\text{ }^\circ\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_{\text{A}} = 25\text{ }^\circ\text{C}$ under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Internal regulators						
$t_{\text{PU_VDD}}$	V_{DD} power-up time (until INT high) • $8.0\text{ V} \leq V_{\text{PWR}}$	–	–	2.0	ms	(38), (45)
$t_{\text{PU_VLS}}$	VLS power-up time • $16\text{ V} \leq V_{\text{PWR}}$	–	–	2.0	ms	(39), (45)
Charge pump						
F_{OSC}	Charge pump oscillator frequency	90	125	190	kHz	
SR_{CP}	Charge pump slew rate	–	100	–	V/ μs	(40)
Gate drive						
t_{ONH}	High-side turn on time • Transition time from 1.0 V to 10 V, load: $C = 500\text{ pF}$, $R_{\text{G}} = 0$, (Figure 7)	–	20	35	ns	(41)
$t_{\text{D_ONH}}$	High-side turn on delay • Delay from command to 1.0 V, (Figure 7)	130	265	386	ns	(42)
t_{OFFH}	High-side turn off time • Transition time from 10 V to 1.0 V, load: $C = 500\text{ pF}$, $R_{\text{G}} = 0$, (Figure 8)	–	20	35	ns	(41)
$t_{\text{D_OFFH}}$	High-side turn off delay • Delay from command to 10 V, (Figure 8)	130	265	386	ns	(42)
t_{ONL}	Low-side turn on time • Transition time from 1.0 V to 10 V, load: $C = 500\text{ pF}$, $R_{\text{G}} = 0$, (Figure 7)	–	20	35	ns	(41)
$t_{\text{D_ONL}}$	Low-side turn on delay • Delay from command to 1.0 V, (Figure 7)	130	265	386	ns	(42)
t_{OFFL}	Low-side turn off time • Transition time from 10 V to 1.0 V, load: $C = 500\text{ pF}$, $R_{\text{G}} = 0$, (Figure 8)	–	20	35	ns	(41)
$t_{\text{D_OFFL}}$	Low-side turn off delay • Delay from command to 10 V, (Figure 8)	130	265	386	ns	(42)
$t_{\text{D_DIFF}}$	Same phase command delay match	-20	0.0	+20	ns	(43)
t_{DUR}	Thermal filter duration	8.0	–	30	μs	(44)

Notes

38. The power-up time of the IC depends in part on the time required for this regulator to charge up the external filter capacitor on V_{DD} .
39. The power-up time of the IC depends in part on the time required for this regulator to charge up the external filter capacitors on VLS and VLS_CAP. This delay includes the expected time for V_{DD} to rise.
40. The charge pump operating at 12 V V_{SYS} , 1.0 μF pump capacitor, MUR120 diodes and 47 μF filter capacitor.
41. This parameter is guaranteed by characterization, not production tested.
42. These delays include all logic delays except deadtime. All internal logic is synchronous with the internal clock. The total delay includes one clock period for state machine decision block, an additional clock period for fullon mux logic, input synchronization time and output driver propagation delay. Subtract one clock period for operation in fullon mode which bypasses the state machine decision block. Synchronization time accounts for up to one clock period of variation. See [Figure 6](#).
43. The maximum separation or overlap of the high and low-side gate drives, due to propagation delays when commanding one on and the other off simultaneously, is guaranteed by design.
44. The output of the overtemperature comparator goes through a digital filter before generating a warning or interrupt.
45. This specification is based on capacitance of 0.47 μF on VDD, 2.2 μF on VLS and 2.2 μF on VLS_CAP.

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions $8.0\text{ V} \leq V_{PWR} = V_{SUP} \leq 48\text{ V}$, $-20\text{ }^\circ\text{C} \leq T_A \leq 105\text{ }^\circ\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^\circ\text{C}$ under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Gate drive (continued)						
t_{DC}	Duty cycle	0.0	–	96	%	(46), (47)
t_{DC}	100% duty cycle duration	–	–	Unlimited	s	(46), (47)
t_{MAX}	Maximum programmable deadtime	10.2	15	19.6	μs	(48)
Overcurrent comparator						
t_{OC}	Overcurrent protection filter time	0.9	–	3.5	μs	
t_{ROC}	Rise time (OC_OUT) • 10% - 90% • $C_L = 100\text{ pF}$	10	–	240	ns	
t_{FOC}	Fall time (OC_OUT) • 90% - 10% • $C_L = 100\text{ pF}$	10	–	200	ns	
Desaturation detector and phase comparator						
t_R t_F	Phase comparator propagation delay time to 50% of V_{DD} ; $C_L \leq 100\text{ pF}$ • Rising Edge Delay • Falling Edge Delay	– –	– –	200 350	ns	
t_{MATCH}	Phase comparator match (prop delay mismatch of three phases) • $C_L = 100\text{ pF}$	–	–	100	ns	(46)
t_{BLANK}	Desaturation and phase error blanking time	4.7	7.1	9.1	μs	(49)
t_{FILT}	Desaturation filter time (filter time is digital) • Fault must be present for this time to trigger	640	937	1231	ns	(46)
Current sense amplifier						
t_{SETTLE}	Output settle time to 99% • $R_L = 1.0\text{ k}\Omega$, $C_L = 500\text{ pF}$, $0.3\text{ V} < V_O < 4.8\text{ V}$, Gain = 5 to 15	–	1.0	2.0	μs	(46), (50)
t_{IS_RISE}	Output rise time to 90% • $R_L = 1.0\text{ k}\Omega$, $C_L = 500\text{ pF}$, $0.3\text{ V} < V_O < 4.8\text{ V}$, Gain = 5.0 to 15	–	–	1.0	μs	(51)
t_{IS_FALL}	Output fall time to 10% • $R_L = 1.0\text{ k}\Omega$, $C_L = 500\text{ pF}$, $0.3\text{ V} < V_O < 4.8\text{ V}$, Gain = 5.0 to 15	–	–	1.0	μs	(51)
SR_5	Slew rate at gain = 5.0 • $R_L = 1.0\text{ k}\Omega$, $C_L = 20\text{ pF}$	5.0	–	–	$\text{V}/\mu\text{s}$	(46)
f_M	Phase margin at gain = 5.0	–	30	–	°	(46)
G_{BW}	Unity gain bandwidth • $R_L = 1.0\text{ k}\Omega$, $C_L = 100\text{ pF}$	–	20	–	MHz	(46)

Notes

46. This parameter is guaranteed by design, not production tested.
47. As duty cycle approaches the limit of 100% or 0% there is a maximum and minimum which is not achievable due to deadtime, propagation delays, switching times and charge time of the bootstrap capacitor (for the high-side FET). 0% is available by definition (FET always off) and unlimited on (100%) is possible as long as gate charge maintenance current is within the trickle charge pump capacity.
48. A minimum deadtime of 0.0 can be set via an SPI command. When deadtime is set via a deadtime command, a minimum of 1 clock cycle duration and a maximum of 255 clock cycles is set using the internal time base clock as a reference. Commands exceeding this value limits at this value.
49. Blanking time, t_{BLANK} , is applied to all phases simultaneously when switching on any output FET. This precludes false errors due to system noise during the switching event.
50. Without considering any offsets such as input offset voltage, internal mismatch and assuming no tolerance error in external resistors.
51. Rise and fall times are measured from the transition of a step function on the input to 90% of the change in output voltage.

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions $8.0\text{ V} \leq V_{\text{PWR}} = V_{\text{SUP}} \leq 48\text{ V}$, $-20\text{ }^\circ\text{C} \leq T_{\text{A}} \leq 105\text{ }^\circ\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_{\text{A}} = 25\text{ }^\circ\text{C}$ under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Current sense amplifier (continued)						
BW_G	Bandwidth at gain = 15 • $R_L = 1.0\text{ k}\Omega$, $C_L = 50\text{ pF}$	2.0	–	–	MHz	(52)
CMR	Common mode rejection (CMR) with V_{IN} • $V_{\text{IN_CM}} = 400\text{ mV} \cdot \sin(2 \cdot \pi \cdot \text{freq} \cdot t)$ • $V_{\text{IN_DIF}} = 0.0\text{ V}$, $R_S = 1.0\text{ k}\Omega$ • $R_{\text{FB}} = 15\text{ k}\Omega$, $V_{\text{REFIN}} = 0.0\text{ V}$ CMR = $20 \cdot \log(V_{\text{OUT}}/V_{\text{IN_CM}})$ • Freq = 100 kHz • Freq = 1.0 MHz • Freq = 10 MHz	50 40 30	– – –	– – –	dB	(52)

Supervisory and control circuits

t_{PROP}	EN1 and EN2 propagation delay	–	–	280	ns	
t_{RINT}	INT rise time $CL = 100\text{ pF}$	10	–	250	ns	
t_{FINT}	INT fall time $CL = 100\text{ pF}$	10	–	200	ns	
t_{PROPINT}	INT propagation time	–	–	250	ns	
t_{TRRST}	RST transition time (rise and fall)	–	–	1.25	μs	(52), (53)

SPI interface timing

f_{OP}	Maximum frequency of SPI operation	–		4.0	MHz	
f_{TB}	Internal time base	13	17	25	MHz	
TC_{TB}	Internal time base drift from value at $25\text{ }^\circ\text{C}$	-5.0	–	5.0	%	(54)
t_{LEAD}	Falling edge of CS to rising edge of SCLK (required setup time)	100	–	–	ns	(54)
t_{LAG}	Falling edge of SCLK to rising edge of CS (required setup time)	100	–	–	ns	(54)
t_{SISU}	SI to falling edge of SCLK (required setup time)	25	–	–	ns	(54)
t_{SIHOLD}	Falling edge of SCLK to SI (required setup time)	25	–	–	ns	(54)
t_{RSI}	SI, CS, SCLK signal rise time	–	5.0	–	ns	(54), (55)
t_{FSI}	SI, CS, SCLK signal fall time	–	5.0	–	ns	(54), (55)
t_{SOEN}	Time from falling edge of CS to SO low-impedance	–	55	100	ns	(54), (56)
t_{SODIS}	Time from rising edge of CS to SO high-impedance	–	100	125	ns	(54), (57)
t_{VALID}	Time from rising edge of SCLK to SO data valid	–	80	125	ns	(54), (58)
t_{DT}	Time from rising edge of CS to falling edge of the next CS	200	–	–	ns	(54)

Notes

52. This parameter is guaranteed by design, not production tested.
53. t_{TRRST} is given as a design guideline. The bounds for this specification are $V_{\text{PWR}} \leq 58\text{ V}$, total capacitance on VLS $> 1.0\text{ }\mu\text{F}$.
54. This parameter is guaranteed by design, not production tested.
55. Rise and Fall time of incoming SI, CS, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
56. Time required for valid output status data to be available on SO pin.
57. Time required for output states data to be terminated at SO pin.
58. Time required to obtain valid data out from SO following the rise of SCLK with 200 pF load.

4.4 Timing diagrams

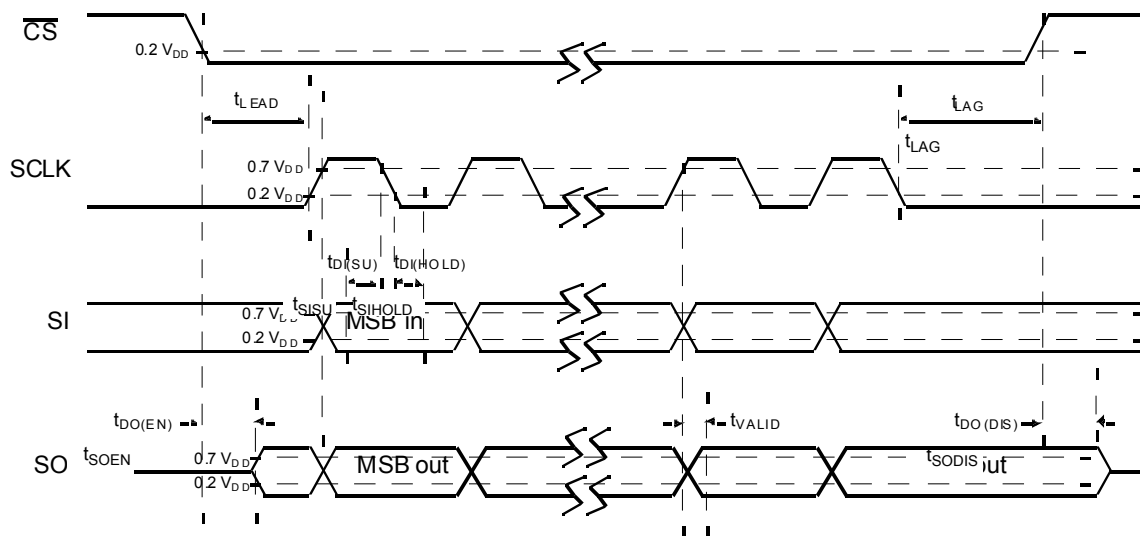


Figure 4. SPI interface timing

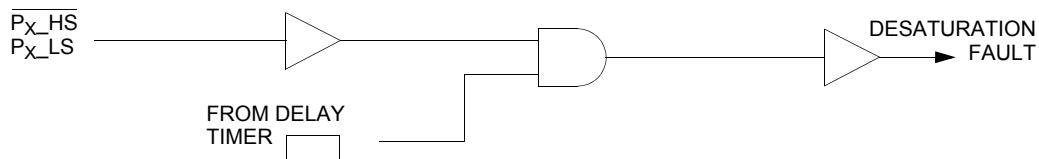


Figure 5. Desaturation blanking and filtering detail

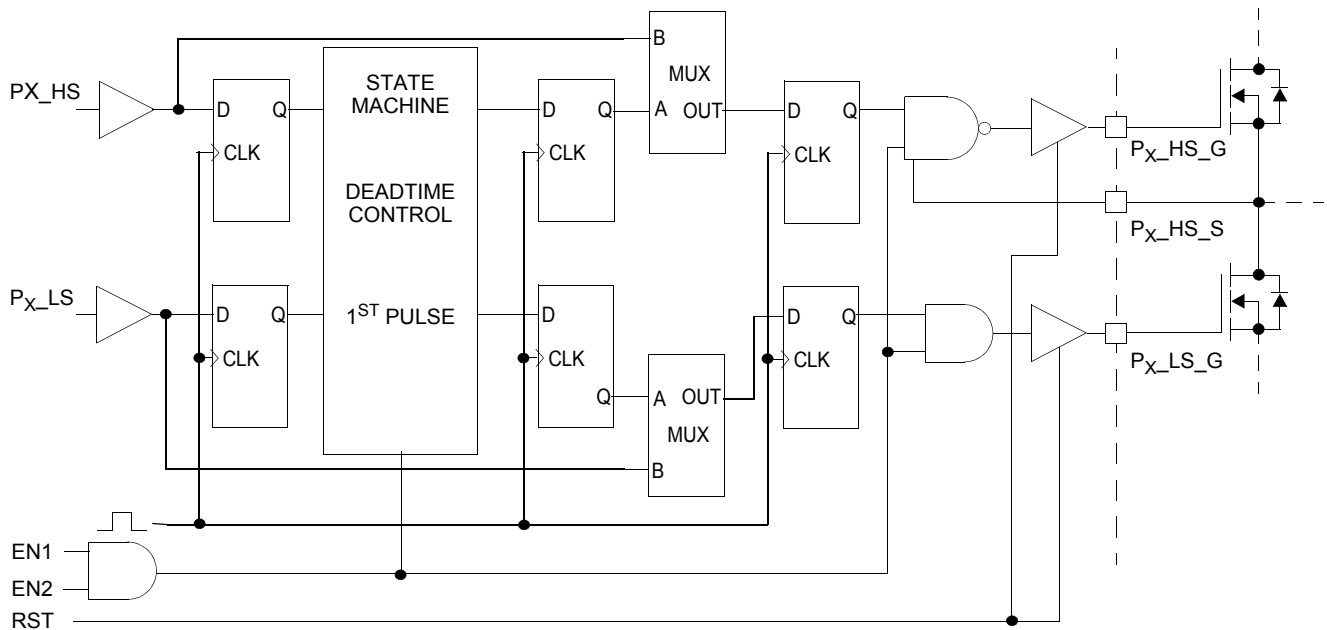


Figure 6. Deadtime control delays

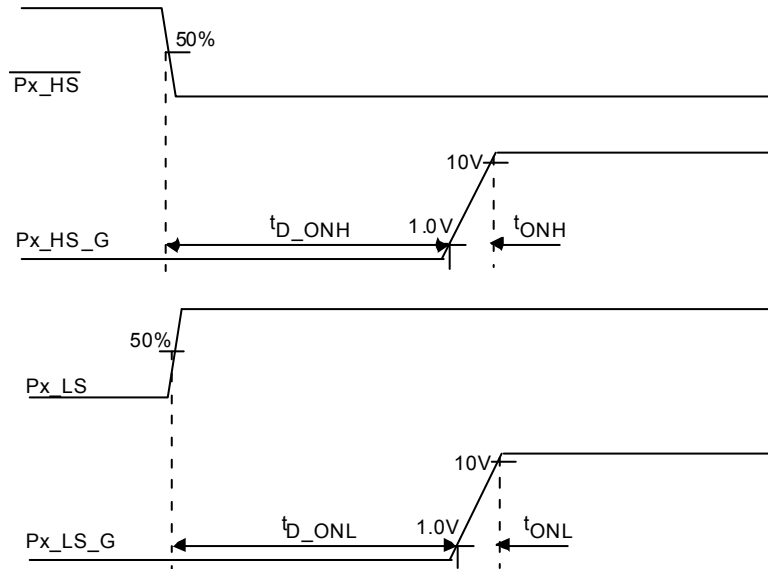


Figure 7. Driver turn-on time and turn-on delay

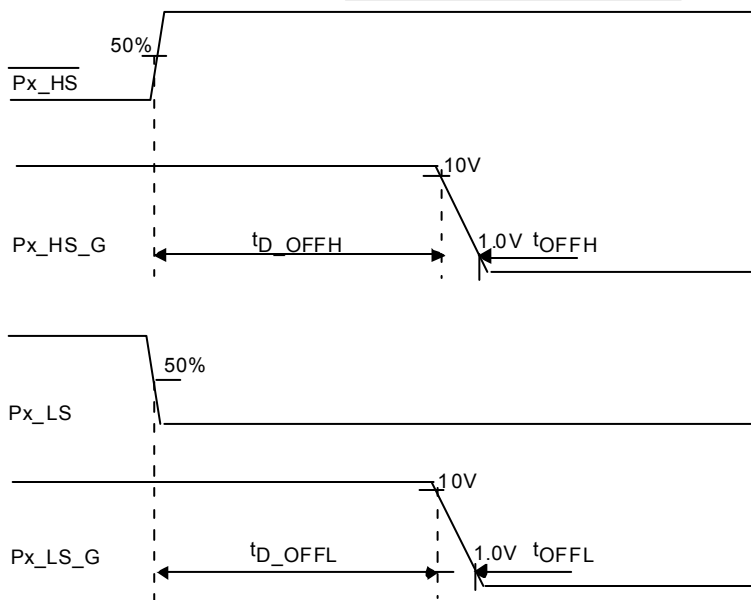


Figure 8. Driver turn-off time and turn-off delay

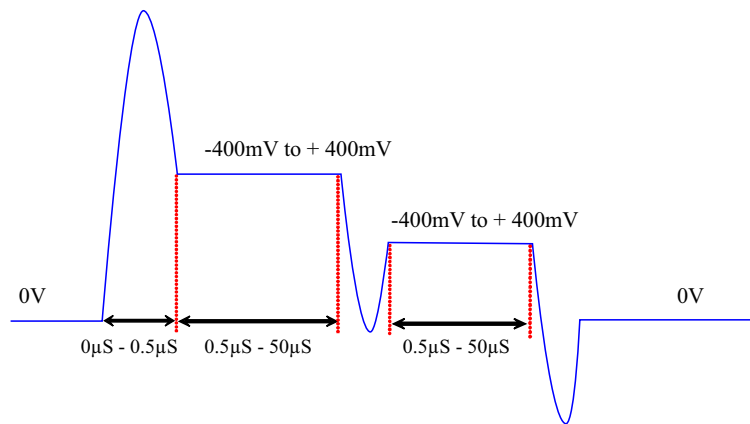
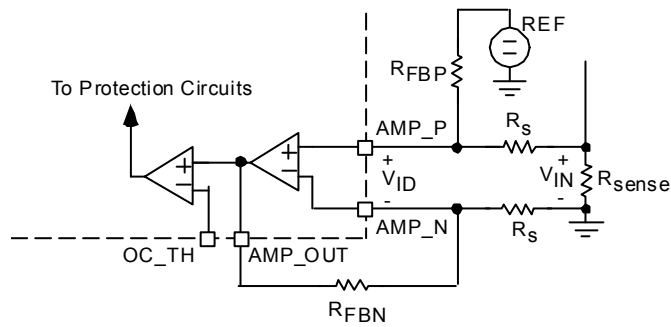


Figure 9. Current amplifier and input waveform (V_{IN} voltage across R_{SENSE})

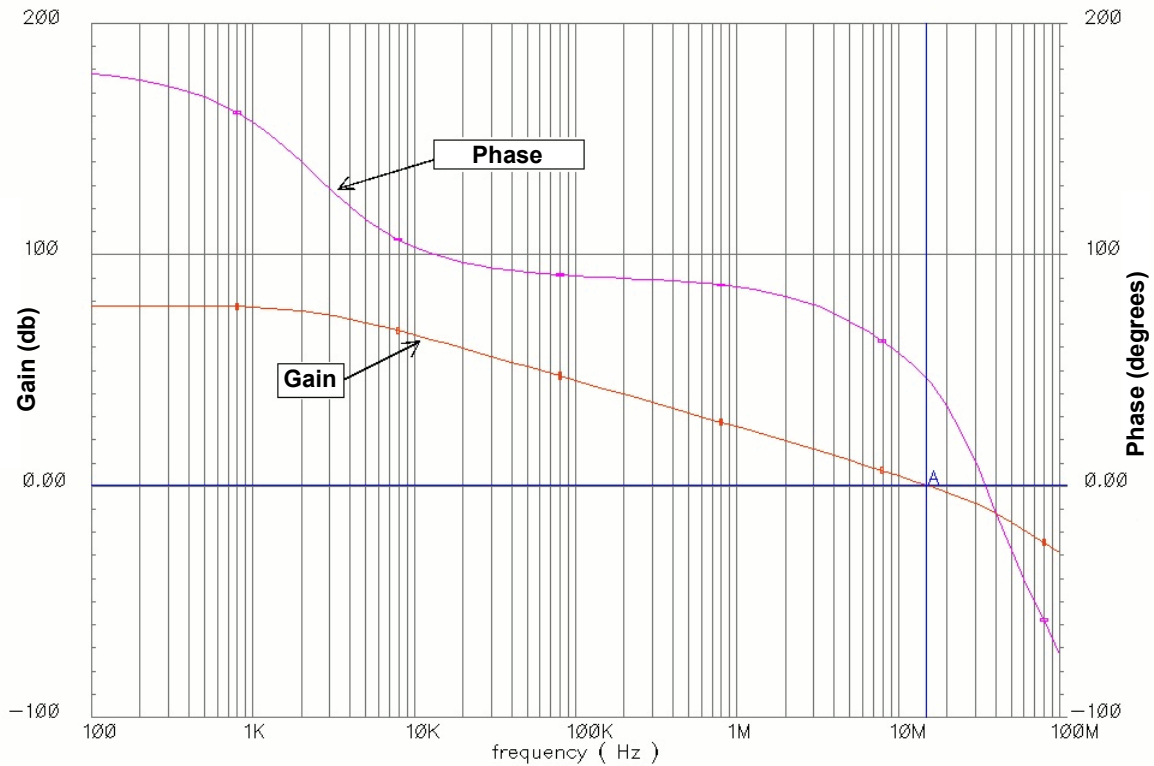


Figure 10. Typical amplifier open-loop gain and phase vs. frequency

5 Functional descriptions

5.1 Introduction

The 34GD3000 provides an interface between an MCU and the external FETs used to drive three phase motors. A typical external FET may have an on resistance of 4.0 mΩ or less and could require a gate charge of over 400 nC to fully turn on. The IC can operate in 12 V to 48 V environments.

There are many methods for controlling three phase motor systems, so the IC enforces few constraints in driving the FETs. The 34GD3000 does however provide deadtime (cross-over) blanking and logic in order to protect the external FETs. Under special configurations, both of these features can be overridden, allowing both FETs in a phase to be simultaneously enabled.

An SPI port is used to configure the 34GD3000's modes.

5.2 Functional pin description

5.2.1 Phase A (PHASEA)

This pin is the totem pole output of the Phase A comparator. This output is low when the voltage on Phase A high-side source (source of the high-side load FET) is less than 50 percent of V_{SUP} .

5.2.2 Power ground (PGND)

This pin is power ground for the charge pump. It should be connected to VSS, however routing to a single point ground on the PCB may help to isolate charge pump noise.

5.2.3 Enable 1 and Enable 2 (EN1, EN2)

Both of these logic signal inputs must be high to enable any gate drive output. When either or both are low, the internal logic (SPI port, etc.) still functions normally, but all gate drives are forced off (external power FET gates pulled low). The signal is asynchronous.

When EN1 and EN2 return high to enable the outputs, each LS driver must be pulsed on before the corresponding HS driver can be commanded on. This ensures the bootstrap capacitors are charged. [See Initialization requirements on page 39.](#)

5.2.4 Reset (RST)

When the reset pin is low the integrated circuit (IC) is in a low-power state. In this mode all outputs are disabled, internal bias circuits are turned off, and a small pull-down current is applied to the output gate drives. The internal logic resets within 77 ns of RESET going low. When RST is low, the IC consumes minimal current.

5.2.5 Charge pump out (PUMP)

This pin is the switching node of the charge pump circuit. The output of the internal charge pump support circuit. When the charge pump is used, it is connected to the external pumping capacitor. This pin may be left floating if the charge pump is not required.

5.2.6 Charge pump input (VPUMP)

This pin is the input supply for the charge pump circuit. When the charge pump is required, this pin should be connected to a polarity protected supply. This input should never be connected to a supply greater than 40 V. If the charge pump is not required this pin may be left floating.

5.2.7 VSUP input (VSUP)

The supply voltage pin should be connected to the common connection of the high-side FETs. It is the reference bias for the phase comparators and desaturation comparator. It is also used to provide power to the internal steady state trickle charge pump and to energize the hold off circuit.

5.2.8 Phase B (PHASEB)

This pin is the totem pole output of the Phase B comparator. This output is low when the voltage on Phase B high-side source (source of the high-side load FET) is less than 50 percent of V_{SUP} .

5.2.9 Phase C (PHASEC)

This pin is the totem pole output of the Phase C comparator. This output is low when the voltage on Phase C high-side source (source of the high-side load FET) is less than 50 percent of V_{SUP} .

5.2.10 Phase A high-side input (PA_HS)

This input logic signal pin enables the high-side driver for Phase A. The signal is active low and is pulled up by an internal current source.

5.2.11 Phase A low-side input (PA_LS)

This input logic signal pin enables the low-side driver for Phase A. The signal is active high and is pulled down by an internal current sink.

5.2.12 VDD voltage regulator (VDD)

VDD is an internally generated 5.0 V supply. The internal regulator provides continuous power to the IC and is a supply reference for the SPI port. A 0.47 μF (min) decoupling capacitor must be connected to this pin. This regulator is intended for internal IC use and can supply only a small (1.0 mA) external load current.

A power-on-reset (POR) circuit monitors this pin and until the voltage rises above the threshold, the internal logic is reset; driver outputs is tri-stated and SPI communication disabled. The VDD regulator can be disabled by asserting the RST signal low. The VDD regulator is powered from the VPWR pin.

5.2.13 Phase B high-side control input (PB_HS)

This pin is the input logic signal, enabling the high-side driver for Phase B. The signal is active low, and is pulled up by an internal current source.

5.2.14 Phase B low-side input (PB_LS)

This pin is the input logic signal, enabling the low-side driver for Phase B. The signal is active high, and is pulled down by an internal current sink.

5.2.15 Interrupt (INT)

The INTERRUPT pin is a totem pole logic output. When a fault is detected, this pin pulls high until it is cleared by executing the clear interrupt command via the SPI port. The faults capable of causing an interrupt can be masked via the MASK0 and MASK1 SPI registers to customize the response.

5.2.16 Chip select (CS)

Chip select is a logic input which frames the SPI commands and enables the SPI port. This signal is active low, and is pulled up by an internal current source.

5.2.17 Serial in (SI)

The SERIAL IN pin is used to input data to the SPI port. Clocked on the falling edge of SCLK, it is the most significant bit (MSB) first. This pin is pulled down by an internal current sink.

5.2.18 Serial clock (SCLK)

This logic input is the clock is used for the SPI port. The SCLK typically runs at 3.0 MHz (up to 5.0 MHz) and is pulled down by an internal current sink.

5.2.19 Serial out (SO)

Output data for the SPI port streams from this pin. It is tri-stated until CS is low. New data appears on rising edges of SCLK in preparation for latching by the falling edge of SCLK on the master.

5.2.20 Phase C low-side input (PC_LS)

This input logic pin enables the low-side driver for Phase C. This pin is an active high, and is pulled down by an internal current sink.

5.2.21 Phase C high-side input (PC_HS)

This input logic pin enables the high-side driver for Phase C. This signal is active low, and is pulled up by an internal current source.

5.2.22 Amplifier output (AMP_OUT)

This pin is the output for the current sensing amplifier. It is also the sense input to the overcurrent comparator.

5.2.23 Amplifier inverting input (AMP_N)

The inverting input to the current sensing amplifier.

5.2.24 Amplifier non-inverting input (AMP_P)

The non-inverting input to the current sensing amplifier.

5.2.25 Overcurrent comparator output (OC_OUT)

The overcurrent comparator output is a totem pole logic level output. A logic high indicates an overcurrent condition.

5.2.26 Overcurrent comparator threshold (OC_TH)

This input sets the threshold level of the overcurrent comparator.

5.2.27 Voltage source supply (VSS)

VSS is the ground reference for the logic interface and power supplies.

5.2.28 Ground (GND0,GND1)

These two pins are connected internally to VSS by a 1.0 Ω resistor. They provide device substrate connections and the primary return path for ESD protection.

5.2.29 VLS regulator capacitor (VLS_CAP)

This connection is for a capacitor which provides a low-impedance for switching currents on the gate drive. A low ESR decoupling capacitor, capable of sourcing the pulsed drive currents must be connected between this pin and VSS. This is the same DC node as VLS, but it is physically placed on the opposite end of the IC to minimize the source impedance to the gate drive circuits.

5.2.30 Phase C low-side source (PC_LS_S)

The phase C low-side source is the pin used to return the gate currents from the low-side FET. Best performance is realized by connecting this node directly to the source of the low-side FET for phase C.

5.2.31 Phase C low-side gate (PC_LS_G)

This is the gate drive for the Phase C low-side output FET. It provides high-current through a low-impedance to turn on and off the low-side FET. A low-impedance drive ensures transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FET. This output has also been designed to resist the influence of negative currents.

5.2.32 Phase C high-side source (PC_HS_S)

The source connection for the Phase C high-side output FET is the reference voltage for the gate drive on the high-side FET and also the low-voltage end of the bootstrap capacitor.

5.2.33 Phase C high-side gate (PC_HS_G)

This is the gate drive for the Phase C high-side output FET. This pin provides the gate bias to turn the external FET on or off. The gate voltage is limited to about 15 V above the FET source voltage. A low-impedance drive is used, ensuring transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FETs. This output has also been designed to resist the influence of negative currents.

5.2.34 Phase C bootstrap (PC_BOOT)

This is the bootstrap capacitor connection for Phase C. A capacitor connected between PC_HS_S and this pin provides the gate voltage and current to drive the external FET gate. Typically, the bootstrap capacitor selection is 10 to 20 times the gate capacitance. The voltage across this capacitor is limited to about 15 V.

5.2.35 Phase B low-side source (PB_LS_S)

The Phase B low-side source is the pin used to return the gate currents from the low-side FET. Best performance is realized by connecting this node directly to the source of the low-side FET for Phase B.

5.2.36 Phase B low-side gate (PC_LS_G)

This is the gate drive for the Phase B low-side output FET. It provides high-current through a low-impedance to turn on and off the low-side FET. A low-impedance drive ensures transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FET. This output has also been designed to resist the influence of negative currents.

5.2.37 Phase B high-side source (PB_HS_S)

The source connection for the Phase B high-side output FET is the reference voltage for the gate drive on the high-side FET and also the low-voltage end of the bootstrap capacitor.

5.2.38 Phase B high-side gate (PB_HS_G)

This is the gate drive for the Phase B high-side output FET. This pin provides the gate bias to turn the external FET on or off. The gate voltage is limited to about 15 V above the FET source voltage. A low-impedance drive is used, ensuring transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FETs. This output has also been designed to resist the influence of negative currents.

5.2.39 Phase B bootstrap (PB_BOOT)

This is the bootstrap capacitor connection for phase B. A capacitor connected between PC_HS_S and this pin provides the gate voltage and current to drive the external FET gate. Typically, the bootstrap capacitor selection is 10 to 20 times the gate capacitance. The voltage across this capacitor is limited to about 15 V.

5.2.40 PHASE A low-side source (PA_LS_S)

The Phase A low-side source is the pin used to return the gate currents from the low-side FET. Best performance is realized by connecting this node directly to the source of the low-side FET for phase A.

5.2.41 Phase A low-side gate (PA_LS_G)

This is the gate drive for the Phase A low-side output FET. It provides high-current through a low-impedance to turn on and off the low-side FET. A low-impedance drive ensures transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FET. This output has also been designed to resist the influence of negative currents.

5.2.42 Phase A high-side source (PA_HS_S)

The source connection for the Phase A high-side output FET is the reference voltage for the gate drive on the high-side FET and the low-voltage end of the bootstrap capacitor.

5.2.43 Phase A high-side gate (PA_HS_G)

This is the gate drive for the Phase A high-side output FET. This pin provides the gate bias to turn the external FET on or off. The gate voltage is limited to about 15 V above the FET source voltage. A low-impedance drive is used, ensuring transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FETs. This output was designed to resist the influence of negative currents.

5.2.44 Phase A bootstrap (PA_BOOT)

This is the bootstrap capacitor connection for phase A. A capacitor connected between PC_HS_S and this pin provides the gate voltage and current to drive the external FET gate. Typically, the bootstrap capacitor selection is 10 to 20 times the gate capacitance. The voltage across this capacitor is limited to about 15 V.

5.2.45 VLS regulator (VLS)

VLS is the gate drive power supply regulated at approximately 15 V. This is an internally generated supply from V_{PWR} . It is the source for the low-side gate drive voltage, and also the high-side bootstrap source. A low ESR decoupling capacitor, capable of sourcing the pulsed drive currents, must be connected between this pin and VSS.

5.2.46 VPWR input (VPWR)

VPWR is the power supply input for V_{LS} and V_{DD} . Current flowing into this input recharges the bootstrap capacitors as well as supplying power to the low-side gate drivers and the V_{DD} regulator. An internal regulator regulates the actual gate voltages. This pin can be connected to system supply voltage if power dissipation is not a concern.

5.2.47 Exposed pad (EP)

The primary function of the exposed pad is to conduct heat out of the device. This pad may be connected electrically to the substrate of the device. The device performs as specified with the exposed pad un-terminated (floating). However, it is recommended the exposed pad be terminated to pin 29 (VSS) and the system ground.

6 Functional internal block description

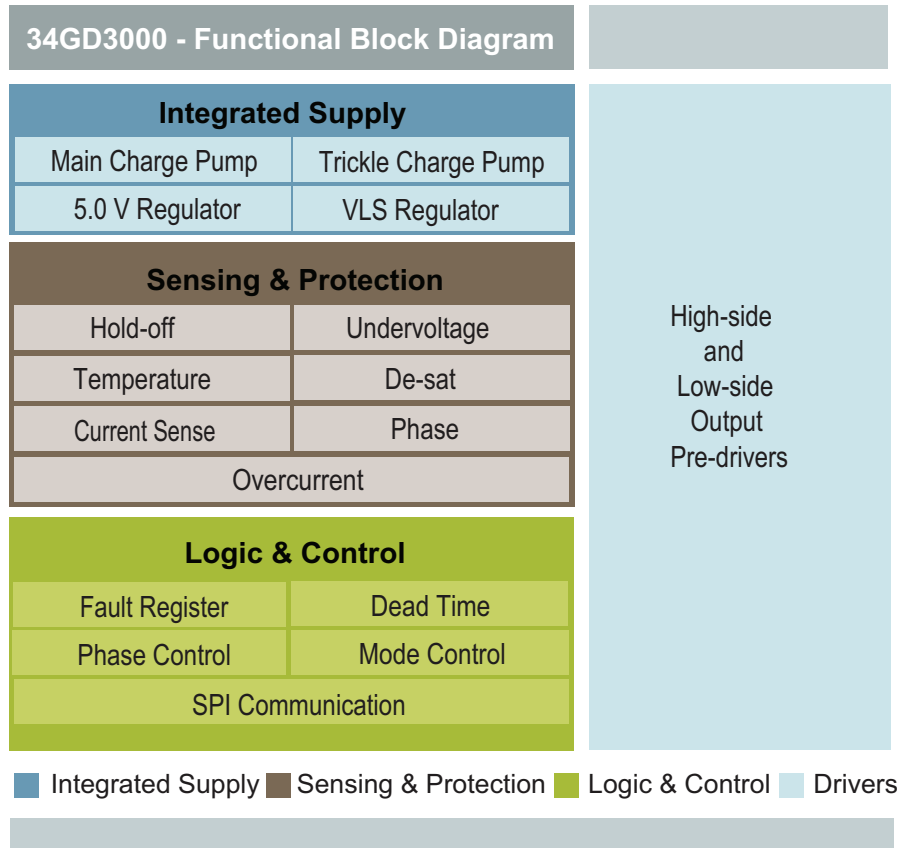


Figure 11. Functional internal block description

All functions of the IC can be described as the following five major functional blocks:

- Logic inputs and control
- Integrated supply
- High-side and low-side drivers
- Sensing and protection

6.1 Logic inputs and control

This section contains the SPI port, control logic, and shoot-through timers. The IC logic inputs have Schmitt trigger inputs with hysteresis. Logic inputs are 3.3 V compatible. The logic outputs are driven from the internal supply of approximately 5.0 V. The SPI registers and functionality is described completely in the [Logic commands and registers](#) section of this document. SPI functionality includes the following:

- **Programming of deadtime delay**—This delay is adjustable in approximately 50 ns steps from 0 ns to 12 μ s. Calibration of the delay, because of internal IC variations, is performed via the SPI.
- **Enabling of simultaneous operation of high-side and low-side FETs**—Normally, both FETs would not be enabled simultaneously. However, for certain applications where the load is connected between the high-side and low-side FETs, this could be advantageous. If this mode is enabled, the blanking time delay is disabled. A sequence of commands may be required to enable this function to prevent inadvertent enabling. In addition, this command can only be executed once after reset to enable or disable simultaneous turn-on.
- **Setting of various operating modes** of the IC and enabling of interrupt sources.
The 34GD3000 allows different operating modes to be set and locked by an SPI command (fullon, desaturation fault, zero deadtime). SPI commands can also determine how the various faults are reported.