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PF1550

Power management integrated circuit (PMIC) for low power application processors

Rev. 4.0 — 28 September 2018 Data sheet: advance information

1 General description

The PF1550 is a power management integrated circuit (PMIC) designed specifically for use with i.MX processors on low-power portable, smart wearable and Internet-of-Things (IoT) applications. It is also capable of providing full power solution to i.MX 7ULP, i.MX 6SL, 6UL, 6ULL and 6SX processors.

With three high efficiency buck converter, three linear regulators, RTC supply, and battery linear charger, the PF1550 can provide power for a complete battery-powered system, including application processors, memory, and system peripherals.

1.1 Features and benefits

This section summarizes the PF1550 features:

- Input voltage range to PMIC VBUSIN pin via USB bus or AC adapter: 4.1 V to 6.0 V
- Buck converters:
  - SW1, 1.0 A; 0.6 V to 1.3875 V in 12.5 mV steps, or 1.1 V to 3.3 V in variable steps
  - SW2, 1.0 A; 0.6 V to 1.3875 V in 12.5 mV steps, or 1.1 V to 3.3 V in variable steps
  - SW3, 1.0 A; 1.8 V to 3.3 V in 100 mV steps
  - Soft start
  - Quiescent current 1.0 µA in ULP mode with light load
  - Peak efficiency > 90 %
  - Dynamic voltage scaling on SW1 and SW2
  - Modes: forced PWM quasi-fixed frequency mode, adaptive variable-frequency mode
  - Programmable output voltage, current limit and soft start
- LDO regulators
  - LDO1, 0.75 to 1.5 V/1.8 to 3.3 V, 300 mA with load switch mode
  - LDO2, 1.8 to 3.3 V, 400 mA
  - LDO3, 0.75 to 1.5 V/1.8 to 3.3 V, 300 mA with load switch mode
  - Quiescent current < 1.5 µA in Low-power mode
  - Programmable output voltage
  - Soft start and ramp
  - Current limit protection
- Battery charger
  - Supports single-cell Lithium Ion/Lithium Polymer batteries
  - Linear charging (10 mA to 1500 mA input limit)
  - Up to 6.5 V input operating range
  - VSYS regulator can withstand transient and DC inputs from 0 V up to +22 V
  - Programmable charge voltage (3.5 V to 4.44 V)
  - Programmable charge current (100 mA to 1000 mA)
  - Programmable charge termination current (5.0 mA to 50 mA)

  - Integrated 50 mΩ battery isolation MOSFET for operation with no/low battery
  - Battery supplement mode
  - Battery discharge overcurrent protection, up to 3.0 A
  - USB_PHY low dropout linear regulator
  - Programmable LED driver (status indicator)
  - JEITA compliant battery temp sensing and charger control
  - Key charging parameters can be configured and permanently stored in OTP
  - I^2C Control Interface permitting processor control and event detection
- LDO/switch supply
  - RTC supply VSNVS 3.0 V, 2.0 mA
  - Battery backed memory including coin cell charger
- DDR memory reference voltage, VREFDDR, 0.5 to 0.9 V, 10 mA
- OTP (One time programmable) memory for device configuration
  - User programmable start-up sequence, timing, soft-start and power-down sequence
  - Programmable regulator output voltages and charger parameters
- I^2C interface
- User programmable Standby, Sleep/Low-power, and Off (REGS_DISABLE) modes
- Ambient temperature range −40 °C to 105 °C

1.2 Applications

- Smart mobile/wearable devices
- Low-power IoT applications
- Wireless game controllers
- Embedded monitoring systems
- Home automation
- POS
- E-Read

2 Application diagram

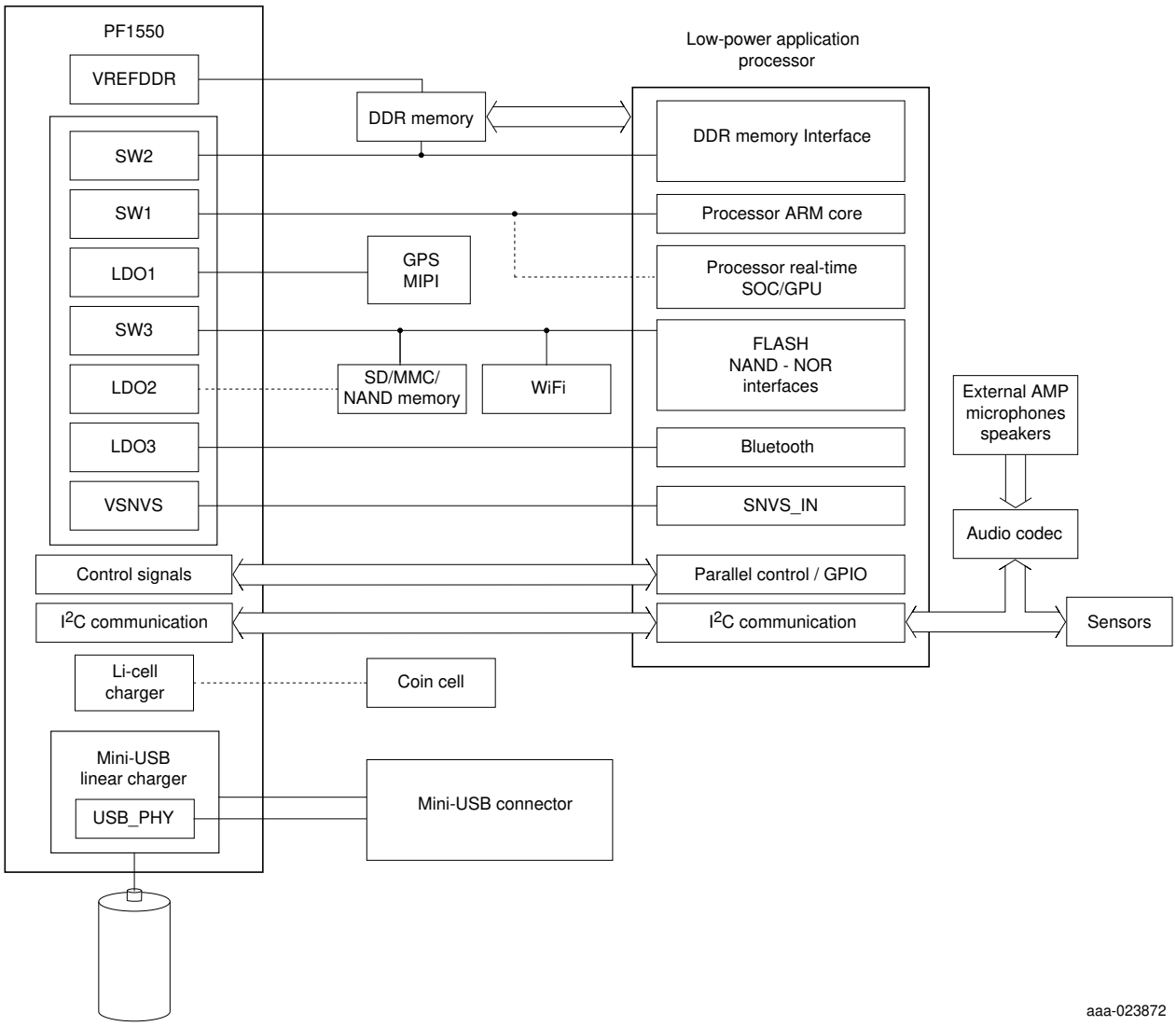

Figure 1. Application diagram

2.1 Functional block diagram

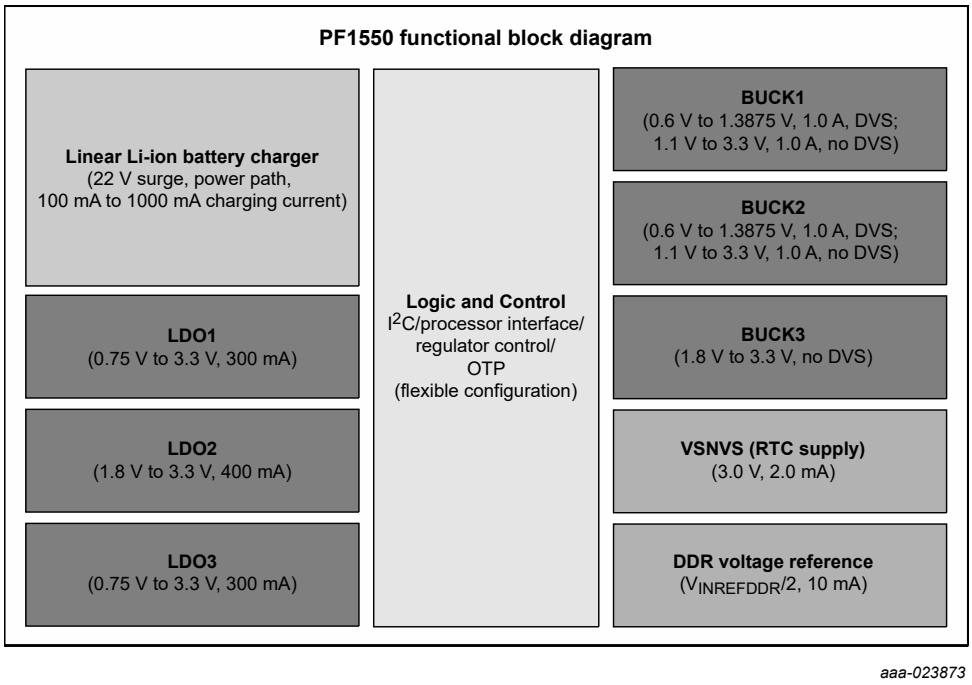

Figure 2. Functional block diagram

2.2 Internal block diagram

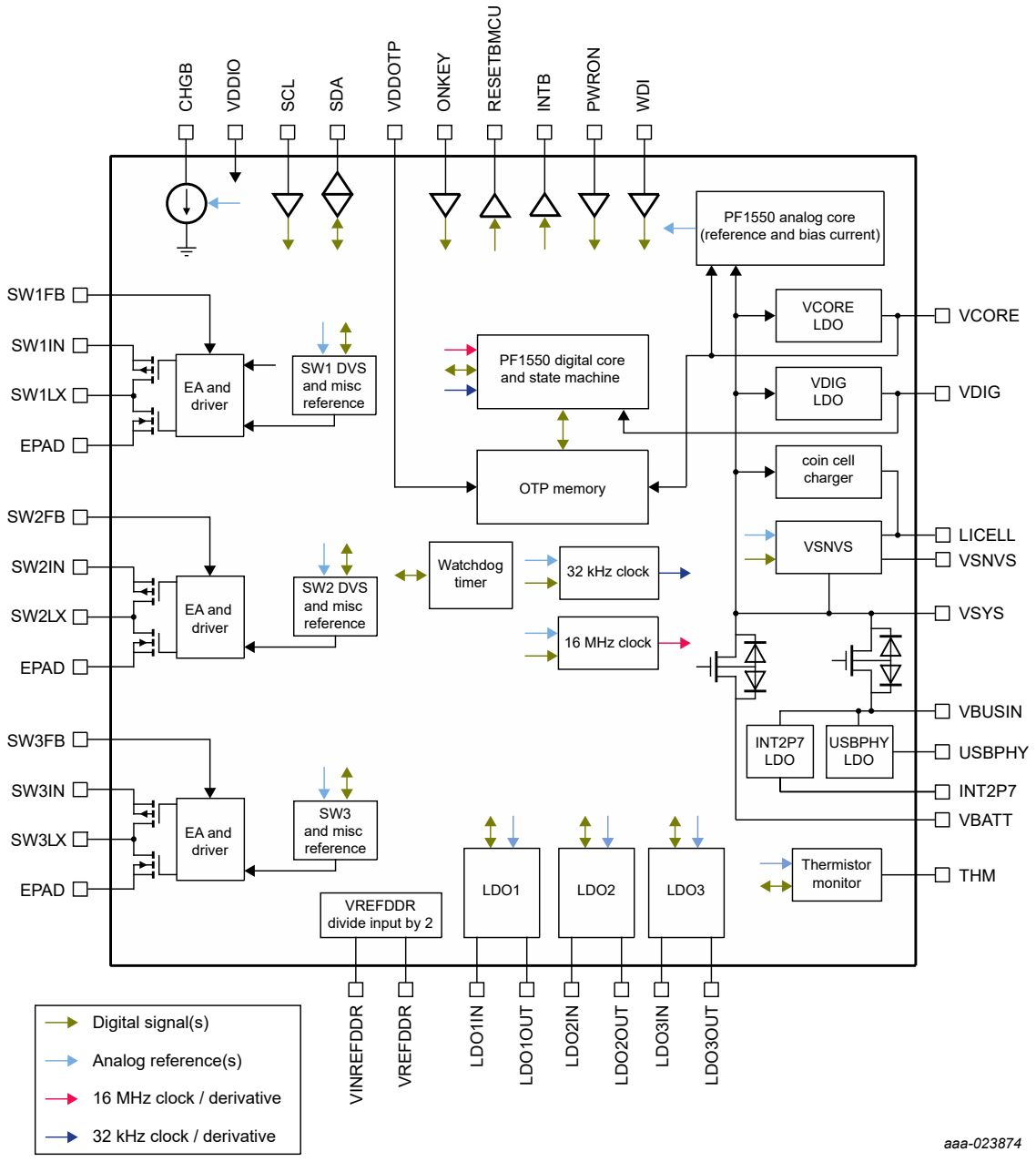

Figure 3. Internal block diagram

3 Orderable parts

The PF1550 is available only with preprogrammed configurations. These preprogrammed devices are identified using the program codes from Table 1, which also list the associated NXP reference designs where applicable. Details of the OTP programming for each device can be found in Table 83.

Table 1. Orderable part variations

Part number[1]	Temperature (T_A)	Package	Programming options
MC32PF1550A0EP	−40 °C to 85 °C (for use in consumer applications)	98ASA00913D, 40-pin QFN 5.0 mm x 5.0 mm with exposed pad	0 - Not programmed
MC32PF1550A1EP			1 (Default)
MC32PF1550A2EP			2 (i.MX 7ULP with LPDDR3) [2]
MC32PF1550A3EP			3 (i.MX 6UL with DDR3L)
MC32PF1550A4EP			4 (i.MX 7ULP with LPDDR3)
MC32PF1550A5EP			5 (i.MX 6UL with DDR3)
MC32PF1550A6EP			6 (i.MX 6ULL with DDR3L)
MC32PF1550A7EP			7 (i.MX 6UL with LPDDR2)
MC32PF1550A8EP			8 (i.MX 6UL with DDR3L, Edge Sensitive)
MC34PF1550A0EP	−40 °C to 105 °C (for use in industrial applications)		0 - Not programmed
MC34PF1550A1EP			1 (Default)
MC34PF1550A2EP			2 (i.MX 7ULP with LPDDR3) [2]
MC34PF1550A3EP			3 (i.MX 6UL with DDR3L)
MC34PF1550A4EP			4 (i.MX 7ULP with LPDDR3)
MC34PF1550A5EP			5 (i.MX 6UL with DDR3)
MC34PF1550A6EP			6 (i.MX 6ULL with DDR3L)
MC34PF1550A7EP			7 (i.MX 6UL with LPDDR2)
MC34PF1550A8EP			8 (i.MX 6UL with DDR3L, Edge Sensitive)

[1] For tape and reel, add an R2 suffix to the part number.
[2] For internal validation only

4 Pinning information

4.1 Pinning

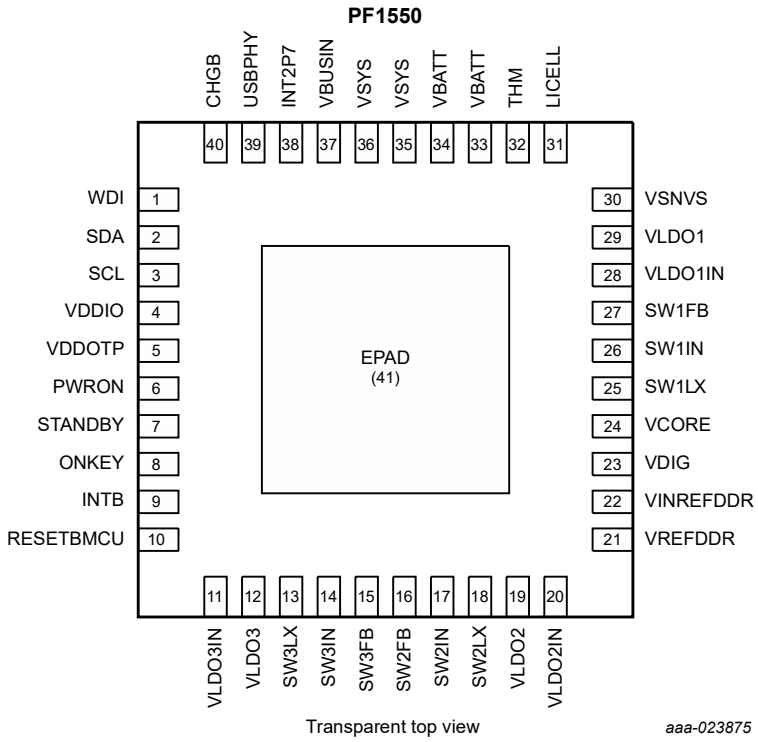

Figure 4. Pinout diagram

4.2 Pin definitions

Table 2. Pin description

Pin number	Pin name	Block	Description
1	WDI	I/Os	Watchdog input from processor
2	SDA		SDA when used in I^2C mode
3	SCL		SCL when used in I^2C mode
4	VDDIO		I/O supply voltage Connect to voltage rail between 1.7 V and 3.3 V
5	VDDOTP	VDDOTP	Connect to ground in application
6	PWRON	I/Os	PWRON input
7	STANDBY		STANDBY input
8	ONKEY		ONKEY push button input
9	INTB		INTB open-drain output
10	RESETBMCU		RESETBMCU open-drain output
11	VLDO3IN	LDO3	LDO3 input supply
12	VLDO3		LDO3 output
13	SW3LX	Buck 3	Buck 3 switching node
14	SW3IN		Buck 3 input supply
15	SW3FB		Buck 3 output voltage feedback
16	SW2FB	Buck 2	Buck 2 output voltage feedback
17	SW2IN		Buck 2 input supply
18	SW2LX		Buck 2 switching node
19	VLDO2	LDO2	LDO2 output
20	VLDO2IN		LDO2 input supply
21	VREFDDR	VREFDDR	VREFDDR output
22	VINREFDDR		VREFDDR input supply
23	VDIG	IC core	VDIG regulator output (used within PF1550)
24	VCORE		VCORE regulator output (used within PF1550)
25	SW1LX	Buck 1	Buck 1 switching node
26	SW1IN		Buck 1 input supply
27	SW1FB		Buck 1 feedback input
28	VLDO1IN	LDO1	LDO1 input supply
29	VLDO1		LDO1 output
30	VSNVS	VSNVS	VSNVS regulator output
31	LICELL		Coin cell input
32	THM	CHARGER	Thermistor connection Connect thermistor to ground from this pin
33	VBATT		Battery input
34			
35	VSYS	IC Core	Main input voltage to PMIC and output of charger
36			

Pin number	Pin name	Block	Description
37	VBUSIN	CHARGER	Charger input
38	INT2P7		INT2P7 regulator output (used within PF1550 and as thermistor bias)
39	USBPHY		USBPHY regulator output
40	CHGB		Charger LED input connection Connect LED from VSYS to this pin
41	EPAD	EPAD	Exposed pad Connect to ground

5 General product characteristics

5.1 Thermal characteristics

Table 3. Thermal ratings

Symbol	Description (Rating)	Min	Max	Unit
THERMAL RATINGS				
T_A	Ambient operating temperature range (industrial) Ambient operating temperature range (consumer)	−40 −40	105 85	°C
T_J	Operating junction temperature range [1]	−40	125	°C
T_{ST}	Storage temperature range	−65	150	°C
T_{PPRT}	Peak package reflow temperature [2] [3]	—	—	°C
QFN40 THERMAL RESISTANCE AND PACKAGE DISSIPATION RATINGS				
$R_{\Theta JA}$	Junction to ambient thermal resistance, natural convection [4] [5] [6] Four layer board (2s2p) Six layer board (2s4p) Eight layer board (2s6p)	—	 27 20.6 17.8	°C/W
$R_{\Theta JMA}$	Junction to ambient (@200ft/min) [4] [6] Four layer board (2s2p)	—	 21.4	°C/W
$R_{\Theta JB}$	Junction to board [7]	—	8.8	°C/W
$R_{\Theta JCBOTTOM}$	Junction to case bottom [8]	—	1.4	°C/W
Ψ_{JT}	Junction to package top – Natural convection [9]	—	0.6	°C/W

[1] Do not operate beyond 125 °C for extended periods of time. Operation above 150 °C may cause permanent damage to the IC. See Thermal Protection Thresholds for thermal protection features.
[2] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
[3] NXP's package reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For peak package reflow temperature and moisture sensitivity levels (MSL), go to http://www.nxp.com, search by part number [remove prefixes/suffixes and enter the core ID to view all orderable parts (for MC33xxxD enter 33xxx), and review parametrics.
[4] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
[5] The Board uses the JEDEC specifications for thermal testing (and simulation) JESD51-7 and JESD51-5.
[6] Per JEDEC JESD51-6 with the board horizontal.
[7] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
[8] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
[9] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

5.2 Absolute maximum ratings

Table 4. Maximum ratings

Symbol	Description (Rating)	Min	Max	Unit
I/Os				
VDDIO	I/O supply voltage. Connect to voltage rail between 1.7 V and 3.3 V.	−0.3	3.6	V
SCL	SCL when used in I^2C mode. SCLK when used in SPI mode.	−0.3	3.6	V
SDA	SDA when used in I^2C mode. MISO when used in SPI mode.	−0.3	3.6	V
RESETBMCU	RESETBMCU open drain output	−0.3	3.6	V
PWRON	PWRON input	−0.3	3.6	V
STANDBY	STANDBY input	−0.3	3.6	V
ONKEY	ONKEY push button input	−0.3	4.8	V
INTB	INTB open-drain output	−0.3	3.6	V
WDI	Watchdog input from processor	−0.3	3.6	V
VDDOTP				
VDDOTP	Connect to ground in the application	−0.3	10	V
BUCK 1				
SW1IN	Buck 1 input supply	−0.3	4.8	V
SW1LX	Buck 1 switching node	−0.3	4.8	V
SW1FB	Buck 1 feedback input	−0.3	3.6	V
BUCK 2				
SW2IN	Buck 2 input supply	−0.3	4.8	V
SW2LX	Buck 2 switching node	−0.3	4.8	V
SW2FB	Buck 2 output voltage feedback	−0.3	3.6	V
BUCK 3				
SW3IN	Buck 3 input supply	−0.3	4.8	V
SW3LX	Buck 3 switching node	−0.3	4.8	V
SW3FB	Buck 3 output voltage feedback	−0.3	3.6	V
LDO1				
VLDO1IN	LDO1 input supply	−0.3	4.8	V
VLDO1	LDO1 output	−0.3	3.6	V
LDO2				
VLDO2IN	LDO2 input supply	−0.3	4.8	V
VLDO2	LDO2 output	−0.3	3.6	V
LDO3				
VLDO3IN	LDO3 input supply	−0.3	4.8	V
VLDO3	LDO3 output	−0.3	3.6	V
VSNVS				
VSNVS	VSNVS regulator output	−0.3	3.6	V

Symbol	Description (Rating)	Min	Max	Unit
LICELL	Coin cell input	−0.3	3.6	V
CHARGER				
VBATT	Battery input	−0.3	4.8	V
INT2P7	INT2P7 regulator output (used within PF1550 and as thermistor bias)	−0.3	3.6	V
THM	Thermistor connection. Connect thermistor to ground from this pin.	−0.3	3.6	V
VBUSIN	Charger input	−0.3	24	V
USBPHY	USBPHY regulator output	−0.3	5.5	V
CHGB	Charger LED input connection. Connect LED from VSYS to this pin.	−0.3	4.8	V
INPUT/OUTPUT SUPPLY				
VINREFDDR	VREFDDR input supply	−0.3	3.6	V
VREFDDR	VREFDDR output	−0.3	3.6	V
IC CORE				
VSYS	Main input voltage to PMIC and output of charger	−0.3	4.8	V
VDIG	VCOREDIG regulator output (used within PF1550)	−0.3	1.65	
VCORE	VCORE regulator output (used within PF1550)	−0.3	1.65	V
ELECTRICAL RATINGS				
V_{ESD}	ESD ratings Human body model [1] Charge device model (corner pins) Charge device model (all other pins)	 — — —	 ±2000 ±750 ±500	V

[1] Testing is performed in accordance with the human body model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the charge device model (CDM), Robotic (C_{ZAP} = 4.0 pF).

5.3 Electrical characteristics

5.3.1 Electrical characteristics – Battery charger

All parameters are specified at T_A = −40 to 105 °C, VBUSIN = 5.0 V, VSYS = 3.7 V, typical external component values, unless otherwise noted. Typical values are characterized at VBUSIN = 5.0 V, VSYS = 3.7 V and 25 °C, unless otherwise noted.

Table 5. Global conditions

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
CHARGER INPUTS						
V_{BUS}	VBUSIN voltage range	Operating voltage	V_{UVLO}	—	V_{OVLO}	V
$V_{BUS\_WITHSTAND}$	VBUSIN maximum withstand voltage rating		—	—	22	V
V_{BUS_OVLO}	VBUSIN overvoltage threshold	Rising	6.0	6.5	7.0	V
V_{OVLO_HYS}	VBUSIN overvoltage threshold hysteresis	Falling	50	150	250	mV
t_{D-OVLO}	VBUSIN overvoltage delay		5.0	10	15	µs
V_{UVLO}	VBUSIN to GND minimum turn on threshold accuracy	VBUS rising	3.8	4.0	4.2	V
$V_{UVLO-HYS}$	VBUSIN UVLO hysteresis		400	500	600	mV
V_{IN2SYS_50}	VBUSIN to VSYS minimum turn on threshold accuracy	VBUS_LIN rising, 50 mV setting	20	50	80	mV
V_{IN2SYS_175}	VBUSIN to VSYS minimum turn on threshold accuracy	VBUS_LIN rising, 175 mV setting	100	175	250	mV
$V_{BUS\_LIN\_DPM\_REG}$	VBUSIN adaptive voltage regulation threshold	4.4 V setting (default)	4.3	4.4	4.5	V
V_{DPM_REG}	VBUSIN adaptive voltage regulation threshold accuracy	Programmable at 3.9 V to 4.6 V	−100	—	100	mV

Table 6. Input currents

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
VBUSIN INPUT CURRENT LIMIT						
$ILIM_{10}$	Charger input current limit (10 mA settings)	10 mA	6.0	8.5	11	mA
$ILIM_{15}$	Charger input current limit (15 mA settings)	15 mA	10.5	12.75	16	mA
$ILIM_{20}$	Charger input current limit (20 mA settings)	20 mA	14	17	21	mA
$ILIM_{25}$	Charger input current limit (25 mA settings)	25 mA	17.5	21.25	26	mA
$ILIM_{30}$	Charger Input Current Limit (30mA setting)	30 mA	21	25.5	30	mA
$ILIM_{35}$	Charger input current limit (35 mA settings)	35 mA	24.5	29.75	35	mA
$ILIM_{40}$	Charger input current limit (40mA settings)	40 mA	28	34	40	mA
$ILIM_{45}$	Charger input current limit (45 mA settings)	45 mA	31.5	38.25	45	mA
$ILIM_{50}$	Charger input current limit (50 mA settings)	50 mA	35	42.5	50	mA
$ILIM_{100}$	Charger input current limit (100 mA settings)	100 mA	85	95	105	mA

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
$ILIM_{150}$	Charger input current limit (150 mA settings)	150 mA	125	137.5	160	mA
$ILIM_{200}$	Charger input current limit (200 mA settings)	200 mA	170	190	210	mA
$ILIM_{300}$	Charger input current limit (300 mA setting)	300 mA	260	285	320	mA
$ILIM_{400}$	Charger input current limit (400 mA settings)	400 mA	345	380	425	mA
$ILIM_{500}$	Charger input current limit (500 mA settings)	500 mA	430	475	530	mA
$ILIM_{600}$	Charger input current limit (600 mA settings)	600 mA	520	570	640	mA
$ILIM_{700}$	Charger input current limit (700 mA settings)	700 mA	610	665	750	mA
$ILIM_{800}$	Charger input current limit (800 mA settings)	800 mA	690	760	850	mA
$ILIM_{900}$	Charger input current limit (900 mA settings)	900 mA	780	855	950	mA
$ILIM_{1000}$	Charger input current limit (1000 mA settings)	1000 mA	855	950	1100	mA
$ILIM_{1500}$	Charger input current limit (1500 mA settings)	1500 mA	1260	1400	1700	mA
R_{INSD}	Input self discharge resistance		18	30	42	kΩ
$I_{BATTLEAK}$	Leakage current	Leakage current from VBATT to VBUSIN. VBATT = 4.2 V, BATFET closed, VBUSIN = 0 V. Current measured into VBATT pin at 25 °C	0	—	5.0	µA
$I_{Q\_CHARGER}$	Charger quiescent current (BATFET enabled, normal mode)	25 °C only; charger in CC state; ICC = 100 mA	0	2.5	5.0	mA
$I_{Q\_CHARGER\_LQM}$	Charger quiescent current (low power mode, charging enabled, 10 to 50 mA input current limit setting, VBATT > 2.8 V and LED driver OFF)	25 °C only; charger in CC state	0	1.5	3.0	mA
T_{SSVBUS_LIN}	Soft start time (VBUSIN = 5.0 V, time between input LDO enabled and VSYS going to 90 % of regulation	No input current limitation event, measured in Normal mode	—	—	30	ms

Table 7. Internal 2.7 V Regulator (INT2P7)

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
V_{GDRV}	Output voltage		2.6	2.7	2.8	V
I_{GDRV}	Output current		5.0	—	—	mA
$V_{DO(GDRV)}$	Dropout voltage		0	—	800	mV

Table 8. Switch impedances and leakage currents

Symbol	Parameter	Measurement Condition	Min	Typ	Max	Unit
$R_{VBUS\_LIN2SYS}$	VBUSIN to VSYS resistance		100	250	550	mΩ
R_{BATFET_QFN}	VBATT to VSYS resistance		50	75	120	mΩ
I_{SYS}	VSYS leakage current	VSYS = 0 V, VBATT = 4.2 V, SHIP mode	0	0.2	10	µA

Symbol	Parameter	Measurement Condition	Min	Typ	Max	Unit
I_{BATT_OC}	VBATT reverse ILIM quiescent current when VBUSIN = 0 V	VBUSIN = 0 V, VSYS = VBATT = 4.2 V, BATFET enabled, battery overcurrent enabled	—	—	100	µA

Table 9. Linear transients

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
V_{PK-PK}	Load transient peak-to-peak	VBUSIN = 5.0 V, VBATT = 3.6 V, I_{CHG} = 500 mA, VSYS load step 1.0 A/µs	10	400	850	mV
V_{OV_SHT}	Load transient overshoot	VBUSIN = 5.0 V, VBATT = 3.6 V, I_{CHG} = 500 mA, VSYS load step 1.0 A/µs	0	200	500	mV
V_{UND_SHT}	Load transient undershoot	VBUSIN = 5.0 V, VBATT = 3.6 V, I_{CHG} = 500 mA, VSYS load step 1.0 A/µs	0	200	500	mV

Table 10. Charger characteristics

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
V_{CHGCV_RANGE}	CHGCV output voltage range	See register map for constant voltage programmable range	3.5	—	4.44	V
CV_{ACC}	CHGCV output accuracy in normal charging		—	—	±1	%
$V_{SYSMIN0}$	VSYS output voltage (3.5 V option)	VSYSMIN = 0x00 (3.5 V option)	3.395	3.5	3.605	V
$V_{SYSMIN1}$	VSYS output voltage (3.7 V option)	VSYSMIN = 0x01 (3.7 V option)	3.589	3.7	3.811	V
$V_{SYSMIN2}$	VSYS output voltage (4.3 V option)	VSYSMIN = 0x02 (4.3 V option)	4.171	4.3	4.429	V
$V_{SYSMINLOOP0}$	VSYSMIN loop threshold (3.5 V option)		3.0	3.2	3.39	V
$V_{SYSMINLOOP1}$	VSYSMIN loop threshold (3.7 V option)		3.2	3.4	3.585	V
$V_{SYSMINLOOP2}$	VSYSMIN loop threshold (4.3 V option)		3.83	4.0	4.17	V
I_{FC}	Output current range	Constant current programmable range CHG_CC[4:0]	100	—	1000	mA
I_{FCACC1}	Output current accuracy		−10	—	10	%
I_{EOC}	Charger IEOC range		5.0	—	50	mA
$t_{DB(IEOC)}$	Debounce time for charge termination		20	32	44	ms
$I_{EOC\_ACC\_5mA}$	Charger IEOC accuracy (5.0 mA settings)	I_{EOC} = 5 mA	1.0	5.0	12	mA
$I_{EOC\_ACC\_10mA}$	Charger IEOC accuracy (10 mA settings)	I_{EOC} = 10 mA	4.0	10	16	mA
$I_{EOC\_ACC\_50mA}$	Charger IEOC accuracy (50 mA setting)	I_{EOC} = 50 mA	40	50	60	mA
V_{PRECHG}	Precharge threshold	VBATT rising	2.7	2.8	2.9	V
V_{PRECHG_HYS}	Precharge threshold hysteresis		50	100	150	mV
I_{PRECHG}	Precharge current		30	45	60	mA
$I_{PRECHG.LPM}$	Charging current in LPM and 2.8 V < VBATT < 3.1 V		0.75	1.0	1.25	mA
$V_{RESTART}$	Charger restart threshold (100 mV settings)	VBATT below CHGCV[5:0]	50	100	150	mV

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
$V_{RESTART}$	Charger restart threshold (150 mV setting)	VBATT below CHGCV[5:0]	100	150	200	mV
$V_{RESTART}$	Charger restart threshold (200 mV settings)	VBATT below CHGCV[5:0]	150	200	250	mV
$t_{DB(VRCH)}$	Debounce time on $V_{RESTART}$		20	32	44	ms
V_{BATOV}	BATTOVP range		CHGCV x 1.025	CHGCV x 1.05	CHGCV x 1.075	V
V_{BATOV_HYS}	BATTOVP hysteresis	VBATT falling from BATTOVP	CHGCV x 0.015	CHGCV x 0.025	CHGCV x 0.035	V

Table 11. Power-path management

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
V_{SPLM}	Supplement mode voltage threshold	Entering supplement mode when VSYS < VBATT	10	40	75	mV

Table 12. Watchdog timer

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
t_{WD}	Watchdog timer period		—	80	—	s
t_{WDACC}	Watchdog timer accuracy		−20	0	20	%

Table 13. Charger timer

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
t_{PRECHG}	Precharge time (fixed 45 mA)	Applies to low battery prequalification mode, 500 mA settings	—	30	—	min
t_{FC}	Fast charge constant current and constant voltage time	Adjustable from 2 to 14 in 2 hour steps	—	4.0	—	hrs
t_{EOC}	End-of-charge time	Adjustable from 0 to 70 in 10 min steps	—	30	—	min
t_{acc}	Timer accuracy	All timers associated with the charger block	−20	—	20	%
t_{SCIDG}	Charger state change interrupt delay		0	1.0	2.0	ms
t_{INLIM}	VBUS_VOK delay from VDIG ready following VBUSIN insertion (see charger startup diagram)		0	100	200	µs

Table 14. Battery overcurrent protection

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
t_{BOVCR}	Battery overcurrent debounce time	Response time to BATFET open (OTP option)	12.8	16	19.2	ms
t_{BOVCRI}	Battery overcurrent interrupt debounce time	Response time to generate interrupt	2.4	3.0	3.6	ms
I_{BOVCR}	Battery overcurrent threshold range	Programmable from 2.0 A to 4.0 A in three steps	2.0	—	4.0	A
$I_{BOVCRACC\_2A}$	Battery overcurrent threshold accuracy (2.2 A setting)		1.0	2.2	3.2	A

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
$I_{BOVCRACC\_3A}$	Battery overcurrent threshold accuracy (2.8 A setting)		1.6	2.8	4	A
$I_{BOVCRACC\_4A}$	Battery overcurrent threshold accuracy (3.2 A setting)		2.0	3.2	4.6	A
$R_{SYSDISCH}$	SYS self-discharge resistor in SHIP mode		480	600	720	Ω

Table 15. Thermal regulation

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
T_{REG}	Thermal regulation threshold (80 °C setting)	Temperature at which charge current begins to decrease	—	80	—	°C
T_{REG}	Thermal regulation threshold (95 °C Setting)	Temperature at which charge current begins to decrease	—	95	—	°C
T_{REG}	Thermal regulation threshold (110 °C setting)	Temperature at which charge current begins to decrease	—	110	—	°C

Table 16. Battery thermistor monitor

Symbol	Parameter	Measurement Condition	Min	Typ	Max	Unit
$V_{NTECREF}$	NTECREF voltage		2.6	2.7	2.8	V
V_{TN10C}	Thermistor threshold (−10 °C settings)	−10 °C	$0.79*V_{NTECREF}$	$0.82*V_{NTECREF}$	$0.85*V_{NTECREF}$	V
V_{T0C}	Thermistor threshold (0 °C settings)	0 °C	$0.71*V_{NTECREF}$	$0.74*V_{NTECREF}$	$0.77*V_{NTECREF}$	V
V_{T10C}	Thermistor threshold (10 °C settings)	10 °C	$0.62*V_{NTECREF}$	$0.65*V_{NTECREF}$	$0.68*V_{NTECREF}$	V
V_{T45C}	Thermistor threshold (45 °C settings)	45 °C	$0.31*V_{NTECREF}$	$0.33*V_{NTECREF}$	$0.35*V_{NTECREF}$	V
V_{T55C}	Thermistor threshold (55 °C settings)	55 °C	$0.25*V_{NTECREF}$	$0.26*V_{NTECREF}$	$0.27*V_{NTECREF}$	V
V_{T60C}	Thermistor threshold (60 °C settings)	60 °C	$0.22*V_{NTECREF}$	$0.23*V_{NTECREF}$	$0.24*V_{NTECREF}$	V
V_{T_HYS}	Battery temperature hysteresis	All settings	0.5	2.5	5.0	°C

Table 17. USBPHY LDO

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
V_{USB_PHY}	Output voltage	I_{OUT} = 10 mA; 3.3 V and 4.9 V settings. VBUSIN = 5.5 V	−5.0	—	5.0	%
I_{USB_PHY}	Maximum output current		60	—	—	mA
USB_{RDIS}	Internal discharge resistance		500	1000	1500	Ω
USB_{CAPSTA}	Output capacitor for stable operation	0 µA < I_{OUT} < 60 mA, MAX ESR = 10 mΩ	0.7	1.0	2.2	µF
I_{QUSB}	Quiescent supply current		—	35	—	µA
$USBPHY_{LDREG}$	DC load regulation	VBUSIN = 5.5 V, 30 µA < I_{OUT} < 60 mA	0	5.0	13	mV
$USBPHY_{DO}$	Dropout voltage	VBUSIN = 5.0 V, I_{OUT} = 60 mA	—	200	350	mV
$USBPHYI_{LIM}$	Output current limit		65	150	200	mA
$PSRR_{USB\_PHY}$	PSRR	VBUSIN = 5.5 V, C_{OUT} = 1.0 µF	55	60	75	dB

Table 18. LED characteristics

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
V_{LED}	LED input voltage operating range (anode to ground)		3.5	—	VSYS	V
V_{CHGB_IN}	CHGB input voltage operating range, LED driver enabled		1.0	—	3.0	V
I_{LED}	LED current accuracy		4.0	6.0	8	mA
T_{ON}	LED duty cycle range	Programmable from 10 % to 100 % duty cycle in 10 % steps	10	—	100	%
$TLED_{RUP}$	LED ramp up	Settings depend on duty cycle	50	—	500	ms
$TLED_{RDN}$	LED ramp down	Settings depend on duty cycle	50	—	500	ms
F_{LED}	LED frequency	Programmable from 0.5 Hz to 256 Hz	0.5	—	256	Hz

5.3.2 Electrical characteristics – SW1 and SW2

All parameters are specified at T_A = −40 to 105 °C, VSYS = V_{SWxIN} = 2.5 to 4.5 V, V_{SWx} = 1.2 V, I_{SWx} = 200 mA, typical external component values, f_{SWx} = 2.0 MHz, unless otherwise noted. Typical values are characterized at VSYS = V_{SWxIN} = 3.6 V, V_{SWx} = 1.1 V, I_{SWx} = 100 mA, and 25 °C, unless otherwise noted.

Table 19. SW1 and SW2 electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{SWxIN}	Operating input voltage	2.5	—	4.5	V
I_{SWx}	Rated output current	1000	—	—	mA
V_{SWx}	Output voltage accuracy DVS enabled mode (OTP_SWx_DVS_SEL = 0) Normal power mode, 2.5 V < V_{SWxIN} < 4.5 V, 0 < I_{SWx} < 1.0 A 0.6 V ≤ V_{SWx} ≤ 1.0 V	−15	—	15	mV
V_{SWx}	Output voltage accuracy DVS enabled mode (OTP_SWx_DVS_SEL = 0) Normal power mode, 2.5 V < V_{SWxIN} < 4.5 V, 0 < I_{SWx} < 1.0 A 1.0 V < V_{SWx} ≤ 1.3875 V	−2.0	—	2.0	%
V_{SWx}	Output voltage accuracy DVS enabled mode (OTP_SWx_DVS_SEL = 0) Low-power mode, 2.5 V < V_{SWxIN} < 4.5 V, 0 < ISWx < 0.1 A 0.6 V ≤ V_{SWx} ≤ 1.0 V	−30	—	30	mV
V_{SWx}	Output voltage accuracy DVS enabled mode (OTP_SWx_DVS_SEL = 0) Low-power mode, 2.5 V < V_{SWxIN} < 4.5 V, 0 < I_{SWx} < 0.1 A 1.0 V < V_{SWx} ≤ 1.3875 V	−3.0	—	3.0	%
V_{SWx}	Output voltage accuracy DVS disabled mode (OTP_SWx_DVS_SEL = 1) Normal power mode, 2.5 V < V_{SWxIN} < 4.5 V, 0 < I_{SWx} < 1.0 A 1.1 V ≤ V_{SWx} ≤ 1.5 V	−45	—	45	mV
V_{SWx}	Output voltage accuracy DVS disabled mode (OTP_SWx_DVS_SEL = 1) Normal power mode, 2.5 V < V_{SWxIN} < 4.5 V, 0 < I_{SWx} < 1.0 A 1.8 V ≤ V_{SWx} ≤ 3.3 V	−3.0	—	3.0	%
V_{SWx}	Output voltage accuracy DVS disabled mode (OTP_SWx_DVS_SEL = 1) Low-power mode, 2.5 V < V_{SWxIN} < 4.5 V, 0 < I_{SWx} < 0.1 A 1.1 V < V_{SWx} ≤ 1.5 V	−55	—	55	mV
V_{SWx}	Output voltage accuracy DVS disabled mode (OTP_SWx_DVS_SEL = 1) Low-power mode, 2.5 V < V_{SWxIN} < 4.5 V, 0 < I_{SWx} < 0.1 A 1.8 V ≤ V_{SWx} ≤ 3.3 V	−4.0	—	4.0	%

Symbol	Parameter	Min	Typ	Max	Unit
ΔV_{SWx}	Output ripple	—	5.0	—	mV
SWxEFF	Efficiency V_{SWxIN} = 3.6 V, L_{SWx} = 1.0 µH, DCR = 50 mΩ LP/ ULP mode, 1.2 V, 1.0 mA	—	88	—	%
SWxEFF	Efficiency V_{SWxIN} = 3.6 V, L_{SWx} = 1.0 µH, DCR = 50 mΩ Normal power mode, 1.2 V, 50 mA	—	90	—	%
SWxEFF	Efficiency V_{SWxIN} = 3.6 V, L_{SWx} = 1.0 µH, DCR = 50 mΩ Normal power mode, 1.2 V, 150 mA	—	92	—	%
SWxEFF	Efficiency V_{SWxIN} = 3.6 V, L_{SWx} = 1.0 µH, DCR = 50 mΩ Normal power mode, 1.2 V, 400 mA	—	89	—	%
SWxEFF	Efficiency V_{SWxIN} = 3.6 V, L_{SWx} = 1.0 µH, DCR = 50 mΩ Normal power mode, 1.2 V, 1000 mA	—	83	—	%
$I_{SWxLIMH}$	Current limiter peak (high-side MOSFET) current detection SWxILIM[1:0] = 00 SWxILIM[1:0] = 01 SWxILIM[1:0] = 10 SWxILIM[1:0] = 11	 0.7 0.8 1.0 1.4	 1.0 1.2 1.5 2.0	 1.3 1.6 2.0 2.6	A
$I_{SWxLIML}$	Current limiter low-side MOSFET current detection (sinking current)	0.7	1.0	1.3	A
I_{SWxQ}	Quiescent current (at 25 °C) Low-power mode with DVS disabled (OTP_SWx_DVS_SEL = 1)	—	1.0	—	µA
I_{SWxQ}	Quiescent current (at 25 °C) Low-power mode with DVS enabled (OTP_SWx_DVS_SEL = 0)	—	6.0	—	µA
I_{SWxQ}	Quiescent current (at 25 °C) Normal power mode with DVS disabled (OTP_SWx_DVS_SEL = 1)	—	5.5	—	µA
I_{SWxQ}	Quiescent current (at 25 °C) Normal power mode with DVS enabled (OTP_SWx_DVS_SEL = 0)	—	10	—	µA
V_{SWxOSH}	Startup overshoot (Normal mode) I_{SWx} = 0 mA DVS speed = 12.5 mV/4 µs, VSYS = V_{SWxIN} = 3.6 V, V_{SWx} = 1.35 V	—	—	25	mV
t_{ONSWx}	Turn on time 10 % to 90 % of end value DVS speed = 12.5 mV/4 µs, VSYS = V_{SWxIN} = 3.6 V, V_{SWx} = 1.35 V	—	—	500	µs
$V_{SWxLOTR}$	Transient load regulation (Normal power mode) Transient load = 50 mA to 250 mA, di/dt = 200 mA/µs Overshoot Undershoot	 — —	 25 25	 — —	mV
R_{ONSWxP}	SWx P-MOSFET $R_{DS(on)}$ at V_{SWxIN} = 3.6 V	—	200	—	mΩ
R_{ONSWxN}	SWx N-MOSFET $R_{DS(on)}$ at V_{SWxIN} = 3.6 V	—	150	—	mΩ
R_{SWxDIS}	Turn off discharge resistance	—	500	—	Ω

5.3.3 Electrical characteristics – SW3

All parameters are specified at T_A = −40 to 105 °C, VSYS = V_{SW3IN} = 2.5 to 4.5 V, V_{SW3} = 1.8 V, I_{SW3} = 200 mA, typical external component values, f_{SW3} = 2.0 MHz, unless otherwise noted. Typical values are characterized at VSYS = V_{SW3IN} = 3.6 V, V_{SW3} = 1.8 V, I_{SW3} = 200 mA, and 25 °C, unless otherwise noted.

Table 20. SW3 electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{SW3IN}	Operating input voltage	2.5	—	4.5	V

Symbol	Parameter	Min	Typ	Max	Unit
V_{SW3}	Output voltage accuracy (all voltage settings) Normal power mode, 2.5 V < V_{SW3IN} < 4.5 V, 0 < I_{SW3} < 1.0 A	−2.0	—	2.0	%
V_{SW3}	Output voltage accuracy (all voltage settings) Low-power mode, 2.5 V < V_{SW3IN} < 4.5 V, 0 < I_{SW3} < 0.1 A	−3.0	—	3.0	%
ΔV_{SW3}	Output ripple	—	5.0	—	mV
SW3EFF	Efficiency V_{SW3IN} = 3.6 V, L_{SW3} = 1.0 µH, DCR = 50 mΩ LP/ ULP Mode, 1.8 V, 1.0 mA	—	88	—	%
SW3EFF	Efficiency V_{SW3IN} = 3.6 V, L_{SWx} = 1.0 µH, DCR = 50 mΩ Normal power mode, 1.8 V, 50 mA	—	90	—	%
SW3EFF	Efficiency V_{SW3IN} = 3.6 V, L_{SWx} = 1.0 mH, DCR = 50 mΩ Normal power mode, 1.8 V, 100 mA	—	91	—	%
SW3EFF	Efficiency V_{SW3IN} = 3.6 V, L_{SWx} = 1.0 µH, DCR = 50 mΩ Normal power mode, 1.8 V, 400 mA	—	92	—	%
SW3EFF	Efficiency V_{SW3IN} = 3.6 V, L_{SWx} = 1.0 µH, DCR = 50 mΩ Normal power mode, 1.8 V, 1000 mA	—	83	—	%
$I_{SW3LIMH}$	Current limiter peak (high-side MOSFET) current detection SW3ILIM[1:0] = 00 SW3ILIM[1:0] = 01 SW3ILIM[1:0] = 10 SW3ILIM[1:0] = 11	 0.7 0.8 1.0 1.4	 1.0 1.2 1.5 2.0	 1.3 1.6 2.0 2.6	A
$I_{SW3LIML}$	Current limiter low-side MOSFET current detection (sinking current)	0.7	1.0	1.3	A
I_{SW3Q}	Quiescent current (at 25 °C) Low-power mode	— —	 1.0	 —	µA
V_{SW3OSH}	Start-up overshoot (Normal mode) I_{SW3} = 0 mA VSYS = V_{SW3IN} = 3.6 V, V_{SW3} = 1.8 V	—	—	50	mV
t_{ONSW3}	Turn on time 10 % to 90 % of end value VSYS = V_{SW3IN} = 3.6 V, V_{SW3} = 1.8 V	—	—	500	µs
$V_{SW3LOTR}$	Transient load regulation (Normal power mode) Transient load = 50 mA to 250 mA, di/dt = 200 mA/µs Overshoot Undershoot	 — —	 50 50	 — —	mV
R_{ONSW3N}	SW3 N-MOSFET $R_{DS(on)}$ at V_{SW3IN} = 3.6 V	—	150	—	mΩ
R_{ONSW3P}	SW3 P-MOSFET $R_{DS(on)}$ at V_{SW3IN} = 3.6 V	—	200	—	mΩ
R_{SW3DIS}	Turn off discharge resistance	—	300	—	Ω

5.3.4 Electrical characteristics – LDO1

All parameters are specified at T_A = −40 to 105 °C, VSYS = 2.5 to 4.5 V, V_{LDOIN1} = 3.6 V, VLDO1[4:0] = 11111, I_{LDO1} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at VSYS = 3.6 V, V_{LDOIN1} = 3.6 V, VLDO1[4:0] = 11111, I_{LDO1} = 10 mA, and 25 °C, unless otherwise noted.

Table 21. LDO1 electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{LDO1IN}	Operating input voltage V_{LDO1} + 250 mV ≤ VSYS ≤ 4.5 V	 1.0	 —	 4.5	V
$V_{LDO1NOM}$	Nominal output voltage	—	See Table 41	—	V

Symbol	Parameter	Min	Typ	Max	Unit
$I_{LDO1MAX}$	Rated output load current, Normal mode	300	—	—	mA
$I_{LDO1MAXLPM}$	Rated output load current, Low-power mode	10	—	—	mA
$V_{LDO1TOL}$	Output voltage tolerance, Normal mode $V_{LDO1INMIN} < V_{LDO1IN} < 4.5$ V, 0 mA < $I_{LDO1} \leq 300$ mA 0.8 V ≤ V_{LDO1} < 1.8 V 1.8 V ≤ $V_{LDO1} \leq 3.3$ V $V_{LDO1INMIN} < V_{LDO1IN} < 4.5$ V, 0 mA < I_{LDO1} < 10 mA (Low-power mode)	 −2.5 −2.5 −4.0	 — — —	 2.5 2.5 4.0	%
$I_{LDO1LIM}$	Current limit I_{LDO1} when V_{LDO1} is forced to $V_{LDO1NOM}/2$	320	—	1000	mA
$I_{LDO1OCP}$	LDO1FAULTI threshold (also used to disable LDO1 when REGSCPEN = 1)	320	—	1000	mA
I_{LDO1Q}	Quiescent current (at 25 °C) No load, change in I_{VSYS} and $I_{VLDOIN1}$ When LDO1 enabled in Normal mode When LDO1 enabled in Low-power mode	 — —	 17 2.5	 — —	µA
$R_{DSON\_QFN\_LDO1}$	Dropout on resistance	—	—	350	mΩ
$PSRR_{LDO1}$	PSRR I_{LDO1} = 150 mA, 20 Hz to 20 kHz V_{LDO1} = 3.30 V, V_{LDO1IN} = 3.8 V, VSYS = 4.2 V	 —	 56	 —	dB
TR_{VLDO1}	Turn on time 10 % to 90 % of end value $V_{LDO1INMIN} < V_{LDO1IN} \leq 4.5$ V, I_{LDO1} = 0.0 mA	 —	 200	 500	µs
$R_{LDO1DIS}$	Turn off discharge resistance	—	250	—	Ω
$LDO1OUT_{OSHT}$	Start-up overshoot (% of final value) $V_{LDO1INMIN} < V_{LDO1IN} \leq 4.5$ V, I_{LDO1} = 0.0 mA	 —	 1.0	 2.0	%
$V_{LDO1LOTR}$	Transient load response $V_{LDO1INMIN} < V_{LDO1IN} \leq 4.5$ V, I_{LDO1} = 10 mA to 200 mA in 10 µs Overshoot Undershoot	 — —	 50 50	 — —	mV

5.3.5 Electrical characteristics – LDO2

All parameters are specified at T_A = −40 to 105 °C, VSYS = 3.6 V, V_{LDOIN2} = 3.6 V, VLDO2[3:0] = 1111, I_{LDO2} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at VSYS = 3.6 V, V_{LDOIN2} = 3.6 V, VLDO2[3:0] = 1111, I_{LDO2} = 10 mA, and 25 °C, unless otherwise noted.

Table 22. LDO2 electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{LDO2IN}	Operating input voltage 1.8 V ≤ $V_{LDO2NOM} \leq 2.5$ V 2.6 V ≤ $V_{LDO2NOM} \leq 3.3$ V	 2.8 $V_{LDO2NOM}$ + 0.250	 – –	 4.5 4.5	V
$V_{LDO2NOM}$	Nominal output voltage	—	See Table 43	—	V
$I_{LDO2MAX}$	Rated output load current, Normal mode	400	—	—	mA
$I_{LDO2MAXLPM}$	Rated output load current, Low-power mode	10	—	—	mA
$V_{LDO2TOL}$	Output voltage tolerance $V_{LDO2INMIN} < V_{LDO2IN} < 4.5$ V 10.0 mA ≤ I_{LDO2} < 400 mA 0.0 mA < I_{LDO2} < 10 mA (Low-power mode)	 −2.0 −4.0	 — —	 2.0 4.0	%
$I_{LDO2LIM}$	Current limit I_{LDO2} when V_{LDO2} is forced to $V_{LDO2NOM}/2$	450	750	1050	mA
$I_{LDO2OCP}$	LDO2FAULTI threshold (also used to disable LDO2 when REGSCPEN = 1)	450	—	1050	mA

Symbol	Parameter	Min	Typ	Max	Unit
I_{LDO2Q}	Quiescent Current (25 °C) No load, change in I_{VSYS} and $I_{VLDO2IN}$ When V_{LDO2} enabled in Normal mode When V_{LDO2} enabled in Low-power mode	 — —	 15 1.5	 — —	µA
$R_{DSON\_QFN\_LDO2}$	Dropout on resistance	—	—	300	mΩ
$PSRR_{VLDO2}$	PSRR I_{LDO2} = 200 mA, 20 Hz to 20 kHz V_{LDO2} = 3.30 V, V_{LDO2IN} = 3.9 V, VSYS = 4.2 V	—	60	—	dB
t_{ONLDO2}	Turn on time 10 % to 90 % of end value $V_{LDO2INMIN} < V_{LDO2IN} \leq 4.5$ V, I_{LDO2} = 0.0 mA	—	200	500	µs
$R_{LDO2DIS}$	Turn off discharge resistance	—	250	—	Ω
$LDO2OUT_{OSHT}$	Start-up overshoot (% of final value) $V_{LDO2INMIN} < V_{LDO2IN} \leq 4.5$ V, I_{LDO2} = 0.0 mA	—	1.0	2.0	%
$V_{LDO2LOTR}$	Transient load response $V_{LDO2INMIN} < V_{LDO2IN} \leq 4.5$ V, I_{LDO2} = 10 mA to 100 mA in 10 µs Overshoot Undershoot	 — —	 50 50	 — —	mV

5.3.6 Electrical characteristics – LDO3

All parameters are specified at T_A = −40 to 105 °C, VSYS = 2.5 to 4.5 V, V_{LDOIN3} = 3.6 V, VLDO3[4:0] = 11111, I_{LDO3} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at VSYS = 3.6 V, V_{LDOIN3} = 3.6 V, VLDO3[4:0] = 11111, I_{LDO3} = 10 mA, and 25 °C, unless otherwise noted.

Table 23. LDO3 electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{LDO3IN}	Operating input voltage V_{LDO3} + 250 mV ≤ VSYS ≤ 4.5 V	1.0	—	4.5	V
$V_{LDO3NOM}$	Nominal output voltage	—	See Table 41	—	V
$I_{LDO3MAX}$	Rated output load current, Normal mode	300	—	—	mA
$I_{LDO3MAXLPM}$	Rated output load current, Low-power mode	10	—	—	mA
$V_{LDO3TOL}$	Output voltage tolerance, Normal mode $V_{LDO3INMIN} < V_{LDO3IN}$ < 4.5 V, 0 mA < I_{LDO3} < 300 mA 0.8 V ≤ V_{LDO3} < 1.8 V 1.8 V ≤ V_{LDO3} ≤ 3.3 V $V_{LDO3INMIN} < V_{LDO3IN}$ < 4.5 V, 0 mA < I_{LDO3} < 10 mA (Low-power mode)	 −2.5 −2.5 −4.0	 — — —	 2.5 2.5 4.0	%
$I_{LDO3LIM}$	Current limit I_{LDO3} when V_{LDO3} is forced to $V_{LDO3NOM}$/2	320	—	1000	mA
$I_{LDO3OCP}$	LDO3FAULTI threshold (also used to disable LDO3 when REGSCPEN = 1)	320	—	1000	mA
I_{LDO3Q}	Quiescent current (at 25 °C) No load, change in I_{VSYS} and $I_{VLDOIN3}$ When LDO3 enabled in Normal mode When LDO3 enabled in Low-power mode	 — —	 17 2.5	 — —	µA
$R_{DSON\_QFN\_LDO3}$	Dropout on resistance	—	—	350	mΩ
$PSRR_{LDO3}$	PSRR I_{LDO3} = 150 mA, 20 Hz to 20 kHz V_{LDO3} = 3.30 V, V_{LDO3IN} = 3.8 V, VSYS = 4.2 V	—	56	—	dB
TR_{VLDO3}	Turn on time 10 % to 90 % of end value $V_{LDO3INMIN} < V_{LDO3IN}$ < 4.5 V, I_{LDO3} = 0.0 mA	—	200	500	µs

Symbol	Parameter	Min	Typ	Max	Unit
$R_{LDO3DIS}$	Turn off discharge resistance	—	250	—	Ω
$LDO3OUT_{OSHT}$	Start-up overshoot (% of final value) $V_{LDO3INMIN} < V_{LDO3IN} \leq 4.5$ V, I_{LDO3} = 0.0 mA	 —	 1.0	 2.0	%
$V_{LDO3LOTR}$	Transient load response $V_{LDO3INMIN} < V_{LDO3IN} \leq 4.5$ V, I_{LDO3} = 10 mA to 100 mA in 10 µs Overshoot Undershoot	 — —	 50 50	 — —	mV

5.3.7 Electrical characteristics – VREFDDR

T_A = −40 to 105 °C, VSYS = 2.5 to 4.5 V, I_{REFDDR} = 0.0 mA, $V_{INREFDDR}$ = 1.35 V and typical external component values, unless otherwise noted. Typical values are characterized at VSYS = 3.6 V, I_{REFDDR} = 0.0 mA, $V_{INREFDDR}$ = 1.35 V, and 25 °C, unless otherwise noted.

Table 24. VREFDDR electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$V_{INREFDDR}$	Operating input voltage range	0.9	—	1.8	V
V_{REFDDR}	Output voltage, 0.9 V < $V_{INREFDDR}$ < 1.8 V, 0 mA < I_{REFDDR} < 10 mA	—	$V_{INREFDDR}$/2	—	V
$V_{REFDDRTOL}$	Output voltage tolerance, as a percentage of $V_{INREFDDR}$, 1.2 V < $V_{INREFDDR}$ < 1.65 V, 0 mA < I_{REFDDR} < 10 mA	49.25	50	50.75	%
$I_{REFDDRQ}$	Quiescent current (at 25 °C)	—	1.1	—	µA
$I_{REFDDRLM}$	Current limit, I_{REFDDR} when V_{REFDDR} is forced to $V_{INREFDDR}$/4	10.5	24	38	mA
$t_{ONREFDDR}$	Turn on time, 10 % to 90 % of end value, $V_{INREFDDR}$ = 1.2 V to 1.65 V, I_{REFDDR} = 0.0 mA	—	—	100	µs

5.3.8 Electrical characteristics – VSNVS

All parameters are specified at T_A = −40 to 105 °C, VSYS = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, typical external component values, unless otherwise noted. Typical values are characterized at VSYS = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, and 25 °C, unless otherwise noted.

Table 25. VSNVS electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{SNVSIN}	Operating input voltage Valid coin cell range Valid VSYS	 1.8 2.45	 — —	 3.3 4.5	V
I_{SNVS}	Operating load current $V_{SNVSINMIN} < V_{SNVSIN} < V_{SNVSINMAX}$	2000	—	—	µA
V_{TL1}	VSYS threshold (VSYS powered to coin cell powered)	—	UVDET failing	—	V
V_{TH1}	VSYS threshold (coin cell powered to VSYS powered)	—	UVDET rising	—	V
V_{SNVS}	Output voltage (when running from VSYS) 0 µA < I_{SNVS} < 2000 µA Output voltage (when running from LICELL) 0 µA < I_{SNVS} < 2000 µA 2.84 V < V_{COIN} < 3.3 V	−7.0 % VCOIN − 0.20	3.0 —	7.0 % —	V
$V_{SNVSDROP}$	Dropout voltage VSYS = 2.9 V I_{SNVS} = 2000 µA	—	—	220	mV
$I_{SNVSLIM}$	Current limit VSYS > V_{TH1}	 5200	 —	 24000	µA

Symbol	Parameter	Min	Typ	Max	Unit
$V_{SNVSTON}$	Turn on time (load capacitor, 0.47 µF) 10 % to 90 % of final value V_{SNVS} V_{COIN} = 0.0 V, I_{SNVS} = 0 µA	—	—	3.0	ms
$V_{SNVSOSH}$	Start-up overshoot I_{SNVS} = 5.0 µA dVSYS/dt = 50 mV/µs	—	40	70	mV
$R_{DSONSNVS}$	Internal switch $R_{DS(on)}$ V_{COIN} = 2.6 V	—	—	100	Ω

5.3.9 Electrical characteristics – IC level bias currents

All parameters are specified at 25 °C, VSYS = 3.6 V, VBUSIN = 0 V, typical external component values, unless otherwise noted. Typical values are characterized at VSYS = 3.6 V, V_{SNVS} = 3.0 V, and 25 °C, unless otherwise noted.

Table 26. IC level electrical characteristics

Mode	PF1550 conditions	System conditions	Typ	Max	Unit
Coin cell	VSNVS from LICELL All other blocks off VSYS = 0.0 V	No load on VSNVS	1.5	4.0	µA
CORE_OFF	VSNVS from VSYS Wake-up from ONKEY active All other blocks off VSYS > UVDET	No load on VSNVS, PMIC able to wake-up	1.5	4.0	µA
Sleep	VSNVS from VSYS Wake-up from PWRON active Trimmed reference active DDR I/O rail in Low-power mode VREFDDR disabled	No load on VSNVS. DDR memories in self refresh.	12.5	25	µA
Standby/Suspend	VSNVS from either VSYS or LICELL SW1 in ultra Low-power mode SW2 in ultra Low-power mode SW3 in ultra Low-power mode Trimmed reference active VLDO1 is disabled VLDO2 enabled in Low-power mode VLDO3 enabled in Low-power mode VREFDDR enabled	No load on VSNVS. Processor enabled in Low-power mode.	23	46	µA
REGS_DISABLE	VSNVS from VSYS Wake-up from ONKEY active Most other blocks off VSYS > UVDET	No load on VSNVS, PMIC able to wake-up	14	20	µA
SHIP	BATFET open, no LICELL connected VSYS = 0 V, only awake from ONKEY enabled		0.45	1.0	µA

6 Detailed description

The PF1550 PMIC features three high efficiency low quiescent current buck regulators, three LDO regulators, a DDR voltage reference to supply voltages for the application processor and peripheral devices.

Additionally, PF1550 incorporates a single cell Li-ion linear battery charger with a USB-PHY regulator.

The buck regulators provide the supply to processor cores and to other low voltage circuits such as I/O and memory. Dynamic voltage scaling is provided to allow controlled supply rail adjustments for the processor cores for power optimization.

The three LDO regulators are general purpose to power various processor rails, system connectivity devices and/or peripherals. Depending on the system power configuration, the general purpose LDO regulators can be directly supplied from the main system supply VSYS or from the switching regulators to power peripherals, such as audio, camera, Bluetooth, Wireless LAN.

A specific VREFDDR voltage reference is included to provide accurate reference voltage for DDR memories operation.

The VSNVS block behaves as an LDO, or as a bypass switch to supply the SNVS (Secure Non-Volatile Storage) /RTC (Real Time Clock) circuitry on the processor. VSNVS is powered from VSYS or from a coin cell.

To accommodate applications that do not include Li-ion battery, the PF1550 battery charger regulates the input voltage at VBUSIN pin down to maximum of 4.5 V at VSYS through the power path circuit.

Table 27. Voltage regulators

Supply	Output voltage (V)	Programming step size (mV)	Load current (mA)
SW1 / SW2	0.60 to 1.3875 / 1.1 to 3.3	12.5 / variable	1000
SW3	1.80 to 3.30	100	1000
LDO1	0.75 to 1.50 1.80 to 3.30	50 100	300
LDO2	1.80 to 3.30	100	400
LDO3	0.75 to 1.50 1.80 to 3.30	50 100	300
USBPHY	3.3 or 4.9	—	60
VSNVS	3.0	N/A	2
VREFDDR	0.5*VINREFDDR	N/A	10

6.1 Buck regulators

The PF1550 features three high efficiency buck regulators with internal compensation. Each buck regulator is capable of meeting optimum power efficiency operation using reduced power variable-frequency pulse skip switching scheme at light loads as well as operating in forced PWM quasi-fixed frequency switching mode at higher loads. The switching regulator controller combines the advantages of hysteretic and voltage mode control which provides outstanding load regulation and transient response, low output ripple voltage and seamless transition between pulse-skip mode and Active Quasi-fixed frequency switching mode. The control circuitry includes an AC loop which senses the output voltage (at SWxFB pin) and directly feeds it to a fast comparator stage. This comparator sets the switching frequency, which is almost constant for steady state operating conditions. It also provides immediate response to dynamic load changes.

In order to achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors. The transition into and out of low power

pulse-skip switching mode takes place automatically according to the load current to maintain optimum power efficiency. Additionally, further power savings through cutting the buck circuitry quiescent current can be achieved by activating a Low-power mode upon entering either STANDBY or SLEEP PMIC power mode or as commanded via I^2C control bits. In SW1 and SW2. An OTP option enables or disables DVS in the regulators. When DVS is disabled and the low-power bit is set, the regulator enters an Ultra Low Power (ULP) mode cuts the operating quiescent current even in order to reach extremely low standby power levels needed for ultra low power processors such as that from Kinetis K and L series.

As indicated above, the buck controller supports PWM (Pulse Width Modulation) mode for medium and high load conditions and low-power variable-frequency pulse skip mode at light loads. During high current mode, it operates in continuous conduction and the switching frequency is up to 2.0 MHz with a controlled on-time variation depending on the input voltage and output voltage. If the load current decreases, the converter seamlessly enters the pulse-skip mode to cut the operating quiescent current and maintain high efficiency down to very light loads. In pulse-skip mode the switching frequency varies linearly with the load current. Since the controller supports both power modes within one single building block, the transition from normal power mode to lower power pulse-skip mode and vice versa is seamless without dramatic effects on the output voltage.

In the adopted pulse-skip scheme, the device generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a non-switching (pause) period where most of the internal circuits are shutdown to achieve a lowest quiescent current. During this time, the load current is supported by the output capacitor. The duration of the pause period depends on the load current and the inductor peak current.

6.2 SW1 and SW2 detailed description

SW1 and SW2 are identical buck regulators designed to carry a nominal load current of 1.0 A. Detailed characteristics and features of SW1 and SW2 are described in this section. Being identical, reference is made only to SWx though the same specifications apply to SW1 and SW2.

6.2.1 SWx dynamic voltage scaling description

SWx integrates an optional DVS circuit that is enabled via OTP. To reduce overall power consumption, when DVS is enabled SWx output voltage can be varied depending on the mode or activity level of the processor.

- **Normal operation:**
  The output voltage is selected by I^2C bits SWx_VOLT[5:0]. A voltage transition initiated by I^2C is governed by the SWx_DVSSPEED I^2C bit as shown in Table 28.
- **Standby mode:**
  The output voltage can be selected by I^2C bits SWx_STBY_VOLT[5:0]. Voltage transitions initiated by a Standby event are governed by the SWx_DVSSPEED I^2C bit as shown in Table 28. This applies only when DVS is enabled.
- **Sleep mode:**
  The output voltage can be higher or lower than in normal operation, but is typically selected to be the lowest state retention voltage of a given processor; it is selected by I^2C bits SWx_SLP_VOLT[5:0]. Voltage transitions initiated by a turn off event are governed by the SWx_DVSSPEED I^2C bit for SWx as shown in Table 28. This applies only when DVS is enabled.