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Rev. 3.0, 8/2016

Fully integrated octal valve controller system on chip

SB0800

INDUSTRIAL CONTROLLER CHIP

AE SUFFIX (PB-FREE)
98ASA10763D
64-PIN LQFP-EP

The SB0800 device is a valves and pump controller system designed for use in harsh industrial environments.

It has eight high-current low-side drivers for use with solenoid valves, and high-side gate drivers for use with controlling two external N-channel MOSFETs, for DC motor and a master relay for solenoid coils. Alongside this, the SB0800 has three analog to digital converters, plus a low-side driver allowing drive resistive charges. The SB0800 boosts an internal charge pump, permitting the high-side drivers to use inexpensive N-channel MOSFETs. The digital I/O pins can be configured for both 5.0 V and 3.3 V levels for easy connection to any microprocessor. The SB0800 uses standard SPI protocol communication.

The SB0800 is a perfect solution for hydraulic and pneumatic applications. This device is powered by SMARTMOS technology.

Features

- Operating voltage 6.0 V to 36 V
- Eight valves control
  - Four current regulated valves up to 2.25 A (5.0 kHz)
  - Four PWMed valves up to 5.0 A (5.0 kHz)
- High-side predriver for valves protection
- Pump motor predriver up to 500 Hz PWM
- 16-bit SPI interface with watchdog
- Three 10-bit ADC channels
- High-side driver for general purpose ($R_{DS(on)}$ 1.0 Ω)
- Low-side driver for resistive charge ($R_{DS(on)}$ 14.0 Ω)
- Die temperature warning
- Supervision

Applications

Industrial Controller

- Spot Welding
- Fluid Coating
- Temperature Control
- Brake Pressure
- Laser Cutting
- Bottle Moulding
- Filling Pressure
- 3D Printer
- Oxygen Concentrator
- Medical test equipment
- Dialysis machines
- Blood pressure
- Soda dispensers
- Heavy equipment and construction machinery
- Fork lifts
- Water control system for irrigation (connected to farm tractor)
- Food control in animal farm

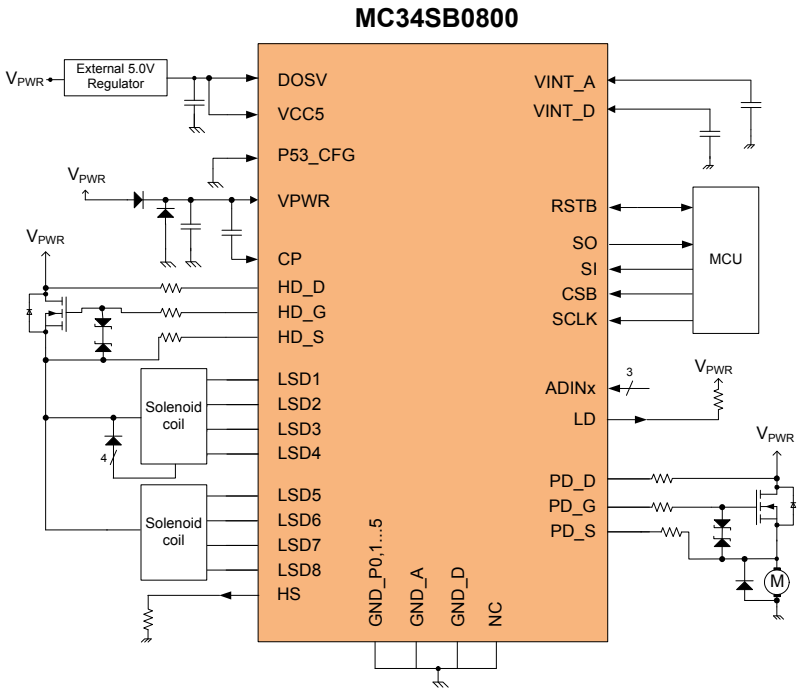

Figure 1. SB0800 simplified 5.0 V application diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

1 Orderable parts

This section describes the part numbers available to be purchased along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.nxp.com and perform a part number search for the following device numbers.

Table 1. Orderable part variations

Part number	Temperature (T_A)	Package	Description	Notes
34SB0800 octal valves and pump controller system on chip for industrial				
MC34SB0800AE	-40 °C to 125 °C	10 x 10, 64 LQFP-EP	• Four PWMed valve controls and four current regulated valve controls • Safe switch control • Pump motor control up to 500 Hz • High-side driver for general purpose • Low-side FET for resistive loads	(1)

Notes
1. To order parts in Tape & Reel, add the R2 suffix to the part number.

Table of Contents

2 Internal block diagram

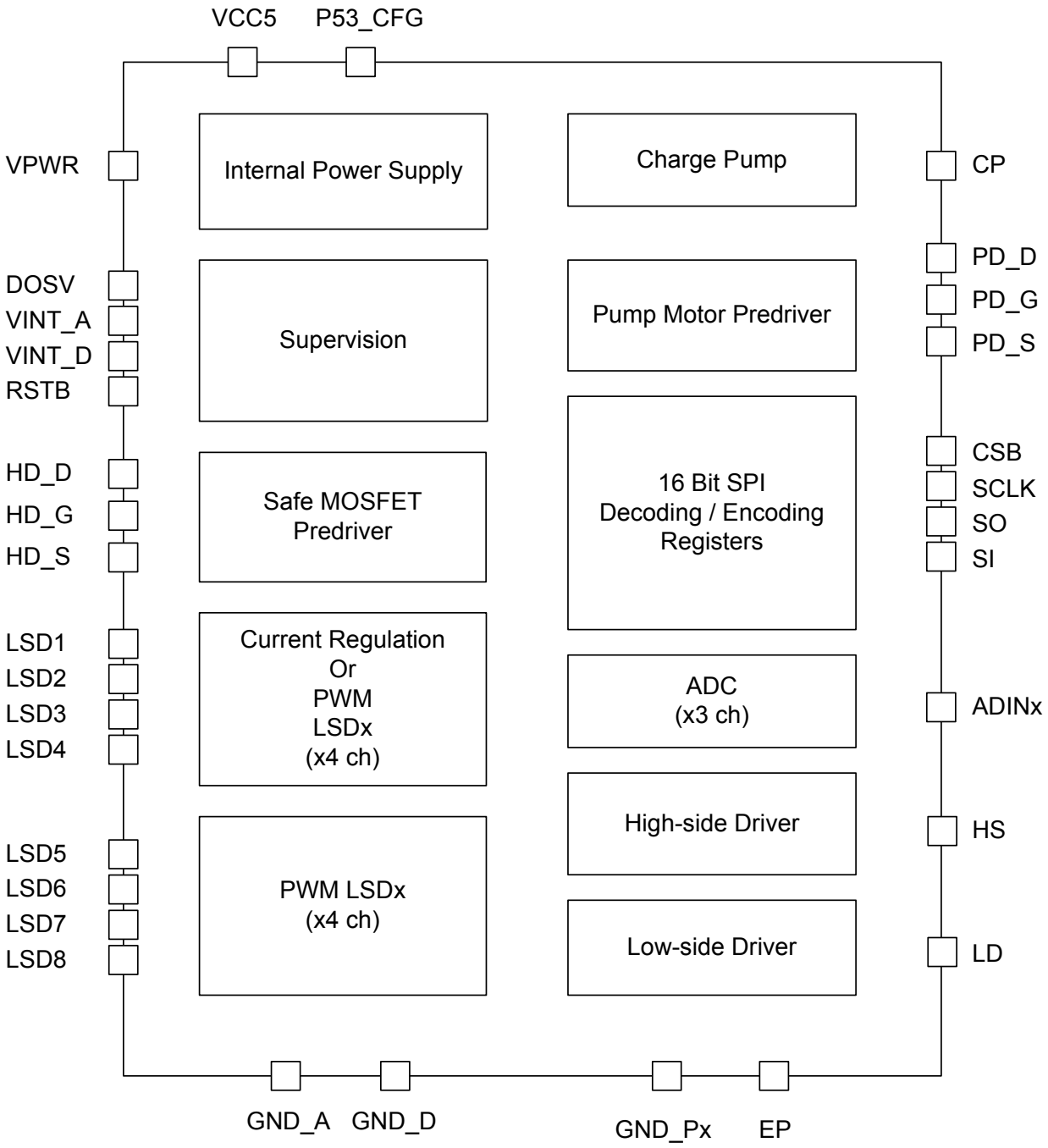

Figure 2. SB0800 simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

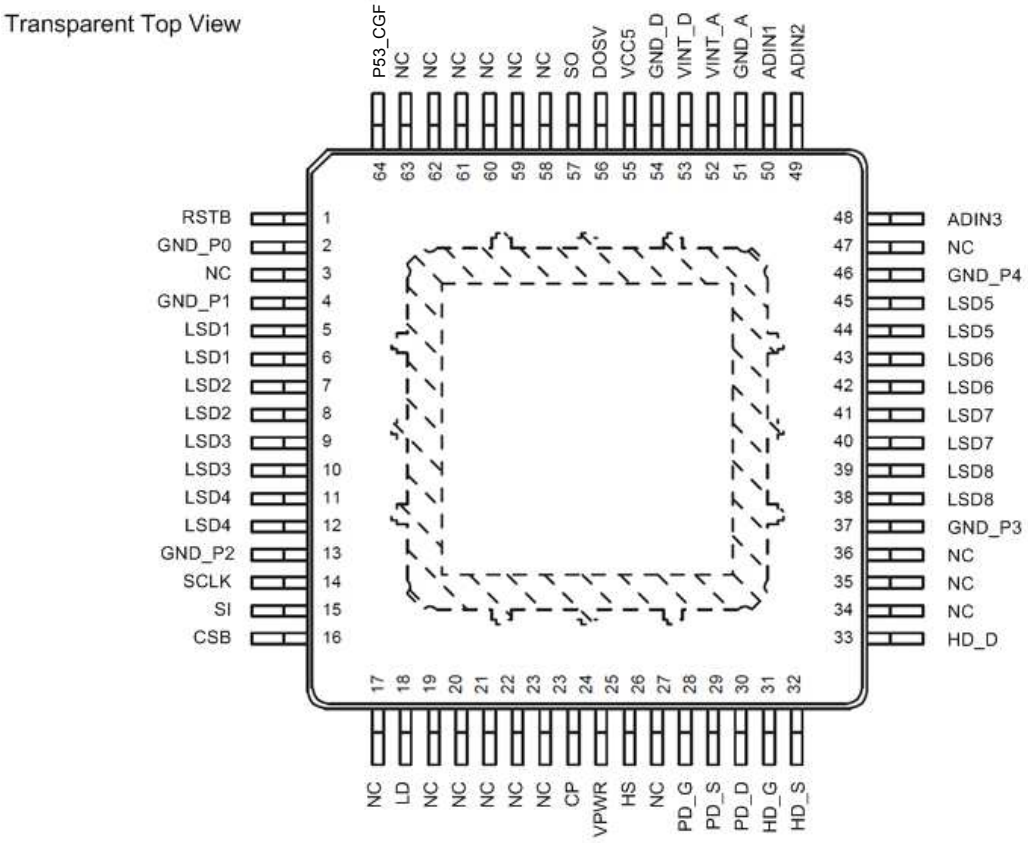

Figure 3. SB0800 64-pin LQFP-EP pinout diagram

3.2 Pin definitions

Table 2. SB0800 pin definitions

Pin number	Pin name	Pin function	Definition	DOSV = 5.0 V	DOSV = 3.3 V	Notes
1	RSTB	Reset	Reset PIN	external pull-up		
2	GND_P0	Supply	Power Ground 0 (4)	no	no	
4	GND_P1	Supply	Power Ground 1	no	no	(4)
5, 6	LSD1	Low-side Driver for Current Regulated & PWMed Valves	Open Drain Output for Low-side Driver 1	no	no	(2)
7, 8	LSD2	Low-side Driver for Current Regulated & PWMed Valves	Open Drain Output for Low-side Driver 2	no	no	(2)
9, 10	LSD3	Low-side Driver for Current Regulated & PWMed Valves	Open Drain Output for Low-side Driver 3	no	no	(2)
11, 12	LSD4	Low-side Driver for Current Regulated & PWMed Valves	Open Drain Output for Low-side Driver 4	no	no	(2)
13	GND_P2	Supply	Power Ground 2	no	no	(4)
14	SCLK	SPI	SPI Interface Clock Input	no	no	
15	SI	SPI	SPI Interface Digital Input	no	no	
16	CSB	SPI	SPI Interface Chip Interface	no	no	
18	LD	Low-side Driver	Open Drain Output for Low-side	no	no	
24	CP	Charge Pump	Charge Pump Output. For internal use, connect a storage capacitor of > 68 nF to VPWR.	no	no	
25	VPWR	Supply	Supply PIN connect to battery through reverse diode	no	no	
26	HS	High-side Driver for General Purpose (optional)	High-side driver for general purpose	no	no	
28	PD_G	Motor Pump Driver	Gate Output to Control Pump Motor FET Connect to gate of external pump motor FET	no	no	
29	PD_S	Motor Pump Driver	Source Feedback Pump Motor FET Connect to source of external pump motor FET	no	no	
30	PD_D	Motor Pump Driver	Drain Feedback Pump Motor FET Connect to drain of external pump motor FET	no	no	
31	HD_G	High-side Driver for Valve's Fail-safe FET	Gate Output to Control High-side FET Connect to gate of external pump motor FET	no	no	
32	HD_S	High-side Driver for Valve's Fail-safe FET	Source Feedback High-side FET Connect to source of external High-side FET	no	no	
33	HD_D	High-side Driver for Valve's Fail-safe FET	Drain Feedback High-side FET Connect to drain of external High-side FET	no	no	
37	GND_P3	Supply	Power Ground 3	no	no	(4)
38, 39 (2)	LSD8	Low-side Driver for PWMed Valves	Open Drain Output for Low-side Driver 8	no	no	
40, 41 (2)	LSD7	Low-side Driver for PWMed Valves	Open Drain Output for Low-side Driver 7	no	no	
42, 43 (2)	LSD6	Low-side Driver for PWMed Valves	Open Drain Output for Low-side Driver 6	no	no	
44, 45 (2)	LSD5	Low-side Driver for PWMed Valves	Open Drain Output for Low-side Driver 5	no	no	
46	GND_P4	Supply	Power Ground 4	no	no	(4)
48	ADIN3	ADC	Analog to Digital Input 3	no	no	

Table 2. SB0800 pin definitions (continued)

Pin number	Pin name	Pin function	Definition	DOSV = 5.0 V	DOSV = 3.3 V	Notes
49	ADIN2	ADC	Analog to Digital Input 2	no	no	
50	ADIN1	ADC	Analog to Digital Input 1	no	no	
51	GND_A	Supply	Analog Ground	no	no	
52	VINT_A	Internal Function	2.5 V internal supply for analog	no	no	(2)
53	VINT_D	Internal Function	2.5 V internal supply for digital	no	no	(2)
54	GND_D	Supply	Digital Ground	no	no	
55	VCC5	Supply	5.0 V Supply PIN	5V	5V	
56	DOSV	Supply	Digital Output Voltage Supply, DOSV under voltage reset	5V	3.3V	
57	SO	SPI	SPI Interface Digital Output	DOSV bias		
64	P53_CFG	Supply	Input to select output voltage at DOSV (5.0 V/ 3.3 V)	no	no	
20, 21, 22, 23, 58, 59, 60, 61, 62	NC	Not connected	Pin used for production tests and must not be grounded	no	no	
3, 17, 19, 27, 34, 35, 36, 47, 63	NC	Not connected	Pin used for production tests and must be grounded	no	no	
Exposed pad	GND_P5	Supply	Power Ground 5	no	no	(4)

Notes

2. Pins must be shorted together
3. 220 nF/10 V capacitor needed
4. All GND_Px pins must be shorted together at the PCB level.

4 General product characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

Voltage parameters are absolute voltages referenced to GND_A, GND_D and flag (tied together internally). Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min.	Max.	Unit	Notes
Supply					
V_{VPWR}	Analog Power supply voltage	-0.3	40	V	
V_{DOSV}	Digital Output Supply Voltage	-0.3	7.0	V	
V_{P53_CFG}	Selection of 5.0 V or 3.3 V for the digital	-0.3	7.0	V	
V_{VCC5}	Digital power supply voltage	-0.3	7.0	V	
V_{GND_A}	Ground analog	-0.3	0.3	V	
V_{GND_D}	Ground digital	-0.3	0.3	V	
V_{GND_P}	Ground exposed pad	-0.3	0.3	V	
Internal function					
V_{VINT_A}	Internal regulator analog power supply	-0.3	3.0	V	
V_{VINT_D}	Internal regulator digital power supply	-0.3	3.0	V	
Charge pump					
V_{CP}	Internal charge pump	-0.3 or V_{PWR} -0.3	V_{PWR} +15	V	
High-side driver for general purpose					
V_{HS}	High-side driver	-0.3	40 or V_{PWR} +0.3	V	
High-side driver for valve's fail-safe FET					
V_{HD_G}	Gate of the high-side predriver	-20	55	V	
V_{HD_S}	Source of the high-side predriver	-0.3	40	V	
V_{HD_D}	Drain of the high-side predriver	-0.3	40	V	
Motor pump driver					
V_{PD_G}	Gate of the Motor Pump predriver	-0.3	55	V	
V_{PD_S}	Source of the Motor Pump predriver	-0.3	40	V	
V_{PD_D}	Drain of the Motor Pump predriver	-0.3	40	V	
Reset					
V_{RSTB}	Reset pin	-0.3	7.0	V	
A to D converter					
V_{ADINx}	Input analog to digital	-0.3	7.0	V	

Table 3. Maximum ratings (continued)

Voltage parameters are absolute voltages referenced to GND_A, GND_D and flag (tied together internally). Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min.	Max.	Unit	Notes
SPI					
V_{SO}	Serial peripheral interface slave output	-0.3	DOSV +0.3	V	
V_{SI}	Serial peripheral interface slave input	-0.3	7.0	V	
V_{CSB}	Serial peripheral interface chip select	-0.3	7.0	V	
V_{SCLK}	Serial peripheral interface clock	-0.3	7.0	V	
Low-side driver for valves (LSD1-8)					
V_{LSDx}	Low-side driver for valves	Table	active clamp		
Low-side driver					
V_{LD}	Low-side driver	-100 mA	40	V	
Energy capability					
$E_{LSD1—4}$	Energy capability (EAR) at 125 °C • LSD1—4, with 20 mH load	—	30	mJ	
$E_{LSD5—8}$	Energy capability (EAR) at 125 °C • LSD5—8, with 20 mH load	—	40	mJ	
E_{HS}	Energy capability (EAR) at 125 °C • HS, with 20 mH load	—	13	mJ	
Currents					
$I_{LSDX(POS)}$	Drain continuous current; during on state • LSDx	—	5.0	A	
$I_{LSDX(NEG)}$	Maximum negative current for 5.0 ms without being destroyed • LSDx	-6.0	—	A	
I_{DIG}	Input current • P53_CFG, SI, CSB, SCLK, RSTB	-20	20	mA	

4.2 Operating conditions

This section describes the operating conditions and the current consumptions. Conditions apply to all the following data, unless otherwise noted.

Table 4. Operating conditions

Voltage parameters are absolute voltages referenced to GND. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min.	Typ.	Max.	Unit	Notes
V_{PWR}	Functional operating supply voltage. Device is fully functional. • All features are operating	6.0	—	36	V	
V_{CC5}	Functional operating supply voltage. Device is fully functional. • All features are operating.	4.75	—	5.25	V	
V_{DOSV}	Functional operating supply voltage. Device is fully functional. • All features are operating.	3.13	—	5.25	V	

4.3 Supply currents

This section describes the operating conditions and the current consumptions. Conditions apply to all the following data, unless otherwise noted.

Table 5. Supply currents

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 36 V, 4.75 V ≤ V_{CC5} ≤ 5.25 V, 3.13 V ≤ V_{DOSV} ≤ 5.25 V, -40 °C ≤ T_J ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Description (rating)	Min.	Typ.	Max.	Unit	Notes
VPWR current consumptions						
I_{QVPWR}	Quiescent current of VPWR measured at 36 V, V_{CC5} = 0 V	—	—	30	μA	
I_{VPWR}	Current of VPWR in operating mode, V_{CC5} = 5.0 V	—	20	—	mA	
VCC5 current consumptions						
I_{VCC5}	Current of VCC5 pin in operating mode (SPI frequency at 10 MHz)	—	10	—	mA	
DOSV current consumptions						
I_{DOSV}	Current of DOSV pin in operating mode (SPI frequency at 10 MHz)	—	—	10	mA	

4.4 Thermal ratings

Table 6. Thermal data

Symbol	Description (rating)	Min.	Typ.	Max.	Unit	Notes
T_J	Operational junction Temperature	-40	—	150	°C	
T_{STG}	Storage Temperature	-65	—	150	°C	
$R_{\theta JC}$	RθJC, Thermal Resistance, Junction to Case (Package exposed pad) - Steady state	—	—	2.0	°C/W	
T_{PPRT}	Peak Package Reflow Temperature During Reflow	—	—	Note 7	°C	(5)(6)

Notes

5. Lead soldering temperature limit is for 10 seconds maximum duration. Lead soldering can be done twice. Device must be delivered in dry pack.
6. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.nxp.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

4.5 Logical inputs and outputs

Table 7. Logical inputs/outputs

V_{PWR} = 6.0 to 36 V, VCC5 = 4.75 to 5.25 V, DOSV = 3.13 to 5.25 V, T_J = -40 to 125 °C, unless otherwise specified.

Symbol	Description (rating)	Min.	Max.	Unit	Notes
Logical inputs					
V_{IH_X}	Input High-voltage • P53_CFG, RSTB, SI, CSB, SCLK, ADIN1, ADIN2, ADIN3	—	2.0	V	
V_{IL_X}	Input Low-voltage • P53_CFG, RSTB, SI, CSB, SCLK, ADIN1, ADIN2, ADIN3	0.8	—	V	
Logical outputs					
V_{OH_X}	Input High-voltage, with 1.0 mA • SO	0.8 x DOSV	—	V	
V_{OL_X}	Input Low-voltage, with 1.0 mA • SO	—	0.4	V	
$VOL_{\_RSTB}$	RSTB Low-voltage, with 1.0 mA • RSTB	—	0.4	V	

5 General description

5.1 Block diagram

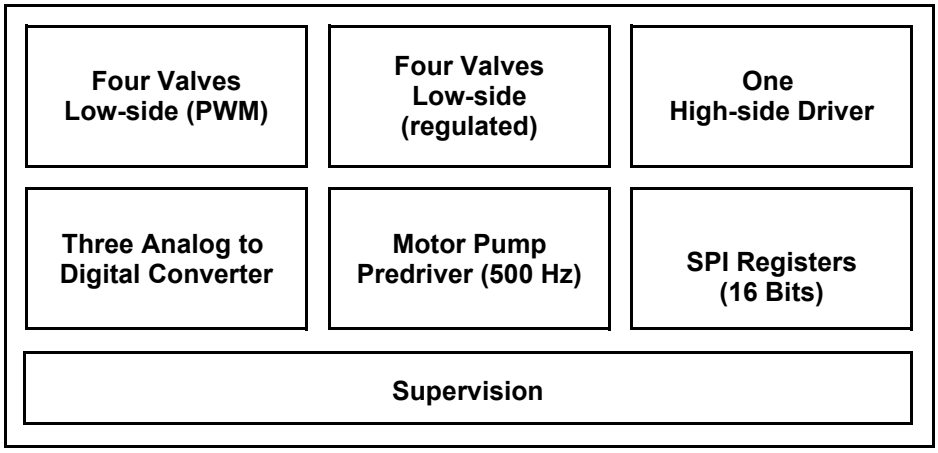

Figure 4. SB0800 functional block diagram

5.2 Functional description

The SB0800 device is a valves and pump controller, designed for use in harsh industrial environments, requiring few external components.

The SB0800 eight high-current low-side drivers for use with solenoid valves, and high-side gate drivers for controlling two external N-channel MOSFETs for use with a pump motor and master relay for a solenoid coil. In conjunction with this primary functionality, the SB0800 has one low-side driver to control a resistive load. The SB0800 boosts an internal charge-pump, allowing the high-side drivers to use inexpensive N-channel MOSFETs. The digital I/O pins can be configured for both 5.0 V and 3.3 V levels for easy connection to any microprocessor. Also, the device integrated three Analog to Digital converters. The SB0800 uses standard SPI protocol for communication.

5.3 Features

This section presents the detailed features of SB0800.

Table 8. Device features set

Function	Description
High-side Driver for Fail-safe FET	• High-side Fail-safe FET driver • Overcurrent shutdown • Load leakage detection
High-side Driver for general purpose	• High-side switch connected to VPWR (1.0 Ω max Rds(on) at 125 °C) • Open load detection • V_{DS} state monitoring • Overcurrent shutdown • Overtemperature shutdown
Pump Driver	• Pump motor driver up to 500 Hz PWM frequency controllable through SPI command or a digital signal • Overcurrent shutdown between external FET drain and source

Table 8. Device features set (continued)

Function	Description
Low-side solenoid driver (x4)	• Solenoid driver (300 mΩ max. $R_{DS(on)}$ at 125 °C) works either as current regulator or as PWM • Current regulation deviation: ±2.0% • Configurable PWM frequency from 3.0 kHz to 5.0 kHz • PWM duty cycle 10-bit resolution • Open load detection • V_{DS} state monitoring • Overcurrent shutdown • Overtemperature shutdown • Send current regulation error flag (only for current regulation modules)
Low-side solenoid driver (x4)	• Solenoid driver (225 mΩ max $R_{DS(ON)}$ at 125 °C) are PWM low-side driver • Configurable PWM frequency from 3.0 kHz to 5.0 kHz • PWM duty cycle resolution 0.39% • Open load detection • V_{DS} state monitoring • Overcurrent shutdown • Overtemperature shutdown • Max switch-off energy 40 mJ
Low-side resistive Driver	• Low-side driver (20 mA max, $R_{DS(on)}$ 8.0 Ω) • Open load detection • V_{DS} state monitoring • Overcurrent shutdown • Overtemperature shutdown
Low-side Driver	• Low-side driver (350 mA max, $R_{DS(on)}$ 1.0 Ω) • Open load detection • V_{DS} state monitoring • Overcurrent shutdown • Overtemperature shutdown
Analog to Digital Converter (x3)	• 10-bit ADC • External ADINx pins • Internal voltages and temperature information • Allow to control the pump by a MCU • Allow to control the low-side resistive driver by a MCU
Supervision	• VINT_x undervoltage (internal regulator) • VCC5 & DOSV undervoltage (supply voltage from external) • Watchdog fault • ALU check counter overflow • External reset fault • VPWR undervoltage and overvoltage detections • Mismatch MAIN-AUX OSC CLK • Temperature warning • SPI failure • Charge pump issue • GND supervision

6 Functional block description

6.1 Error handling

Table 9. Error handling

Type of error	Detection condition	Action	Clear SPI flag	Restart condition	Notes
High-side driver					
Overcurrent between external FET Drain and Source	ON	HD_G Off + SPI fault flag (HD_oc)	Write 1 to HD_clr_flt 1	Write 1 to HD_clr_ fit and then turn on by SPI command (hd_ on)	
Load leakage	hd_on rise-edge (SPI bit)	Ignore hd_on rise-edge command + SPI fault flag (HD lkg)	Write 1 to HD_clr_flt	Write 1 to HD_clr_flt and then turn on by SPI command (hd_ on)	
Pump motor PWM driver					
Overcurrent between external FET Drain and Source	ON	PD_G Off+ SPI fault flag (PD_oc)	Write 1 to PD_clr_flt	Write 1 to PD_clr_flt and then turn-on by SPI command (pd on)	
LSDx					
Open Load	OFF	SPI flag only (LSDx_op)	Read diagnosis	No	
V_{DS} state monitoring	ON/OFF	Read V_{DS} state by SPI (vds_LSDx)	update with min filter time (T1) rise and fall edge	No	
Overcurrent	ON	OFF fault FET only + SPI fault flag (LSDx_oc)	Write 1 to LSD_clr_flt	Write 1 to LSD_clr_flt and turn on by SPI command (LSDx duty cycle or current set point)	
Overtemperature	ON	OFF fault FET only + SPI fault flag (LSDx_ot)	Write 1 to LSD_clr_flt	Write 1 to LSD_clr_flt and turn on by SPI command (LSDx duty cycle or current set point)	
Current regulation error (only for LSD1-4)	ON	Read SPI flag only (LSDx_crer)	Read diagnosis	No	
LDx					
Open Load	OFF	SPI flag only (LDx_op)	Read diagnosis	No	
V_{DS} state monitoring	ON/OFF	Send V_{DS} state by SPI (V_{DS_LD})	update with min filter time (T1) rise and fall edge	No	
Overcurrent	ON	OFF fault FET only + SPI fault flag (LD_oc)	Write 1 to LD_clr_flt	Write 1 to LD_clr_flt and turn on by SPI command (LD_on)	
Overtemperature	ON	OFF fault FET only + SPI fault flag (LD_ot)	Write 1 to LD_clr_flt	Write 1 to LD_clr_flt and turn on by SPI command (LD_on)	
HS					
Open Load	OFF	SPI flag only (HS_ op)	Read diagnosis	No	
V_{DS} state monitoring	ON/OFF	Send V_{DS} state by SPI (V_{DS_HS})	update with min filter time	No	
Overcurrent	ON	OFF fault FET only + SPI fault flag (HS_oc)	Write 1 to HS_clr_flt	Write 1 to HS_clr_flt and then turn on by SPI command (HS_ on)	

Table 9. Error handling (continued)

Type of error	Detection condition	Action	Clear SPI flag	Restart condition	Notes
Overtemperature	ON	OFF fault FET only + SPI fault flag (HS_ot)	Write 1 to HS_clr_flt	Write 1 to HS_clr_flt and then turn on by SPI command (HS_on)	
Supervision					
VINT_x Undervoltage	All except Sleep mode	SPI register reset & Vint_uv go to High	Read Vint_uv bit	No	
VCC5 & DOSV Undervoltage	All except Sleep mode	SPI register reset except VCC5_uv go to High	Wait undervoltage reset filter time T1 (see Table 19)	See Table 19,	
External reset fault	No internal RSTB pulldown	SPI registers go to initial state	Read the Message 0 of SPI register (see Table 19)	See Table 19,	
VPWR Undervoltage	RSTB is high state	All LSDx Off (Clear all LSDx duty cycle registers or current set point) + SPI fault flag (V_{PWR_UV})	1. Normal condition 2. Read diagnosis (V_{PWR_UV})	1. Normal condition 2. Turn on by SPI command (LSDx duty cycle or current set point)	
VPWR Overvoltage	RSTB is in high state	All LSDx Off (Clear all LSDx duty cycle registers or current set point) + SPI fault flag (V_{PWR_OV})	1. Normal condition 2. Read diagnosis (V_{PWR_OV})	1. Normal condition 2. Turn on by SPI command (LSDx duty cycle or current set point)	
Mismatch SB0800 MAIN-AUX OSC CLK	RSTB is in high state	SPI registers goes to initial state low except, see Table 27	Read RST_clk bit	No	
Temperature Warning	RSTB is in high state	SPI flag	1. Normal condition 2. Read diagnosis	No	
SPI Failure	RSTB is in high state	SPI flag (Fmsg)	Read diagnosis	No	
V_{PRE} 10 Monitoring	RSTB is in high state	Send by SPI (ADC)	No	No	(9)
V_{PRE} 12 Monitoring	RSTB is in high state	Send by SPI (ADC)	No	No	(9)
VINT_x Monitoring	RSTB is in high state	Send by SPI (ADC)	No	No	(9)
V_{cp_vpwr} Monitoring	RSTB is in high state	Send by SPI (ADC)	No	No	
Temperature Monitoring	RSTB is in high state	Send by SPI (ADC)	No	No	(9)
GND_D Supervision	RSTB is in high state	SPI flag only (FGND)	No	No	
GND_A Supervision; indirect detection by VCC5 or DOSV	RSTB is in high state	SPI flag only (VCC5_UV or DOSV_UV)	No	No	

Notes

7. If xxx_clr_flt is written “1” by SPI, all SPI flags are set “0”, so SW engineer has to read the SPI flag first and then write xxx_clr_flt to default value “0”.
8. SW engineering can monitor internal supply voltage in real time with ADC reading, and can use fail-safe function. If these ADC results are not in a certain range, uC can reset the SB0800 (see ADC section).
9. Fail-safe switch off until power is off

6.2 High-side driver

6.2.1 Function description

The high-side driver is intended to control the fail-safe switch for the overall solenoid path, and HD_G is controlled by the SPI command.

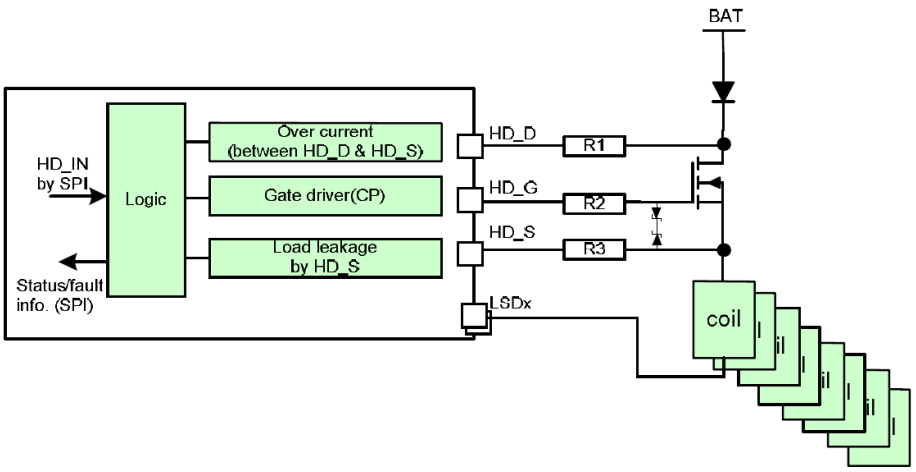

Figure 5. High-side driver

6.2.2 High-side driver and fault protection

6.2.2.1 Overcurrent

High-side driver protects the external n-channel power FET on HD_G in overcurrent conditions. The drain-source voltage of the FET on HD_G is checked if the high-side driver is switched on. If the measured drain-source voltage exceeds the overcurrent voltage threshold, the output of the overcurrent comparator is enabled. If the output of the comparator is active longer than the defined filter time, the output HD_G is switched off. Overcurrent detection logic has a masking time from hd_on turn-on against malfunctions on transient time. After switching off the power FET on HD_G by an overcurrent condition, the power FET can be turned back to a “normal state” by a SPI write 1 to the “HD_clr_flt” register, and then turned on by a SPI command.

6.2.2.2 Load leakage detection

Each time HD_G is turned on, the ILCdet current is sourced out of the HD_S pin for the time t_{HD_LC}, to check the external leakage current on the node in the application. The high-side switch on HD_G is turned on if the measured voltage is over the detection threshold. If this test fails, HD_G does not turn-on and the fault flag is set to high. The power FET can be turned back to a “normal state” only by a SPI write 1 to the “HD_clr_flt” register, and then turned on by a SPI command. When the power FET is switched off, the gate capacitance of the FET is discharged by a constant current, which is controlled fast and slow by a SPI command (HPD_sr).

6.2.2.3 External components of high-side driver

For protection, external resistors R_{HD_D}, R_{HD_G}, and R_{HD_S} are required (for example: R_{HD_D} = 100 Ω, R_{HD_G} = 100 Ω, R_{HD_S} = 100 Ω). The zener clamping is necessary to protect the gate and source. The zener chains are used for avalanche clamping and protection against transients.

Table 10. High-side driver electrical characteristics

V_{PWR} = 6.0 to 36 V, VCC5 = 4.75 to 5.25 V, DOSV = 3.13 to 5.25 V, T_J = -40 to +125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
HD_G						
V_{HD_ON}	HD_G switch-on voltage - with pd_on: PWMat 500 Hz, 50% duty cycle through the SPI • 5.5 V ≤ V_{PWR} < 6.0 V • 6.0 V ≤ V_{PWR} < 7.0V • 7.0 V ≤ V_{PWR} < 10 V • 10 V ≤ V_{PWR} < 36 V	V_{PWR}+ 4 V_{PWR}+5 V_{PWR}+7 V_{PWR}+10	— — — —	V_{PWR}+ 15 V_{PWR}+15 V_{PWR}+15 V_{PWR}+15	V	
V_{HD_OFF}	HD_G switch-off voltage	—	—	1	V	
t_{HD_ON}	Turn-on time - After t_{HD_LC}	—	—	1.4	ms	
$I_{HD\_OFF\_SLOW}$	Turn-off current slow - V_{HD_G} > 2.0 V. HPD_sr = 0	70	100	200	µA	
$I_{HD\_OFF\_FAST}$	Turn-off current fast - V_{HD_G} > 2.0 V, HPD_sr = 1	1.0	2.0	4.5	mA	
HD_S						
$I_{LEAK\_HD\_SRC}$	Leakage current - 0 ≤ V_{HD_S} ≤ 36 V, 6.0 ≤ VPWR ≤ 36 V	—	—	50	µA	
HD_D						
$L_{LEAK\_HD\_DRN}$	Leakage current - VCC5 = DOSV = 0 V, HD_D = PD_D = V_{PWR} = 36 V	—	—	10	µA	
Overcurrent detection						
V_{HD_OC}	Overcurrent detection threshold - V_{HD_D}-V_{HD_S}, R_{DRN}, R_{SRC} = 100 Ω	-15%	1.0	+15%	V	
Load leakage current detection						
$I_{HD\ LC}$	HD_S source current	—	1.5	—	mA	

6.3 Pump motor pre-driver

6.3.1 Function description

This module is designed for pump motor predrivers, a maximum of 500 Hz PWM is possible. The pump motor pre-driver can be driven by a SPI command (pd_on) or through the ADIN1 pin by selecting Adin1_dis bit at “1”.

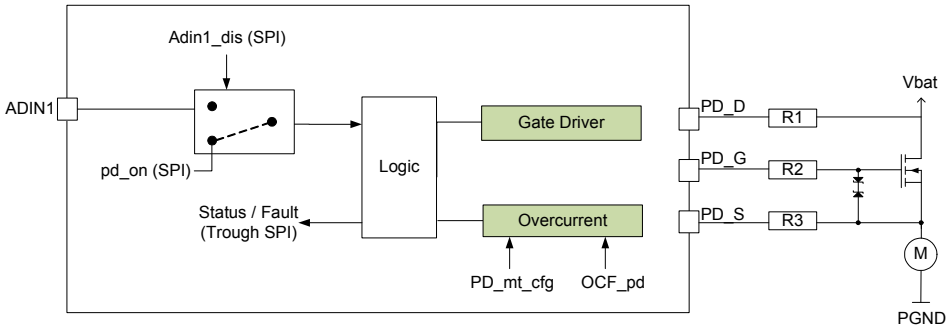

Figure 6. Pump motor predriver

6.3.2 Fault Detection

6.3.2.1 Overcurrent

The pump pre-driver protects the external n-channel power FET on PD_G in overcurrent conditions. The drain-source voltage of the FET on PD_G is checked if the high-side predriver is switched on. If the measured drain-source voltage exceeds the overcurrent voltage threshold, the output of the overcurrent comparator is enabled. If the output of the comparator is active longer than the defined filter time, the output PD_G is switched off. Overcurrent detection logic has a masking time from pd_on turn-on against malfunctions in transient time. The masking time and filter time of the pump predriver is controllable by the SPI bit (See SPI and data register). After switching off the power FET on PD_G by an overcurrent condition, the power FET can be turned back to a “normal state” by a SPI write 1 to the “PD_clr_flt” register, and then turned on by a SPI command.

When the power FET is switched off, the gate capacitance of the FET is discharged by a constant current, which is controlled fast and slow by a SPI command (HPD_sr).

6.3.2.2 External components of pump predriver

Protection of the resistors R_{PD_D}, R_{PD_G}, and R_{PD_S} is required (for example: R_{PD_D} = 2.0 kΩ, R_{PD_G} = 100 Ω, R_{PD_S} = 2.0 kΩ). Zener clamping is necessary to protect the gate and source. The zener chains are used for avalanche clamping and protection against transients.

Table 11. Pump motor predriver electrical characteristics

V_{PWR} = 6.0 to 36 V, VCC5 = 4.75 to 5.25 V, DOSV = 3.13 to 5.25 V, T_J = -40 to +125 °C, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
PD_G						
V_{PD_ON}	PD_G switch-on voltage - with pd_on: PWM at 500 Hz, 50% duty cycle through the SPI, 16 nF between PD_G & GND. pd_on = 1 without PWM • 5.5 V ≤ VPWR < 6.0 V • 6.0 V ≤ VPWR < 7.0V • 7.0 V ≤ VPWR < 10 V • 10 V ≤ VPWR < 36 V	V_{PWR}+ 4 V_{PWR}+5 V_{PWR}+7 V_{PWR}+10	— — — —	V_{PWR}+ 15 V_{PWR}+15 V_{PWR}+15 V_{PWR}+15	V	
V_{PD_OFF}	PD_G switch-off voltage - pull-up current < 20 µA	—	—	1	V	
t_{PD_ON}	Turn-on time	—	0.5	—	ms	
$I_{PD\_OFF\_SLOW}$	Turn-off current slow - PD_G > 2.0 V. HPD_sr = 0	70	100	200	µA	
$I_{PD\_OFF\_FAST}$	Turn-off current fast - PD_G >2.0 V, HPD_sr = 1	1.0	2.0	4.5	nA	
PD_S						
$I_{LEAK\_PD\_SRC}$	Leakage current - 0 ≤ VPD_src ≤ 36 V, 6.0 ≤ VPWR ≤ 36 V	—	—	10	µA	
PD_D						
$I_{LEAK\_PD\_DRN}$	Leakage current - VCC5 = DOSV = 0 V, HD_D = PD_D = VPWR = 36 V	—	—	10	µA	
Overcurrent detection						
V_{PD_OC}	Overcurrent detection threshold - V_{PD_D} - V_{PD_SRC}, R_{DRN}, R_{SRC} = 2.0 kΩ	-15%	1.0	+15%	V	
t_{PD_OC1}	Overcurrent detection filter time - OCF_pd = 0	—	T2	—	µs	
t_{PD_OC2}	Overcurrent detection filter time - OCF_pd = 1	—	4*T1	—	µs	

6.4 Low-side driver

6.4.1 Functional description

The SB0800 is designed to drive inductive loads in low-side configuration. All four channels are monitored by logic and faults are individually reported by the SPI. All external wiring to the loads and supply pins of the device are controlled. The device is self-protected against short-circuit and overtemperature at the outputs.

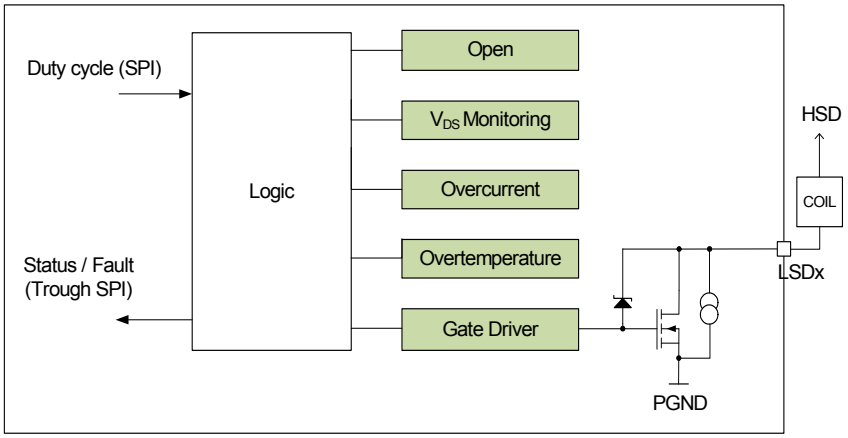

Figure 7. PWM low-side driver

Channel 1 to 4 can work either as current regulator or as PWM. When Channels 1 to 4 work as a current regulator, freewheeling diodes must be connected. Each channel comprises an output transistor, a predriver circuit, a diagnostic circuitry, and a current regulator. The SPI register defines the target output current. The output current is controlled through the output PWM of the power stage. The LSD1-4 current slopes are controlled by a SPI command to reduce switching loss.

The four power outputs consist of DMOS-power transistors with open drain outputs. The output transistor is equipped with an active clamp to limit the voltage at its output during turn-off with inductive loads. When the external fly-back diode is connected, the current re-circulation executes via the diode to the battery. When the diode is not connected, the PWM driver is equivalent to a digital driver. In those conditions, the inductive load forces the output voltage to increase until the voltage at the output is such that the output transistor turns on again. This lasts until the inductor current becomes zero. At that moment, the output transistor turns off. The predriver is in charge of applying the necessary voltage on the output transistor gate to minimize the On-resistance of the output switch.

The duty cycle of PWM low-side drivers is programmed via an 8-bit SPI message. The duty cycle between 0% and 100% can be selected and the LSB of the 8 bits is weighted with an 0.39% duty. Each channel has an 8-bit SPI register of PWM duty cycle.

The PWM low-side driver uses each channel as a digital low-side switch.

PWMx duty cycle = 1111 1111 - Digital low-side switch ON (conducting)

PWMx duty cycle = 0000 0000 - Digital low-side switch OFF

The SB0800 provides interleaved phase shift switching to minimize switching noise of the solenoid coil. Each LSD1 to 4 have this cycle.

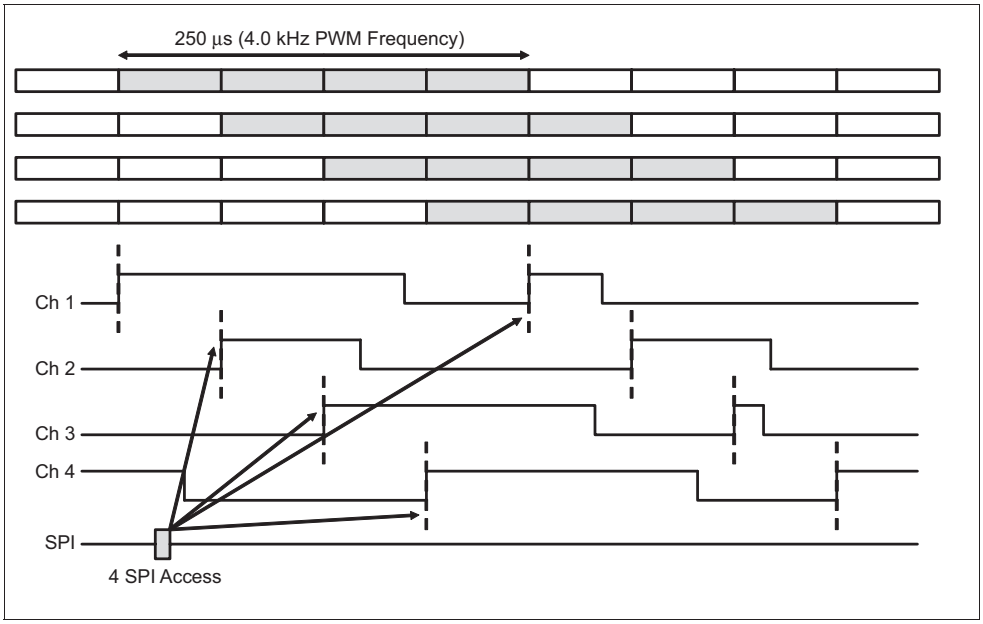

Figure 8. PWM valve control interleave

Table 12. Low-side driver electrical characteristics

V_{PWR} = 6.0 to 36 V, DOSV = 3.13 to 5.25 V, T_J = -40 to 125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power output						
R_{ON_LSD14}	On Resistance Channel 1 to 4: CR • T_J = 125 °C; 9.0 V ≤ V_{PWR} ≤ 36 V; I_{LOAD} = 2.0 A	—	—	0.255	Ω	
$R_{ON\_LSD14\_E}$	On Resistance Channel 1 to 4: CR (extended mode) • T_J = 125 °C; 5.5 V ≤ V_{PWR} ≤ 9.0 V; I_{LOAD} = 2.0 A	—	—	0.33	Ω	
I_{LEAK_LSD}	Drain Leakage Current • LSD = 36 V	—	—	10	µA	
V_{CL_LSD}	Active Clamp Voltage	—	38	45	V	
Timings						
t_{R_CR1} t_{F_CR1}	Rise Time/Fall Time • 10% to 90%, I_{LOAD} = 1.0 A, V_{PWR} =24 V; no capacitor didt = 0 (SPI bit)	1.0 0.1	1.7 1.35	3.0 3.0	µs	
t_{R_CR2} t_{F_CR2}	Rise Time/Fall Time • 10% to 90%, I_{LOAD} = 1.0 A, V_{PWR} = 24 V; no capacitor didt = 1 (SPI bit)	0.05 0.1	0.5 1.0	1.0 3.0	µs	
t_D on CR t_D off CR	Turn on/off Delay Time • Digital 1 to 10% or 90%, I_{LOAD} = 1.0 A, V_{PWR} = 24 V, no capacitor	0.0	—	3.0	µs	(10)

Table 12. Low-side driver electrical characteristics (continued)

V_{PWR} = 6.0 to 36 V, DOSV = 3.13 to 5.25 V, T_J = -40 to 125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Timings						
LF_PWM	Output PWM frequency for LSD1-4 • LF_PWM xx = 111 • LF_PWM xx = 110 • LF_PWM xx = 101 • LF_PWM xx = 100 • LF_PWM xx = 000 (default) • LF_PWM xx = 011 • LF_PWM xx = 001 • LF_PWM xx = 010	-20%	 3.0 3.2 3.4 3.6 3.9 4.2 4.5 5.0	20%	kHz	
0000 0000 0000 0001 … 1111 1110 1111 1111	PWM Duty Cycle Programming (8-bits) • Can be used for digital low-side driver	— — — — —	OFF 0.39 — 99.61 ON	— — — — —	%	

Notes

10. Digital: internal digital signal delivered by interleave synchronization block. See Figure 8.

6.4.2 LSD1 to LSD4 current regulation driver

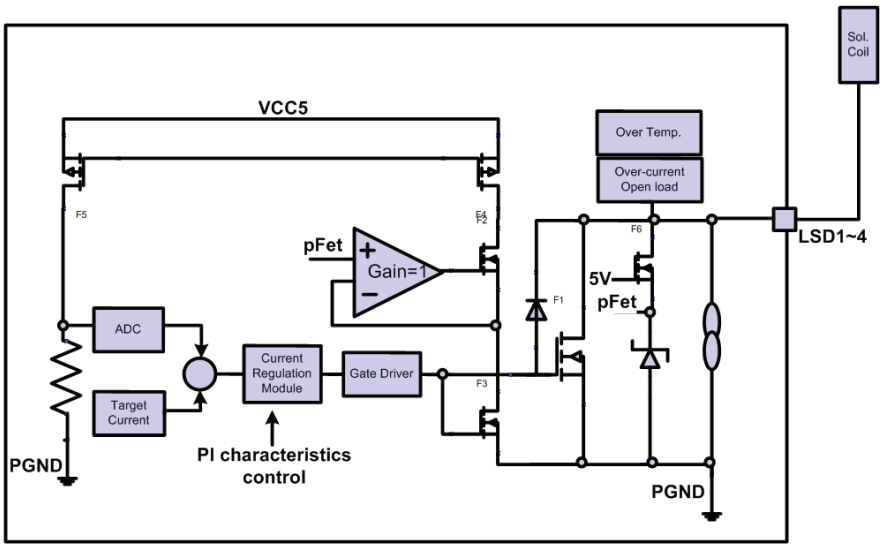

Figure 9. PWM low-side driver (current regulated)

The load current is sensed by an internal low-side sense FET and digitized by an internal A/D converter. The target value of the current is given SPI messages. A digital current regulation circuitry compares the actual load current with the target current value and steers the duty cycle of the low-side power switch. The PI regulator characteristic can be adjusted via the SPI.

6.4.2.1 Target current

Each current regulator channel has its own 10-bit target current register. The LSB of the 10 bits is weighted with 2.2 mA. A zero value disables the power stage of the respective channel. A new target current is instantaneously passed to the settling time, which is the settling of the new current value.

PWMx target current value = 00 0000 0000 → 0 mA

PWMx target current value = 00 0000 0001 → 2.2 mA

...

PWMx target current value = 11 1111 1110 → 2.248 A

PWMx target current value = 11 1111 1111 → 2.250 A

CR_DIS12/34	CR_fb	Mode	LSD1-4 duty cycle (8-bit) or current read (10-bit)
0	0	current regulation	Read current target (to check SPI write)
0	1	current regulation	Read output duty cycle value for gate driver.
1	0	PWM	Read programmed PWM duty cycle (to check SPI write)
1	1	PWM	Read hardware ADC current value

6.4.2.2 Current measurement

The output current is measured during the “ON’ phase of the low-side driver. A fraction of the output current is diverted and (using a “current mirror” circuit) generates across an internal resistance a voltage relative to ground, this being proportional to the output current.

6.4.3 PI characteristics

Digital PI-regulator with the Transfer function is programmed via the SPI register.

Transfer function: $\frac{KI}{z-1} + KP$

The integrator feedback register I charac bits define the regulation behavior of all channels. The default value is 1/8. Both current regulators remain idle until a non-zero value in I charac was programmed. A high proportional feedback value accelerates the regulator feedback and provides a faster settling of the regulated current after disturbances like battery voltage surge.

Table 13. Duty cycle descriptions

The duty cycle of PWM output is clamped minimum by options and maximum 100% (see 6.10, “SPI and data register").

Option	LLC<1>	LLC<0>	Minimum duty cycle
0	0	0	10% • the measurement is done at $t_{ON}/2$ by consequence • the regulation current will be set at $t_{ON}/2$
1	0	1	3.12% • for a duty cycle > 10%, the measurement is done at $t_{ON}/2$ • for a duty cycle 3.2% < DC < 10%, the measurement is done at $t_{ON}/2$ for 10% of duty cycle up at t_{ON} for 3.2% of duty cycle

Table 13. Duty cycle descriptions

The duty cycle of PWM output is clamped minimum by options and maximum 100% (see 6.10, “SPI and data register").

Option	LLC<1>	LLC<0>	Minimum duty cycle
2	1	0	3.12% + forced min duty cycle to 1.56% every two cycles • for a duty cycle > 10%, the measurement is done at $t_{ON}/2$ • for a duty cycle 3.2% < DC < 10%, the measurement is done at $t_{ON}/2$ for 10% of duty cycle up at t_{ON} for 3.2% of duty cycle • for a duty cycle set at 1.56%, no measurement is done
3	1	1	3.12% + skip min duty cycle every two cycles • for a duty cycle > 10%, the measurement is done at $t_{ON}/2$ by consequence the regulation current will be set at $t_{ON}/2$ • for a duty cycle 3.2% < DC < 10%, the measurement is done at $t_{ON}/2$ for 10% of duty cycle up at t_{ON} for 3.2% of duty cycle • no measurement is done during the skipping mode

If the target current value is not reached within the regulation error delay time of t_{CR_ERR}, the flag of the SPI register “LSDx_crer” is set to high. The current regulation loop is still running and tries to regulate at the target. Because it is not at the target, the duty cycle is either 100%, or minimum duty cycle by option. LSDx_crer error detection has no effect on the driver, only SPI fault reporting. The microcontroller can detect the fault through the SPI (LSDx_crer bit + ADC current reading), and shutdown the driver by sending 0 target current. Set Current – ADC result > “error threshold” during t_{CR_ERR} then LSDx_crer is set to 1.

This flag is latched & can be reset by the SPI read (LSDx_crer). Each of the four current regulation low-side drivers can be used as a PWM low-side switch. CR_disxx flag is enabled HIGH. The 8 MSB bits of the target current message are the PWM duty cycle. The first duty is controlled by the SPI bit FDCL (See SPI and data register).

Table 14. LSD1 to LSD4 current regulation driver electrical characteristics

V_{PWR} = 6.0 to 36 V, VCC5 = 4.75 to 5.25 V, DOSV = 3.13 to 5.25 V, T_J = -40 to +125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Current regulation						
0000 0000 0000 0001 ... 1111 1111	Target current programming (10-bits)	— — — —	OFF 2.2 ... 2.25	— — — —	mA A	
I_{CR_DEV}	Maximum regulation deviation • 0 mA ≤ I_{TARGET} < 50 mA, includes ADC error • 50 mA ≤ I_{TARGET} < 100 mA, includes ADC error • 100 mA ≤ I_{TARGET} < 250 mA, includes ADC error • 250 mA ≤ I_{TARGET} < 400 mA, includes ADC error • 400 mA ≤ I_{TARGET} < 2.25 A, includes ADC error	— — — — —	— — — — —	65 50 25 ±10 ±2.0	mA %	(11)

Notes

11. Maximum regulation deviation performances noted in the table depend on external conditions (V_{PWR}, load (R,L)).

6.5 Low-side driver for resistive load

6.5.1 Power output stages

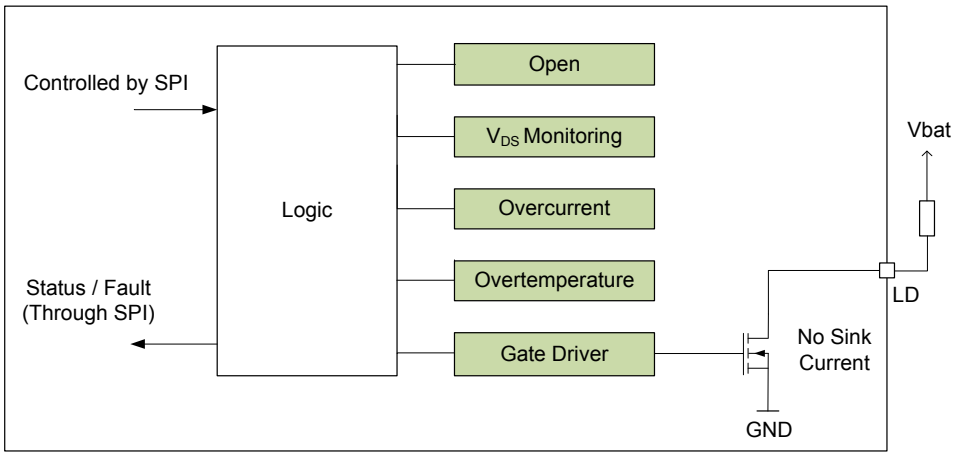

Figure 10. Low-side driver for resistive load diagram block

The low-side driver consists of DMOS-power transistors with open drain output. The low-side driver can be driven by SPI commands or by a MCU through the ADIN2. The low-side driver is composed of an output transistor, a predriver circuit, and diagnostic circuitry. The predriver applies the necessary voltage on the output transistor gate to minimize the On resistance of the output switch. To avoid leakage current path, LD has no sink current.

Table 15. Low-side driver electrical characteristics

V_{PWR} = 6.0 to 36 V, VCC5 = 4.75 to 5.25 V, DOSV = 3.13 to 5.25 V, T_J = -40 to 125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power output LD						
R_{ON_LD}	On Resistance for LD • T_J = 125 °C, 6.0 V ≤ V_{PWR} ≤ 36 V	—	—	14	Ω	
	DC Current Capability	—	—	20	mA	
I_{LEAK_LD}	Drain Leakage Current • V_{PWR} = 0, V_{CC5} = 0, LD = 30 V, no sink current	—	—	5.0	µA	
Timings						
$t_{D\_ON\_LD}$	Turn On Delay Time for LD	—	—	1.0	µs	(12)
$t_{D\_OFF\_LD}$	Turn Off Delay Time for LD	—	—	1.0	µs	(12)

Notes

12. From Digital Signal to 50% (turn ON) or 50% (turn OFF). R_L = 1.0 kΩ, V_{PWR} = 30V, no capacitor

6.5.2 Fault detection

Open load

An open condition is detected when the LD output is below the threshold OP_{LD} for the defined filter time t_{OP_LD}, the fault bit is set ld_OP (SPI error flag only). This function only operates during the off state.

V_{DS} state monitoring

The V_{DS} state monitoring gives real time state of LD drain voltage vs OP_{LD} voltage. This signal is filtered and sent through the SPI vds_ld bit. If the V_{DS} voltage is higher than OP_{LD} with a filter time (T1), vds_ld is set to “1”.

Overcurrent

When the current is above the overcurrent threshold OC_{LD} for the defined filter time t_{OC_LD}, the driver is switched off, a SPI fault bit ld_OC is set, and the turn-on SPI command is cleared. The driver can be returned to the “normal state” by a SPI write “1” to “LD_clr_flt”, then turned on by a SPI command (LD_on).

Overtemperature

When the temperature is above the overtemperature threshold OT_{LD} for the defined filter time t_{OT_LD}, the driver is switched off, a SPI fault bit ld_OT is set, and the turn-on SPI command is cleared. The driver can be returned to the “normal state” when the temperature returns to the normal state, a SPI write “1” to “LD_clr_flt”, then turning on a SPI command (LD_on).

Table 16. Low-side driver electrical characteristics

V_{PWR} = 6.0 to 36 V, VCC5 = 4.75 to 5.25 V, DOSV = 3.13 to 5.25 V, T_J = -40 to 125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Overcurrent shutdown						
OC_{LD}	Overcurrent Shutdown Threshold Current for LD	—	100	—	mA	
t_{OC_LD}	Overcurrent Shutdown Filter Time	—	T1	—	µs	
Open load detection						
OP_{LD}	Open Load Detection Threshold (also used for V_{DS} monitoring)	—	2.0	—	V	
t_{OP_LD}	Open Load Detection Filter Time	—	T2	—	µs	
V_{DS} monitoring						
t_{VDS_LD}	V_{DS} State Filter Time (rise & fall edge filter time)	—	T1	—	µs	
Overtemperature shutdown						
OT_{LD}	Overtemperature Detection Threshold	180	195	210	°C	
t_{OT_LD}	Overtemperature Detection Filter Time	—	T1	—	µs	