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Document Number: MC34VR500
Rev. 4.0, 7/2015

Multi-output DC/DC Regulator for QorIQ LS1/T1 Family of Communications Processors

34VR500

Power Management

ES SUFFIX (WF-TYPE)
98ASA00589D
56 QFN-EP WF8X8

The 34VR500 is a high performance, highly integrated, multi-output, SMARTMOS, DC/DC regulator solution, with integrated power MOSFETs ideally suited for the LS1/T1 family of communication processors. Integrating four switching and five linear regulators, the 34VR500 provides power to the complete system, including the processor, DDR memory, and system peripherals.

Features:

- Four buck converters:
  - SW1: 4.5 A
  - SW2: 2.0 A
  - SW3: 2.5 A
  - SW4: 1.0 A, (VTT tracking regulator)
- Five general purpose linear regulators
- DDR termination reference voltage (DDR3L and DDR4)
- Programmable low-power modes
- I^2C control of all the regulators
- Power Control Logic with processor interface and event detection
- Auto qualified AEC Q100 grade 2

Applications:

- Internet of Things (IoT) gateway
- Mobile wireless router
- MFP printer
- Network attached storage
- Automatic teller machine

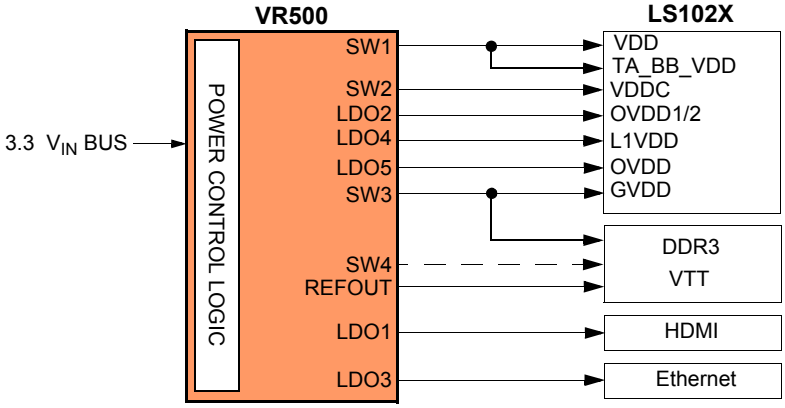

Figure 1. 34VR500 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table of Contents

1 Orderable Parts

This section describes the part numbers available to be purchased along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.freescale.com and perform a part number search for the following device numbers.

Table 1. Orderable Part Variations

Part Number	Temperature (T_A)	Package	SW4 VTT Mode	Processor	Reference Design	DDR Memory	Notes
MC34VR500V1ES	-40 °C to 105 °C	56 QFN 8x8 mm	Enabled	LS1020/21/22A	LS1021A IOT Gateway TWR-LS1021A	DDR3L (VTT = 0.675 V)	(1) (2)
MC34VR500V2ES			Disabled			N/A	
MC34VR500V3ES			Enabled			DDR4 (VTT = 0.6 V)	
MC34VR500V4ES			Enabled	LS1043/23A T1023/13	LS1043ARDB T1023RDB		
MC34VR500V5ES			Enabled			DDR3L (VTT = 0.675 V)	

Notes
1. For Tape and Reel add an R2 suffix to the part number.
2. Refer Table 8 for the start-up configuration.

2 Internal Block Diagram

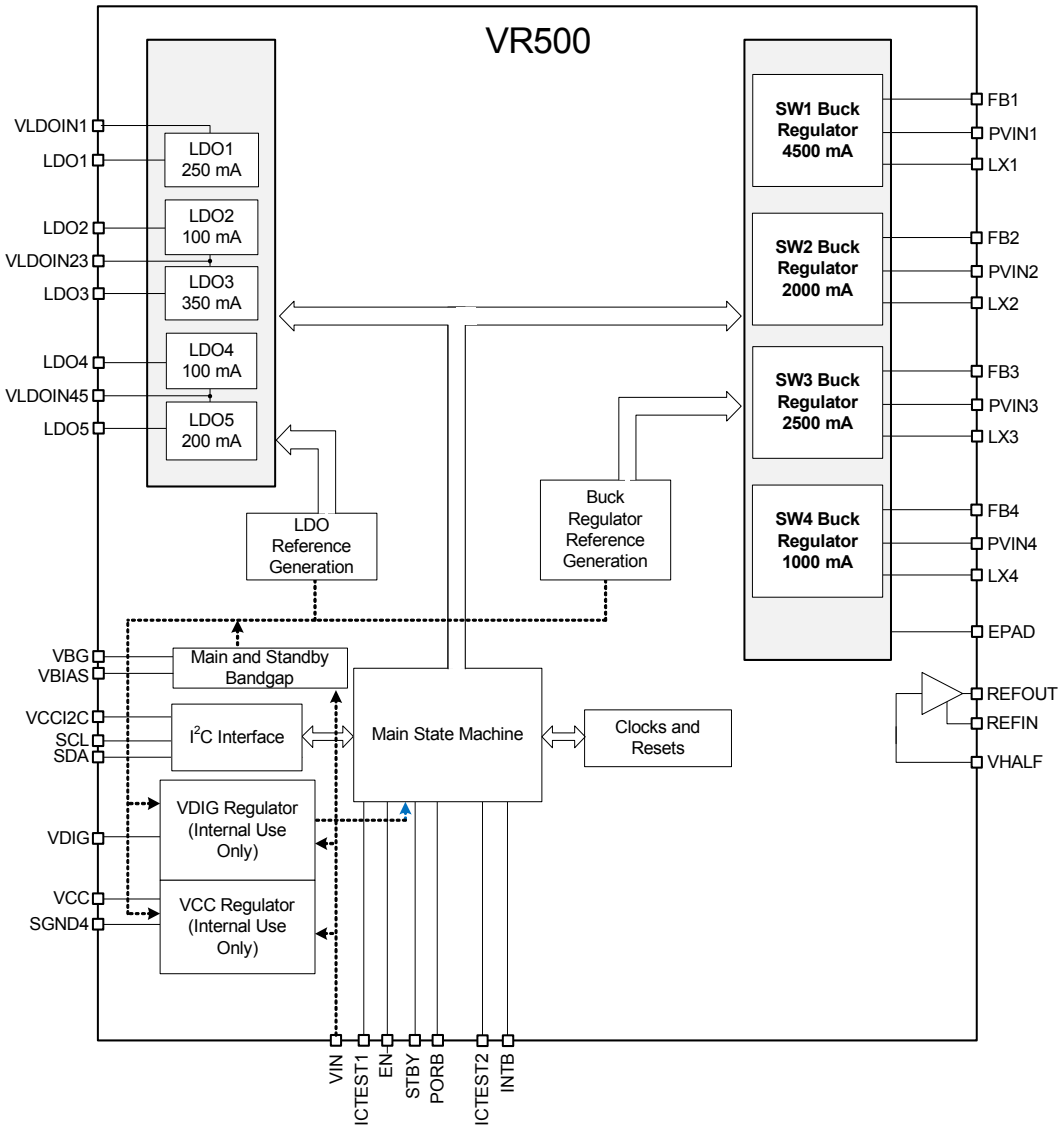

Figure 2. 34VR500 Simplified Internal Block Diagram

3 Pin Connections

3.1 Pinout Diagram

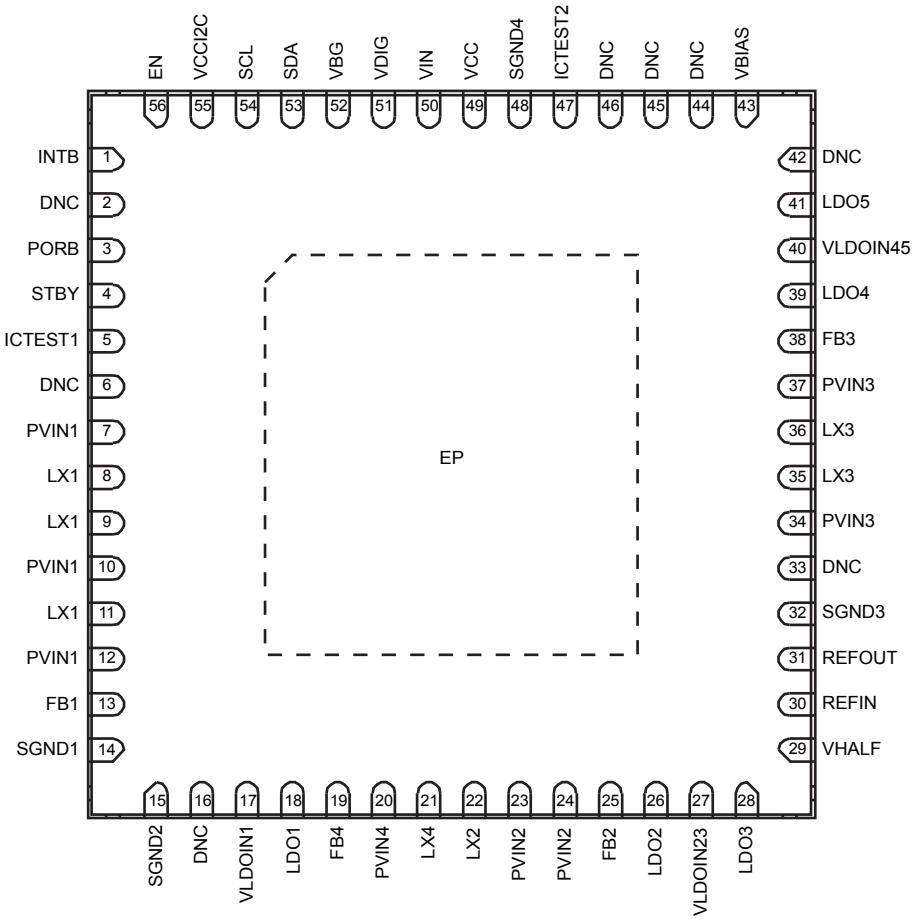

Figure 3. 34VR500 Pinout Diagram

3.2 Pin Definitions

Table 2. 34VR500 Pin Definitions

Pin Number	Pin Name	Pin Function	Max. Rating	Type	Definition
1	INTB	O	3.6 V	Digital	Open drain interrupt signal to processor
2, 6, 16, 33, 42, 44, 45, 46	DNC	—	—	Reserved	Leave floating
3	PORB	O	3.6 V	Digital	Open drain reset output to processor.
4	STBY	I	3.6 V	Digital	Standby input signal from processor
5	ICTEST1	I	7.5 V	Digital/ Analog	Reserved pin. Connect to GND in application.

Table 2. 34VR500 Pin Definitions (continued)

Pin Number	Pin Name	Pin Function	Max. Rating	Type	Definition
7, 10, 12	PVIN1 (3)	I	4.8 V	Analog	Input to SW1 regulator. Bypass with at least a 4.7 μF ceramic capacitor and a 0.1 μF decoupling capacitor as close to the pin as possible.
8, 9, 11	LX1 (3)	O	4.8 V	Analog	SW1 switching node connection
13	FB1 (3)	I	3.6 V	Analog	Output voltage feedback for SW1. Route this trace separately from the high current path and terminate at the output capacitance.
14	SGND1	GND	-	GND	Signal ground for SW1 regulator. Connect to ground plane directly.
15	SGND2	GND	-	GND	Signal ground for SW2 and SW4 regulators. Connect to ground plane directly.
17	VLDOIN1	I	3.6 V	Analog	Input supply for LDO1. Bypass with a 1.0 μF decoupling capacitor as close to the pin as possible.
18	LDO1	O	2.5 V	Analog	LDO1 regulator output, Bypass with a 4.7 μF ceramic output capacitor.
19	FB4 (3)	I	3.6 V	Analog	Output voltage feedback for SW4. Route this trace separately from the high current path and terminate at the output capacitance.
20	PVIN4 (3)	I	4.8 V	Analog	Input to SW4 regulator. Bypass with at least a 4.7μF ceramic capacitor and a 0.1 μF decoupling capacitor as close to the pin as possible.
21	LX4 (3)	O	4.8 V	Analog	Regulator 4 switching node connection
22	LX2 (3)	O	4.8 V	Analog	Regulator 2 switching node connection
23, 24	PVIN2 (3)	I	4.8 V	Analog	Input to SW2 regulator. Connect pins 23 and 24 together and bypass with at least a 4.7 μF ceramic capacitor and a 0.1 μF decoupling capacitor as close to these pins as possible.
25	FB2 (3)	I	3.6 V	Analog	Output voltage feedback for SW2. Route this trace separately from the high current path and terminate at the output capacitance.
26	LDO2	O	3.6 V	Analog	LDO2 regulator output. Bypass with a 2.2 μF ceramic output capacitor.
27	VLDOIN23	I	3.6 V	Analog	Input supply for LDO2 and LDO3. Bypass with a 1.0 μF decoupling capacitor as close to the pin as possible.
28	LDO3	O	3.6 V	Analog	LDO3 regulator output, Bypass with a 4.7 μF ceramic output capacitor.
29	VHALF	I	3.6 V	Analog	Half supply reference for DDR reference.
30	REFIN	I	3.6 V	Analog	REFOUT regulator input. Bypass with at least 1.0 μF decoupling capacitor as close to the pin as possible.
31	REFOUT	O	3.6 V	Analog	REFOUT regulator output
32	SGND3	GND	-	GND	Ground reference for the SW3 regulator. Connect directly to ground plane.
34, 37	PVIN3 (3)	I	4.8 V	Analog	Input to SW3 regulator. Bypass with at least a 4.7 μF ceramic capacitor and a 0.1 μF decoupling capacitor as close to the pin as possible.
35, 36	LX3 (3)	O	4.8 V	Analog	Regulator SW3 switching node connection
38	FB3 (3)	I	3.6 V	Analog	Output voltage feedback for SW3. Route this trace separately from the high current path and terminate at the output capacitance.
39	LDO4	O	3.6 V	Analog	LDO4 regulator output. Bypass with a 2.2 μF ceramic output capacitor.
40	VLDOIN45	I	4.8 V	Analog	Input supply for LDO4 and LDO5. Bypass with a 1.0 μF decoupling capacitor as close to the pin as possible.
43	VBIAS	I	1.8 V	Analog	Bypass the pin with a 0.47 μF capacitor.
41	LDO5	O	3.6 V	Analog	LDO5 regulator output. By pass with a 2.2 μF ceramic output capacitor.
47	ICTEST2	I	7.5 V	Digital/ Analog	Reserved pin. Connect to GND in application.
48	SGND4	GND	-	GND	Ground for the main band gap regulator. Connect directly to ground plane.
49	VCC	O	3.6 V	Analog	Analog Core supply

Table 2. 34VR500 Pin Definitions (continued)

Pin Number	Pin Name	Pin Function	Max. Rating	Type	Definition
50	VIN	I	4.8 V	Analog	Main chip supply
51	VDIG	O	1.5 V	Analog	Digital Core supply
52	VBG	O	1.5 V	Analog	Main band gap reference. Bypass with 0.22uF capacitor.
53	SDA	I/O	3.6 V	Digital	I^2C data line (Open drain)
54	SCL	I	3.6 V	Digital	I^2C clock
55	VCCI2C	I	3.6 V	Analog	Supply for I^2C bus. Bypass with 0.1 μF ceramic capacitor
56	EN	I	3.6 V	Digital	Enable input. Connect to the processor. Pull-up via an 8.0 kΩ to 100 kΩ to VBIAS if required
-	EP	GND	-	GND	Expose pad. Functions as ground return for buck regulators. Tie this pad to the inner and external ground planes through vias to allow effective thermal dissipation.

Notes

3. Unused switching regulators should be connected as follow: Pins SWxLX and SWxFB should be unconnected and Pin SWxIN should be connected to the VIN pin with a 0.1 μF bypass capacitor.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause malfunction or permanent damage to the device. The detailed maximum voltage rating per pin can be found in the pin list section.

Symbol	Description	Value	Unit	Notes
ELECTRICAL RATINGS				
V_{IN}	Main input supply voltage	-0.3 to 4.8	V	
V_{ESD}	ESD Ratings Human Body Model Charge Device Model	 ±2000 ±500	V	(4)

Notes

4. ESD testing is performed in accordance with the Human Body Model (HBM) (CZAP = 100 pF, RZAP = 1500 Ω), and the Charge Device Model (CDM), Robotic (CZAP = 4.0 pF).

4.2 Thermal Characteristics

Table 4. Thermal Ratings

Symbol	Description (Rating)	Min.	Max.	Unit	Notes
THERMAL RATINGS					
T_A	Ambient Operating Temperature Range	-40	105	°C	
T_J	Operating Junction Temperature Range	-40	125	°C	(5)
T_{ST}	Storage Temperature Range	-65	150	°C	
T_{PPRT}	Peak Package Reflow Temperature	–	Note 7	°C	(6) (7)
QFN56 THERMAL RESISTANCE AND PACKAGE DISSIPATION RATINGS					
$R_{\theta JA}$	Junction to Ambient Natural Convection Four layer board (2s2p) Eight layer board (2s6p)	 – –	 28 15	°C/W	(8) (9) (10)
$R_{\theta JMA}$	Junction to Ambient (at 200 ft/min) Four layer board (2s2p)	 –	 22	°C/W	(8) (10)
$R_{\theta JB}$	Junction to Board	–	10	°C/W	(11)
$R_{\Theta JCBOTTOM}$	Junction to Case Bottom	–	1.2	°C/W	(12)
ΨJT	Junction to Package Top Natural Convection	–	2.0	°C/W	(12)

Notes

5. Do not operate beyond 125 °C for extended periods of time. Operation above 150 °C may cause permanent damage to the IC. See Table 5 for thermal protection features.
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
7. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx), and review parametrics.
8. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
9. The Board uses the JEDEC specifications for thermal testing (and simulation) JESD51-7 and JESD51-5.
10. Per JEDEC JESD51-6 with the board horizontal.
11. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
12. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
13. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.2.1 Power Dissipation

During operation, the temperature of the die should not exceed the operating junction temperature noted in Table 4. To optimize the thermal management and to avoid overheating, the 34VR500 provides thermal protection. An internal comparator monitors the die temperature. Interrupts THERM110I, THERM120I, THERM125I, and THERM130I will be generated when the respective thresholds specified in Table 5 are crossed in either direction. The temperature range can be determined by reading the THERMxxxS bits in register INTSENSE0.

In the event of excessive power dissipation, thermal protection circuitry will shut down the 34VR500. This thermal protection will act above the thermal protection threshold listed in Table 5. To avoid any unwanted power downs resulting from internal noise, the protection is debounced for 8.0 ms. This protection should be considered as a fail-safe mechanism and therefore the system should be configured such that this protection is not tripped under normal conditions.

Table 5. Thermal Protection Thresholds

Parameter	Min.	Typ.	Max.	Units	Notes
Thermal 110 °C Threshold (THERM110)	100	110	120	°C	
Thermal 120 °C Threshold (THERM120)	110	120	130	°C	
Thermal 125 °C Threshold (THERM125)	115	125	135	°C	
Thermal 130 °C Threshold (THERM130)	120	130	140	°C	
Thermal Warning Hysteresis	2.0	–	4.0	°C	
Thermal Protection Threshold	130	140	150	°C	

4.3 Electrical Characteristics

4.3.1 I/O Specifications

Table 6. General PMIC Static Characteristics.

T_A = -40 to 105 °C, V_{VIN} = 2.8 to 4.5 V, V_{VCCI2C} = 1.7 to 3.6 V, V_{VBIAS} = 1.0 V ±4.0%, typical external component values and full load current range, unless otherwise noted.

Pin Name	Parameter	Load Condition	Min.	Max.	Unit	Notes
EN	V_{IL}	–	0.0	0.2 *V_{VBIAS}	V	
	V_{IH}	–	0.8 *V_{VBIAS}	3.6	V	
PORB	V_{OL}	-2.0 mA	0.0	0.4	V	
	V_{OH}	Open Drain	0.7* V_{VIN}	V_{VIN}	V	
SCL	V_{IL}	–	0.0	0.2 * V_{VCCI2C}	V	
	V_{IH}	–	0.8 * V_{VCCI2C}	3.6	V	
SDA	V_{IL}	–	0.0	0.2 * V_{VCCI2C}	V	
	V_{IH}	–	0.8 * V_{VCCI2C}	3.6	V	
	V_{OL}	-2.0 mA	0.0	0.4	V	
	V_{OH}	Open Drain	0.7 * V_{VCCI2C}	V_{VCCI2C}	V	
INTB	V_{OL}	-2.0 mA	0.0	0.4	V	
	V_{OH}	Open Drain	0.7* V_{VIN}	V_{VIN}	V	
STBY	V_{IL}	–	0.0	0.2 *V_{VBIAS}	V	
	V_{IH}	–	0.8 *V_{VBIAS}	3.6	V	

4.3.2 Current Consumption

Table 7. Current Consumption Summary

T_A = -40 to 105 °C, (See Table 3), V_{VIN} = 3.6 V, V_{VCCI2C} = 1.7 to 3.6 V, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, unless otherwise noted. Typical values are characterized at V_{VIN} = 3.6 V, V_{VCCI2C} = 3.3 V, and 25 °C, unless otherwise noted.

Mode	34VR500 Conditions	System Conditions	Typical	Max.	Unit	Notes
Off	Wake-up from EN active 32 k RC on All other blocks off VIN ≥ UVDET	PMIC able to wake-up	17	25	µA	(14) (15)
Sleep	Wake-up from EN active Trimmed reference active SW3 PFM Trimmed 16 MHz RC off 32 k RC on REFOUT disabled	DDR memories in self refresh	122	250	µA	(15)
Standby	SW1 in PFM SW2 in PFM SW3 in PFM SW4 in PFM Trimmed 16 MHz RC enabled Trimmed reference active LDO1 - 5 enabled REFOUT enabled	Processor enabled in low power mode. All rails powered on except boost (load = 0 mA)	297	550	µA	(15)

Notes

14. When VIN is below the UVDET threshold, in the range of 1.8 V ≤ VIN < 2.65 V, the quiescent current increases by 50 µA, typically.
15. For PFM operation (as defined in Table 23).

5 General Description

The 34VR500 is a high performance, highly integrated, multi-output, DC/DC regulator solution, with integrated power MOSFETs ideally suited for the LS1/T1 family of communication processors.

5.1 Features

This section summarizes the 34VR500 features.

- Input voltage range: 2.8 V to 4.5 V
- Buck regulators
- Four independent outputs
  - SW1, 4.5 A; 0.625 V to 1.875 V
  - SW2, 2.0 A; 0.625 V to 1.975 V
  - SW3, 2.5 A; 0.625 V to 1.975 V
  - SW4, 1.0 A; operates in VTT mode for DDR termination at 50% of SW3 for 34VR500V1, 34VR500V3, 34VR500V4, 34VR500V5 and 0.625 V to 1.975 V for 34VR500V2
- Dynamic voltage scaling
- Modes: PWM, PFM, APS
- Programmable output voltage
- Programmable current limit
- Programmable soft start
- Programmable PWM switching frequency
- Programmable OCP with fault interrupt
  - LDOs
- Five general purpose LDOs
  - LDO1, 0.80 V to 1.55 V, 250 mA
  - LDO2, 1.8 V to 3.3 V, 100 mA
  - LDO3, 1.8 V to 3.3 V, 350 mA
  - LDO4, 1.8 V to 3.3 V, 100 mA
  - LDO5, 1.8 V to 3.3 V, 200 mA
- Soft start
  - DDR memory reference voltage
- REFOUT, 10 mA
  - 16 MHz internal master clock
  - I^2C interface
  - User programmable Standby, Sleep, and OFF modes

5.2 Functional Block Diagram

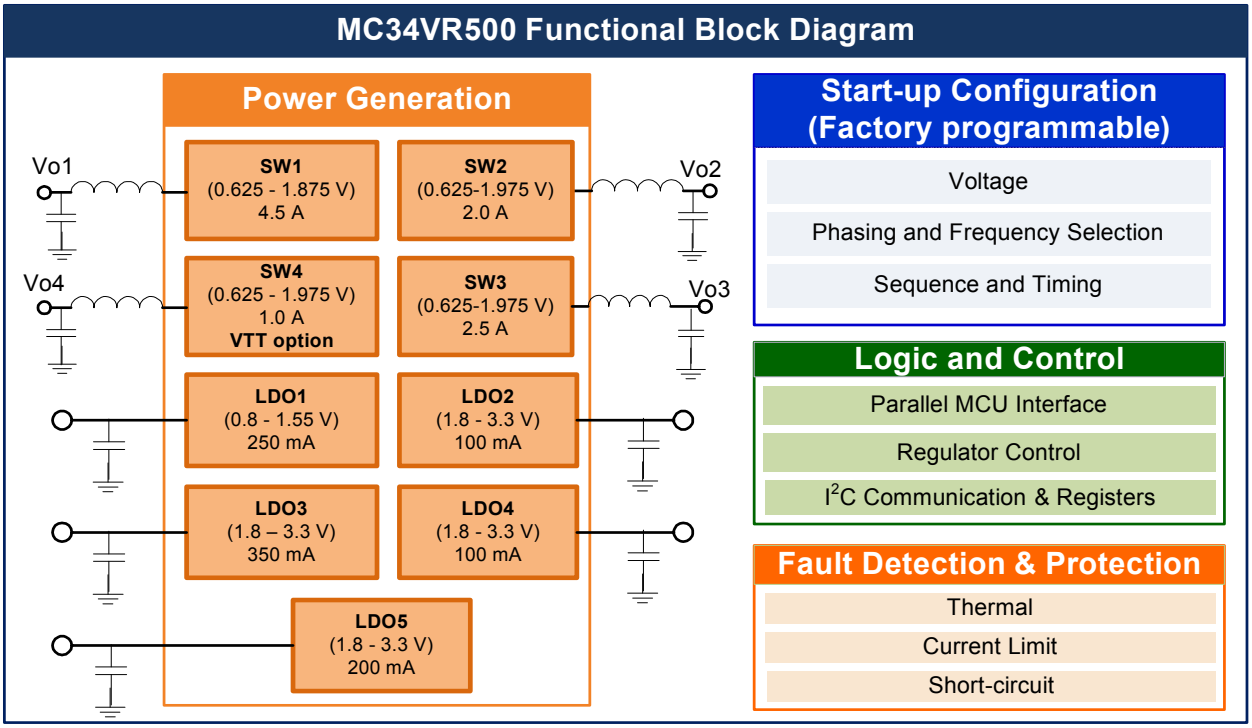

Figure 4. 34VR500 Functional Block Diagram

5.3 Functional Description

5.3.1 Power Generation

The 34VR500 PMIC features four buck regulators, five general purpose LDOs, and a DDR voltage reference to supply voltages for the processor, memory, and peripheral devices.

Depending on the system power path configuration, the five general purpose LDO regulators can be directly supplied from the main input supply or from the switching regulators to power peripherals, such as audio, camera, Bluetooth, Wireless LAN, etc. A specific REFOUT voltage reference is included to provide accurate reference voltage for DDR memories operating with or without VTT termination

5.3.2 Control Logic

The 34VR500 PMIC is fully programmable via the I^2C interface. Additional communication is provided by direct logic interfacing including interrupt and reset. Startup voltage and sequence are internally programed. After power up, the regulator voltages can be changed via I^2C. The 34VR500 PMIC has the interfaces for the power buttons and dedicated signaling interfacing with the processor.

5.3.2.1 Interface Signals

EN

EN is an input signal to the IC that generates a turn-on event. Refer to section Turn ON Events for more details.

STBY

STBY is an input signal to the IC. When it is asserted the part enters standby mode and when de-asserted, the part exits standby mode. STBY can be configured as active high or active low using the STBYINV bit. Refer to the section Standby Mode for more details.

PORB

PORB is an open-drain, active low output. In its default mode, it is de-asserted 2.0 to 4.0 ms after the last regulator in the start-up sequence is enabled; refer to Figure 8 as an example. In this mode, the signal can be used to bring the processor out of reset, or as an indicator that all supplies have been enabled; it is only asserted for a turn-off event.

INTB

INTB is an open-drain, active low output. It is asserted when any fault occurs, provided that the fault interrupt is unmasked. INTB is de-asserted after the fault interrupt is cleared by software, which requires writing a “1” to the fault interrupt bit.

6 Functional Block Requirements and Behaviors

6.1 Start-up

The 34VR500 starts up from the internal configuration, which is hard-coded into the device. However, the 34VR500 can be controlled through the I^{2}C port after the Start-up sequence. It is also possible to modify the contents of the Internal Registers via the bus I^{2}C to modify the start up parameters (see section Start Sequence Creation).

6.1.1 Device Start-up Configuration

Table 8 shows the internal configuration for the 34VR500V1, 34VR500V2, 34VR500V3, 34VR500V4, 34VR500V5.

Table 8. Start-up Configuration

Registers	34VR500V1	34VR500V2	34VR500V3	34VR500V4	34VR500V5
Default I2C Address	0x08				
LDO2_VOLT	1.8 V	1.8 V	1.8 V	2.5 V	2.5 V
LDO2_SEQ	1	1	1	2	2
LDO3_VOLT	2.5 V				
LDO3_SEQ	1	1	3	2	2
LDO4_VOLT	2.5 V	2.5 V	2.5 V	1.8 V	1.8 V
LDO4_SEQ	1	1	1	3	3
LDO5_VOLT	1.8 V	1.8 V	1.8 V	3.3 V	3.3 V
LDO5_SEQ	1	1	1	3	3
SW1_VOLT	1.0 V	1.0 V	1.0 V	1.5 V	1.5 V
SW1_SEQ	2				
SW2_VOLT	1.0 V	1.0 V	1.0 V	1.8 V	1.8 V
SW2_SEQ	2	2	2	1	1
SW3_VOLT	1.35 V	1.35 V	1.2 V	1.2 V	1.35 V
SW3_SEQ	3	3	3	12	12
SW4_VOLT	VTT	1.8 V	VTT	VTT	VTT
SW4_SEQ	3	3	3	12	12
REFOUT_SEQ	3	3	3	12	12
LDO1_VOLT	1.2 V	1.2 V	1.2 V	1.35 V	1.35 V
LDO1_SEQ	4	4	4	1	12
PU CONFIG, SEQ_CLK_SPEED	1.0 ms				
PU CONFIG, SWDVS_CLK	6.25 mV/µs				
SW1 CONFIG	2.0 MHz				
SW2 CONFIG	2.0 MHz				
SW3 CONFIG	2.0 MHz				
SW4 CONFIG	2.0 MHz				

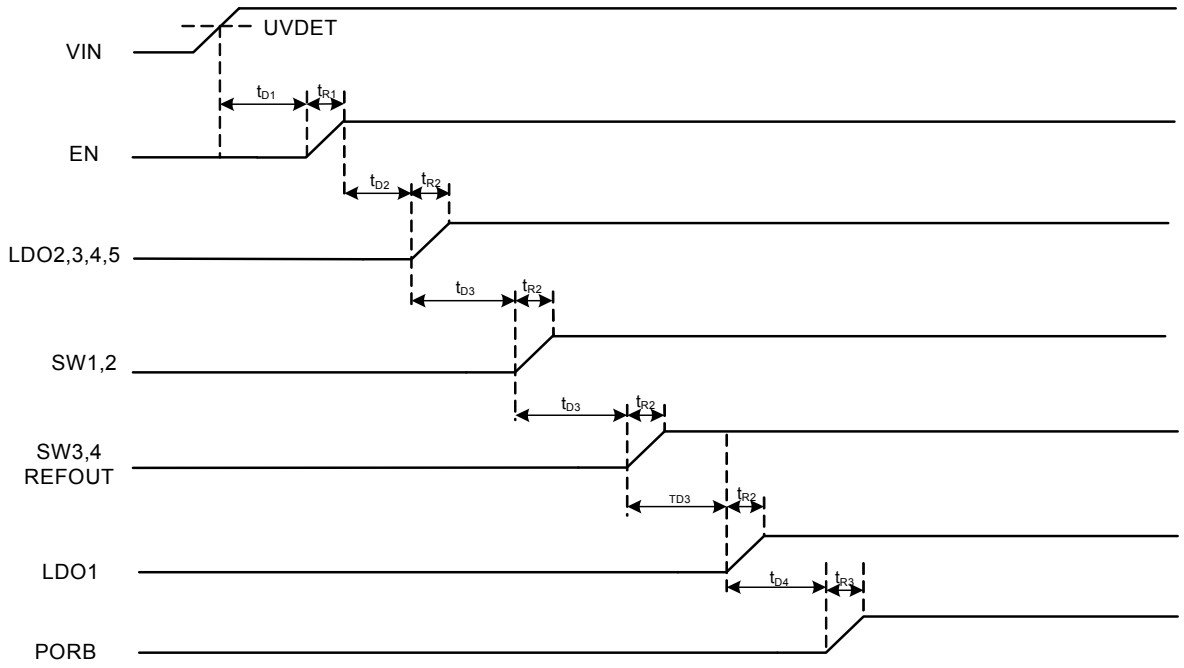

Figure 5. Starting Sequence: Example for V1 and V2

Table 9. 34VR500V1 and V2 Start-up Sequence Timing

Parameter	Description	Typ.	Unit
t_{D1}	Turn-on delay	6.0	ms
t_{R1}	Rise time of EN	(16)	ms
t_{D2}	Turn-on delay of first regulator	2.5	ms
t_{R2}	Rise time of regulators (17)	0.2	ms
t_{D3}	Delay between regulators	1.0	ms
t_{D4}	Turn-on delay of PORB	2.0	ms
t_{R3}	Rise time of PORB	0.2	ms

Notes
16. Depends on the external signal driving EN.
17. Rise time is a function of slew rate of regulators and nominal voltage selected.

6.1.2 Start Sequence Creation

The 34VR500 powers up based on the contents of the internal registers. Depending on certain bit settings, the internal registers are loaded from different sources, as shown in Figure 6.

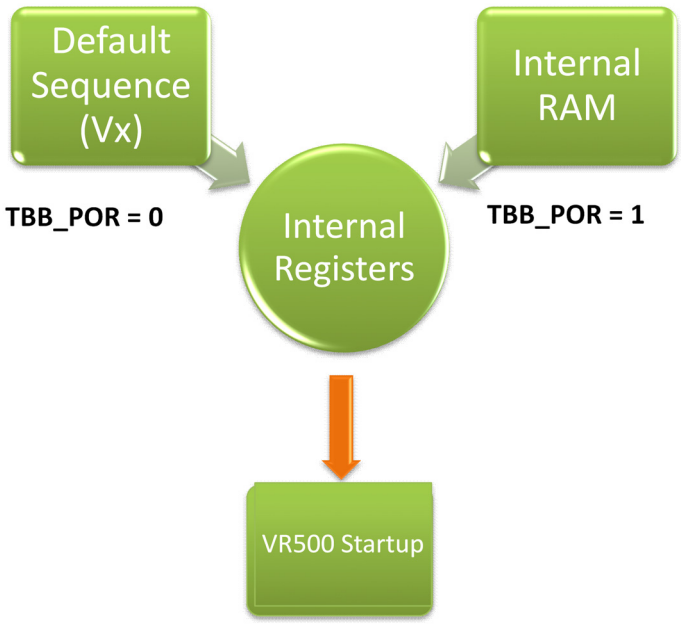

Figure 6. Starting Sequence

The contents of the internal registers are initialized to zero when a valid V_{IN} is first applied. The values that are then loaded into the internal registers depend on the value of the TBB_POR (the initial value of TBB_POR is always “0”):

- If TBB_POR = 0 the values are loaded from the Default Sequence (this is the case always for first starting)
- If TBB_POR = 1 the values are loaded from the internal RAM. V_{IN} must be valid to maintain the contents of the internal RAM.

To power on with the contents of the internal RAM, the following conditions must exist:

- V_{IN} is valid
- TBB_POR = 1 and there is a valid turn-on event via the EN pin

To keep a regulator off during a start-up sequence is to set its sequence to 0. This corresponds to the XX_SEQ setting of 0x00.

For example, 0x01 corresponds to a sequence of 1, and so on.

Figure 7 explains how to start from a new configuration.

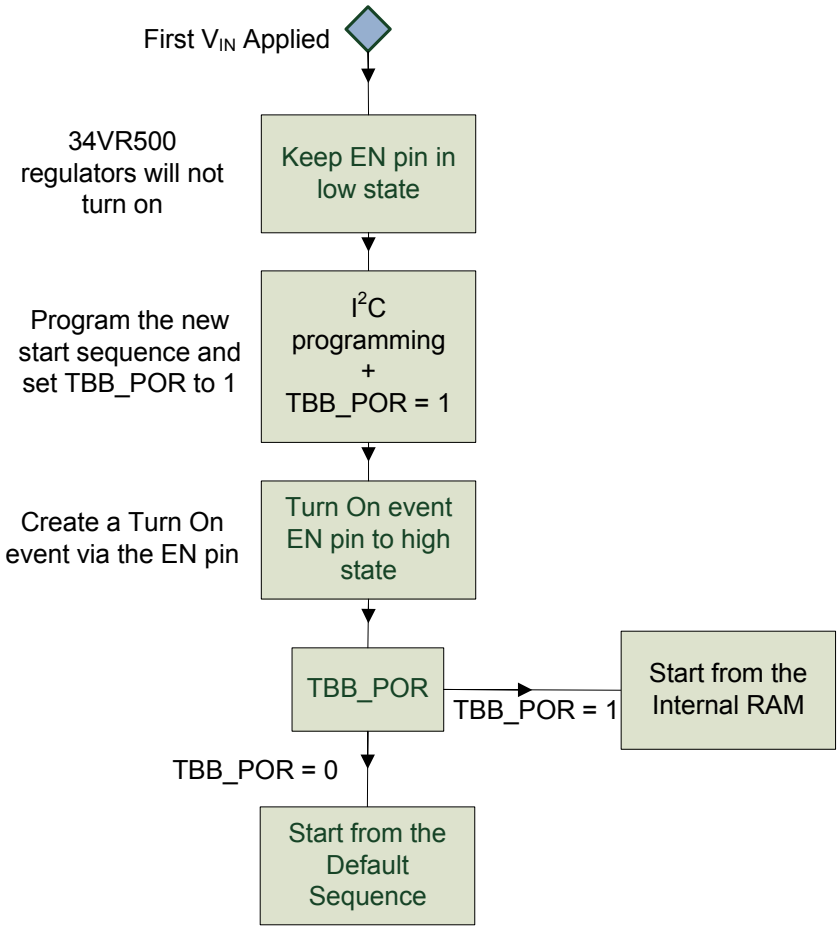

Figure 7. Modifying a Starting Sequence

Table 95 shows the portion of the register map concerning the programming of a new starting sequence.

6.2 16 MHz and 32 kHz Clocks

There are two clocks: a trimmed 16 MHz, RC oscillator and an untrimmed 32 kHz, RC oscillator. The 16 MHz oscillator is specified within -8.0/+8.0%. The 32 kHz untrimmed clock is only used in the following conditions:

- V_{IN} < UVDET
- All regulators are in SLEEP mode
- All regulators are in PFM switching mode

A 32 kHz clock, derived from the 16 MHz trimmed clock, is used when accurate timing is needed under the following conditions:

- During start-up, V_{IN} > UVDET

In addition, when the 16 MHz is active in the ON mode, the debounce times in Table 20 are referenced to the 32 kHz derived from the 16 MHz clock. The exceptions are the LOWVINI and ENI interrupts, which are referenced to the 32 kHz untrimmed clock.

Table 10. 16 MHz Clock Specifications

T_A = -40 to 105 °C (See Table 3), V_{VIN} = 2.8 to 4.5 V, V_{VBIAS} = 1.0 V ±4.0%, and typical external component values. Typical values are characterized at V_{VIN} = 3.6 V, and 25 °C, unless otherwise noted.

Symbol	Parameters	Min.	Typ.	Max.	Units	Notes
V_{IN}	Operating Voltage from the VIN pin	2.8	–	4.5	V	
f_{16MHZ}	16 MHz Clock Frequency	14.7	16	17.3	MHz	
f_{2MHZ}	2.0 MHz Clock Frequency	1.84	–	2.16	MHz	(18)

Notes
18. 2.0 MHz clock is derived from the 16 MHz clock.

6.2.1 Clock adjustment

The 16 MHz clock and hence the switching frequency of the regulators, can be adjusted to improve the noise integrity of the system. By changing the factory trim values of the 16 MHz clock, the user may add an offset as small as ±3.0% of the nominal frequency. Contact a Freescale representative for detailed information on this feature.

6.3 Bias and References Block Description

6.3.1 Internal Core Voltage References

All regulators use the main bandgap as the reference. The main bandgap is bypassed with a capacitor at VBG. The bandgap and the rest of the core circuitry are supplied from VCC. Table 11 shows the main characteristics of the core circuitry.

Table 11. Core Voltages Electrical Specifications(20)

T_A = -40 to 105 °C (See Table 3), V_{VIN} = 2.8 to 4.5 V, V_{VBIAS} = 1.0 V ±4.0%, and typical external component values. Typical values are characterized at V_{VIN} = 3.6 V, and 25 °C, unless otherwise noted.

Symbol	Parameters	Min.	Typ.	Max.	Units	Notes
VDIG (digital core supply)						
V_{DIG}	Output Voltage ON mode OFF mode	 – –	 1.5 1.3	 – –	V	(19)
VCC (Analog core supply)						
V_{CC}	Output Voltage ON mode OFF mode	 – –	 2.775 0.0	 – –	V	(19)
VBG (BANDGAP / REGULATOR REFERENCE)						
V_{BG}	Output Voltage	–	1.2	–	V	(19)
VBG_{ACC}	Absolute Accuracy	–	0.5	–	%	
VBG_{TACC}	Temperature Drift	–	0.25	–	%	

Notes
19. 3.0 V < V_{IN} < 4.5 V, no external loading on VDIG, VCC, or VBG. Extended operation down to UVDET, but no system malfunction.
20. For information only.

6.3.1.1 External Components

Table 12. External Components for Core Voltages

Regulator	Capacitor Value (μF)
VDIG	1.0
VCC	1.0
VBG	0.22

6.3.2 REFOUT Voltage Reference

REFOUT is an internal PMOS half supply voltage follower capable of supplying up to 10 mA. The output voltage is at one half the input voltage. Its typically used as the reference voltage for DDR memories. A filtered resistor divider is utilized to create a low frequency pole. This divider then utilizes a voltage follower to drive the load.

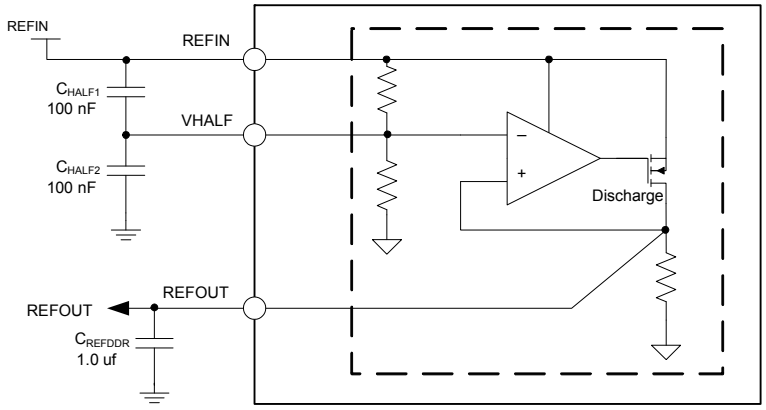

Figure 8. REFOUT Block Diagram

6.3.2.1 REFOUT Control Register

The REFOUT voltage reference is controlled by a single bit in REFOUTCTRL register in Table 13.

Table 13. Register REFOUTCTRL - ADDR 0x6A

Name	Bit #	R/W	Default	Description
UNUSED	3:0	–	0x00	UNUSED
REFOUTEN	4	R/W	0x00	Enable or disables REFOUT output voltage 0 = REFOUT Disabled 1 = REFOUT Enabled
UNUSED	7:5	–	0x00	UNUSED

External Components

Table 14. REFOUT External Components[21]

Capacitor	Capacitance (μF)
REFIN[22] to VHALF	0.1
VHALF to GND	0.1
REFOUT	1.0

Notes
21. Use X5R or X7R capacitors.
22. REFIN to GND, 1.0 μF minimum capacitance is provided by buck regulator output.

REFOUT Specifications

Table 15. REFOUT Electrical Characteristics

T_A = -40 to 105 °C (See Table 3), V_{IN} = 3.6 V, I_{REFDDR} = 0.0 mA, V_{REFIN} = 1.5 V, V_{VBIAS} = 1.0 V ±4.0%, and typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, I_{REFDDR} = 0.0 mA, V_{REFIN} = 1.5 V, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
REFOUT						
V_{REFIN}	Operating Input Voltage Range	1.2	–	1.8	V	
I_{REFDDR}	Operating Load Current Range	0.0	–	10	mA	
$I_{REFDDRLIM}$	Current Limit, I_{REFDDR} when V_{REFOUT} is forced to V_{REFIN}/4	10.5	15	25	mA	
$I_{REFDDRQ}$	Quiescent Current	–	8.0	–	μA	23
Active Mode – DC						
V_{REFOUT}	Output Voltage 1.2 V < V_{REFIN} < 1.8 V, 0.0 mA < I_{REFDDR} < 10 mA	–	V_{REFIN}/2	–	V	
$V_{REFOUTTOL}$	Output Voltage Tolerance 1.2 V < V_{REFIN} < 1.8 V, 0.6 mA ≤ I_{REFDDR} ≤ 10 mA	–1.0	–	1.0	%	
$V_{REFOUTLOR}$	Load Regulation 1.0 mA < I_{REFDDR} < 10 mA, 1.2 V < V_{REFIN} < 1.8 V	–	0.40	–	mV/mA	
Active Mode – AC						
$t_{ONREFDDR}$	Turn-on Time, Enable to 90% of end value V_{REFIN} = 1.2 V, 1.8 V, I_{REFDDR} = 0.0 mA	–	–	100	μs	
$t_{OFFREFDDR}$	Turn-Off Time, Disable to 10% of initial value V_{REFIN} = 1.2 V, 1.8 V, I_{REFDDR} = 0.0 mA	–	–	10	ms	
$V_{REFOUTOSH}$	Start-up Overshoot V_{REFIN} = 1.2 V, 1.8 V, I_{REFDDR} = 0.0 mA	–	1.0	6.0	%	
$V_{REFOUTTLR}$	Transient Load Response V_{REFIN} = 1.2 V, 1.8 V	–	5.0	–	mV	

Notes
23. When REFOUT is off there is a quiescent current of 1.5 μA typical.

6.4 Power Generation

6.4.1 Modes of Operation

The operation of the 34VR500 can be reduced to four states, or modes: ON, OFF, Sleep, and Standby. Figure 9 shows the state diagram of the 34VR500, along with the conditions to enter and exit from each state.

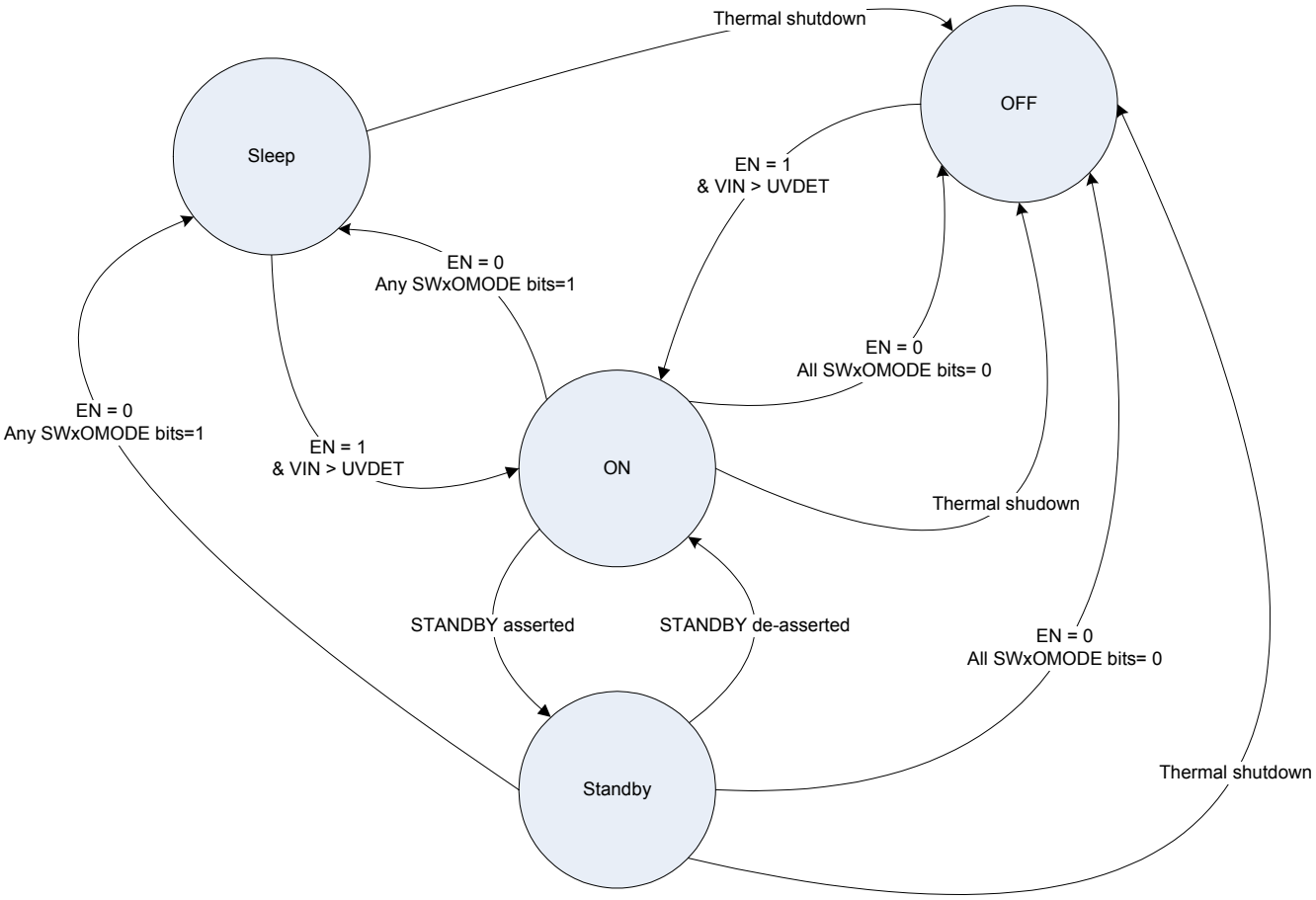

Figure 9. State Diagram

To complement the state diagram in Figure 9, a description of the states is provided in following sections. Note that V_{IN} must exceed the rising UVDET threshold to allow a power up. Refer to Table 22 for the UVDET thresholds. Additionally, the interrupt signal and INTB are only active in Sleep, Standby, and ON states.

6.4.1.1 ON Mode

The 34VR500 enters the ON mode after a turn-on event. PORB is de-asserted, high, in this mode of operation.

6.4.1.2 OFF Mode

The 34VR500 enters the OFF mode after a turn-off event. A thermal shutdown event also forces the 34VR500 into the OFF mode. Only VDIG is powered in this mode of operation. To exit the OFF mode, a valid turn-on event is required. PORB is asserted, LOW, in this mode.

6.4.1.3 Standby Mode

- Depending on STBY pin configuration, Standby is entered when the STBY pin is asserted. This is typically used for low-power mode of operation.
- When STBY is de-asserted, Standby mode is exited.

A product may be designed to go into a Low-power mode after periods of inactivity. The STBY pin is provided for board level control of going in and out of such deep sleep modes (DSM).

When a product is in DSM, it may be able to reduce the overall platform current by lowering the regulator output voltage, changing the operating mode of the regulators or disabling some regulators. The configuration of the regulators in Standby are pre-programmed through the I^2C interface.

Note that the STBY pin is programmable for Active High or Active Low polarity, and that decoding of a Standby event will take into account the programmed input polarity as shown in Table 16. When the 34VR500 is powered up first, regulator settings for the Standby mode are mirrored from the regulator settings for the ON mode. To change the STBY pin polarity to Active Low, set the STBYINV bit via software first, and then change the regulator settings for Standby mode as required. For simplicity, STBY will generally be referred to as active high throughout this document.

Table 16. STBY Pin and Polarity Control

STBY (Pin)[25]	STBYINV (I^2C bit)[26]	STBY Control [24]
0	0	0
0	1	1
1	0	1
1	1	0

Notes
24. STBY = 0: System is not in Standby, STBY = 1: System is in Standby
25. The state of the STBY pin only has influence in On mode.
26. Bit 6 in Power Control Register (ADDR - 0x1B)

Since STBY pin activity is driven asynchronously to the system, a finite time is required for the internal logic to qualify and respond to the pin level changes. A programmable delay is provided to hold off the system response to a Standby event. This allows the processor and peripherals some time after a standby instruction has been received to terminate processes to facilitate seamless entering into Standby mode.

When enabled (STBYDLY = 01, 10, or 11) per Table 17, STBYDLY will delay the Standby initiated response for the entire IC, until the STBYDLY counter expires.

An allowance should be made for three additional 32 k cycles required to synchronize the Standby event.

Table 17. STBY Delay - Initiated Response

STBYDLY[1:0][27]	Function
00	No Delay
01	One 32 k period (default)
10	Two 32 k periods
11	Three 32 k periods

Notes
27. Bits [5:4] in Power Control Register (ADDR - 0x1B)

6.4.1.4 Sleep Mode

- Depending on EN pin configuration, Sleep mode is entered when EN is de-asserted and SWxOMODE bit is set.
- To exit Sleep mode, assert the EN pin.

In the Sleep mode, the regulator will use the set point as programmed by SW1OFF[5:0] for SW1, SW2, SW3, and SW4. The activated regulators will maintain settings for this mode and voltage until the next turn-on event. Table 18 shows the control bits in Sleep mode. During Sleep mode, interrupts are active and the INTB pin will report any unmasked fault event.

Table 18. Regulator Mode Control

SWxOMODE	Off Operational Mode (Sleep) (28)
0	Off
1	PFM

Notes
28. For sleep mode, an activated switching regulator, should use the off mode set point as programmed by SW1OFF[5:0] for SW1, SW2, SW3, and SW4.

6.4.2 State Machine Flow Summary

Table 19 provides a summary matrix of the 34VR500 flow diagram to show the conditions needed to transition from one state to another.

Table 19. State Machine Flow Summary

STATE		Next State			
		OFF	Sleep	Standby	ON
Initial State	OFF	X	X	X	EN = 1 & V_{IN} > UVDET
	Sleep	Thermal Shutdown	X	X	EN = 1 & V_{IN} > UVDET
	Standby	Thermal Shutdown	EN = 0, Any SWxOMODE = 1	X	Standby de-asserted
		EN = 0, All SWxOMODE = 0			
	ON	Thermal Shutdown	EN = 0, Any SWxOMODE = 1	Standby asserted	X
		EN = 0, All SWxOMODE = 0			

6.4.2.1 Turn ON Events

From OFF and Sleep modes, the PMIC is powered on by a turn ON event. V_{IN} must be greater than UVDET for the PMIC to turn-on. When V_{IN} is greater than UVDET, a logic high on the EN pin is a turn ON event, when EN is high before V_{IN} is valid, a V_{IN} transition, from 0.0 V to a voltage greater than UVDET, also a Turn ON event. See the State diagram, Figure 9, and the Table 19 for more details. Any regulator enabled in the Sleep mode will remain enabled when transitioning from Sleep to ON, i.e., the regulator will not be turned OFF and then ON again to match the start-up sequence. The following is a more detailed description of the EN configuration:

- The EN signal is high and V_{IN} > UVDET, the PMIC will turn ON; the interrupt and sense bits, ENI and ENS respectively, will be set.

The sense bit will show the real time status of the EN pin. In this configuration, the EN input can be a mechanical switch debounced through a programmable debouncer, ENDBNC[1:0], to avoid a response to a very short (i.e., unintentional) key press. The interrupt is generated for both the falling and the rising edge of the EN pin. By default, a 30 ms interrupt debounce is applied to both falling and rising edges. The falling edge debounce timing can be extended with ENDBNC[1:0] as defined in the table below. The interrupt is cleared by software, or when cycling through the OFF mode.

Table 20. EN Hardware Debounce Bit Settings

Bits	State	Turn On Debounce (ms)	Falling Edge INT Debounce (ms)	Rising Edge INT Debounce (ms)
ENDBNC[1:0]	00	0.0	31.25	31.25
	01	31.25	31.25	31.25
	10	125	125	31.25
	11	750	750	31.25

Notes
29. The sense bit, ENS, is not debounced and follows the state of the EN pin.

6.4.2.2 Turn OFF Events

EN Pin

The EN pin is used to power off the 34VR500. The Off mode is entered when the EN pin is low and SWxOMODE = 0.

Thermal Protection

If the die temperature surpasses a given threshold, the thermal protection circuit will power off the 34VR500 to avoid damage. A turn-on event will not power on the PMIC while it is in thermal protection. The part will remain in Off mode until the die temperature decreases below a given threshold. There are no specific interrupts related to this other than the warning interrupt. See Power Dissipation section for more detailed information.

Undervoltage Detection

The state machine will transition to the OFF mode when the voltage at the VIN pin drops below the UVDET undervoltage falling threshold.

6.4.3 Power Tree

The 34VR500 features four buck regulators, five general purpose LDOs, and a DDR voltage reference, to supply voltages for the application and peripheral devices. The buck regulators are supplied directly from the main input supply (V_{IN}). The inputs to all of the buck regulators must be tied to V_{IN}, whether they are powered ON or OFF. The five general use LDO regulators are directly supplied from the main input supply or from the switching regulators depending on the application requirements. Since REFOUT is intended to provide DDR memory reference voltage, it should be supplied by any rail supplying voltage to DDR memories; the typical application recommends the use of SW3 as the input supply for REFOUT. Refer to Table 21 for a summary of all power supplies provided by the 34VR500.

Table 21. Power Tree Summary

Supply	Output Voltage (V)	Step Size (mV)	Maximum Load Current (mA)
SW1	0.625 - 1.875	25	4500
SW2	0.625 - 1.975	25	2000
SW3	0.625 - 1.975	25	2500
SW4	0.5*SW3_OUT (VTT for V1, V3, V4, V5), 0.625 - 1.975 (for V2)		1000
LDO1	0.80 – 1.55	50	250
LDO2	1.8 – 3.3	100	100
LDO3	1.8 – 3.3	100	350
LDO4	1.8 – 3.3	100	100
LDO5	1.8 – 3.3	100	200
REFOUT	0.5*SW3_OUT	NA	10