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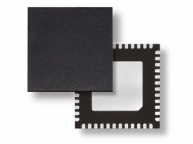
NXP Semiconductors
Data sheet: Advance Information

Document Number: VR5100
Rev. 4.0, 2/2017

Multi-output DC/DC regulator for low-power LS1 communication processors

VR5100

POWER MANAGEMENT



EP SUFFIX
98ASA00719D
48 QFN 7.0 X 7.0

The VR5100 is a high performance, highly integrated, multi-output, DC/DC regulator solution, with integrated power MOSFETs, ideally suited for the LS1 family of communications processors. Integrating three buck converters, six linear regulators, RTC supply and a coin-cell charger, the VR5100 can provide power for a complete system, including communications processors, memory, and system peripherals.

Features:

- Three adjustable high efficiency buck regulators: 3.8 A, 1.25 A, 1.5 A
  - Selectable modes: PWM, PFM, APS
- 5.0 V, 600 mA boost regulator with PFM or Auto mode
- Six adjustable general purpose linear regulators
- Input voltage range: 2.8 V to 4.5 V
- OTP (One Time Programmable) memory for device configuration
  - Programmable start-up sequence and timing
  - Selectable output voltage, frequency, soft start
- I^2C control
- Always ON RTC supply and Coin cell charger
- DDR reference voltage
- -40 °C to +125 °C operating junction temperature

Applications:

- Network attached storage (NAS)
- Value IOT gateway
- Mobile NAS
- Industrial control
- Home/Factory automation

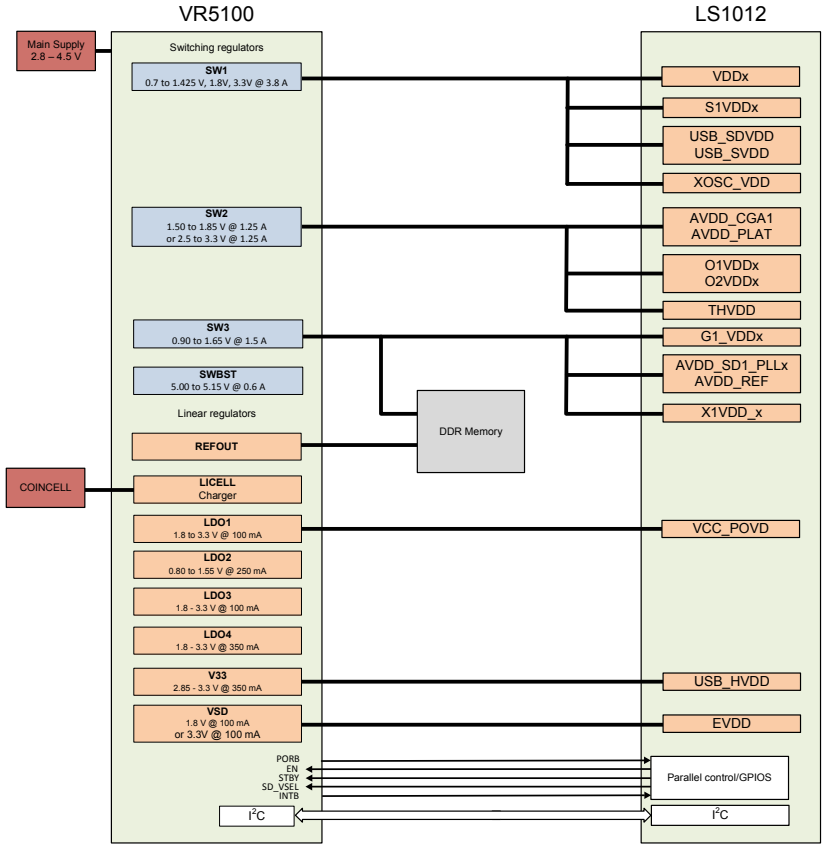


Figure 1. VR5100 simplified application diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table of Contents

1 Orderable parts

The VR5100 is available with pre-programmed OTP memory configurations. The devices are identified using the program codes from Table 1. Details of the OTP programming for each device can be found in Table 37.

Table 1. Orderable part variations

Part Number	Temperature (T_A)	Package	Programming Options	Notes
MC34VR5100A0EP	-40 °C to 105 °C (For use in Industrial applications)	48 QFN 7.0 mm x 7.0 mm	0 - Not programmed	(1)
MC34VR5100A1EP			1 (LS1012 with DDR3L)	

Notes
1. For tape and reel, add an R2 suffix to the part number.

2 Internal block diagram

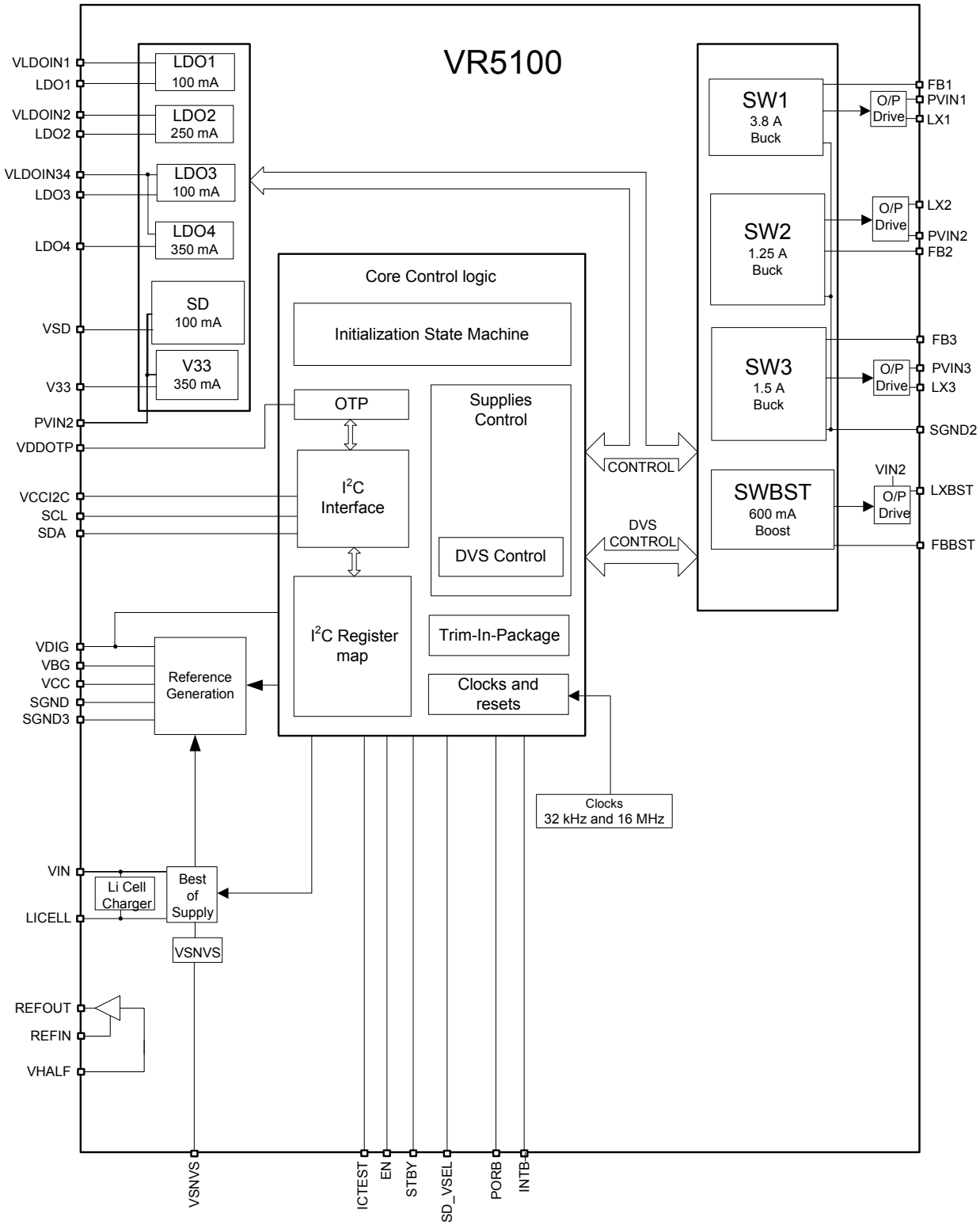


Figure 2. VR5100 simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

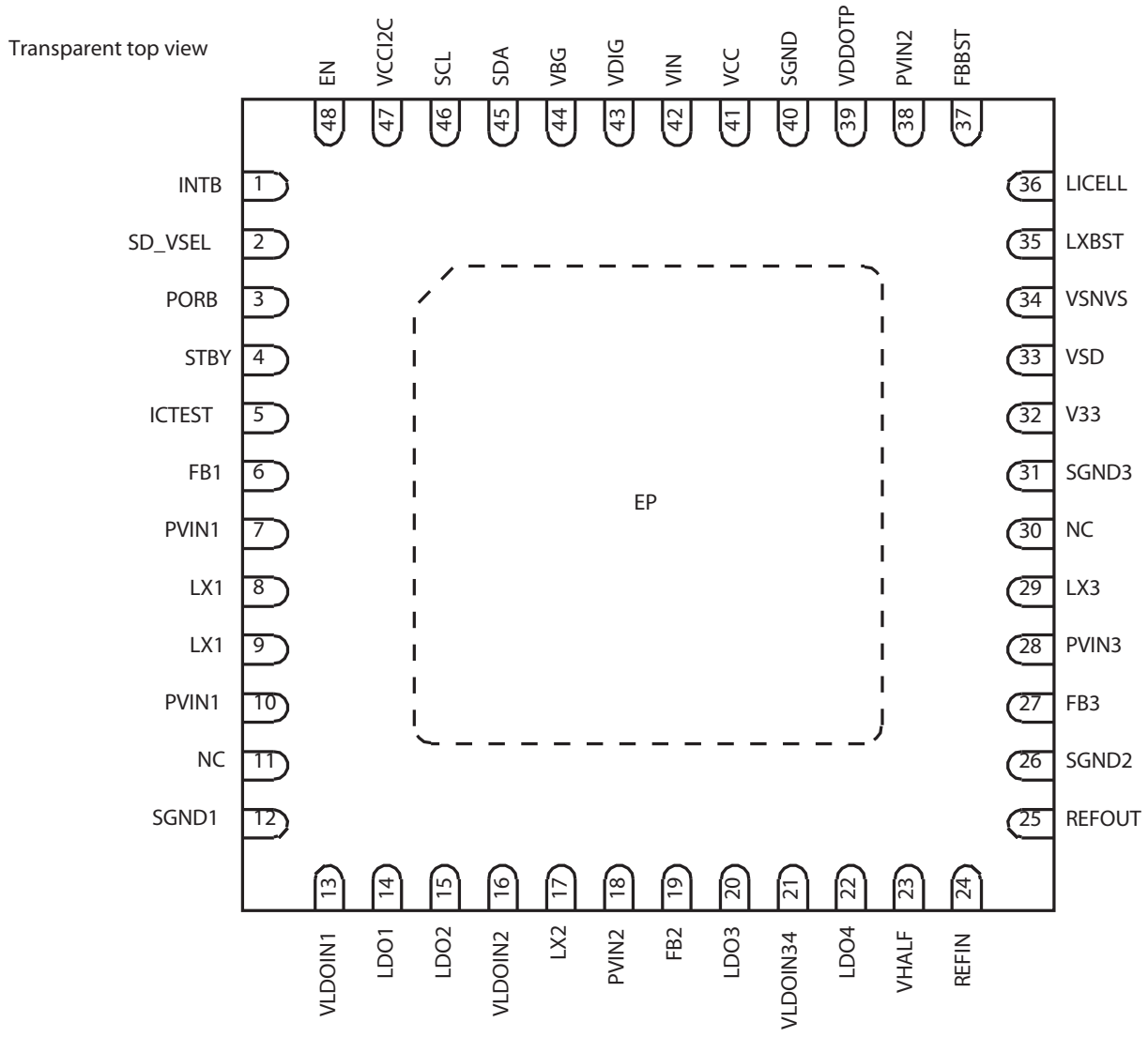


Figure 3. Pinout diagram

3.2 Pin definitions

Table 2. Pin definitions

Pin number	Pin name	Pin function	Type	Definition
-	EP	GND	GND	Expose pad. Functions as ground return for buck and boost regulators. Tie this pad to the inner and external ground planes through vias to allow effective thermal dissipation
1	INTB	O	Digital	Open drain interrupt signal to processor
2	SD_VSEL	I/O	Digital	Input from LS1 processor to select SD regulator voltage • SD_VSEL=0, SD = 3.3 V • SD_VSEL= 1, VSD = 1.8 V
3	PORB	O	Digital	Open drain reset output to processor
4	STBY	I	Digital	Standby input signal from processor
5	ICTEST	I	Digital and Analog	Reserved pin. Connect to GND in application
6	FB1	I	Analog	SW1 output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitance or near the load, if possible for best regulation
7	PVIN1	I	Analog	Input to SW1 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible
8, 9	LX1	O	Analog	Switcher 1 switch node connection. Connect to SW1 inductor
10	PVIN1	I	Analog	Input to SW1 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible
11, 30	NC	—	—	Leave this pin floating
12	SGND1	GND	GND	Ground reference for SW1. Connect to GND. Keep away from high current ground return paths
13	VLDOIN1	I	Analog	LDO1 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible
14	LDO1	O	Analog	LDO1 regulator output. Bypass with a 2.2 µF ceramic output capacitor
15	LDO2	O	Analog	LDO2 regulator output. Bypass with a 4.7 µF ceramic output capacitor
16	VLDOIN2	I	Analog	LDO2 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible
17	LX2 (2)	O	Analog	Switcher 2 switch node connection.Connect to SW2 inductor
18	PVIN2 (2)	I	Analog	Input to SW2 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible
19	FB2 (2)	I	Analog	SW2 output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitor or near the load, if possible for best regulation
20	LDO3	O	Analog	LDO3 regulator output. Bypass with a 2.2 µF ceramic output capacitor
21	VLDOIN34	I	Analog	LDO3 and LDO4 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible
22	LDO4	O	Analog	LDO4 regulator output. Bypass with a 2.2 µF ceramic output capacitor
23	VHALF	I	Analog	Half supply reference for REFOUT. Bypass with 0.1 µF to ground.
24	REFIN	I	Analog	REFOUT regulator input. Connect a 0.1 µF capacitor between REFIN and VHALF pin. Ensure there is at least 1.0 µF net capacitance from REFIN to ground
25	REFOUT	O	Analog	REFOUT regulator output. Bypass with 1.0 µF to ground
26	SGND2	GND	GND	Reference ground for SW2 and SW3 regulators. Connect to GND. Keep away from high current ground return paths
27	FB3 (2)	I	Analog	SW3 output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitor or near the load, if possible for best regulation
28	PVIN3 (2)	I	Analog	Input to SW3 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible
29	LX3 (2)	O	Analog	Switcher 3 switch node connection. Connect the SW3 inductor

Table 2. Pin definitions (continued)

31	SGND3	GND	GND	Connect to GND.
32	V33	O	Analog	V33 regulator output. Bypass with a 4.7 µF ceramic output capacitor
33	VSD	O	Analog	Output of VSD regulator. Bypass with a 2.2 µF ceramic output capacitor.
34	VSNVS	O	Analog	VSNVS regulator/switch output. Bypass with 0.47 µF capacitor to ground.
35	LXBST (2)	I/O	Analog	SWBST switch node connection. Connect to SWBST inductor and anode of Schottky diode
36	LICELL	I/O	Analog	Coin cell supply input/output. Bypass with 0.1 µF capacitor. Connect to optional coin cell
37	FBBST (2)	I	Analog	SWBST output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitor
38	PVIN2	I	Analog	Input to SD, V33 regulators and SWBST control circuitry. Connect to VIN rail and bypass with 10 µF capacitor
39	VDDOTP	I	Digital & Analog	Supply to program OTP fuses. Connect VDDOTP to GND during normal application
40	SGND	GND	GND	Ground reference for IC core circuitry. Connect to ground. Keep away from high current ground return paths
41	VCC	O	Analog	Internal analog core supply. Bypass with 1 µF capacitor to ground
42	VIN	I	Analog	Main IC supply. Bypass with 1.0 µF capacitor to ground. Connect to system input supply.
43	VDIG	O	Analog	Internal digital core supply. Bypass with 1.0 µF capacitor to ground
44	VBG	O	Analog	Main band gap reference. Bypass with 220 nF capacitor to ground
45	SDA	I/O	Digital	I^2C data line (open drain). Pull up to VCCI2C with a 4.7 kΩ resistor
46	SCL	I	Digital	I^2C clock. Pull up to VCCI2C with a 4.7 kΩ resistor
47	VCCI2C	I	Analog	Supply for I^2C bus. Bypass with 0.1 µF ceramic capacitor. Connect to 1.7 to 3.6 V supply. Ensure VCCI2C is always lesser than or equal to VIN
48	EN	I	Digital	Power ON/OFF input from processor

Notes

2. Unused switching regulators should be connected as follows: Pins SWxLX and SWxFB should be unconnected and Pin SWxIN should be connected to VIN with a 0.1 µF bypass capacitor.

4 General product characteristics

4.1 Absolute maximum ratings

Table 3. Absolute maximum voltage ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause malfunction or permanent damage to the device. The detailed maximum voltage rating per pin can be found in the pin list section.

Symbol	Description	Value	Unit	Notes
Electrical ratings				
ICTEST, LXBST	–	-0.3 to 7.5	V	
VIN, PVIN2, VLDOIN1, PVIN1, PVIN2, PVIN3, LX1, LX2, LX3	–	-0.3 to 4.8	V	
VDDOTP	OTP programming input supply voltage	-0.3 to 10.0	V	(3)
FBBST	Boost switcher feedback	-0.3 to 5.5	V	
INTB, SD_VSEL, PORB, STBY, FB1, FB2, FB3, LDO1, VLDOIN2, VLDOIN34, LDO3, LDO4, VHALF, REFIN, REFOUT, V33, VSD, VSNVS, LICELL, VCC, SDA, SCL, VCCI2C, EN	–	-0.3 to 3.6	V	
LDO2	LDO2 linear regulator output	-0.3 to 2.5	V	
VDIG	Digital core supply voltage output	-0.3 to 1.65	V	
VBG	Bandgap reference voltage output	-0.3 to 1.5	V	
V_{ESD}	ESD ratings • Human body model • Charge device model	 ±2000 ±500	V	(4)

Notes

3. 10 V Maximum voltage rating during OTP fuse programming. 7.5 V Maximum DC voltage rated otherwise.
4. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the Charge device model (CDM), Robotic (C_{ZAP} = 4.0 pF).

4.2 Thermal characteristics

Table 4. Thermal ratings

Symbol	Description (Rating)	Min.	Max.	Unit	Notes
Thermal ratings					
T_A	Ambient operating temperature range • Industrial version	-40	105	°C	
T_J	Operating junction temperature range	-40	125	°C	(5)
T_{ST}	Storage temperature range	-65	150	°C	
T_{PPRT}	Peak package reflow temperature	–	(7)	°C	(6) (7)
QFN48 thermal resistance and package dissipation ratings					
$R_{\theta JA}$	Junction to ambient, natural convection • Four layer board (2s2p) • Eight layer board (2s6p)	 – –	 24 15	°C/W	(8) (9) (10)
$R_{\theta JB}$	Junction to board	–	11	°C/W	(11)
$R_{\Theta JCBOTTOM}$	Junction to case bottom	–	1.4	°C/W	(12)
ΨJT	Junction to package top • Natural convection	–	1.3	°C/W	(13)

Notes

5. Do not operate beyond 125 °C for extended periods of time. Operation above 150 °C may cause permanent damage to the IC. See Thermal Protection Thresholds for thermal protection features.
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
7. NXP's package reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For peak package reflow temperature and moisture sensitivity levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts, and review parametrics.
8. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
9. The Board uses the JEDEC specifications for thermal testing (and simulation) JESD51-7 and JESD51-5.
10. Per JEDEC JESD51-6 with the board horizontal.
11. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
12. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
13. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters (ΨJT) are not available, the thermal characterization parameter is written as Psi-JT.

4.3 Current consumption

The current consumption of the individual blocks is described in detail in the following table.

Table 5. Current consumption summary

T_A= -40 °C to 105 °C, V_{IN} = 3.6 V, V_{CCI2C} = 1.7 V to 3.6 V, L_{ICELL} = 1.8 V to 3.3 V, V_{SNVS} = 3.0 V, typical external component values, unless otherwise noted. Typical values are characterized at VIN = 3.6 V, V_{CCI2C} = 3.3 V, L_{ICELL} = 3.0 V, V_{SNVS} = 3.0 V and 25 °C, unless otherwise noted.

Mode	VR5100 Conditions	System Conditions	Typ.	Max.	Unit	Notes
Coin Cell	VSNVS from LICELL, All other blocks off, VIN = 0.0 V	No load on VSNVS	4.0	7.0	µA	(14) (15)
Off	VSNVS from VIN or LICELL Wake-up from EN active 32 kHz RC on All other blocks off VIN ≥ UVDET	No load on VSNVS, PMIC able to wake-up	16	25	µA	(14) (15)
Sleep LPSR	VSNVS from VIN Wake-up from EN active Trimmed reference active SW3 PFM. All other regulators off. Trimmed 16 MHz RC off 32 kHz RC on REFOUT disabled	No load on any of the regulators	130 (14) 200 (17)	220 (14)	µA	(16)
	LDO1 & LDO3 activated in addition to SW3	No load on any of the regulators	170 (14) 260 (17)	248 (14)	µA	(16)
Standby	VSNVS from either VIN or LICELL SW1 in PFM SW2 in PFM SW3 in PFM SWBST off Trimmed 16 MHz RC enabled Trimmed reference active LDO1-4 enabled V33 enabled VSD enabled REFOUT enabled	No load on any of the regulators	297	450	µA	(16)
ON	VSNVS from VIN SW1 in APS SW2 in APS SW3 in APS SWBST off Trimmed 16 MHz RC enabled Trimmed reference active LDO1-4 enabled V33 enabled VSD enabled REFOUT enabled	No load on any of the regulators	1.2		mA	

Notes

14. At 25 °C only
15. When V_{IN} is below the UVDET threshold, in the range of 1.8 V ≤ V_{IN} < 2.65 V, the quiescent current increases by 50 µA, typically.
16. For PFM operation, headroom should be 300 mV or greater.
17. At 105 °C only

4.4 Electrical characteristics

Table 6. Static electrical characteristics – SW1

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{PVIN1} = 3.6 V, V_{SW1} = 1.2 V, I_{SW1} = 100 mA, typical external component values, f_{SW1} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{PVIN1} = 3.6 V, V_{SW1} = 1.2 V, I_{SW1} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW1						
V_{PVIN1}	Operating input voltage	2.8	–	4.5	V	(18)
V_{SW1}	Nominal output voltage	–	Table 46	–	V	
V_{SW1ACC}	Output voltage accuracy • PWM, APS, 2.8 V < V_{PVIN1} < 4.5 V, 0 < I_{SW1} < 3.8 A 0.7 V ≤ V_{SW1} ≤ 1.2 V • PFM, APS, 2.8 V < V_{PVIN1} < 4.5 V, 0 < I_{SW1} < 3.8 A 1.225 V < V_{SW1} < 1.425 V • PFM, steady state, 2.8 V < V_{PVIN1} < 4.5 V, 0 < I_{SW1} < 150 mA 1.8 V ≤ V_{SW1} ≤ 1.425 V • PWM, APS, 2.8 V < V_{PVIN1} < 4.5 V, 0 < I_{SW1} < 2.75A 1.8 V < V_{SW1} < 3.3 V • PFM, steady state, 2.8 V < V_{PVIN1} < 4.5 V, 0 < I_{SW1} < 150 mA 1.8 V ≤ V_{SW1} ≤ 3.3 V	-25 -25 -45 -6.0 -6.0	–	25 35 45 6.0 6.0	mV mV mV % %	
I_{SW1}	Rated output load current, • 2.8 V ≤ V_{PVIN1} ≤ 4.5 V, 0.7 V < V_{SW1} < 1.425 V, 1.8V, 3.3V	3800	–	–	mA	
I_{SW1Q}	Quiescent current • PFM Mode • APS Mode	 – –	 22 300	 – –	µA	
I_{SW1LIM}	Current limiter peak current detection , current through inductor • SW1ILIM = 0 • SW1ILIM = 1	 4 2.6	 5.5 4.0	 8.0 5.4	A	
ΔV_{SW1}	Output ripple	–	5.0	–	mV	
R_{SW1DIS}	Discharge resistance	–	600	–	Ω	
Switch mode supply SW1						
V_{SW1OSH}	Start-up overshoot, I_{SW1} = 0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{PVIN1} = 4.5 V, V_{SW1} = 1.425 V	–	–	66	mV	
t_{ONSW1}	Turn-on time, enable to 90% of end value, I_{SW1} = 0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{PVIN1} = 4.5 V, V_{SW1} = 1.425 V	–	–	500	µs	

Notes

18. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any VR5100 regulator, or external system supply.

Table 7. Static electrical characteristics – SW2

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{PVIN2} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, typical external component values, f_{SW2} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{PVIN2} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW2						
V_{PVIN2}	Operating input voltage	2.8	–	4.5	V	(19)
V_{SW2}	Nominal output voltage	–	Table 48	–	V	
V_{SW2ACC}	Output voltage accuracy • PWM, APS, 2.8 V ≤ V_{PVIN2} ≤ 4.5 V, 0 ≤ I_{SW2} ≤ 1.25 A • 1.50 V ≤ V_{SW2} ≤ 1.85 V • 2.5 V ≤ V_{SW2} ≤ 3.3 V • PFM, 2.8 V ≤ V_{PVIN2} ≤ 4.5 V, 0 ≤ I_{SW2} ≤ 50 mA • 1.50 V ≤ V_{SW2} ≤ 1.85 V • 2.5 V ≤ V_{SW2} ≤ 3.3 V	 -3.0% -6.0% -6.0% -6.0%	 – – – –	 3.0% 6.0% 6.0% 6.0%	%	
I_{SW2}	Rated output load current, 2.8 V < V_{PVIN2} < 4.5 V, 1.50 V < V_{SW2} < 1.85 V, 2.5 V < V_{SW2} < 3.3 V	1250	–	–	mA	(20)
I_{SW2Q}	Quiescent current • PFM mode • APS mode (Low output voltage settings) • APS mode (High output voltage settings, SW2_HI=1)	 – – –	 23 145 305	 – – –	µA	
I_{SW2LIM}	Current limiter peak current detection, current through inductor • SW2ILIM = 0 • SW2ILIM = 1	 1.625 1.235	 2.5 1.9	 3.375 2.565	A	
ΔV_{SW2}	Output ripple	–	5.0	–	mV	
R_{ONSW2P}	SW2 P-MOSFET $R_{DS(on)}$ at V_{IN} = V_{PVIN2} = 3.3 V	–	215	245	mΩ	
R_{ONSW2N}	SW2 N-MOSFET $R_{DS(on)}$ at V_{IN} = V_{PVIN2} = 3.3 V	–	258	326	mΩ	
I_{SW2PQ}	SW2 P-MOSFET leakage current, V_{IN} = V_{PVIN2} = 4.5 V	–	–	10.5	µA	
I_{SW2NQ}	SW2 N-MOSFET leakage current, V_{IN} = V_{PVIN2} = 4.5 V	–	–	3.0	µA	
R_{SW2DIS}	Discharge resistance during OFF mode	–	600	–	Ω	
V_{SW2OSH}	Start-up overshoot, I_{SW2} = 0.0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{PVIN2} = 4.5 V	–	–	66	mV	
t_{ONSW2}	Turn-on time, enable to 90% of end value, I_{SW2} = 0.0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{PVIN2} = 4.5 V	–	–	500	µs	

Notes

19. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any VR5100 regulator, or external system supply.
20. The higher output voltages available depend on the voltage drop in the conduction path as given by the following equation: (V_{PVIN2} - V_{SW2}) = I_{SW2}* (DCR of Inductor + R_{ONSW2P} + PCB trace resistance).

Table 8. Static electrical characteristics – SW3

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{PVIN3} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, typical external component values, f_{SW3} = 2.0 MHz. Typical values are characterized at V_{IN} = V_{PVIN3} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW3						
V_{PVIN3}	Operating input voltage	2.8	–	4.5	V	(21)
V_{SW3}	Nominal output voltage	–	Table 50	–	V	
V_{SW3ACC}	Output voltage accuracy • PWM, APS, 2.8 V < V_{PVIN3} < 4.5 V, 0 < I_{SW3} < 1.5 A, 0.9 V < V_{SW3} < 1.65 V • PFM, steady state (2.8 V < V_{PVIN3} < 4.5 V, 0 < I_{SW3} < 50 mA), 0.9 V < V_{SW3} < 1.65 V	-3.0% -6.0%	– –	3.0% 6.0%	%	
I_{SW3}	Rated output load current, 2.8 V < V_{PVIN3} < 4.5 V, 0.9 V < V_{SW3} < 1.65 V, PWM, APS mode	1500	–	–	mA	(22)
I_{SW3Q}	Quiescent current • PFM Mode • APS Mode	– –	50 150	– –	µA	
I_{SW3LIM}	Current limiter peak current detection, current through inductor • SW3ILIM = 0 • SW3ILIM = 1	1.95 1.45	3.0 2.25	4.05 3.05	A	
ΔV_{SW3}	Output ripple	–	5.0	–	mV	
R_{ONSW3P}	SW3 P-MOSFET $R_{DS(on)}$at V_{IN} = V_{SW3IN} = 3.3 V	–	205	235	mΩ	
R_{ONSW3N}	SW3 N-MOSFET $R_{DS(on)}$ at V_{IN} = V_{SW3IN} = 3.3 V	–	250	315	mΩ	
I_{SW3PQ}	SW3 P-MOSFET leakage current, V_{IN} = V_{SW3IN} = 4.5 V	–	–	12	µA	
I_{SW3NQ}	SW3 N-MOSFET leakage current, V_{IN} = V_{SW3IN} = 4.5 V	–	–	4.0	µA	
R_{SW3DIS}	Discharge resistance during Off mode	–	600	–	Ω	
V_{SW3OSH}	Start-up overshoot, I_{SW3} = 0.0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{PVIN3} = 4.5 V	–	–	66	mV	
t_{ONSW3}	Turn-on time, enable to 90% of end value, I_{SW3} = 0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{PVIN3} = 4.5 V	–	–	500	µs	

Notes

21. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any VR5100 regulator, or external system supply.
22. The higher output voltages available depend on the voltage drop in the conduction path as given by the following equation: (V_{SW3IN} - V_{SW3}) = I_{SW3}* (DCR of Inductor +R_{ONSW3P} + PCB trace resistance).

Table 9. Static electrical characteristics - SWBST

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = $V_{SWBSTIN}$ = 3.6 V, V_{SWBST} = 5.0 V, I_{SWBST} = 100 mA, typical external component values, f_{SWBST} = 2.0 MHz, otherwise noted. Typical values are characterized at V_{IN} = $V_{SWBSTIN}$ = 3.6 V, V_{SWBST} = 5.0 V, I_{SWBST} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameters	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SWBST						
$V_{SWBSTIN}$	Input voltage range	2.8	–	4.5	V	(23)
V_{SWBST}	Nominal output voltage	–	Table 52	–	V	
I_{SWBST}	Continuous load current • 2.8 V ≤ V_{IN} ≤ 3.0 V • 3.0 V ≤ V_{IN} ≤ 4.5 V	 500 600	 – –	 – –	mA	
$V_{SWBSTACC}$	Output voltage accuracy, 2.8 V ≤ V_{IN} ≤ 4.5 V, 0 < I_{SWBST} < $I_{SWBSTMAX}$	-4.0	–	3.0	%	
I_{SWBSTQ}	Quiescent current (auto mode)	–	222	289	µA	
ΔV_{SWBST}	Output ripple, 2.8 V ≤ V_{IN} ≤ 4.5 V, 0 < I_{SWBST} < $I_{SWBSTMAX}$, excluding reverse recovery of Schottky diode	–	–	120	mVp-p	
$I_{SWBSTLIM}$	Peak Current Limit	1400	2200	3200	mA	(24)
$R_{DSONBST}$	MOSFET on resistance	–	206	306	mΩ	
$I_{SWBSTHSQ}$	NMOS Off leakage, V_{SWBST} = 4.5 V, SWBSTMODE [1:0] = 00	–	1.0	5.0	µA	
$V_{SWBSTOSH}$	Start-up overshoot, I_{SWBST} = 0.0 mA	–	–	500	mV	
$t_{ONSWBST}$	Turn-on time, enable to 90% of VSWBST, ISWBST = 0.0 mA	–	–	2.0	ms	

Notes

23. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any VR5100 regulator, or external system supply.
24. Only in Auto and APS modes.

Table 10. Static electrical characteristics - VSNVS

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VSNVS						
V_{IN}	Operating input voltage • Valid coin cell range • Valid V_{IN}	 1.8 2.25	 - –	 3.3 4.5	V	
I_{SNVS}	Operating load current, V_{INMIN} < V_{IN} < V_{INMAX}	1.0	–	1000	µA	
V_{SNVS}	Output voltage • 5.0 µA < I_{SNVS} < 1000 µA (OFF), 3.20 V < V_{IN} < 4.5 V • 5.0 µA < I_{SNVS} < 1000 µA (ON), 3.20 V < V_{IN} < 4.5 V • 5.0 µA < I_{SNVS} < 1000 µA (Coin Cell mode), 2.84 V < V_{COIN} < 3.3 V	 -5.0% -5.0% V_{COIN}-0.10	 3.0 3.0	 7.0% 5.0% V_{COIN}	V	
$V_{SNVSDROP}$	Dropout voltage, 2.85 V < V_{IN} < 2.9 V, 1.0 µA < I_{SNVS} < 1000 µA	–	–	110	mV	
$I_{SNVSLIM}$	Current limit, V_{IN} > V_{TH1}	1100	–	6750	µA	
VSNVS DC, SWITCH						
V_{LICELL}	Operating input voltage, valid coin cell range	1.8	–	3.3	V	
I_{SNVS}	Operating load current	1.0	–	1000	µA	
$R_{DSONSNVS}$	Internal switch $R_{DS(on)}$	–	–	100	Ω	

Table 11. Dynamic electrical characteristics - VSNVS

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VSNVS						
$V_{SNVSTON}$	Turn-on time (load capacitor, 0.47 µF), from V_{IN} = V_{TH1} to 90% of V_{SNVS}, V_{COIN} = 0.0 V, I_{SNVS} = 5.0 µA	–	–	24	ms	(25),(26)
$V_{SNVSOSH}$	Start-up overshoot, I_{SNVS} = 5.0 µA	–	40	70	mV	
$V_{SNVSLOTR}$	Transient load response, 3.2 < V_{IN} ≤ 4.5 V, I_{SNVS} = 100 to 1000 µA	2.8	–	–	V	
V_{TL1}	V_{IN} falling threshold (V_{IN} powered to coin cell powered)	2.45	2.70	3.05	V	
V_{TH1}	V_{IN} Rising Threshold (coin cell powered to V_{IN} powered)	2.5	2.75	3.10	V	
V_{HYST1}	V_{IN} threshold hysteresis for V_{TH1}-V_{TL1}	5.0	-	-	mV	
$V_{SNVSCROSS}$	Output voltage during crossover, V_{COIN} > 2.9 V, Switch to LDO: V_{IN} > V_{TH1}, I_{SNVS} = 100 µA, LDO to Switch: V_{IN} < V_{TL1}, I_{SNVS} = 100 µA	2.45	-	-	V	

Notes

25. The start-up of V_{SNVS} is not monotonic. It first rises to 1.0 V and then settles to 3.0 V.
26. From coin cell insertion to VSNVS = 1.0 V, the delay time is typically 400 ms.

Table 12. Static electrical characteristics - LDO1

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{LDOIN1} = 3.6 V, V_{LDO1} = 3.3 V, I_{LDO1} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDOIN1} = 3.6 V, V_{LDO1} = 3.3 V, I_{LDO1} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
LDO1 linear regulator						
V_{LDOIN1}	Operating input voltage • 1.8 V ≤ $V_{LDO1NOM}$ ≤ 2.5 V • 2.6 V ≤ $V_{LDO1NOM}$ ≤ 3.3 V	2.8 $V_{LDO1NOM}$ +0.250	– –	4.5 4.5	V	(27)
$V_{LDO1NOM}$	Nominal output voltage	–	Table 55	–	V	
I_{LDO1}	Rated output load current	100	–	–	mA	
$V_{LDO1TOL}$	Output voltage tolerance, $V_{LDO1INMIN}$ < V_{LDOIN1} < 4.5 V, 0.0 mA < I_{LDO1} < 100 mA, LDO1 = 1.8 V to 3.3 V	-3.0	–	3.0	%	
I_{LDO1Q}	Quiescent current, no load, change in $I_{VIN,}$ when LDO1 enabled	–	13	–	µA	
$I_{LDO1LIM}$	Current limit, I_{LDO1} when V_{LDO1} is forced to $V_{LDO1NOM}$/2	122	167	280	mA	

Notes

27. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any VR5100 regulator, or external system supply.

Table 13. Dynamic electrical characteristics - LDO1

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{LDOIN1} = 3.6 V, V_{LDO1} = 3.3 V, I_{LDO1} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDOIN1} = 3.6 V, V_{LDO1} = 3.3 V, I_{LDO1} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
LDO1 linear regulator						
$PSRR_{LDO1}$	PSRR, I_{LDO1} = 75 mA, 20 Hz to 20 kHz • LDO1 = 1.8 V to 3.3 V, V_{LDOIN1} = $V_{LDO1INMIN}$ + 100 mV • LDO1 = 1.8 V to 3.3 V, V_{LDOIN1} = $V_{LDO1NOM}$ + 1.0 V	 35 52	 40 60	 – –	dB	
$NOISE_{LDO1}$	Output noise density, V_{LDOIN1} = $V_{LDO1INMIN}$, I_{LDO1} = 75 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/ √Hz	
t_{ONLDO1}	Turn-On time, enable to 90% of end value, V_{LDOIN1} = $V_{LDO1INMIN}$ to 4.5 V, I_{LDO1} = 0.0 mA, all output voltage settings	60	–	500	µs	
$t_{OFFLDO1}$	Turn-Off time, disable to 10% of initial value, V_{LDOIN1} = $V_{LDO1INMIN}$, I_{LDO1} = 0.0 mA	–	–	10	ms	
$LDO1_{OSHT}$	Start-up overshoot, V_{LDOIN1} = $V_{LDO1INMIN}$ to 4.5 V, I_{LDO1} = 0.0 mA	–	1.0	2.0	%	

Table 14. Static electrical characteristics - LDO2

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{LDOIN2} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDOIN2} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
LDO2 linear regulator						
V_{LDOIN2}	Operating Input Voltage	1.75	–	3.40	V	
$V_{LDO2NOM}$	Nominal output voltage	–	Table 56	–	V	
I_{LDO2}	Rated output load current	250	–	–	mA	
$V_{LDO2TOL}$	Output voltage tolerance, 1.75 V < V_{LDOIN2} < 3.40 V, 0.0 mA < I_{LDO2} < 250 mA, LDO2 = 0.8 V to 1.55 V	-3.0	–	3.0	%	
I_{LDO2Q}	Quiescent current, no load, change in I_{VIN} and $I_{VLDOIN2}$, when V_{LDO2} enabled	–	16	–	µA	
$I_{LDO2LIM}$	Current limit, I_{LDO2} when V_{LDO2} is forced to $V_{LDO2NOM}$/2	333	417	612	mA	

Table 15. Dynamic electrical characteristics - LDO2

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{LDOIN2} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDOIN2} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
LDO2 linear regulator						
$PSRR_{LDO2}$	PSRR, I_{LDO2} = 187.5 mA, 20 Hz to 20 kHz • LDO2 = 0.8 V to 1.55 V • LDO2 = 1.1 V to 1.55 V	 50 37	 60 45	 – –	dB	
$NOISE_{LDO2}$	Output noise density, V_{LDOIN2} = 1.75 V, I_{LDO2} = 187.5 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	 – – –	 -108 -118 -124	 -100 -108 -112	dBV/√Hz	
t_{ONLDO2}	Turn-on time, enable to 90% of end value, V_{LDO2IN} = 1.75 V to 3.4 V, I_{LDO2} = 0.0 mA	60	–	500	µs	
$t_{OFFLDO2}$	Turn-Off time, disable to 10% of initial value, V_{LDO2IN} = 1.75 V, I_{LDO2} = 0.0 mA	–	–	10	ms	
$LDO2_{OSHT}$	Start-up overshoot, V_{LDO2IN} = 1.75 V to 3.4 V, I_{LDO2} = 0.0 mA	–	1.0	2.0	%	

Table 16. Static electrical characteristics – VSD

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V18 = 1.85 V, I_{VSD} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V18 = 1.85 V, I_{VSD} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V18 linear regulator						
V_{PVIN2}	Operating input voltage	2.8	–	4.5	V	(28)
V_{VSD}	Nominal output voltage	–	Table	–	V	
I_{VSD}	Rated output load current	100	–	–	mA	
V_{VSD}	Output voltage accuracy, 2.8 V < V_{IN} < 4.5 V, 0.0 mA < I_{VSD} < 100 mA	-3.0	–	3.0	%	
I_{VSD}	Quiescent current, no load, change in I_{VIN} and I_{PVIN2}, When V_{18} enabled	–	13	–	µA	
I_{VSDLIM}	Current limit, I_{VSD} when V_{VSD} is forced to V_{VSDNOM}/2	122	167	280	mA	

Notes

28. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any VR5100 regulator, or external system supply.

Table 17. Dynamic Electrical Characteristics - VSD

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V18 = 1.85 V, I_{VSD} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V18 = 1.85 V, I_{VSD} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V18 LINEAR REGULATOR						
$PSRR_{VSD}$	PSRR, I_{VSD} = 75 mA, 20 Hz to 20 kHz • V18, V_{IN} = V_{VSDNOM} + 1.0 V	 52	 60	 –	dB	
$NOISE_{VSD}$	Output Noise Density, V_{IN} = 2.8V, I_{VSD} = 75 mA • 100 Hz – <1.0 kHz • 1.0 kHz – <10 kHz • 10 kHz – 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/√Hz	

Table 17. Dynamic Electrical Characteristics - VSD(continued)

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V18 = 1.85 V, I_{VSD} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V18 = 1.85 V, I_{VSD} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V18 linear regulator (Continued)						
t_{ONVSD}	Turn-on time, enable to 90% of end value, V_{IN} = 2.8 V to 4.5 V, I_{VSD} = 0.0 mA	60	–	500	µs	
t_{OFFVSD}	Turn-off time, disable to 10% of initial value, V_{IN} = 2.8 V, I_{VSD} = 0.0 mA	–	–	10	ms	
VSD_{OSHT}	Start-up overshoot, V_{IN} = 2.8 V to 4.5 V, I_{VSD} = 0.0 mA	–	1.0	2.0	%	

Table 18. Static Electrical Characteristics – V33

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V33 linear regulator						
V_{IN}	Operating input voltage, 2.9 V ≤ V_{33NOM} ≤ 3.6 V	2.8	–	4.5	V	(29), (30)
V_{33NOM}	Nominal output voltage	–	Table 57	–	V	
I_{V33}	Rated output load current	350	–	–	mA	
V_{33TOL}	Output voltage tolerance, 2.8 V < V_{IN} < 4.5 V, 0.0 mA < I_{V33} < 350 mA, V_{33}[1:0] = 00 to 11	-3.0	–	3.0	%	
I_{V33Q}	Quiescent current, no load, change in I_{VIN}, When V_{33} enabled	–	13	–	µA	
I_{V33LIM}	Current limit, I_{V33} when V_{33} is forced to V_{33NOM}/2	435	584.5	950	mA	

Notes

29. When the LDO output voltage is set above 2.6 V the minimum allowed input voltage need to be at least the output voltage plus 0.25 V for proper regulation due to the dropout voltage generated through the internal LDO transistor.
30. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any VR5100 regulator, or external system supply.

Table 19. Dynamic electrical characteristics – V33

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V33 linear regulator						
$PSRR_{V33}$	PSRR, I_{V33} = 262.5 mA, 20 Hz to 20 kHz, V_{33}[1:0] = 00 - 11, V_{IN} = V_{33NOM} + 1.0 V	52	60	–	dB	(31)
$NOISE_{V33}$	Output noise density, V_{IN} = 2.8 V, I_{V33} = 262.5 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/√Hz	
t_{ONV33}	Turn-On time, enable to 90% of end value, V_{IN} = 2.8 V, to 4.5 V, I_{V33} = 0.0 mA	60	–	500	µs	

Table 19. Dynamic electrical characteristics – V33 (continued)

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V33 linear regulator (Continued)						
t_{OFFV33}	Turn-Off time, disable to 10% of initial value, V_{IN} = 2.8 V, I_{V33} = 0.0 mA	–	–	10	ms	
V_{33OSHT}	Start-up overshoot, V_{IN} = 2.8 V to 4.5 V, I_{V33} = 0.0 mA	–	1.0	2.0	%	

Notes

31. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any VR5100 regulator, or external system supply.

Table 20. Static electrical characteristics – LDO3

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDOIN34}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDOIN34}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
LDO3 linear regulator						
$V_{LDOIN34}$	Operating input voltage • 1.8 V ≤ $V_{LDO3NOM}$ ≤ 2.5 V • 2.6 V ≤ $V_{LDO3NOM}$ ≤ 3.3 V	2.8 $V_{LDO3NOM}$ +0.250	– –	3.6 3.6	V	(32)
$V_{LDO3NOM}$	Nominal output voltage	–	Table 56	–	V	
I_{LDO3}	Rated output load current	100	–	–	mA	
$V_{LDO3TOL}$	Output voltage tolerance, $V_{LDOIN34MIN}$ < $V_{LDOIN34}$ < 3.6 V, 0.0 mA < I_{LDO3} < 100 mA, LDO3 = 1.8 V to 3.3 V	-3.0	–	3.0	%	
I_{LDO3Q}	Quiescent current, no load, change in I_{VIN} and $I_{VLDOIN34}$, when V_{LDO3} enabled	–	13	–	µA	
$I_{LDO3LIM}$	Current limit, I_{LDO3} when V_{LDO3} is forced to $V_{LDO3NOM}$/2	122	167	280	mA	

Notes

32. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any VR5100 regulator, or external system supply.

Table 21. Dynamic electrical characteristics – LDO3

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDOIN34}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDOIN34}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
LDO3 linear regulator						
$PSRR_{LDO3}$	PSRR, I_{LDO3} = 75 mA, 20 Hz to 20 kHz • LDO3 = 1.8 V to 3.3 V, $V_{LDOIN34}$ = $V_{LDO34INMIN}$ + 100 mV • LDO3 = 1.8 V to 3.3 V, $V_{LDOIN34}$ = $V_{LDO3NOM}$ + 1.0 V	 35 52	 40 60	 – –	dB	
$NOISE_{LDO3}$	Output noise density, $V_{LDO34IN}$ = $V_{LDOIN34MIN}$, I_{LDO3} = 75 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/√Hz	

Table 21. Dynamic electrical characteristics – LDO3 (continued)

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDOIN34}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDOIN34}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
LDO3 linear regulator (Continued)						
t_{ONLDO3}	Turn-on time, enable to 90% of end value, $V_{LDOIN34}$ = $V_{LDOIN34MIN}$ to 3.6 V, I_{LDO3} = 0.0 mA	60	–	500	µs	
$t_{OFFLDO3}$	Turn-off time, disable to 10% of initial value, $V_{LDOIN34}$ = $V_{LDOIN34MIN}$, I_{LDO3} = 0.0 mA	–	–	10	ms	
$LDO3_{OSHT}$	Start-up overshoot, $V_{LDOIN34}$ = $V_{LDOIN34MIN}$ to 3.6 V, I_{LDO3} = 0.0 mA	–	1.0	2.0	%	

Table 22. Static electrical characteristics - LDO4

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDOIN34}$ = 3.6 V, VLDO4 = 3.3 V, I_{LDO4} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDOIN34}$ = 3.6 V, VLDO4 = 3.3 V, I_{LDO4} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
LDO4 LINEAR REGULATOR						
$V_{LDOIN34}$	Operating input voltage • 1.8 V ≤ $V_{LDO4NOM}$ ≤ 2.5 V • 2.6 V ≤ $V_{LDO4NOM}$ ≤ 3.3 V	2.8 $V_{LDO4NOM}$ +0.250	– –	3.6 3.6	V	(33)
$V_{LDO4NOM}$	Nominal output voltage	–	Table 56	–	V	
I_{LDO4}	Rated output load current	350	–	–	mA	
$V_{LDO4TOL}$	Output voltage tolerance, $V_{LDOIN34MIN}$ < $V_{LDOIN34}$ < 3.6 V, 0.0 mA < I_{LDO3} < 100 mA, VLDO4 = 1.9 V to 3.3 V	-3.0	–	3.0	%	
I_{LDO4Q}	Quiescent current, no load, change in I_{VIN} and $I_{VLDOIN34}$, When V_{LDO4} enabled	–	13	–	µA	
$I_{LDO4LIM}$	Current limit, I_{LDO4} when V_{LDO4} is forced to $V_{LDO4NOM}$/2	435	584.5	950	mA	
$PSRR_{VLDO4}$	PSRR, I_{LDO4} = 262.5 mA, 20 Hz to 20 kHz • LDO4 = 1.9 V to 3.3 V, $V_{LDOIN34}$ = $V_{LDOIN34MIN}$ + 100 mV • LDO4 = 1.9 V to 3.3 V, $V_{LDOIN34}$ = $V_{LDO4NOM}$ + 1.0 V	 35 52	 40 60	 – –	dB	

Notes

33. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any VR5100 regulator, or external system supply.

Table 23. Dynamic electrical characteristics - LDO4

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDOIN34}$ = 3.6 V, LDO4 = 3.3 V, I_{LDO4} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDOIN34}$ = 3.6 V, LDO4 = 3.3 V, I_{LDO4} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
LDO4 linear regulator						
$NOISE_{LDO4}$	Output noise density, $V_{LDOIN342}$ = $V_{LDOIN34MIN}$, I_{LDO4} = 262.5 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/√Hz	
t_{ONLDO4}	Turn-on time, enable to 90% of end value, $V_{LDO34IN}$ = $V_{LDOIN34MIN}$, 3.6 V, I_{LDO4} = 0.0 mA	60	–	500	µs	
$t_{OFFLDO4}$	Turn-off time, disable to 10% of initial value, $V_{LDOIN34}$ = $V_{LDOIN34MIN}$, I_{LDO4} = 0.0 mA	–	–	10	ms	
$LDO4_{OSHT}$	Start-up overshoot, $V_{LDOIN34}$ = $V_{LDOIN34MIN}$, 3.6 V, I_{LDO4} = 0.0 mA	–	1.0	2.0	%	

Table 24. Static electrical characteristics - REFOUT

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, I_{REFOUT} = 0.0 mA, V_{REFIN} = 1.5 V, and typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, I_{REFOUT} = 0.0 mA, V_{REFIN} = 1.5 V, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
REFOUT linear regulator						
V_{REFIN}	Operating input voltage range	1.2	–	1.65	V	(34)
V_{REFOUT}	Output voltage, 1.2 V < V_{REFIN} < 1.65 V, 0.0 mA < I_{REFOUT} < 10 mA	–	V_{REFIN}/2	–	V	
$V_{REFOUTTOL}$	Output voltage tolerance, as a percentage of V_{REFIN}, 1.2 V < V_{REFIN} < 1.65 V, 0.6 mA < I_{REFOUT} < 10 mA	49.5	50	50.5	%	
I_{REFOUT}	Rated output load current	10	–	–	mA	
$I_{REFOUTQ}$	Quiescent current	–	12	–	µA	(35)
$I_{REFOUTLM}$	Current limit, I_{REFOUT} when V_{REFOUT} is forced to $V_{INREFOUT}$/4	10.5	15	25	mA	

Notes

34. When using SW3 as input, the REFOUT input voltage range specification refers to the voltage set point of SW3 and not the absolute value
35. When REFOUT is off there is a quiescent current of a typical 2.0 µA.

Table 25. Dynamic electrical characteristics - REFOUT

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, I_{REFOUT} = 0.0 mA, V_{REFIN} = 1.5 V, and typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, I_{REFOUT} = 0.0 mA, V_{REFIN} = 1.5 V, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
REFOUT linear regulator						
$t_{ONREFOUT}$	Turn-on time, enable to 90% of end value, V_{REFIN} = 1.2 V to 1.65 V, I_{REFOUT} = 0.0 mA	–	–	100	µs	
$t_{OFFREFOUT}$	Turn-off time, disable to 10% of initial value, V_{REFIN} = 1.2 V to 1.65 V, I_{REFOUT} = 0.0 mA	–	–	10	ms	
$V_{REFOUTOSH}$	Start-up overshoot, V_{REFIN} = 1.2 V to 1.65 V, I_{REFOUT} = 0.0 mA	–	1.0	6.0	%	

Table 26. Static electrical characteristics - Coin Cell

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, typical external component values, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Coin cell						
$V_{COINACC}$	Charge voltage accuracy	-100	–	-100	mV	
$I_{COINACC}$	Charge current accuracy	-30	–	30	%	
I_{COIN}	Coin cell charge current • I_{COINHI} (in On mode) • I_{COINLO} (in On mode)	 – –	 60 10	 – –	µA	

Table 27. Static electrical characteristics - Digital I/O

All parameters are specified at T_A = -40 °C to 105 °C, V_{CCI2C} = 1.7 V to 3.6 V, and typical external component values and full load current range, unless otherwise noted.

Pin name	Parameter	Load condition	Min.	Max.	Unit	Notes
EN	• V_L • V_H	– –	0.0 0.8 * V_{SNVS}	0.2 * V_{SNVS} 3.6	V	
PORB	• V_{OL} • V_{OH}	-2.0 mA Open drain	0.0 0.7 * V_{CCI2C}	0.4 * V_{CCI2C} V_{CCI2C}	V	
SCL	• V_L • V_H	– –	0.0 0.8 * V_{CCI2C}	0.2 * V_{CCI2C} 3.6	V	
SDA	• V_L • V_H • V_{OL} • V_{OH}	– – -2.0 mA Open drain	0.0 0.8 * V_{CCI2C} 0.0 0.7 * V_{CCI2C}	0.2 * V_{CCI2C} 3.6 0.4 * V_{CCI2C} V_{CCI2C}	V	
INTB	• V_{OL} • V_{OH}	-2.0 mA Open drain	0.0 0.7 * V_{CCI2C}	0.4 * V_{CCI2C} V_{CCI2C}	V	
STBY	• V_L • V_H	– –	0.0 0.8 * V_{SNVS}	0.2 * V_{SNVS} 3.6	V	
SD_VSEL	• V_L • V_H	–	0.0 0.8 * V_{CCI2C}	0.2 * V_{CCI2C} 3.6	V	
VDDOTP	• V_L • V_H	– –	0.0 1.1	0.3 1.7	V	

Table 28. Static electrical characteristics - internal supplies

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 2.8 V to 4.5 V, Licell = 1.8 V to 3.3 V and typical external component values. Typical values are characterized at V_{IN} = 3.6 V, Licell = 3.0 V, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VDIG (digital core supply)						
V_{DIG}	Output voltage • ON mode • Coin cell mode and OFF mode	 – –	 1.5 1.3	 – –	V	(36)
VCC (analog core supply)						
V_{CC}	Output voltage • ON mode and charging • Coin cell mode and OFF mode	 – –	 2.775 0.0	 – –	V	(36)

Table 28. Static electrical characteristics - internal supplies (continued)

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 2.8 V to 4.5 V, Licell = 1.8 V to 3.3 V and typical external component values. Typical values are characterized at V_{IN} = 3.6 V, Licell = 3.0 V, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VBG (BANDGAP regulator reference)						
V_{BG}	Output voltage at 25 °C	–	1.2	–	V	(36)
V_{BGACC}	Absolute trim accuracy	–	0.5	–	%	
V_{BGTACC}	Temperature drift	–	0.25	–	%	

Notes

36. 3.1 V < V_{IN} < 4.5 V, no external loading on VDIG, VCC, or VBG.

Table 29. Static electrical characteristics - UVDET threshold

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 2.8 V to 4.5 V, Licell = 1.8 V to 3.3 V and typical external component values. Typical values are characterized at V_{IN} = 3.6 V, Licell = 3.0 V, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{IN} UVDET threshold						
V_{UVDET}	• Rising • Falling	– 2.5	– –	3.1 –	V	

5 General description

The VR5100 is a high performance, highly integrate, multi-output, SMARTMOS, DC/DC regulator solution, with integrated power MOSFETs ideally suited for the LS1 family of communications processors.

5.1 Features

This section summarizes the VR5100 features.

- Input voltage range to PMIC: 2.8 V to 4.5 V
  - Buck regulators
    - Configurable three channels
    - SW1, 3.8 A (single); 0.7 V to 1.425 V, 1.8 V, 3.3 V
    - SW2, 1.25 A; 1.50 V to 1.85 V or 2.50 V to 3.30 V
    - SW3, 1.5 A; 0.90 V to 1.65 V
    - Dynamic voltage scaling
    - Modes: PWM, PFM, APS
    - Programmable output voltage
    - Programmable current limit
    - Programmable soft start sequence
    - Programmable PWM switching frequency
  - Boost regulator
    - SWBST, 5.0 V to 5.15 V, 0.6 A, OTG support
    - Modes: PFM and Auto
    - OCP fault interrupt
  - LDOs
    - VSD, 1.8 V or 3.3 V, 100 mA, based on SD_VSEL
    - V33, 2.85 V to 3.30 V, 350 mA
    - LDO1, 1.8 V to 3.3 V, 100 mA
    - LDO2, 0.80 V to 1.55 V, 250 mA
    - LDO3, 1.8 V to 3.3 V, 100 mA
    - LDO4, 1.8 V to 3.3 V, 350 mA
- Always ON RTC regulator/switch VSNVS 3.0 V, 1.0 mA
- Coin cell charger
- DDR memory reference voltage, REFOUT, 0.5 V to 0.9 V, 10 mA
- OTP (one time programmable) memory for device configuration, user-programmable start-up sequence and timing
- I^2C interface
- User programmable Standby, Sleep/LPSR, and Off modes

5.2 Functional block diagram

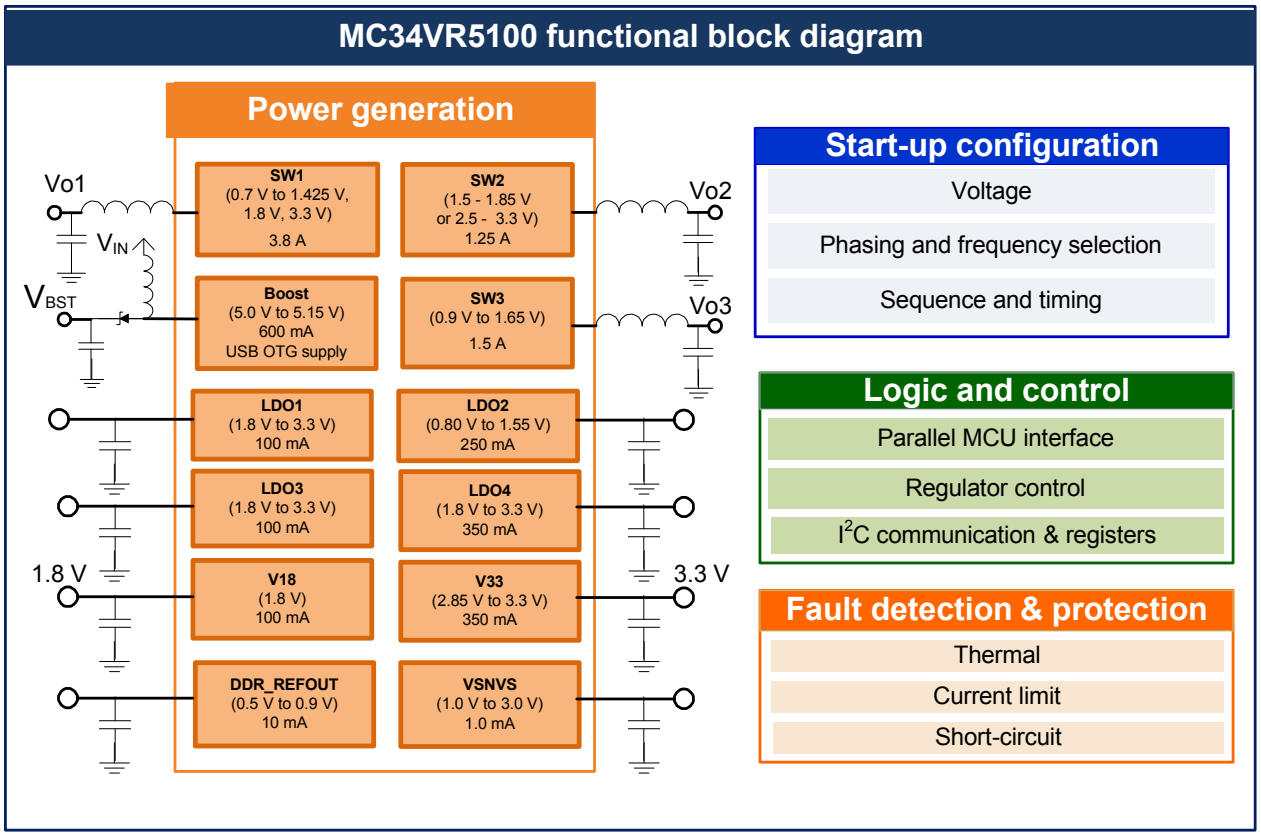


Figure 4. Functional block diagram