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Document Number: MC35XS3400
Rev. 10.0, 8/2013

RoHS

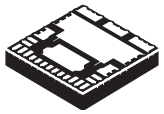
# Quad High Side Switch (Quad 35 mOhm)

**35XS3400**

**HIGH SIDE SWITCH**

The 35XS3400 is one in a family of devices designed for low-voltage automotive lighting applications. Its four low $R_{DS(ON)}$ MOSFETs (quad 35 mOhm) can control four separate 28 W bulbs, and/or LEDs.

Programming, control and diagnostics are accomplished using a 16-bit SPI interface. Its output with selectable slew rate improves electromagnetic compatibility (EMC) behavior. Additionally, each output has its own parallel input or SPI control for pulse-width modulation (PWM) control. The 35XS3400 allows the user to program via the SPI the fault current trip levels and duration of acceptable lamp inrush. The device has Fail-safe mode to provide functionality of the outputs in case of MCU damage. This device is powered by SMARTMOS technology.



**FK SUFFIX (PB-FREE)**
**98ARL10596D**
**24-PIN PQFN**

### Features

- Four protected 35 mΩ high side switches (at 25 °C)
- Operating voltage range of 6.0 V to 20 V with standby current < 5.0 μA, extended mode from 4.0 V to 28 V
- 8.0 MHz 16-bit 3.3 V and 5.0 V SPI control and status reporting with daisy chain capability
- PWM module using external clock or calibratable internal oscillator with programmable outputs delay management
- Smart over-current shutdown, severe short-circuit, over-temperature protection with time limited autoretry, and Fail-safe mode in case of MCU damage
- Output OFF or ON OpenLoad detection compliant to bulbs or LEDs and short to battery detection
- Analog current feedback with selectable ratio and board temperature feedback

**ORDERING INFORMATION**

| Device (for Tape and Reel orders add an R2 suffix to the part) | Temperature Range ($T_A$) | Package |
|---|---|---|
| MC35XS3400CHFK | -40 to 125°C | 24 PQFN |
| MC35XS3400DHFK | | |

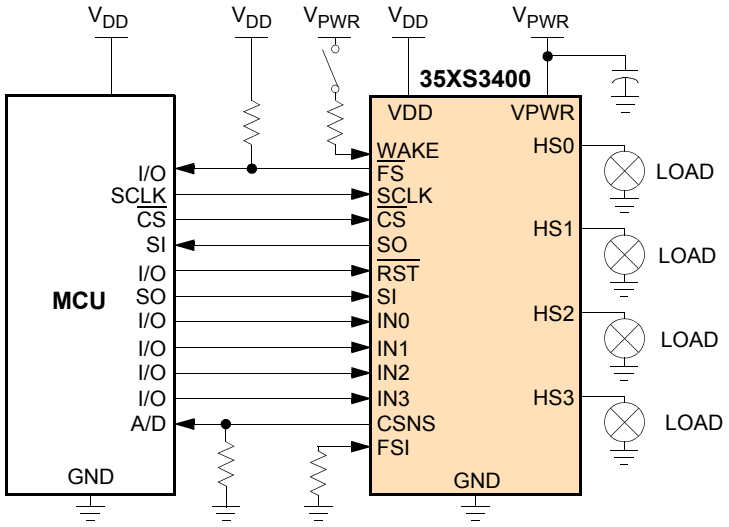



**Figure 1. 35XS3400 Simplified Application Diagram**

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

# DEVICE VARIATIONS

**Table 1. Device Variations**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Wake Input Clamp Voltage, $I_{CL(WAKE)}$ < 2.5 mA | $V_{CL(WAKE)}$ | | | | V |
| 35XS3400CHFK | | 18 | 25 | 32 | |
| 35XS3400DHFK | | 20 | 27 | 35 | |
| Fault Detection Blanking Time | $t_{FAULT}$ | | | | µs |
| 35XS3400CHFK | | - | 5.0 | 20 | |
| 35XS3400DHFK | | - | 5.0 | 10 | |
| Output Shutdown Delay Time | $t_{DETECT}$ | | | | µs |
| 35XS3400CHFK | | - | 7.0 | 30 | |
| 35XS3400DHFK | | - | 7.0 | 20 | |
| OpenLoad detection time in OFF state (1) | $t_{OLOFF}$ | | | | µs |
| 35XS3400CHFK and 35XS3400DHFK | | 170 | 212 | 270 | |
| Peak Package Reflow Temperature During Reflow(2), (3) | $T_{PPRT}$ | Note 3 | | | °C |

Notes

1. Guaranteed by design.
2. Pin soldering temperature limit is for 40 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
3. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx), and review parametrics.

# INTERNAL BLOCK DIAGRAM

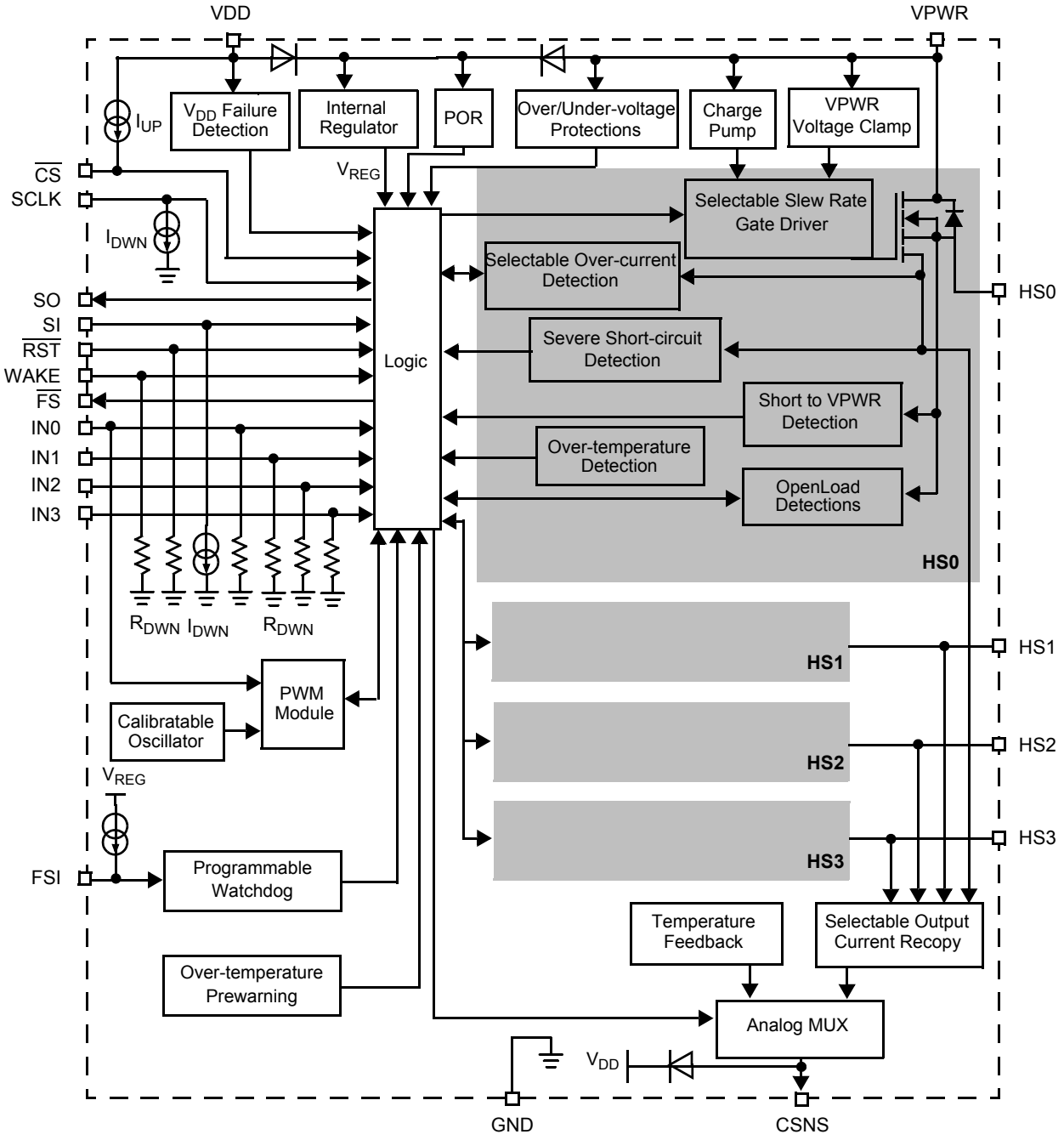



**Figure 2. 35XS3400 Simplified Internal Block Diagram**

# PIN CONNECTIONS

**Transparent Top View of Package**

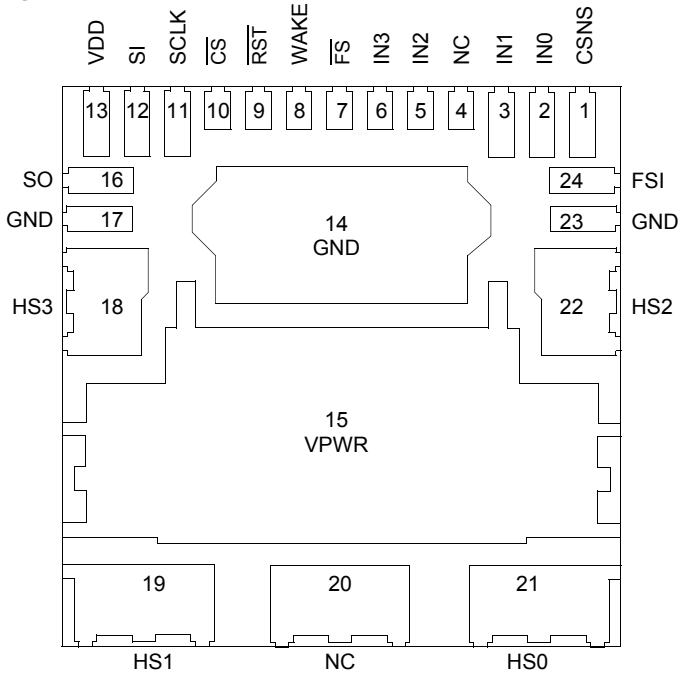



**Figure 3. 35XS3400 Pin Connections**

**Table 2. 35XS3400 Pin Definitions**

A functional description of each pin can be found in the Functional Pin Description section beginning on page 19.

| Pin Number | Pin Name | Pin Function | Formal Name | Definition |
|---|---|---|---|---|
| 1 | CSNS | Output | Output Current Monitoring | This pin reports an analog value proportional to the designated HS[0:3] output current or the temperature of the GND flag (pin 14). It is used externally to generate a ground-referenced voltage for the microcontroller (MCU). Current recopy and temperature feedback is SPI programmable. |
| 2<br>3<br>5<br>6 | IN0<br>IN1<br>IN2<br>IN3 | Input | Direct Inputs | Each direct input controls the device mode. The IN[0:3] high side input pins are used to directly control HS0:HS3 high side output pins.<br>The PWM frequency can be generated from IN0 pin to PWM module in case the external clock is set. |
| 7 | $\overline{FS}$ | Output | Fault Status (Active Low) | This pin is an open drain configured output requiring an external pull-up resistor to $V_{DD}$ for fault reporting. |
| 8 | WAKE | Input | Wake | This input pin controls the device mode. |
| 9 | $\overline{RST}$ | Input | Reset | This input pin is used to initialize the device configuration and fault registers, as well as place the device in a low-current Sleep mode. |
| 10 | $\overline{CS}$ | Input | Chip Select (Active Low) | This input pin is connected to a chip select output of a master microcontroller (MCU). |
| 11 | SCLK | Input | Serial Clock | This input pin is connected to the MCU providing the required bit shift clock for SPI communication. |
| 12 | SI | Input | Serial Input | This pin is a command data input pin connected to the SPI serial data output of the MCU or to the SO pin of the previous device of a daisy-chain of devices. |

**Table 2. 35XS3400 Pin Definitions (continued)**

A functional description of each pin can be found in the Functional Pin Description section beginning on page 19.

| Pin Number | Pin Name | Pin Function | Formal Name | Definition |
|---|---|---|---|---|
| 13 | VDD | Power | Digital Drain Voltage | This pin is an external voltage input pin used to supply power interfaces to the SPI bus. |
| 14, 17, 23 | GND | Ground | Ground | These pins, internally shorted, are the ground for the logic and analog circuitry of the device. These ground pins must be also shorted in the board. |
| 15 | VPWR | Power | Positive Power Supply | This pin connects to the positive power supply and is the source of operational power for the device. |
| 16 | SO | Output | Serial Output | This output pin is connected to the SPI serial data input pin of the MCU or to the SI pin of the next device of a daisy-chain of devices. |
| 18<br>19<br>21<br>22 | HS3<br>HS1<br>HS0<br>HS2 | Output | High Side Outputs | Protected 35 mΩ high side power output pins to the load. |
| 4, 20 | NC | N/A | No Connect | These pins may not be connected. |
| 24 | FSI | Input | Fail-safe Input | This input enables the watchdog timeout feature. |

# ELECTRICAL CHARACTERISTICS

## MAXIMUM RATINGS

**Table 3. Maximum Ratings**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Ratings | Symbol | Value | Unit |
|---|---|---|---|
| **ELECTRICAL RATINGS** | | | |
| $V_{PWR}$ Supply Voltage Range<br>Load Dump at 25 °C (400 ms)<br>Maximum Operating Voltage<br>Reverse Battery at 25 °C (2.0 min.) | $V_{PWR(SS)}$ | <br>41<br>28<br>-18 | V |
| $V_{DD}$ Supply Voltage Range | $V_{DD}$ | -0.3 to 5.5 | V |
| Input/Output Voltage | (7) | -0.3 to $V_{DD}$+0.3 | V |
| WAKE Input Clamp Current | $I_{CL(WAKE)}$ | 2.5 | mA |
| CSNS Input Clamp Current | $I_{CL(CSNS)}$ | 2.5 | mA |
| HS [0:3] Voltage<br>Positive<br>Negative | $V_{HS[0:3]}$ | <br>41<br>-16 | V |
| Output Current(4) | $I_{HS[0:3]}$ | 6 | A |
| Output Clamp Energy using single-pulse method(5) | $E_{CL[0:3]}$ | 35 | mJ |
| ESD Voltage(6)<br>Human Body Model (HBM) for HS[0:3], VPWR and GND<br>Human Body Model (HBM) for other pins<br>Charge Device Model (CDM)<br>Corner Pins (1, 13, 19, 21)<br>All Other Pins (2-12, 14-18, 20, 22-24) | <br>$V_{ESD1}$<br>$V_{ESD2}$<br>$V_{ESD3}$<br>$V_{ESD4}$ | <br>±8000<br>±2000<br>±750<br>±500 | V |
| **THERMAL RATINGS** | | | |
| Operating Temperature<br>Ambient<br>Junction | <br>$T_A$<br>$T_J$ | <br>-40 to 125<br>-40 to 150 | °C |
| Storage Temperature | $T_{STG}$ | -55 to 150 | °C |
| **THERMAL RESISTANCE** | | | |
| Thermal Resistance(8)<br>Junction to Case<br>Junction to Ambient | <br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br><1.0<br>30 | °C/W |
| Peak Package Reflow Temperature During Reflow(9), (10) | $T_{PPRT}$ | Note 10 | °C |

Notes

4. Continuous high side output current rating so long as maximum junction temperature is not exceeded. Calculation of maximum output current using package thermal resistance is required.
5. Active clamp energy using single-pulse method (L = 2.0 mH, $R_L$ = 0 Ω, $V_{PWR}$ = 14 V, $T_J$ = 150°C initial).
6. ESD testing is performed in accordance with the Human Body Model (HBM) ($C_{ZAP}$ = 100 pF, $R_{ZAP}$ = 1500 Ω), the Machine Model (MM) ($C_{ZAP}$ = 200 pF, $R_{ZAP}$ = 0 Ω), and the Charge Device Model (CDM), Robotic ($C_{ZAP}$ = 4.0 pF).
7. Input / Output pins are: IN[0:3], $\overline{RST}$, FSI, CSNS, SI, SCLK, $\overline{CS}$, SO, $\overline{FS}$
8. Device mounted on a 2s2p test board per JEDEC JESD51-2. 15 °C/W of $R_{\theta JA}$ can be reached in a real application case (4 layers board).
9. Pin soldering temperature limit is for 40 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
10. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx), and review parametrics.

## STATIC ELECTRICAL CHARACTERISTICS

**Table 4. Static Electrical Characteristics**

Characteristics noted under conditions 6.0 V ≤ $V_{PWR}$ ≤ 20 V, 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **POWER INPUTS** | | | | | |
| Battery Supply Voltage Range | $V_{PWR}$ | | | | V |
| Fully Operational | | 6.0 | – | 20 | |
| Extended mode(11) | | 4.0 | – | 28 | |
| Battery Clamp Voltage(12) | $V_{PWR(CLAMP)}$ | 41 | 47 | 53 | V |
| $V_{PWR}$ Operating Supply Current | $I_{PWR(ON)}$ | | | | mA |
| Outputs commanded ON, HS[0:3] open, IN[0:3] > $V_{IH}$ | | – | 6.5 | 20 | |
| $V_{PWR}$ Supply Current | $I_{PWR(SBY)}$ | | | | mA |
| Outputs commanded OFF, OFF OpenLoad Detection Disabled, HS[0:3] shorted to the ground with $V_{DD}$= 5.5 V<br>WAKE > $V_{IH}$ or $\overline{RST}$ > $V_{IH}$ and IN[0:3] < $V_{IL}$ | | – | 6.0 | 8.0 | |
| Sleep State Supply Current | $I_{PWR(SLEEP)}$ | | | | µA |
| $V_{PWR}$ = 12 V, $\overline{RST}$ = WAKE = IN[0:3] < $V_{IL}$, HS[0:3] shorted to the ground | | | | | |
| $T_A$ = 25 °C | | – | 1.0 | 5.0 | |
| $T_A$ = 85 °C | | – | – | 30 | |
| $V_{DD}$ Supply Voltage | $V_{DD(ON)}$ | 3.0 | – | 5.5 | V |
| $V_{DD}$ Supply Current at $V_{DD}$ = 5.5 V | $I_{DD(ON)}$ | | | | mA |
| No SPI Communication | | – | 1.6 | 2.2 | |
| 8.0 MHz SPI Communication(13) | | – | 5.0 | – | |
| $V_{DD}$ Sleep State Current at $V_{DD}$ = 5.5 V | $I_{DD(SLEEP)}$ | – | – | 5.0 | µA |
| Over-voltage Shutdown Threshold | $V_{PWR(OV)}$ | 28 | 32 | 36 | V |
| Over-voltage Shutdown Hysteresis | $V_{PWR(OVHYS)}$ | 0.2 | 0.8 | 1.5 | V |
| Under-voltage Shutdown Threshold(14) | $V_{PWR(UV)}$ | 3.3 | 3.9 | 4.3 | V |
| $V_{PWR}$ and $V_{DD}$ Power on Reset Threshold | $V_{SUPPLY(POR)}$ | 0.5 | – | 0.9 | $V_{PWR(UV)}$ |
| $V_{DD}$ Supply Failure Threshold ( for $V_{PWR}$ > $V_{PWR(UV)}$ ) | $V_{DD(FAIL)}$ | 2.2 | 2.5 | 2.8 | V |
| Recovery Under-voltage Threshold | $V_{PWR(UV)\_UP}$ | 3.4 | 4.1 | 4.5 | V |
| **OUTPUTS HS0 TO HS3** | | | | | |
| Output Drain-to-Source ON Resistance ($I_{HS}$ = 2.0 A, $T_A$ = 25 °C) | $R_{DS(ON)\_25}$ | | | | mΩ |
| $V_{PWR}$ = 4.0 V | | – | – | 100 | |
| $V_{PWR}$ = 6.0 V | | – | – | 55 | |
| $V_{PWR}$ = 10 V | | – | – | 35 | |
| $V_{PWR}$ = 13 V | | – | – | 35 | |

Notes

11. In extended mode, the functionality is guaranteed but not the electrical parameters. From 4.0 to 6.0 V voltage range, the device is only protected with the thermal shutdown detection.
12. Measured with the outputs open.
13. Typical value guaranteed per design.
14. Output will automatically recover with time limited autoretry to instructed state when $V_{PWR}$ voltage is restored to normal as long as the $V_{PWR}$ degradation level did not go below the under-voltage power-ON reset threshold. This applies to all internal device logic that is supplied by $V_{PWR}$ and assumes that the external $V_{DD}$ supply is within specification.

**Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions 6.0 V ≤ $V_{PWR}$ ≤ 20 V, 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OUTPUTS HS0 TO HS3 (Continued)** | | | | | |
| Output Drain-to-Source ON Resistance ($I_{HS}$ = 2.0 A, $T_A$ = 150 °C) | $R_{DS(ON)\_150}$ | | | | mΩ |
| $V_{PWR}$ = 4.5 V | | – | – | 170 | |
| $V_{PWR}$ = 6.0 V | | – | – | 94 | |
| $V_{PWR}$ = 10 V | | – | – | 66 | |
| $V_{PWR}$ = 13 V | | – | – | 66 | |
| Output Source-to-Drain ON Resistance ($I_{HS}$ = -2.0 A, $V_{PWR}$ = -18 V)(15) | $R_{SD(ON)}$ | | | | mΩ |
| $T_A$ = 25 °C | | – | – | 52.5 | |
| $T_A$ = 150 °C | | – | – | 70 | |
| Maximum Severe Short-circuit Impedance Detection(16) | $R_{SHORT}$ | 70 | 160 | 200 | mΩ |
| Output Over-current Detection Levels (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V) | | | | | A |
| | OCHI1_0 | 39.5 | 47 | 54.5 | |
| | OCHI2_0 | 25.2 | 30 | 34.8 | |
| | OC1_0 | 22 | 26.2 | 30.4 | |
| | OC2_0 | 18.9 | 22.5 | 26.1 | |
| | OC3_0 | 15.7 | 18.7 | 21.7 | |
| | OC4_0 | 12.6 | 15 | 17.4 | |
| | OCLO4_0 | 9.4 | 11.2 | 13.0 | |
| | OCLO3_0 | 6.3 | 7.5 | 8.7 | |
| | OCLO2_0 | 5.0 | 6.0 | 7.0 | |
| | OCLO1_0 | 3.2 | 4.0 | 4.8 | |
| $C_{SR0}$ Current Recopy Accuracy with one calibration point (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V)(18) | $C_{SR0\_0\_ACC(CAL)}$ | | | | % |
| Output Current | | | | | |
| 2.0 A | | -5.0 | – | 5.0 | |
| Current Sense Ratio (6.0 V ≤ $_{HS[0:3]}$ ≤ 20 V, CSNS ≤ 5.0 V)(17) | | | | | – |
| CSNS_ratio bit = 0 | $C_{SR0\_0}$ | – | 1/4300 | – | |
| CSNS_ratio bit = 1 | $C_{SR1\_0}$ | – | 1/25800 | – | |
| Current Sense Ratio ($C_{SR0}$) Accuracy (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V) | $C_{SR0\_0\_ACC}$ | | | | % |
| Output Current | | | | | |
| 6.75 A | | -12 | – | 12 | |
| 2.5 A | | -13 | – | 13 | |
| 1.5 A | | -16 | – | 16 | |
| 0.75 A | | -20 | – | 20 | |

Notes

15. Source-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity $V_{PWR}$.
16. Short-circuit impedance calculated from HS[0:3] to GND pins. Value guaranteed per design.
17. Current sense ratio = $I_{CSNS}$ / $I_{HS[0:3]}$.
18. Based on statistical analysis, it is not production tested.

**Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions 6.0 V ≤ $V_{PWR}$ ≤ 20 V, 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OUTPUTS HS0 TO HS3 (continued)** | | | | | |
| $C_{SR0}$ Current Recopy Temperature Drift (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V)(19)<br>Output Current<br>2.0 A | $\Delta(C_{SR0\_0})/\Delta(T)$ | | | 0.04 | %/°C |
| Current Sense Ratio ($C_{SR1}$) Accuracy (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V)<br>Output Current<br>6.25 A<br>39.5 A | $C_{SR1\_0\_ACC}$ | <br><br>-17<br>-12 | <br><br>–<br>– | <br><br>+17<br>+12 | % |
| Current Sense Clamp Voltage<br>CSNS Open; $I_{HS[0:3]}$ = 2.0 A with $C_{SR0}$ ratio | $V_{CL(CSNS)}$ | $V_{DD}$+0.25 | – | $V_{DD}$+1.0 | V |
| OFF OpenLoad Detection Source Current(20) | $I_{OLD(OFF)}$ | 30 | – | 100 | µA |
| OFF OpenLoad Fault Detection Voltage Threshold | $V_{OLD(THRES)}$ | 2.0 | 3.0 | 4.0 | V |
| ON OpenLoad Fault Detection Current Threshold | $I_{OLD(ON)}$ | 100 | 300 | 600 | mA |
| ON OpenLoad Fault Detection Current Threshold with LED<br>$V_{HS[0:3]}$ = $V_{PWR}$ - 0.75 V | $I_{OLD(ON\_LED)}$ | 2.5 | 5.0 | 10 | mA |
| Output Short to $V_{PWR}$ Detection Voltage Threshold<br>Output programmed OFF | $V_{OSD(THRES)}$ | $V_{PWR}$-1.2 | $V_{PWR}$-0.8 | $V_{PWR}$-0.4 | V |
| Output Negative Clamp Voltage<br>0.5 A ≤ $I_{HS[0:3]}$ ≤ 5.0 A, Output programmed OFF | $V_{CL}$ | -22 | – | -16 | V |
| Output Over-temperature Shutdown for 4.5 V < VPWR < 28 V | $T_{SD}$ | 155 | 175 | 195 | °C |

Notes

19. Based on statistical data: delta($C_{SR0}$)/delta(T)={(measured $I_{CSNS}$ at $T_1$ - measured $I_{CSNS}$ at $T_2$) / measured $I_{CSNS}$ at room} / {$T_1$-$T_2$}. No production tested.
20. Output OFF OpenLoad Detection Current is the current required to flow through the load for the purpose of detecting the existence of an OpenLoad condition when the specific output is commanded OFF. Pull-up current is measured for $V_{HS}$=$V_{OLD(THRES)}$

**Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions 6.0 V ≤ $V_{PWR}$ ≤ 20 V, 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CONTROL INTERFACE** | | | | | |
| Input Logic High Voltage[21] | $V_{IH}$ | 2.0 | – | $V_{DD}$+0.3 | V |
| Input Logic Low Voltage[21] | $V_{IL}$ | -0.3 | – | 0.8 | V |
| Input Logic Pull-down Current (SCLK, SI)[24] | $I_{DWN}$ | 5.0 | – | 20 | µA |
| Input Logic Pull-up Current ($\overline{CS}$)[25] | $I_{UP}$ | 5.0 | – | 20 | µA |
| SO, $\overline{FS}$ Tri-state Capacitance[22] | $C_{SO}$ | – | – | 20 | pF |
| Input Logic Pull-down Resistor ($\overline{RST}$, WAKE and IN[0:3]) | $R_{DWN}$ | 125 | 250 | 500 | kΩ |
| Input Capacitance[22] | $C_{IN}$ | – | 4.0 | 12 | pF |
| Wake Input Clamp Voltage[23], $I_{CL(WAKE)}$ < 2.5 mA<br>35XS3400CHFK<br>35XS3400DHFK | $V_{CL(WAKE)}$ | <br>18<br>20 | <br>25<br>27 | <br>32<br>35 | V |
| Wake Input Forward Voltage<br>$I_{CL(WAKE)}$ = -2.5 mA | $V_{F(WAKE)}$ | -2.0 | – | -0.3 | V |
| SO High State Output Voltage<br>$I_{OH}$ = 1.0 mA | $V_{SOH}$ | $V_{DD}$-0.4 | – | – | V |
| SO and $\overline{FS}$ Low-state Output Voltage<br>$I_{OL}$ = -1.0 mA | $V_{SOL}$ | – | – | 0.4 | V |
| SO, CSNS and $\overline{FS}$ Tri-state Leakage Current<br>$\overline{CS}$ = $V_{IH}$ and 0 V ≤ $V_{SO}$ ≤ $V_{DD}$, or $\overline{FS}$ = 5.5 V, or CSNS=0.0 V | $I_{SO(LEAK)}$ | -2.0 | 0 | 2.0 | µA |
| FSI External Pull-down Resistance[26]<br>Watchdog Disabled<br>Watchdog Enabled | RFS | <br>–<br>10 | <br>0<br>Infinite | <br>1.0<br>– | kΩ |

Notes

21. Upper and lower logic threshold voltage range applies to SI, $\overline{CS}$, SCLK, $\overline{RST}$, IN[0:3] and WAKE input signals. The WAKE and $\overline{RST}$ signals may be supplied by a derived voltage referenced to $V_{PWR}$.
22. Input capacitance of SI, $\overline{CS}$, SCLK, $\overline{RST}$, IN[0:3] and WAKE. This parameter is guaranteed by process monitoring but is not production tested.
23. The current must be limited by a series resistance when using voltages > 7.0 V.
24. Pull-down current is with $V_{SI} \geq$ 1.0 V and $V_{SCLK} \geq$ 1.0 V.
25. Pull-up current is with $V_{\overline{CS}} \leq$ 2.0 V. $\overline{CS}$ has an active internal pull-up to $V_{DD}$.
26. In Fail-Safe HS[0:3] depends respectively on ON[0:3]. FSI has an active internal pull-up to $V_{REG}$ ~ 3.0 V.

## DYNAMIC ELECTRICAL CHARACTERISTICS

**Table 5. Dynamic Electrical Characteristics**

Characteristics noted under conditions 6.0 V ≤ $V_{PWR}$ ≤ 20 V, 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **POWER OUTPUT TIMING HS0 TO HS3** | | | | | |
| Output Rising Medium Slew Rate (medium speed slew rate / SR[1:0]=00)[27]<br>$V_{PWR}$ = 14 V | $SR_{R\_00}$ | 0.2 | 0.4 | 0.8 | V/µs |
| Output Rising Slow Slew Rate (low speed slew rate / SR[1:0]=01)[27]<br>$V_{PWR}$ = 14 V | $SR_{R\_01}$ | 0.1 | 0.2 | 0.4 | V/µs |
| Output Falling Fast Slew Rate (high speed slew rate / SR[1:0]=10)[27]<br>$V_{PWR}$ = 14 V | $SR_{R\_10}$ | 0.4 | 0.8 | 1.6 | V/µs |
| Output Falling Medium Slew Rate (medium speed slew rate / SR[1:0]=00)[27]<br>$V_{PWR}$ = 14 V | $SR_{F\_00}$ | 0.2 | 0.4 | 0.8 | V/µs |
| Output Falling Slow Slew Rate (low speed slew rate / SR[1:0]=01)[27]<br>$V_{PWR}$ = 14 V | $SR_{F\_01}$ | 0.1 | 0.2 | 0.4 | V/µs |
| Output Rising Fast Slew Rate (high speed slew rate / SR[1:0]=10)[27]<br>$V_{PWR}$ = 14 V | $SR_{F\_10}$ | 0.4 | 0.8 | 1.6 | V/µs |
| Output Turn-ON Delay Time[28]<br>$V_{PWR}$ = 14 V for medium speed slew rate (SR[1:0]=00) | $t_{DLY(ON)}$ | 35 | 60 | 85 | µs |
| Output Turn-OFF Delay Time[29]<br>$V_{PWR}$ = 14 V for medium speed slew rate (SR[1:0]=00) | $t_{DLY(OFF)}$ | 35 | 60 | 85 | µs |
| Driver Output Matching Slew Rate ($SR_R$ /$SR_F$)<br>$V_{PWR}$ = 14 V @ 25 °C and for medium speed slew rate (SR[1:0]=00) | ΔSR | 0.8 | 1.0 | 1.2 | |
| Driver Output Matching Time ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$)<br>$V_{PWR}$ = 14 V, $f_{PWM}$ = 240 Hz, PWM duty-cycle = 50%, @ 25 °C for medium speed slew rate (SR[1:0]=00) | $\Delta t_{RF}$ | -25 | 0 | 25 | µs |

Notes

27. Rise and Fall Slew rates measured across a 5.0 Ω resistive load at high side output = 30% to 70% (see Figure 4, page 16).
28. Turn-ON delay time measured from rising edge of any signal (IN[0:3] and $\overline{CS}$) that would turn the output ON to $V_{HS[0:3]}$ = $V_{PWR}$ / 2 with $R_L$ = 5.0 Ω resistive load.
29. Turn-OFF delay time measured from falling edge of any signal (IN[0:3] and $\overline{CS}$) that would turn the output OFF to $V_{HS[0:3]}$ =$V_{PWR}$ / 2 with $R_L$ = 5.0 Ω resistive load.

**Table 5. Dynamic Electrical Characteristics (continued)**

Characteristics noted under conditions 6.0 V ≤ $V_{PWR}$ ≤ 20 V, 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **POWER OUTPUT TIMING HS0 TO HS3 (CONTINUED)** | | | | | |
| Fault Detection Blanking Time[30] | $t_{FAULT}$ | | | | µs |
| 35XS3400CHFK | | - | 5.0 | 20 | |
| 35XS3400DHFK | | - | 5.0 | 10 | |
| Output Shutdown Delay Time[31] | $t_{DETECT}$ | | | | µs |
| 35XS3400CHFK | | - | 7.0 | 30 | |
| 35XS3400DHFK | | - | 7.0 | 20 | |
| $\overline{CS}$ to CSNS Valid Time[32] | $t_{CNSVAL}$ | – | 70 | 100 | µs |
| Watchdog Timeout[33] | $t_{WDTO}$ | 217 | 310 | 400 | ms |
| ON OpenLoad Fault Cyclic Detection Time with LED | | - | $f_{IN0}$ / 128 | - | ms |

Notes

30. Time necessary to report the fault to $\overline{FS}$ pin.
31. Time necessary to switch-off the output in case of OT or OC or SC or UV fault detection (from negative edge of $\overline{FS}$ pin to HS voltage = 50% of $V_{PWR}$
32. Time necessary for the CSNS to be with ±5% of the targeted value.
33. For FSI open, the watchdog timeout delay measured from the rising edge of RST, to HS[0,2] output state depend on the corresponding input command.

**Table 5. Dynamic Electrical Characteristics (continued)**

Characteristics noted under conditions 6.0 V ≤ $V_{PWR}$ ≤ 20 V, 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Over-current Time Step | | | | | ms |
| OC[1:0]=00 (slow by default) | $t_{OC1\_00}$ | 3.4 | 5.0 | 6.6 | |
| | $t_{OC2\_00}$ | 1.0 | 1.72 | 2.0 | |
| | $t_{OC3\_00}$ | 1.4 | 2.0 | 2.6 | |
| | $t_{OC4\_00}$ | 2.0 | 3.0 | 4.0 | |
| | $t_{OC5\_00}$ | 3.4 | 5.0 | 6.74 | |
| | $t_{OC6\_00}$ | 8.4 | 12.2 | 16 | |
| | $t_{OC7\_00}$ | 31.2 | 44.6 | 48 | |
| OC[1:0]=01 (fast) | $t_{OC1\_01}$ | 1.72 | 2.48 | 3.22 | |
| | $t_{OC2\_01}$ | 0.56 | 0.8 | 1.04 | |
| | $t_{OC3\_01}$ | 0.72 | 1.04 | 1.36 | |
| | $t_{OC4\_01}$ | 1.02 | 1.58 | 1.92 | |
| | $t_{OC5\_01}$ | 1.56 | 2.24 | 2.92 | |
| | $t_{OC6\_01}$ | 4.28 | 6.12 | 7.96 | |
| | $t_{OC7\_01}$ | 15.4 | 22.2 | 29 | |
| OC[1:0]=10 (medium) | $t_{OC1\_10}$ | 6.8 | 9.8 | 12.8 | |
| | $t_{OC2\_10}$ | 2.2 | 3.2 | 4.2 | |
| | $t_{OC3\_10}$ | 2.8 | 4.2 | 5.6 | |
| | $t_{OC4\_10}$ | 4.0 | 5.8 | 7.6 | |
| | $t_{OC5\_10}$ | 6.8 | 9.8 | 12.8 | |
| | $t_{OC6\_10}$ | 17 | 24.4 | 31.8 | |
| | $t_{OC7\_10}$ | 6.24 | 89.2 | 116 | |
| OC[1:0]=11 (very slow) | $t_{OC1\_11}$ | 13.7 | 19.6 | 25.5 | |
| | $t_{OC2\_11}$ | 4.5 | 6.4 | 8.3 | |
| | $t_{OC3\_11}$ | 5.9 | 8.4 | 10.9 | |
| | $t_{OC4\_11}$ | 8.1 | 11.6 | 15.1 | |
| | $t_{OC5\_11}$ | 13.7 | 19.6 | 25.5 | |
| | $t_{OC6\_11}$ | 34.2 | 48.8 | 63.4 | |
| | $t_{OC7\_11}$ | 124.9 | 178.4 | 231.9 | |

**Table 5. Dynamic Electrical Characteristics (continued)**

Characteristics noted under conditions 6.0 V ≤ $V_{PWR}$ ≤ 20 V, 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Bulb Cooling Time Step | | | | | ms |
| CB[1:0]=00 or 11 (medium) | $t_{BC1\_00}$ | 582 | 834 | 1084 | |
| | $t_{BC2\_00}$ | 312 | 448 | 584 | |
| | $t_{BC3\_00}$ | 356 | 510 | 664 | |
| | $t_{BC4\_00}$ | 416 | 596 | 776 | |
| | $t_{BC5\_00}$ | 502 | 718 | 934 | |
| | $t_{BC6\_00}$ | 628 | 898 | 1168 | |
| CB[1:0]=01 (fast) | $t_{BC1\_01}$ | 296 | 418 | 544 | |
| | $t_{BC2\_01}$ | 156 | 224 | 292 | |
| | $t_{BC3\_01}$ | 176 | 254 | 332 | |
| | $t_{BC4\_01}$ | 202 | 290 | 378 | |
| | $t_{BC5\_01}$ | 256 | 360 | 468 | |
| | $t_{BC6\_01}$ | 452 | 648 | 884 | |
| CB[1:0]=10 (slow) | $t_{BC1\_10}$ | 1166 | 1668 | 2170 | |
| | $t_{BC2\_10}$ | 624 | 894 | 1164 | |
| | $t_{BC3\_10}$ | 714 | 1022 | 1310 | |
| | $t_{BC4\_10}$ | 834 | 1192 | 1552 | |
| | $t_{BC5\_10}$ | 1002 | 1434 | 1866 | |
| | $t_{BC6\_10}$ | 1256 | 1796 | 2340 | |
| **PWM MODULE TIMING** | | | | | |
| Input PWM Clock Range on IN0 | $f_{IN0}$ | 7.68 | – | 30.72 | kHz |
| Input PWM Clock Low Frequency Detection Range on IN0(34) | $f_{IN0(LOW)}$ | 1.0 | 2.0 | 4.0 | kHz |
| Input PWM Clock High Frequency Detection Range on IN0(34) | $f_{IN0(HIGH)}$ | 100 | 200 | 400 | kHz |
| Output PWM Frequency Range | $f_{PWM}$ | – | – | 1.0 | kHz |
| Output PWM Frequency Accuracy using Calibrated Oscillator | $A_{FPWM(CAL)}$ | -10 | – | +10 | % |
| Default Output PWM Frequency using Internal Oscillator | $f_{PWM(0)}$ | 84 | 120 | 156 | Hz |
| $\overline{CS}$ Calibration Low Minimum Time Detection Range | $t_{CSB(MIN)}$ | 14 | 20 | 26 | µs |
| $\overline{CS}$ Calibration Low Maximum Tine Detection Range | $t_{CSB(MAX)}$ | 140 | 200 | 260 | µs |
| Output PWM Duty-cycle Range for $f_{PWM}$ = 400 Hz(35) | $R_{PWM\_400}$ | 10 | – | 98 | % |
| Output PWM Duty-cycle Range for $f_{PWM}$ = 200 Hz(35) | $R_{PWM\_200}$ | 5.0 | – | 98 | % |
| Output PWM Duty-cycle Range for $f_{PWM}$ = 1.0 kHz for high speed slew rate(35) | $R_{PWM\_1k}$ | 6.0 | – | 94 | % |
| **INPUT TIMING** | | | | | |
| Direct Input Toggle Timeout | $t_{IN}$ | 175 | 250 | 325 | ms |
| **AUTO-RETRY TIMING** | | | | | |
| Auto-retry Period | $t_{AUTO}$ | 105 | 150 | 195 | ms |

Notes

34. Clock Fail detector available for PWM_en bit is set to logic [1] and CLOCK_sel is set to logic [0].
35. The PWM ratio is measured at $V_{HS}$ = 50% of $V_{PWR}$ and for the default SR value. It is possible to put the device fully-on (PWM duty-cycle 100%) and fully-off (duty-cycle 0%). For values outside this range, a calibration is needed between the PWM duty-cycle programming and the PWM on the output with $R_L$ = 5.0 Ω resistive load.

**Table 5. Dynamic Electrical Characteristics (continued)**

Characteristics noted under conditions 6.0 V ≤ $V_{PWR}$ ≤ 20 V, 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **TEMPERATURE ON THE GND FLAG** | | | | | |
| Thermal Prewarning Detection[36] | $T_{OTWAR}$ | 110 | 125 | 140 | °C |
| Analog Temperature Feedback at $T_A$ = 25 °C with $R_{CSNS}$ = 2.5 kΩ | $T_{FEED}$ | 1.15 | 1.20 | 1.25 | V |
| Analog Temperature Feedback Derating with $R_{CSNS}$ = 2.5 kΩ[37] | $DT_{FEED}$ | -3.5 | -3.7 | -3.9 | mV/°C |
| **SPI INTERFACE CHARACTERISTICS**[36] | | | | | |
| Maximum Frequency of SPI Operation | $f_{SPI}$ | – | – | 8.0 | MHz |
| Required Low State Duration for $\overline{RST}$[38] | $t_{W\overline{RST}}$ | 10 | – | – | µs |
| Rising Edge of $\overline{CS}$ to Falling Edge of $\overline{CS}$ (Required Setup Time)[39] | $t_{\overline{CS}}$ | – | – | 1.0 | µs |
| Rising Edge of $\overline{RST}$ to Falling Edge of $\overline{CS}$ (Required Setup Time)[39] | $t_{ENBL}$ | – | – | 5.0 | µs |
| Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (Required Setup Time)[39] | $t_{LEAD}$ | – | – | 500 | ns |
| Required High State Duration of SCLK (Required Setup Time)[39] | $t_{WSCLKh}$ | – | – | 50 | ns |
| Required Low State Duration of SCLK (Required Setup Time)[39] | $t_{WSCLKl}$ | – | – | 50 | ns |
| Falling Edge of SCLK to Rising Edge of $\overline{CS}$ (Required Setup Time)[39] | $t_{LAG}$ | – | – | 60 | ns |
| SI to Falling Edge of SCLK (Required Setup Time)[40] | $t_{SI(SU)}$ | – | – | 37 | ns |
| Falling Edge of SCLK to SI (Required Setup Time)[40] | $t_{SI(HOLD)}$ | – | – | 49 | ns |
| SO Rise Time<br>$C_L$ = 80 pF | $t_{RSO}$ | – | – | 13 | ns |
| SO Fall Time<br>$C_L$ = 80 pF | $t_{FSO}$ | – | – | 13 | ns |
| SI, $\overline{CS}$, SCLK, Incoming Signal Rise Time[40] | $t_{RSI}$ | – | – | 13 | ns |
| SI, $\overline{CS}$, SCLK, Incoming Signal Fall Time[40] | $t_{FSI}$ | – | – | 13 | ns |
| Time from Rising Edge of SCLK to SO Low Logic Level[41] | $t_{SO(EN)}$ | – | – | 60 | ns |
| Time from Rising Edge of SCLK to SO High Logic Level[42] | $t_{SO(DIS)}$ | – | – | 60 | ns |

Notes
36. Parameters guaranteed by design.
37. Value guaranteed per statistical analysis
38. $\overline{RST}$ low duration measured with outputs enabled and going to OFF or disabled condition.
39. Maximum setup time required for the 35XS3400 is the minimum guaranteed time needed from the microcontroller.
40. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
41. Time required for output status data to be available for use at SO. 1.0 kΩ on pull-up on $\overline{CS}$.
42. Time required for output status data to be terminated at SO. 1.0 kΩ on pull-up on $\overline{CS}$.

## TIMING DIAGRAMS

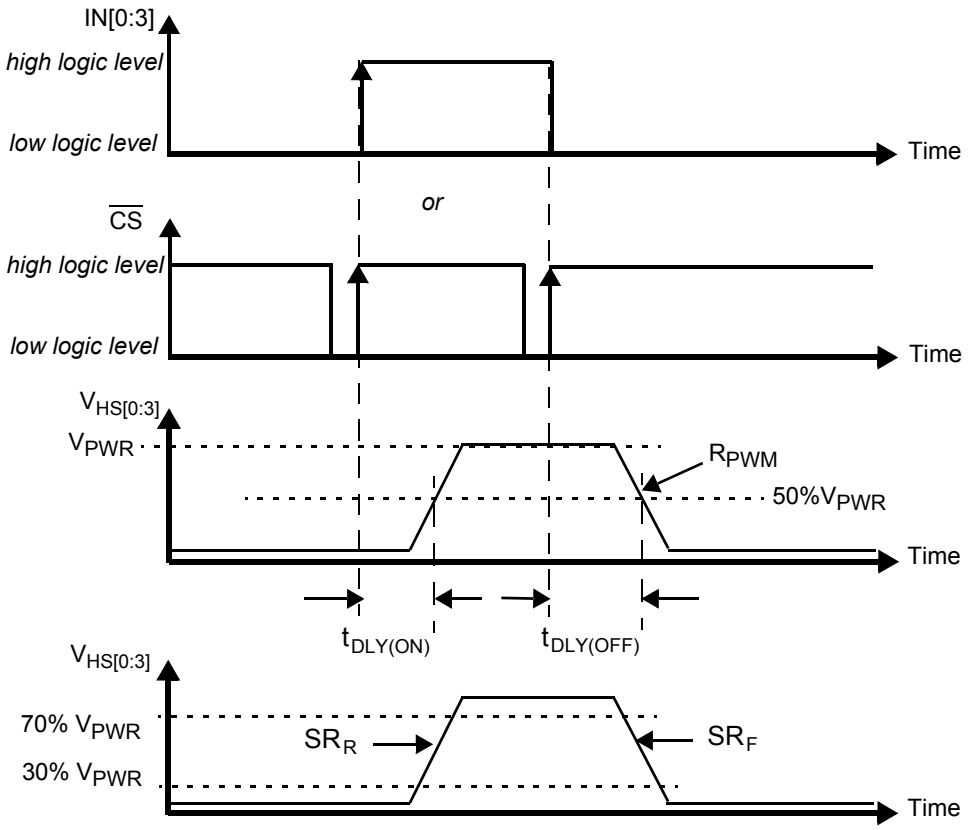



**Figure 4. Output Slew Rate and Time Delays**

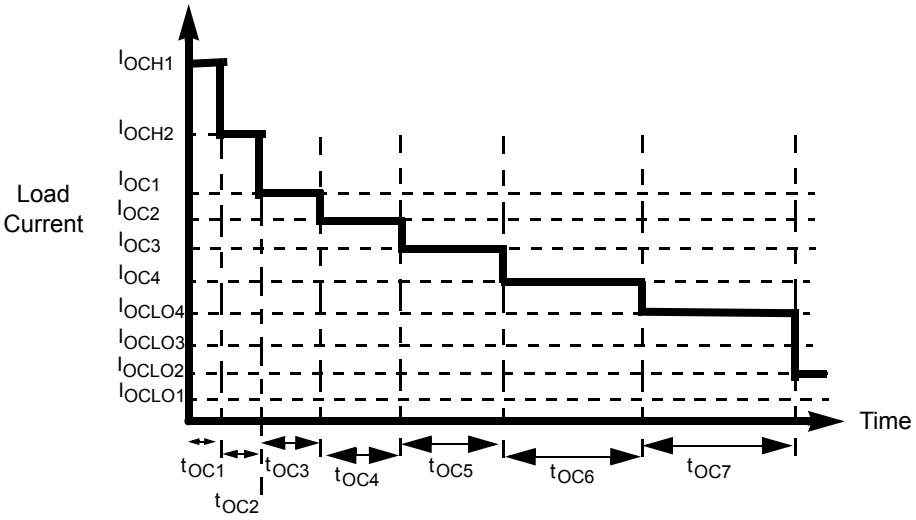



**Figure 5. Over-current Shutdown Protection**

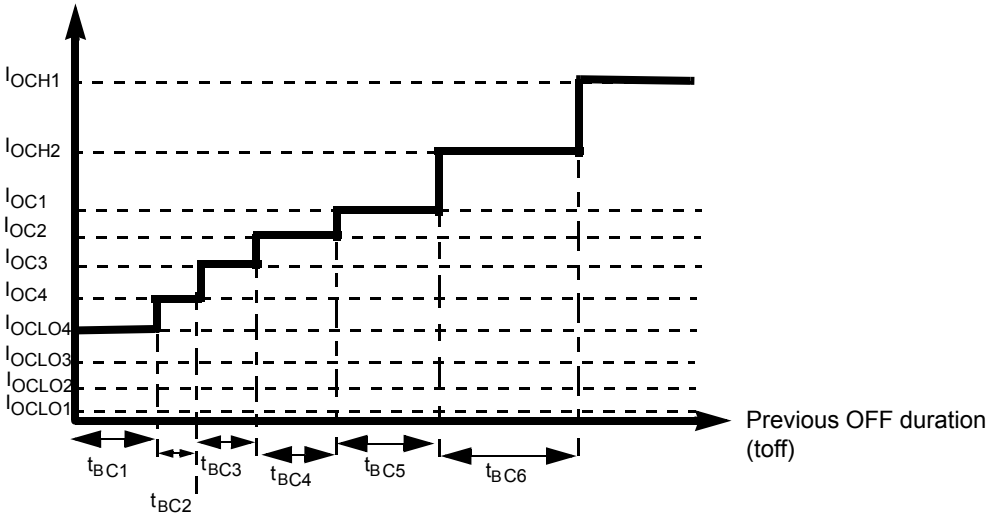



**Figure 6. Bulb Cooling Management**

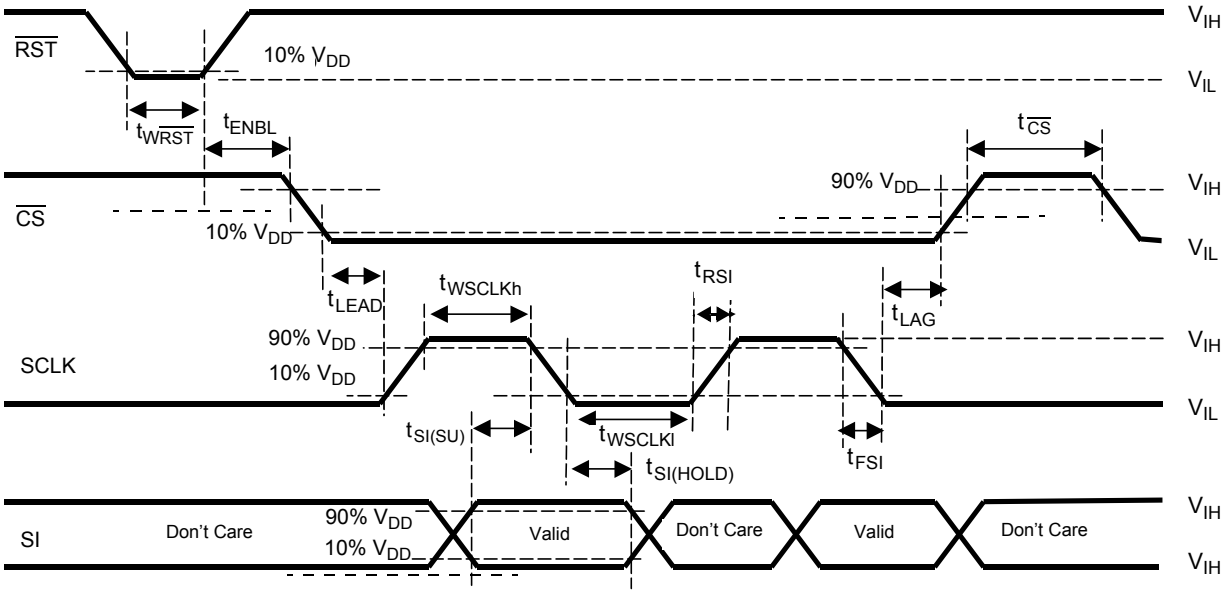



**Figure 7. Input Timing Switching Characteristics**

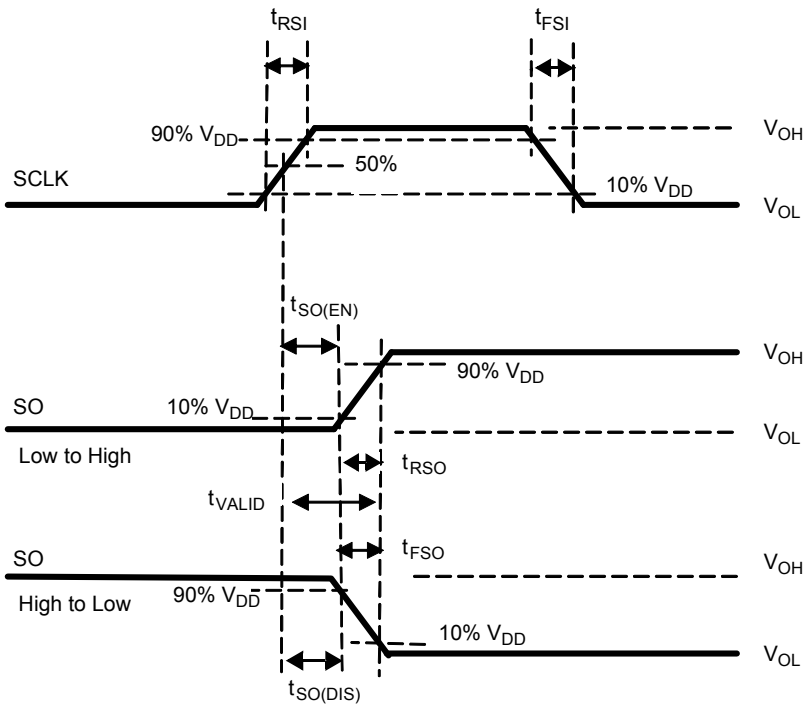



**Figure 8. SCLK Waveform and Valid SO Data Delay Time**

# FUNCTIONAL DESCRIPTION

## INTRODUCTION

The 35XS3400 is one in a family of devices designed for low-voltage automotive lighting applications. Its four low $R_{DS(ON)}$ MOSFETs (quad 35 mΩ) can control four separate 28 W bulbs.

Programming, control and diagnostics are accomplished using a 16-bit SPI interface. Its output with selectable slew-rate improves electromagnetic compatibility (EMC) behavior. Additionally, each output has its own parallel input or SPI control for pulse-width modulation (PWM) control if desired. The 35XS3400 allows the user to program via the SPI the fault current trip levels and duration of acceptable lamp inrush. The device has Fail-safe mode to provide functionality of the outputs in case of MCU damage.

## FUNCTIONAL PIN DESCRIPTION

### OUTPUT CURRENT MONITORING (CSNS)

The Current Sense pin provides a current proportional to the designated HS0:HS3 output or a voltage proportional to the temperature on the GND flag. That current is fed into a ground-referenced resistor (4.7 kΩ typical) and its voltage is monitored by an MCU's A/D. The output type is selected via the SPI. This pin can be tri-stated through the SPI.

### DIRECT INPUTS (IN0, IN1, IN2, IN3)

Each IN input wakes the device. The IN0:IN3 high side input pins are also used to directly control HS0:HS3 high side output pins. If the outputs are controlled by the PWM module, the external PWM clock is applied to IN0 pin. These pins are to be driven with CMOS levels, and they have a passive internal pull-down, $R_{DWN}$.

### FAULT STATUS ($\overline{FS}$)

This pin is an open drain configured output requiring an external pull-up resistor to $V_{DD}$ for fault reporting. If a device fault condition is detected, this pin is active LOW. Specific device diagnostics and faults are reported via the SPI SO pin.

### WAKE

The wake input wakes the device. An internal clamp protects this pin from high damaging voltages with a series resistor (10 kΩ typ). This input has a passive internal pull-down, $R_{DWN}$.

### RESET ($\overline{RST}$)

The reset input wakes the device. This is used to initialize the device configuration and fault registers, as well as place the device in a low-current Sleep mode. The pin also starts the watchdog timer when transitioning from logic [0] to logic [1]. This pin has a passive internal pull-down, $R_{DWN}$.

### CHIP SELECT ($\overline{CS}$)

The $\overline{CS}$ pin enables communication with the master microcontroller (MCU). When this pin is in a logic [0] state, the device is capable of transferring information to, and receiving information from, the MCU. The 35XS3400 latches in data from the input shift registers to the addressed registers on the rising edge of $\overline{CS}$. The device transfers status information from the power output to the Shift register on the falling edge of $\overline{CS}$. The SO output driver is enabled when $\overline{CS}$ is logic [0]. $\overline{CS}$ should transition from a logic [1] to a logic [0] state only when SCLK is a logic [0]. $\overline{CS}$ has an active internal pull-up from $V_{DD}$, $I_{UP}$.

### SERIAL CLOCK (SCLK)

The SCLK pin clocks the internal shift registers of the 35XS3400 device. The serial input (SI) pin accepts data into the input shift register on the falling edge of the SCLK signal while the serial output (SO) pin shifts data information out of the SO line driver on the rising edge of the SCLK signal. It is important the SCLK pin be in a logic low state whenever $\overline{CS}$ makes any transition. For this reason, it is recommended the SCLK pin be in a logic [0] whenever the device is not accessed ($\overline{CS}$ logic [1] state). SCLK has an active internal pull-down. When $\overline{CS}$ is logic [1], signals at the SCLK and SI pins are ignored and SO is tri-stated (high-impedance) (see Figure 9, page 22). SCLK input has an active internal pull-down, $I_{DWN}$.

### SERIAL INPUT (SI)

This is a serial interface (SI) command data input pin. Each SI bit is read on the falling edge of SCLK. A 16-bit stream of serial data is required on the SI pin, starting with D15 (MSB) to D0 (LSB). The internal registers of the 35XS3400 are configured and controlled using a 5-bit addressing scheme described in Table 10, page 29. Register addressing and configuration are described in Table 11, page 29. SI input has an active internal pull-down, $I_{DWN}$.

### DIGITAL DRAIN VOLTAGE (VDD)

This pin is an external voltage input pin used to supply power to the SPI circuit. In the event $V_{DD}$ is lost ($V_{DD}$ Failure), the device goes to Fail-safe mode.

### GROUND (GND)

These pins are the ground for the device.

### POSITIVE POWER SUPPLY (VPWR)

This pin connects to the positive power supply and is the source of operational power for the device. The VPWR contact is the backside surface mount tab of the package.

### SERIAL OUTPUT (SO)

The SO data pin is a tri-stateable output from the shift register. The SO pin remains in a high-impedance state until the $\overline{CS}$ pin is put into a logic [0] state. The SO data is capable of reporting the status of the output, the device configuration, the state of the key inputs, etc. The SO pin changes state on the rising edge of SCLK and reads out on the falling edge of SCLK. SO reporting descriptions are provided in Table 23, page 33.

### HIGH SIDE OUTPUTS (HS3, HS1, HS0, HS2)

Protected 35 mΩ high side power outputs to the load.

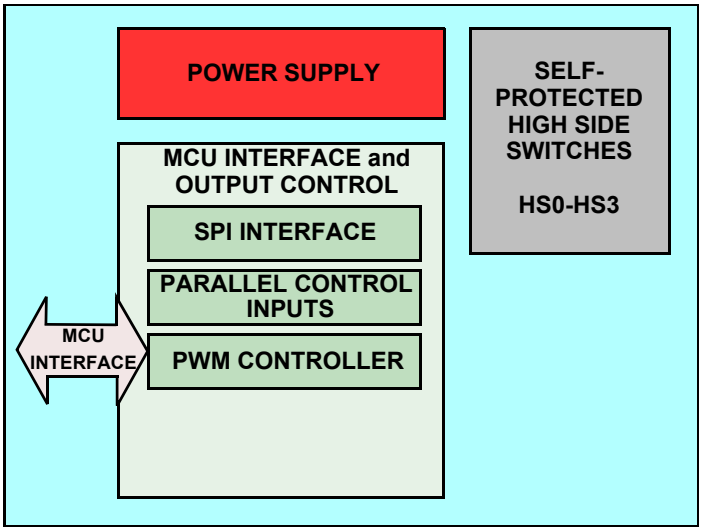
### FAIL-SAFE INPUT (FSI)

This pin incorporates an active internal pull-up current source from internal supply ($V_{REG}$). This enables the watchdog timeout feature.

When the FSI pin is opened, the watchdog circuit is enabled. After a watchdog timeout occurs, the output states depends on IN[0:3].

When the FSI pin is connected to GND, the watchdog circuit is disabled. The output states depends on IN[0:3] in case of $V_{DD}$ failure condition, in case $V_{DD}$ failure detection is activated (VDD_FAIL_en bit sets to logic [1]).

## FUNCTIONAL INTERNAL BLOCK DESCRIPTION




### POWER SUPPLY

The 35XS3400 is designed to operate from 4.0 to 28 V on the VPWR pin. Characteristics are provided from 6.0 to 20 V for the device. The VPWR pin supplies power to internal regulator, analog, and logic circuit blocks. The VDD supply is used for Serial Peripheral Interface (SPI) communication in order to configure and diagnose the device. This IC architecture provides a low quiescent current Sleep mode. Applying $V_{PWR}$ and $V_{DD}$ to the device will place the device in the Normal mode. The device will transit to Fail-safe mode in case of failures on the SPI or/and on the $V_{DD}$ voltage.

### HIGH SIDE SWITCHES: HS0 – HS3

These pins are the high side outputs controlling automotive lamps located for the rear of vehicle, such as 28 W bulbs and LED modules. 55 W/65 W lamps can be driven for two outputs shorted together. Those N-channel MOSFETs with 35 mΩ $R_{DS(ON)}$ are self-protected and present extended diagnostics in order to detect bulb outage and short-circuit fault condition. The HS output is actively clamped during turn off of inductive loads and inductive battery line.

When driving DC motor or solenoid loads demanding multiple switching, an external recirculation device must be used to maintain the device in its Safe Operating Area.

### MCU INTERFACE AND OUTPUT CONTROL

In Normal mode, each bulb is controlled directly from the MCU through SPI. A pulse width modulation control module allows improvement of lamp lifetime with bulb power

regulation (PWM frequency range from 100 to 400 Hz) and addressing the dimming application (day running light). An analog feedback output provides a current proportional to the load current or the temperature of the board. The SPI is used to configure and to read the diagnostic status (faults) of high side outputs. The reported fault conditions are: OpenLoad, short-circuit to battery, short-circuit to ground (over-current and severe short-circuit), thermal shutdown, and under/over-voltage. Thanks to accurate and configurable over-current detection circuitry and wire-harness optimization, the vehicle is lighter.

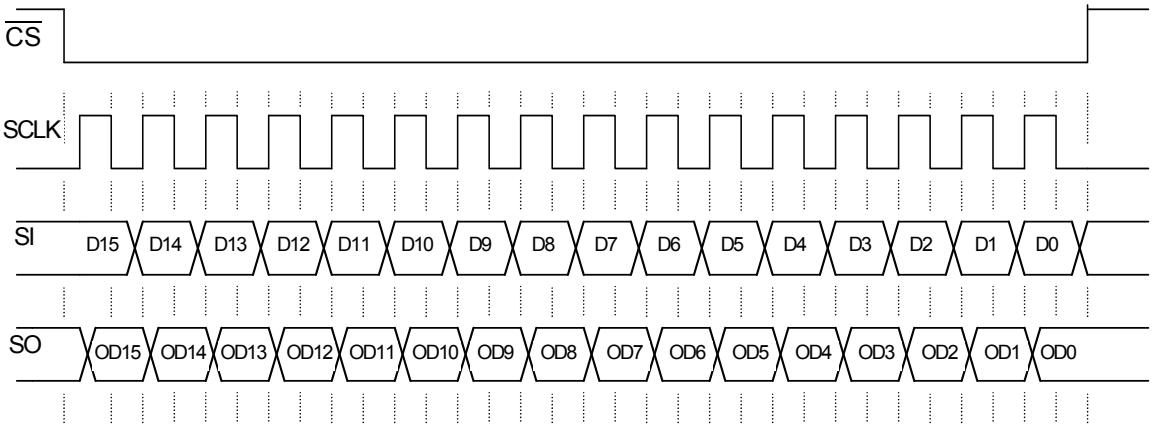
In Fail-safe mode, each lamp is controlled with dedicated parallel input pins. The device is configured in default mode.

# FUNCTIONAL DEVICE OPERATION

## SPI PROTOCOL DESCRIPTION

The SPI interface has a full duplex, three-wire synchronous data transfer with four I/O lines associated with it: Serial Input (SI), Serial Output (SO), Serial Clock (SCLK), and Chip Select ($\overline{CS}$).

The SI/SO pins of the 35XS3400 follow a first-in first-out (D15 to D0) protocol, with both input and output words transferring the most significant bit (MSB) first. All inputs are compatible with 5.0 V or 3.3 V CMOS logic levels.




Notes 1. $\overline{RST}$ is a logic [1] state during the above operation.
2. D15:D0 relate to the most recent ordered entry of data into the device.
3. OD15:OD0 relate to the first 16 bits of ordered fault and status data out of the device.

**Figure 9. Single 16-Bit Word SPI Communication**

## OPERATIONAL MODES

The 35XS3400 has four operating modes: Sleep, Normal, Fail-safe and Fault. Table 6 and Figure 11 summarize details contained in succeeding paragraphs.

The Figure 10 describes an internal signal called IN_ON[x] depending on IN[x] input.

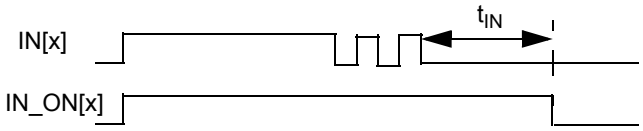



**Figure 10. IN_ON[x] internal signal**

The 35XS3400 transits to operating modes according to the following signals:

- wake-up = $\overline{RST}$ or WAKE or IN_ON[0] or IN_ON[1] or IN_ON[2] or IN_ON[3],
- fail = ($V_{DD}$ Failure and VDD_FAIL_en) or ( Watchdog time-out and FSI input not shorted to ground ),
- fault = OC[0:3] or OT[0:3] or SC[0:3] or UV ( UV ) or ( OV and $\overline{OV\_dis}$ ).

**Table 6. 35XS3400 Operating Modes**

| Mode | wake-up | fail | fault | Comments |
|---|---|---|---|---|
| Sleep | 0 | x | x | Device is in Sleep mode. All outputs are OFF. |
| Normal | 1 | 0 | 0 | Device is currently in Normal mode. Watchdog is active if enabled. |
| Fail-safe | 1 | 1 | 0 | Device is currently in Fail-safe mode due to watchdog timeout or $V_{DD}$ Failure conditions. The output states depend on the corresponding input in case FSI is open. |
| Fault | 1 | X | 1 | Device is currently in Fault mode. The faulted output(s) is (are) OFF. The safe autoretry circuitry is active to turn-on again the output(s). |

x = Don't care.

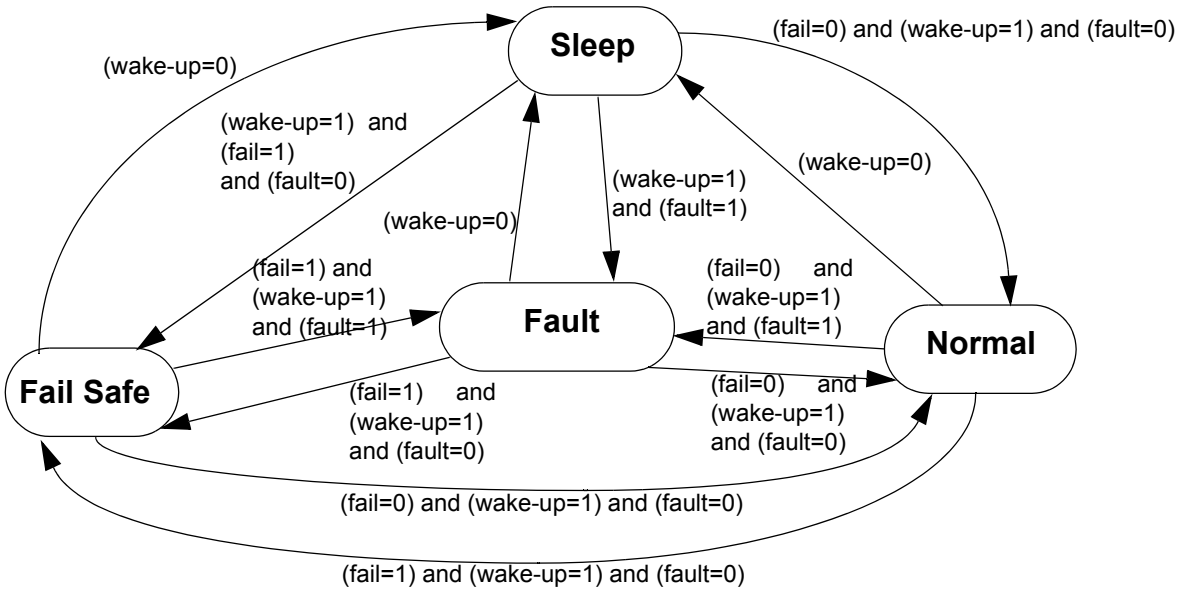



**Figure 11. Operating Modes**

## SLEEP MODE

The 35XS3400 is in Sleep mode when:

- $V_{PWR}$ and $V_{DD}$ are within the normal voltage range,
- wake-up = 0,
- fail = X,
- fault = X.

This is the Default mode of the device after first applying battery voltage (VPWR) prior to any I/O transitions. This is also the state of the device when the WAKE and $\overline{RST}$ and IN_ON[0:3] are logic [0]. In the Sleep mode, the output and all unused internal circuitry, such as the internal regulator, are off to minimize draw current. In addition, all SPI-configurable features of the device are as if set to logic [0].

## NORMAL MODE

The 35XS3400 is in Normal mode when:

- $V_{PWR}$ and $V_{DD}$ are within the normal voltage range,
- wake-up = 1,
- fail = 0,
- fault = 0.

In this mode, the NM bit is set to Ifault_contrologic [1] and the outputs HS[0:3] are under control, as defined by hson signal:

hson[x] = ( ( (IN[x] and $\overline{DIR\_dis}$[x]) or On bit[x] ) and PWM_en ) or (On bit [x] and Duty_cycle[x] and PWM_en).

In this mode and also in Fail-safe, the fault condition reset depends on fault_control signal, as defined below:

fault_control[x] = ( (IN_ON[x] and $\overline{DIR\_dis}$[x]) and PWM_en ) or (On bit [x]).

### Programmable PWM module

The outputs HS[0:3] are controlled by the programmable PWM module if PWM_en and On bits are set to logic [1].

The clock frequency from IN0 input pin or from internal clock is the factor $2^7$ (128) of the output PWM frequency (CLOCK_sel bit). The outputs HS[0:3] can be controlled in the range of 5% to 98% with a resolution of 7 bits of duty-cycle (Table 7). The state of other IN pin is ignored.

**Table 7. Output PWM Resolution**

| On bit | Duty-cycle | Output state |
|---|---|---|
| 0 | X | OFF |
| 1 | 0000000 | PWM (1/128 duty-cycle) |
| 1 | 0000001 | PWM (2/128 duty-cycle) |
| 1 | 0000010 | PWM (3/128 duty-cycle) |
| 1 | n | PWM ((n+1)/128 duty-cycle) |
| 1 | 1111111 | fully ON |

The timing includes seven programmable PWM switching delay (number of PWM clock rising edges) to improve overall EMC behavior of the light module (Table 8).

**Table 8. Output PWM Switching Delay**

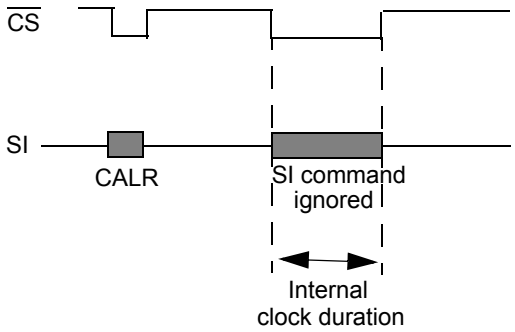
| Delay bits | Output delay |
|---|---|
| 000 | no delay |
| 001 | 16 PWM clock periods |
| 010 | 32 PWM clock periods |
| 011 | 48 PWM clock periods |
| 100 | 64 PWM clock periods |
| 101 | 80 PWM clock periods |
| 110 | 96 PWM clock periods |
| 111 | 112 PWM clock periods |

The clock frequency from IN0 is permanently monitored in order to report a clock failure in case of the frequency is out a specified frequency range (from $f_{IN0(LOW)}$ to $f_{IN0(HIGH)}$). In case of clock failure, no PWM feature is provided, the On bit defines the outputs state and the CLOCK_fail bit reports [1].

### Calibratable Internal Clock

The internal clock can vary as much as +/-30 percent corresponding to typical $f_{PWM(0)}$ output switching period.

Using the existing SPI inputs and the precision timing reference already available to the MCU, the 35XS3400 allows clock period setting within ±10 percent of accuracy. Calibrating the internal clock is initiated by defined word to CALR register. The calibration pulse is provided by the MCU. The pulse is sent on the $\overline{CS}$ pin after the SPI word is launched. At the moment, the $\overline{CS}$ pin transitions from logic [1] to [0] until from logic [0] to [1] determine the period of internal clock with a multiplicative factor of 128.




In case of negative $\overline{CS}$ pulse is outside a predefined time range (from $t_{CSB(MIN)}$ to $t_{CSB(MAX)}$), the calibration event will be ignored and the internal clock will be unaltered or reset to default value ($f_{PWM(0)}$) if this was not calibrated before.

The calibratable clock is used, instead of the clock from IN0 input, when CLOCK_sel is set to [1].

## FAIL-SAFE MODE

The 35XS3400 is in Fail-safe mode when:

- $V_{PWR}$ is within the normal voltage range,
- wake-up = 1,
- fail = 1,
- fault = 0.

### Watchdog

If the FSI input is not grounded, the watchdog timeout detection is active when either the WAKE or IN_ON[0:3] or $\overline{RST}$ input pin transitions from logic [0] to logic [1]. The WAKE input is capable of being pulled up to VPWR with a series of limiting resistance limiting the internal clamp current according to the specification.

The watchdog timeout is a multiple of an internal oscillator. As long as the WD bit (D15) of an incoming SPI message is toggled within the minimum watchdog timeout period (WDTO), the device will operate normally.

### Fail Safe Conditions

If an internal watchdog time-out occurs before the WD bit for FSI open (Table 9) or in case of $V_{DD}$ failure condition ($V_{DD}$< $V_{DD(FAIL)}$)) for VDD_FAIL_en bit is set to logic [1], the device will revert to a Fail-safe mode until the WD bit is written to logic [1] (see fail-safe to normal mode transition paragraph) and $V_{DD}$ is within the normal voltage range.

**Table 9. SPI Watchdog Activation**

| Typical RFSI (Ω) | Watchdog |
|---|---|
| 0 (shorted to ground) | Disabled |
| (open) | Enable |

During the Fail-safe mode, the outputs will depend on the corresponding input. The SPI register content is reset to their default value (except POR bit) and fault protections are fully operational.

The Fail-safe mode can be detected by monitoring the NM bit is set to [0].

## NORMAL & FAIL SAFE MODE TRANSITIONS

### Transition Fail-safe to Normal mode

To leave the Fail-safe mode, $V_{DD}$ must be in nominal voltage and the microcontroller has to send a SPI command with WDIN bit set to logic [1]; the other bits are not considered. The previous latched faults are reset by the transition into Normal mode (auto-retry included).

Moreover, the device can be brought out of the Fail-safe mode due to watchdog timeout issue by forcing the FSI pin to logic [0].

### Transition Normal to Fail-Safe Mode

To leave the Normal mode, a Fail-safe condition must occurred (fail=1). The previous latched faults are reset by the transition into Fail-safe mode (autoretry included).

## FAULT MODE

The 35XS3400 is in Fault mode when:

- $V_{PWR}$ and $V_{DD}$ are within the normal voltage range,
- wake-up = 1,
- fail = X,
- fault=1.

This device indicates the faults below as they occur by driving the $\overline{FS}$ pin to logic [0] for $\overline{RST}$ input is pulled up:

- Over-temperature fault,
- Over-current fault,
- Severe short-circuit fault,
- Output(s) shorted to VPWR fault in OFF state,
- OpenLoad fault in OFF state,
- Over-voltage fault (enabled by default),
- Under-voltage fault.

The $\overline{FS}$ pin will automatically return to logic [1] when the fault condition is removed, except for over-current, severe short-circuit, over-temperature and under-voltage which will be reset by a new turn-on command (each fault_control signal to be toggled).

Fault information is retained in the SPI fault register and is available (and reset) via the SO pin during the first valid SPI communication.

The OpenLoad fault in ON state is only reported through SPI register without effect on the corresponding output state (HS[x]) and the $\overline{FS}$ pin.

## START-UP SEQUENCE

The 35XS3400 enters in Normal mode after start-up if following sequence is provided:

- VPWR and VDD power supplies must be above their under-voltage thresholds,
- generate wake-up event (wake-up=1) from 0 to 1 on RSTB. The device switches to Normal mode with SPI register content is reset (as defined in Table 11 and Table 23). All features of 35XS3400 will be available after 50µs typical and all SPI registers are set to default values (set to logic [0]). The UV fault is reported in the SPI status registers.

And, in case of the PWM module is used (PWM_en bit is set to logic [1]) with an external reference clock:

- apply PWM clock on IN0 input pin after maximum 200 µs (min. 50 µs).

If the correct start-up sequence is not provided, the PWM function is not guaranteed.

# *PROTECTION AND DIAGNOSTIC FEATURES*

## PROTECTIONS

### Over-temperature Fault

The 35XS3400 incorporates over-temperature detection and shutdown circuitry for each output structure.

Two cases need to be considered when the output temperature is higher than $T_{SD}$:

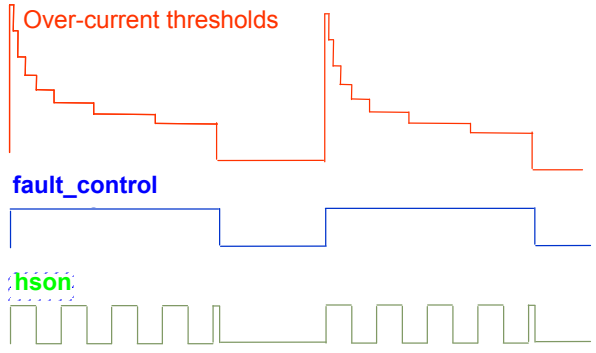
- If the output command is ON: the corresponding output is latched OFF. $\overline{FS}$ will be also latched to logic [0]. To delatch the fault and be able to turn ON again the outputs, the failure condition must disappear and the autoretry circuitry must be active or the corresponding output must be commanded OFF and then ON (toggling fault_control signal of corresponding output) or $V_{SUPPLY(POR)}$ condition if $V_{DD}$ = 0.
- If the output command is OFF: $\overline{FS}$ will go to logic [0] until the corresponding output temperature will be below $T_{SD}$.

For both cases, the fault register OT[0:3] bit into the status register will be set to [1]. The fault bits will be cleared in the status register after a SPI read command.

### Over-current Fault

The 35XS3400 incorporates output shutdown in order to protect each output structure against resistive short-circuit condition. This protection is composed by eight predefined current levels (time dependent) to fit 28 W bulb profiles.

In the first turn-on, the lamp filament is cold and the current will be huge. fault_control signal transition from logic [0] to [1] or an auto-retry define this event. In this case, the over-current protection will be fitted to inrush current, as shown in Figure 5. This over-current protection is programmable: OC[1:0] bits select over-current slope speed and OCHI1 current step can be removed in case the OCHI bit is set to [1].




In steady state, the wire harness will be protected by OCLO2 current level by default. Three other DC over-current levels are available: OCLO1 or OCLO3 or OCLO4 based on the state of the OCLO[1,0] bits.

If the load current level ever reaches the over-current detection level, the corresponding output will latch the output OFF and $\overline{FS}$ will be also latched to logic [0]. To delatch the fault and be able to turn ON again the corresponding output,