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Document Number: MC35XS3500
Rev. 7.0, 12/2012

RoHS

Smart Rear Corner Light Switch (Penta 35 mOhm)

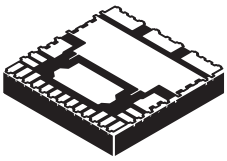
35XS3500

HIGH SIDE SWITCH

The 35XS3500 is designed for low-voltage automotive and industrial lighting applications. Its five low $R_{DS(ON)}$ MOSFETs (five 35 mΩ) can control the high sides of five separate resistive loads (bulbs and LEDs).

Programming, control and diagnostics are accomplished using a 16-bit SPI interface (3.3 V or 5.0 V). Each output has its own pulse-width modulation (PWM) control via the SPI. The 35XS3500 has highly sophisticated failure mode handling to provide high availability of the outputs. Its multiphase control and output edge shaping improves electromagnetic compatibility (EMC) behavior.

The 35XS3500 is packaged in a power-enhanced 12 x 12 mm nonleaded PQFN package with exposed tabs.



Bottom View

FK SUFFIX
98ART10511D
24-PIN PQFN
PB FREE

Features

- Penta 35 mΩ high side switches
- 16-bit SPI communication interface with daisy chain capability
- Current sense output with SPI-programmable multiplex switch and board temperature feedback
- Digital diagnosis feature
- PWM module with multiphase feature including prescaler
- LEDs control including accurate current sensing and low duty-cycle capability
- Fully protected switches
- Over-current shutdown detection
- Power net and reverse polarity protection
- Low-power mode
- Fail-safe mode functions including autorestart feature
- External smart power switch control including current recopy

ORDERING INFORMATION

Device (For Tape and Reel, Add R2 Suffix)	Temperature Range (T_A)	Package
MC35XS3500HFK	-40 to 125 °C	24 PQFN
* MC35XS3500DHFK		

* Recommended for all new designs

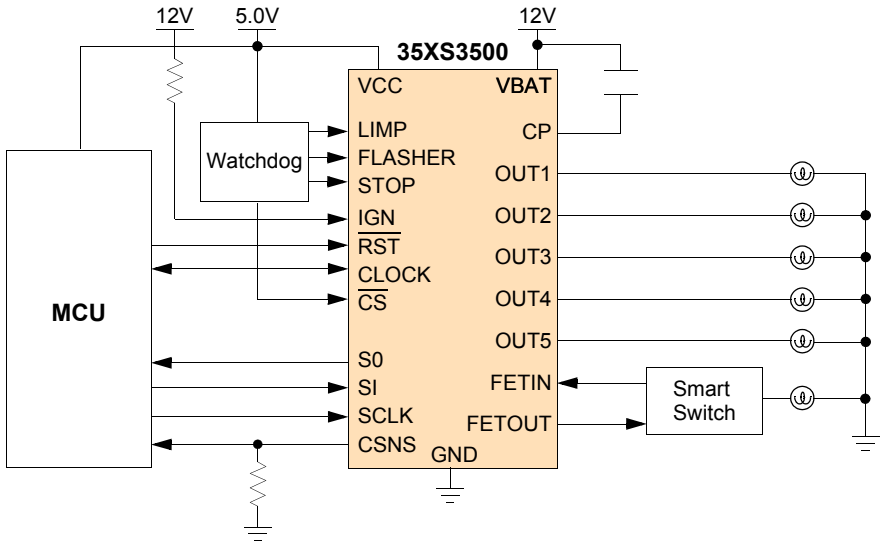


Figure 1. 35XS3500 Simplified Application Diagram

DEVICE VARIATIONS

Table 1. MC35XS3500 Device Variations

Part Number	Package	Temp.	Comment
MC35XS3500HFK	24 PQFN	-40 to 125 °C	Initial release
MC35XS3500DHFK			D version is more robust against V_{BAT} interrupt

INTERNAL BLOCK DIAGRAM

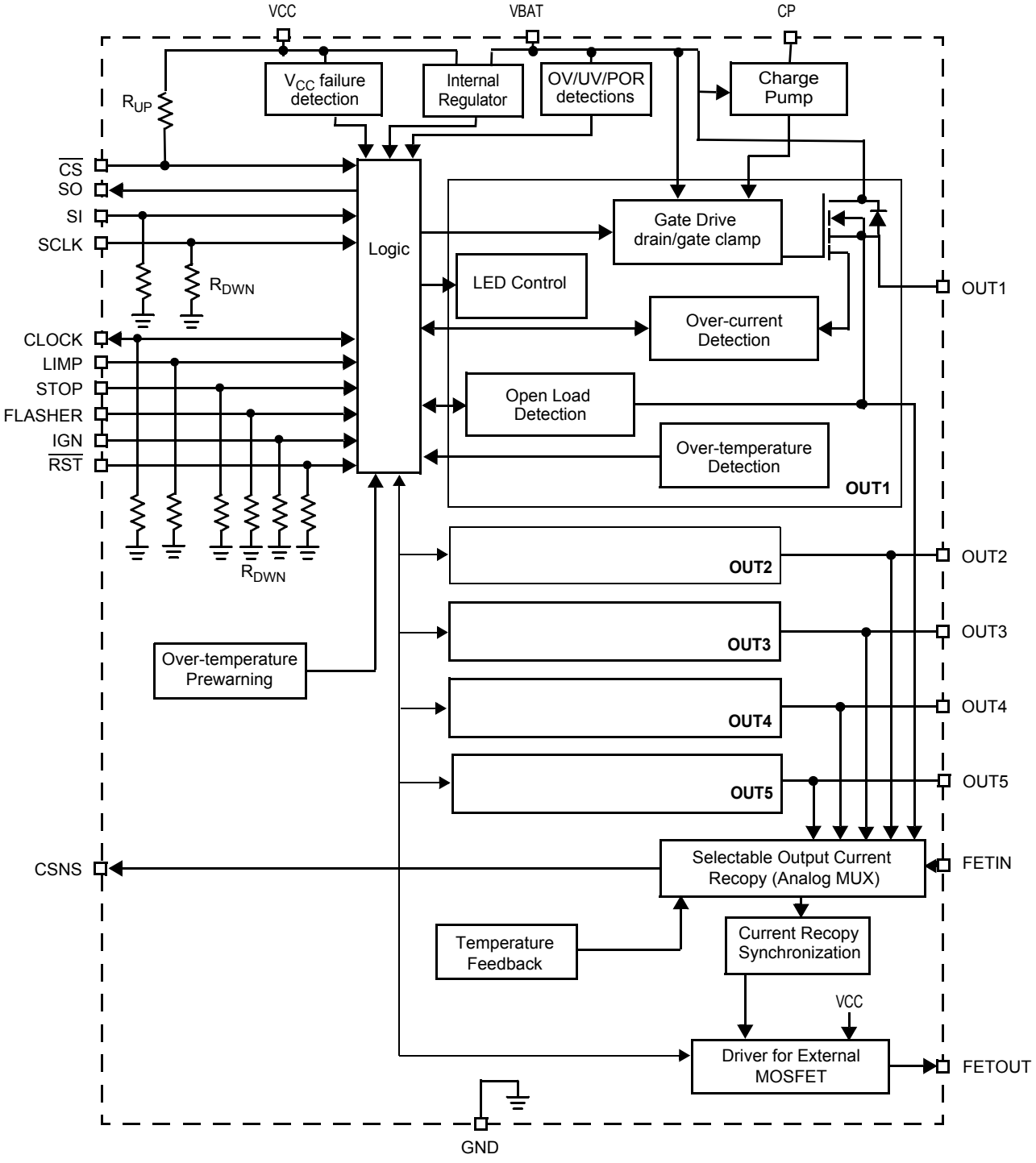


Figure 2. 35XS3500 Simplified Internal Block Diagram

PIN CONNECTIONS

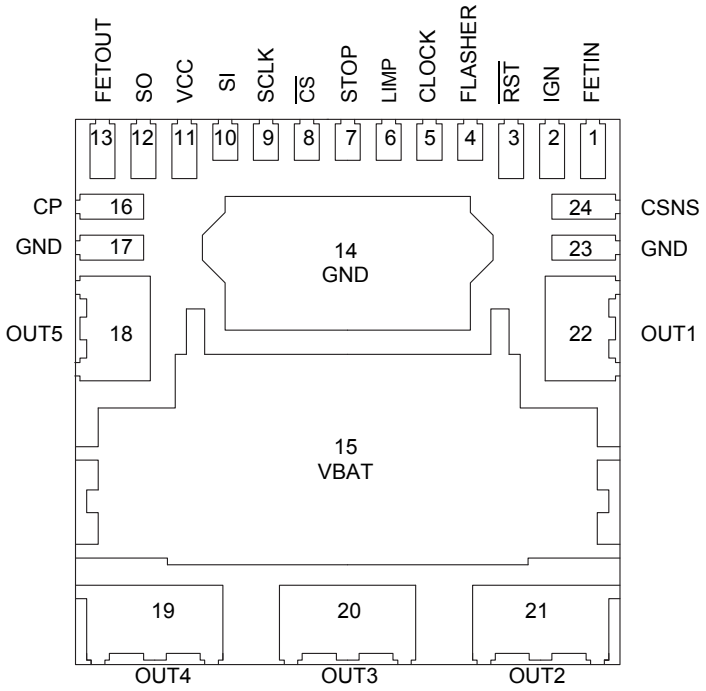


Figure 3. 35XS3500 Pin Connections (Transparent Package Top View)

Table 2. 35XS3500 Pin Definitions

Functional descriptions these pins can be found in the Functional Description section beginning on page 22.

Pin	Pin Name	Pin Function	Formal Name	Definition
1	FETIN	Input	External FET Input	This pin is the current sense recopy of the external MOSFET.
2	IGN	Input	Ignition Input (Active High)	This input wakes the device. It also controls outputs 1 and 2 in case of Fail mode activation. This pin has a passive internal pull-down.
3	$\overline{\text{RST}}$	Input	Reset	This input wakes the device. It is also used to initialize the device configuration and fault registers through the SPI. This pin has a passive internal pull-down.
4	FLASHER	Input	Flasher Input (Active High)	This input wakes the device. This pin has a passive internal pull-down.
5	CLOCK	Input	Clock Input	This pin state depends on $\overline{\text{RST}}$ logic level. As long as $\overline{\text{RST}}$ input pin is set to logic [0], this pin is pulled up in order to report wake event. Otherwise, the PWM frequency and timing are generated from this digital clock input by the PWM module. This pin has a passive internal pull-down.
6	LIMP	Input	Limp Home Input (Active High)	The Fail mode can be activated by this digital input. This pin has an active internal pull-down current source.
7	STOP	Input	Stop Light Input (Active High)	This input wakes the device. This pin has a passive internal pull-down.
8	$\overline{\text{CS}}$	Input	Chip Select (Active Low)	When this signal is high, SPI signals are ignored. Asserting this pin low starts a SPI transaction. The transaction is signaled as completed when this signal returns high. This pin has a passive internal pull-up resistance.

Table 2. 35XS3500 Pin Definitions (continued)

Functional descriptions these pins can be found in the Functional Description section beginning on page 22.

Pin	Pin Name	Pin Function	Formal Name	Definition
9	SCLK	Input	SPI Clock Input	This input pin is connected to the master microcontroller providing the required bit shift clock for SPI communication. This pin has a passive internal pull-down resistance.
10	SI	Input	Master-Out Slave-In	This data input is sampled on the positive edge of the SCLK. This pin has a passive internal pull-down resistance.
11	VCC	Input	Logic Supply	SPI Logic power supply.
12	SO	Output	Master-In Slave-Out	SPI data sent to the MCU by this pin. This data output changes on the negative edge of SCLK, and when $\overline{CS}$ is high. This pin is high-impedance.
13	FETOUT	Output	External FET Gate	This pin controls an external SMART MOSFET by logic level. This output called OUT6. If OUT6 is not used in the application, this output pin is set to logic high when the current sense output becomes valid when CSNS sync SPI bit is set to logic [1].
14, 17, 23	GND	Ground	Ground	This pin is the ground for the logic and analog circuitry of the device.(1)
15	VBAT	Input	Battery Input	Power supply pin.
16	CP	Output	Charge Pump	This pin is the connection for an external tank capacitor (for internal use only).
18 19 20 21 22	OUT5 OUT4 OUT3 OUT2 OUT1	Output Output Output Output Output	Output 5 Output 4 Output 3 Output 2 Output 1	Protected 35 mΩ high side power output to the load.
24	CSNS	Output	Current Sense Output	This pin is used to output a current proportional to OUT1:OUT5, FETin current, and it is used externally to generate a ground-referenced voltage for the microcontroller to monitor output current. Moreover, this pin can report a voltage proportional to the temperature on the GND flag. OUT1:OUT5, FETin current sensing and Temperature feedback choice is SPI programmable.

Notes

1. The pins 14, 17, and 23 must be shorted on the board.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Over-voltage Test Range Maximum Operation Voltage Load Dump (400 ms) at 25 °C	V_{BAT}	 28 40	V
Reverse Polarity Voltage Range 2.0 Min at 25 °C	V_{BAT}	 -18	V
VCC Supply Voltage	V_{CC}	-0.3 to 5.5	V
Output Voltage Positive Negative (ground disconnected)	V_{OUT}	 40 -16	V
Digital Input Current in Clamping Mode (SI, SCLK, $\overline{CS}$, IGN, FLASHER, STOP, LIMP)	I_{IN}	±1.0	mA
FETIN Input Current	I_{FETIN}	+10 -1.0	mA
SO and FETOUT Output Voltage	V_{SO}	-0.3 to V_{CC}+0.3	V
Outputs clamp energy using single pulse method (L = 2.0 mH; R = 0 Ω; VBAT = 14 V at 150 °C initial)	E	30	mJ
ESD Voltage[2] Human Body Model (HBM) OUT[1:5], VPWR, and GND Charge Device Model (CDM) Corner Pins (1,13,19,21) All Other Pins (2-12, 14-18, 20, 22-24)	V_{ESD}	 ±2000 ±8000 ±750 ±500	V
THERMAL RATINGS			
Operating Temperature Ambient Junction	 T_A T_J	 -40 to 125 -40 to 150	°C
Peak Package Reflow Temperature During Reflow[3], [4]	T_{PPRT}	Note 4	°C
Storage Temperature	T_{STG}	-55 to 150	°C
THERMAL RESISTANCE			
Thermal Resistance, Junction to Case[5]	$R_{\theta JC}$	1.0	°C/W

Notes

2. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω) and the Charge Device Model.
3. Pin soldering temperature limit is for 40 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
4. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
5. Typical value is guaranteed per design.

STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT (VBAT, VCC)					
Battery Supply Voltage Range	V_{BAT}				V
Full Performance and Short-circuit		7.0	–	20	
Extended Voltage Range[6]		6.0	–	28	
Battery Supply Under-voltage (UV flag is set ON)	V_{BATUV}	5.0	5.5	6.0	V
Battery Voltage Clamp (OV flag is set ON)	$V_{BATCLAMP\_OV}$	27.5	30	32.5	V
Battery Voltage Clamp	$V_{BATCLAMP}$	40	–	48	V
Battery Supply Power on Reset[9]					V
If V_{BAT} < 5.5 V, V_{BAT} = V_{CC}	$V_{BATPOR1}$	2.0	–	3.0	
If V_{BAT} < 5.5 V, V_{BAT} = 0	$V_{BATPOR2}$	2.0	–	4.0	
VBAT Supply Current at 25 °C and V_{BAT} =12 V and V_{CC} = 5.0 V					
Sleep State Current, Outputs Open	$I_{BATSLEEP1}$	–	0.5	5.0	µA
Sleep State Current, Outputs Grounded	$I_{BATSLEEP2}$	–	0.5	5.0	µA
Normal Mode, IGN = 5.0 V, $\overline{RST}$ = 5.0 V, Outputs Open	I_{BAT}	–	10	20	mA
Digital Voltage Range, Full Performance	V_{CC}	3.0	–	5.5	V
Digital Supply Under-voltage (V_{CC} Failure)	V_{CCUV}	2.2	2.5	2.8	V
Sleep Current Consumption on V_{CC} at 25 °C and V_{BAT} = 12 V	$I_{CCSLEEP}$				µA
Output OFF		–	0.2	5.0	
Supply Current Consumption on V_{CC} and V_{BAT} = 12 V	I_{CC}				mA
No SPI		–	–	2.6	
3.0 MHz SPI Communication		–	–	5.0	
LOGIC INPUT/OUTPUT (IGN, $\overline{CS}$, CSNS, SI, SCLK, CLOCK, SO, FLASHER, $\overline{RST}$, LIMP, STOP)					
Input High Logic Level[7]	V_{IH}	2.0	–	–	V
Input Low Logic Level[7]	V_{IL}	–	–	0.8	V
Ignition Threshold Level (IGN, FLASHER, STOP and $\overline{RST}$)	V_{IGNTH}	1.0		2.2	V
Input Clamp Voltage (IGN, FLASHER, LIMP, STOP, $\overline{CS}$, SCLK, SI, $\overline{RST}$)	V_{CL_POS}				V
I = 1.0 mA		7.5	–	13	
Input Forward Voltage (IGN, FLASHER, LIMP, STOP, $\overline{CS}$, SCLK, SI, $\overline{RST}$)	V_{CL_NEG}				V
I = 1.0 mA		-2.0	–	-0.3	
Input Passive Pull-up Resistance on $\overline{CS}$ pin[8]	R_{UP}	100	200	400	kΩ
Input Passive Pull-down Resistance on SI, SCLK, FLASHER, IGN, FOG, CLOCK, LIMP and $\overline{RST}$ pins[8]	R_{DWN}	100	200	500	kΩ
SO High-state Output Voltage	V_{SOH}				V_{CC}
I_{OH} = 1.0 mA		0.8	0.95	–	
CLOCK Output Voltage reporting wake-up event (I_{CLOCK}=1.0 mA)	V_{CLOCKH}	0.8	0.95	–	V_{CC}

Notes

6. In extended mode, the functionality is guaranteed but not the electrical parameters.
7. Valid for $\overline{RST}$, SI, SCLK, CLOCK, FLASHER, STOP, and LIMP pins.
8. Valid for the following input voltage range: VCC = -0.3 to +0.3 V.
9. Please refer to Loss of VBAT section for more details.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INPUT/OUTPUT (IGN, $\overline{CS}$, CSNS, SI, SCLK, CLOCK, SO, FLASHER, $\overline{RST}$, LIMP, STOP) (CONTINUED)					
SO Low-state Output Voltage I_{OL} = -1.6 mA	V_{SOL}	–	0.2	0.4	V
SO Tri-state Leakage Current $\overline{CS} \geq 0.7\ V_{CC}$	I_{SOLEAK}	-1.0	0.0	1.0	µA
CSNS Tri-state Leakage Current VCC = 5.5 V, CSNS = 5.5 V VCC = 5.0 V, CSNS = 5.5 V VCC = 5.0 V, CSNS = 4.5 V	$I_{CSNSLEAK}$	 -5.0 -10 -1.0	 0.0 0.0 0.0	 1.0 1.0 1.0	µA
Current Sense Output Clamp Voltage I_{CSNS} < 10.0 mA	V_{CSNS}	5.0	6.0	7.0	V
OUTPUT (OUT 1:5)					
Output Leakage Current in OFF state Sleep mode, Outputs Grounded Normal mode, Outputs Grounded	$I_{OUTLEAK}$	 – –	 0 20	 2.0 25	µA
Output Negative Clamp Voltage I_{OUT} = -500 mA, Outputs OFF	V_{OUT}	-22	–	-16	V
Current Sense Output Precision[10] Full-Scale Range (FSR) for LED Control bit = 0 0.75 FSR 0.50 FSR 0.25 FSR 0.10 FSR Full-Scale Range (FSR) for LED Control bit = 1 0.187 FSR = 0.75 FSR_{LED} 0.125 FSR = 0.50 FSR_{LED} 0.062 FSR = 0.25 FSR_{LED} 0.025 FSR = 0.10 FSR_{LED}	$\delta I_{CS}/I_{CS}$	 -14 -15 -17 -22 -13 -13 -20 -30	 - - - - - - - -	 14 15 17 22 13 13 20 30	%
Current Sense Output Precision Over-temperature Range [-40;125 °C], V_{BAT} Range [10 V-16 V] and FSR Range [25%-100%], calculated with one calibration point (Taken at 25 °C, VBAT = 13.5 V and 50% FSR)[12]		-6.0	-	6.0	%
Current Sense Output Precision with one calibration point (50% FSR_{LED}, V_{BAT} = 13.5 at 25 °C[12]		-6.0	–	6.0	%
Temperature Drift of Current Sense Output[11] V_{BAT} = 13.5 V, I_{OUT} = 2.8 A reference taken at T_A = 25 °C	$\Delta I_{CS}/\Delta T$	–	±280	±400	ppm/°C
Minimum Output Current Reported in CSNS for OUT[1-5][13] 10 V ≤ VBAT ≤ 16 V	$I_{35MIN(CSNS)}$	65	–	–	mA
Minimum Output Current Reported in CSNS for OUT[1-5] in LED Mode[13] 10 V ≤ VBAT ≤ 16 V	$I_{35MIN(CSNS)\ LED}$	40	–	–	mA

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit

Notes

10. 10 V < V_{BAT} < 16 V. ($\delta I_{CS}/I_{CS}$ = (measured I_{CS}- targeted I_{CS})/ targeted I_{CS} with targeted I_{CS} = 5.0 mA
11. Based on statistical data. Not production tested. $\Delta I_{CS}/\Delta T$ = [(measured at I_{CS} at T_1 - measured at I_{CS} at T_2) measured at I_{CS} at room]/ (T_1 - T_2)
12. Based on statistical analysis covering 99.74% of parts.
13. Output current value computed after leakage current removal (open load condition)

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT (OUT 1:5) (CONTINUED)					
Over-temperature Shutdown	T_{OTS}	155	175	195	°C
Thermal Prewarning[14]	$T_{OTSWARN}$	110	125	140	°C
Output Voltage Threshold	V_{OUT_TH}	0.475	0.5	0.525	V_{BAT}
TAIL LIGHT (OUT1)					
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, T_A = 25 °C) V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)}$	 – –	 – –	 35 55	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, V_{BAT} = 13.5 V, T_A = 150 °C)[14]	$R_{DS(ON)}$	–	–	59.5	mΩ
Reverse Output ON Resistance (I_{OUT} = -2.8 A, V_{BAT} = -12 V, T_A = 25 °C)[15]	$R_{SD(ON)}$	–	–	70	mΩ
TAIL LIGHT (OUT1)					
Output Drain-to-Source ON Resistance (I_{OUT} = 1.5 A, T_A = 25 °C) for LED Control = 1 V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25\_LED}$	 – –	 – –	 70 110	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 1.5 A, V_{BAT} = 13.5 V, T_A = 150 °C) for LED Control = 1	$R_{DS(ON)150\_LED}$	–	–	119	mΩ
High Over-current Shutdown Threshold 1 V_{BAT} = 16 V, T_A = -40 °C V_{BAT} = 16 V, T_A = 25 °C V_{BAT} = 16 V, T_A = 125 °C	I_{OCHI1}	28.0 30.2 29.4 28.3	35.0 36.0 35.0 33.8	43.5 41.8 40.6 39.3	A
High Over-current Shutdown Threshold 2	I_{OCHI2}	12.3	15.4	18.5	A
Low Over-current Shutdown Threshold	I_{OCLO}	5.7	7.2	8.9	A
Open Load Current Threshold in ON State[16]	I_{OL}	0.05	0.2	0.5	A
Open Load Current Threshold in ON State with LED[17] V_{OL} = V_{BAT} - 0.5 V	I_{OLLED}	4.0	10	20	mA
Current Sense Full-scale Range[18]	$I_{CS\ FSR}$	–	6.0	–	A
Current Sense Full-scale Range[14] depending on LED Control = 1	$I_{CS\ FSR\_LED}$	–	1.6	–	A
Severe Short-circuit Impedance Range[14]	$R_{SC1(OUT1)}$	350	–	–	mΩ

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit

Notes

14. Parameter guaranteed by design; however it is not production tested.
15. Source-to-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{BAT}.
16. OLLED1, bit D0 in SI data is set to [0]
17. OLLED1, bit D0 in SI data is set to [1]
18. For a typical value of $I_{CS\ FSR,}$ I_{CSNS} = 5.0 mA. If the range is exceeded, no current clamp and the precision is not guaranteed.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LICENSE LIGHT (OUT2)					
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, T_A = 25 °C) V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)}$	 – –	 – –	 35 55	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = -2.8 A, V_{BAT} = -13.5 V, T_A = 25 °C)[19]	$R_{DS(ON)}$	–	–	59.5	mΩ
Reverse Output ON Resistance (I_{OUT} = 2.8 A, V_{BAT} = 12 V, T_A = 150 °C)[20]	$R_{SD(ON)}$	–	–	70	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} =1.5 A, T_A = 25 °C) for LED Control = 1 V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25\_LED}$	 – –	 – –	 70 110	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 1.5 A, V_{BAT} = 13.5 V, T_A = 150 °C) for LED Control = 1	$R_{DS(ON)150\_LED}$	–	–	119	mΩ
High Over-current Shutdown Threshold 1 V_{BAT} = 16 V, T_A = -40 °C V_{BAT} = 16 V, T_A = 25 °C V_{BAT} = 16 V, T_A = 125 °C	I_{OCHI1}	28.0 30.2 29.4 28.3	35.0 36.0 35.0 33.8	43.5 41.8 40.6 39.3	A
High Over-current Shutdown Threshold 2	I_{OCHI2}	12.3	15.4	18.5	A
Low Over-current Shutdown Threshold	I_{OCLO}	5.7	7.2	8.9	A
Open Load Current Threshold in ON State[21]	I_{OL}	0.05	0.2	0.5	A
Open Load Current Threshold in ON State with LED[22] V_{OL} = V_{BAT} - 0.5 V	I_{OLLED}	4.0	10	20	mA
Current Sense Full-Scale Range[23]	$I_{CS\ FSR}$	–	6.0	–	A
Current Sense Full-Scale Range[19] depending on LED Control = 1	$I_{CS\ FSR\_LED}$	–	1.6	–	A
Severe short-circuit impedance range[19]	$R_{SC1(OUT2)}$	350	–	–	mΩ

Notes

19. Parameter guaranteed by design; however, it is not production tested.
20. Source-to-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{BAT}.
21. OLLED2, bit D0 in SI data is set to [0]
22. OLLED2, bit D0 in SI data is set to [1]
23. For typical value of $I_{CS\ FSR}$, I_{CSNS} = 5.0 mA. If the range is exceeded, no current clamp and the precision is not guaranteed.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
TAIL LIGHT (OUT3)					
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, T_A = 25 °C) V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25}$	 – –	 – –	 35 55	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, V_{BAT} = 13.5 V, T_A = 150 °C)[24]	$R_{DS(ON)150}$	–	–	59.5	mΩ
Reverse Source-to-Drain ON Resistance (I_{OUT} = -2.8 A, V_{BAT} = -12 V, T_A = 25 °C)[25]	$R_{SD(ON)25}$	–	–	70	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 1.5 A, T_A = 25 °C) for LED Control = 1 V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25\_LED}$	 – –	 – –	 70 110	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 1.5 A, V_{BAT} = 13.5 V, T_A = 150 °C) for LED Control = 1	$R_{DS(ON)150\_LED}$	–	–	119	mΩ
High Over Current Shutdown Threshold 1 V_{BAT} = 16 V, T_A = -40 °C V_{BAT} = 16 V, T_A = 25 °C V_{BAT} = 16 V, T_A = 125 °C	I_{OCHI1}	28.0 30.2 29.4 28.3	35.0 36.0 35.0 33.8	43.5 41.8 40.6 39.3	A
High Over-current Shutdown Threshold 2	I_{OCHI2}	12.3	15.4	18.5	A
Low Over-current Shutdown Threshold	I_{OCLO}	5.7	7.2	8.9	A
Open Load Current Threshold in ON State[26]	I_{OL}	0.05	0.2	0.5	A
Open Load Current Threshold in ON State with LED[27] V_{OL} = V_{BAT} - 0.5 V	I_{OLLED}	 4.0	 10	 20	mA
Current Sense Full-scale Range[28]	$I_{CS\ FSR}$	–	6.0	–	A
Current Sense Full-scale Range[24] depending on LED Control = 1	$I_{CS\ FSR\_LED}$	–	1.6	–	A
Severe short-circuit impedance range[24]	$R_{SC1(OUT3)}$	350	–	–	mΩ

Notes

24. Parameter guaranteed by design; however, it is not production tested.
25. Source-to-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{BAT}.
26. OLLED3, bit D2 in SI data is set to [0]
27. OLLED3, bit D2 in SI data is set to [1]
28. For a typical value of $I_{CS\ FSR}$, I_{CSNS} = 5.0 mA. If the range is exceeded, no current clamp and the precision is not guaranteed.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
STOP LIGHT (OUT4)					
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, T_A = 25 °C) V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25}$	 – –	 – –	 35 55	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, V_{BAT} = 13.5 V, T_A = 150 °C)[29]	$R_{DS(ON)150}$	–	–	59.5	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 1.5 A, T_A = 25 °C) for LED Control = 1 V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25\_LED}$	 – –	 – –	 70 110	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} =1.5 A, V_{BAT} = 13.5 V, T_A = 150 °C) for LED Control = 1	$R_{DS(ON)150\_LED}$	–	–	119	mΩ
Reverse Source-to-Drain ON Resistance (I_{OUT} = -2.8 A, V_{BAT} = -12 V, T_A = 25 °C)[30]	$R_{DS(ON)25}$	–	–	70	mΩ
High Over-current Shutdown Threshold 1 V_{BAT} = 16 V, T_A = -40 °C V_{BAT} = 16 V, T_A = 25 °C V_{BAT} = 16 V, T_A = 125 °C	I_{OCHI1}	28.0 30.2 29.4 28.3	35.0 36.0 35.0 33.8	43.5 41.8 40.6 39.3	A
High Over-current Shutdown Threshold 2	I_{OCHI2}	12.3	15.4	18.5	A
Low Over-current Shutdown Threshold	I_{OCLO}	5.7	7.2	8.9	A
Open Load Current Threshold in ON State[31]	I_{OL}	0.05	0.2	0.5	A
Open Load Current Threshold in ON State with LED[32] V_{OL} = V_{BAT} - 0.5 V	I_{OLLED}	4.0	10	20	mA
Current Sense Full-scale Range[33]	$I_{CS\ FSR}$	–	6.0	–	A
Current Sense Full-scale Range[29] depending on LED Control = 1	$I_{CS\ FSR\_LED}$	–	1.6	–	A
Severe Short-circuit Impedance Range[29]	$R_{SC1(OUT4)}$	350			mΩ

Notes
29. Parameter guaranteed by design; however, it is not production tested.
30. Source-to-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{BAT}.
31. OLLED3, bit D2 in SI data is set to [0]
32. OLLED3, bit D2 in SI data is set to [1]
33. For a typical value of $I_{CS\ FSR}$, I_{CSNS} = 5.0 mA. If the range is exceeded, no current clamp and the precision is not guaranteed.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
FLASHER (OUT5)					
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, T_A = 25 °C) V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25}$	 – –	 – –	 35 55	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, V_{BAT} = 13.5 V, T_A = 150 °C)[34]	$R_{DS(ON)150}$	–	–	59.5	mΩ
Reverse Source-to-Drain ON Resistance (I_{OUT} = -2.8 A, V_{BAT} = -12 V, T_A = 25 °C)[35]	$R_{SD(ON)25}$	–	–	70	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} =1.5 A, T_A = 25 °C) for LED Control = 1 V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25\_LED}$	 – –	 – –	 70 110	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 1.5 A, V_{BAT} = 13.5 V, T_A = 150 °C) for LED Control = 1	$R_{DS(ON)150\_LED}$	–	–	119	mΩ
High Over-current Shutdown Threshold 1 V_{BAT} = 16 V, T_A = -40 °C V_{BAT} = 16 V, T_A = 25 °C V_{BAT} = 16 V, T_A = 125 °C	I_{OCHI1}	28.0 30.2 29.4 28.3	35.0 36.0 35.0 33.8	43.5 41.8 40.6 39.3	A
High Over-current Shutdown Threshold 2	I_{OCHI2}	12.3	15.4	18.5	A
Low Over-current Shutdown Threshold	I_{OCLO}	5.7	7.2	8.9	A
Open Load Current Threshold in ON State[36]	I_{OL}	0.05	0.2	0.5	A
Open Load Current Threshold in ON State with LED[37] V_{OL} = V_{BAT} - 0.5 V	I_{OLLED}	4.0	10	20	mA
Current Sense Full-scale Range[38]	$I_{CS\ FSR}$	–	6.0	–	A
Current Sense Full-scale Range[34] depending on LED Control = 1	$I_{CS\ FSR\_LED}$	–	1.6	–	A
Severe Short-circuit Impedance Range[34]	$R_{SC1(OUT5)}$	350	–	–	mΩ

Notes

34. Parameter guaranteed by design; however, it is not production tested.
35. Source-to-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{BAT}.
36. OLLED3, bit D2 in SI data is set to [0]
37. OLLED3, bit D2 in SI data is set to [1]
38. For a typical value of $I_{CS\ FSR}$, I_{CSNS} = 5.0 mA. If the range is exceeded, no current clamp and the precision is not guaranteed.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPARE (FETOUT, FETIN)					
FETOUT Output High Level at I = 1.0 mA	$V_{H\ MAX}$	0.8	–	–	V_{CC}
FETOUT Output Low Level at I = 1.0 mA	$V_{H\ MIN}$	–	0.2	0.4	V
FETIN Input Full Scale Range Current	I_{FETIN}	–	5.0	–	mA
FETIN Input Clamp Voltage	V_{CLIN}	5.3	–	7.0	V
Drop Voltage between FETIN and CSNS for MUX[2:0] = 110 I_{FETIN} = 5 mA, 5.5 V > CSNS > 0.0 V	V_{DRIN}	0.0	–	0.4	V
FETIN Leakage Current when external current switch sense is enabled VCC > V_{FETIN} > 0 V, 5.5 V > VCC 4.5 V, CSNS open VCC > V_{FETIN} > 0 V, 4.5 V > VCC > 0, CSNS open	$I_{FETINLEAK}$	 -1.0 -1.0	 – –	 5.0 1.0	µA
TEMPERATURE OF GND FLAG					
Analog Temperature Feedback at T_A = 25 °C with 5.0 kΩ > R_{CSNS} > 500 Ω	V_{T_FEED}	920	1025	1140	mV
Analog Temperature Feedback Derating with 5.0 kΩ > R_{CSNS} > 500 Ω[39]	V_{DT_FEED}	10.9	11.3	11.7	mV/ °C
Analog Temperature Feedback Precision[39]	V_{DT_ACC}	-15	–	15	°C
Analog Temperature Feedback Precision with calibration point at 25 °C[39]	$V_{DT\_ACC\_CAL}$	-5.0	–	5.0	°C

Notes
39. Parameter guaranteed by design; however, it is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUTS TIMING (OUT1:5)					
Current Sense Valid Time on resistive load only(40) SR bit = 0 SR bit = 1	$t_{CSNS(VAL)}$	 – –	 90 45	 150 75	µs
Current Sense Synchronization Time on FETOUT SR bit = 0 SR bit = 1	$t_{CSNS(SYNC)}$	 – –	 130 70	 185 110	µs
Current Sense Settling Time on resistive load only(40)	$t_{CSNS(SET)}$	–	10	30	µs
Driver Output Positive Slew Rate (30% to 70% at V_{BAT} = 14 V) SR bit = 0, I_{OUT} = 2.8 A SR bit = 1, I_{OUT} = 0.7 A	SR_R	 0.10 0.20	 0.25 0.40	 0.56 0.80	V/µs
Driver Output Negative Slew Rate (70% to 30% at V_{BAT} = 14 V) SR bit = 0, I_{OUT} = 2.8 A SR bit = 1, I_{OUT} = 0.7 A	SR_F	 0.10 0.20	 0.25 0.40	 0.56 0.80	V/µs
Driver Output Matching Slew Rate (SR_R/SR_F)(70% to 30% at V_{BAT} = 14 V at 25 °C)	ΔSR	0.8	1.0	1.2	
Driver Output Turn-ON Delay (SPI ON Command [No PWM, $\overline{CS}$ Positive Edge] to Output = 50% V_{BAT} at V_{BAT} = 14 V) SR bit = 0, I_{OUT} = 2.8 A SR bit = 1, I_{OUT} = 0.7 A	t_{DLYON}	 50 25	 – –	 120 65	µs
Driver Output Turn-OFF Delay (SPI OFF command [$\overline{CS}$ Positive Edge] to Output = 50% V_{BAT} at V_{BAT} = 14 V) SR bit = 0, I_{OUT} = 2.8 A SR bit = 1, I_{OUT} = 0.7 A	t_{DLYOFF}	 50 25	 – –	 120 65	µs
Driver Output Matching Time ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$) at Output = 50% V_{BAT} with V_{BAT} = 14 V, f_{PWM} = 240 Hz, δ_{PWM} = 50%, at 25 °C	Δt_{RF}	-30	–	30	µs

Notes
40. Not production tested.

Table 5. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
PWM MODULE					
Nominal PWM Frequency Range[43]	f_{PWM}	30	–	400	Hz
Clock Input Frequency Range	f_{CLK}	7.68	–	51.2	kHz
Output PWM Duty Cycle maximum range for 11 V<V_{BAT}<18 V[41], [43]	PWM_MAX	4.0	–	96	%
Output PWM Duty Cycle linear range for 11 V<V_{BAT}<18 V[42], [43]	PWM_LIN	5.5	–	96	%
Output PWM Duty Cycle range for full diagnostic for 11 V<VBAT<18 V[44]	PWM_DIAG				%
200 Hz Output PWM frequency		5.5	–	96	
400 Hz Output PWM frequency		11	–	90	
WATCHDOG TIMING					
Watchdog Timeout (SPI Failure)	t_{WDTO}	50	75	100	ms
I/O PLAUSIBILITY CHECK TIMING					
Fault Shutdown Delay Time (from Over-temperature or OCHI1 or OHCI2 or OCLO Fault Detection to Output = 50% V_{BAT} without round shaping feature for turn off)	t_{SD}	–	7.0	30	µs
Under-voltage Deglitch Time[45]	t_{UV}	0.8	1.25	2.0	µs
High Over-current Threshold Time 1	t_1	7.0	10	13.5	ms
High Over-current Threshold Time 2	t_2	52.5	75	97.5	ms
Autorestart Period	$t_{AUTORST}$	52.5	75	97.5	ms
Autorestart Over-current Shutdown Delay Time	t_{OCSH_AUTO}	3.5	5.0	6.5	ms
Limp Home Input pin Deglicher Time	t_{LIMP}	7.0	10.0	13.0	ms
Cyclic Open Load Detection Timing with LED[46]	t_{OLLED}	105	150	195	ms
Flasher Toggle Timeout	$t_{FLASHER}$	1.4	2.3	3.0	s
Ignition Toggle Timeout	$t_{IGNITION}$	1.4	2.3	3.0	s
Stop Toggle Timeout	t_{STOP}	1.4	2.3	3.0	s
Clock Input Low Frequency Detection Range	$f_{LCLK\ DET}$	1.0	2.0	4.0	kHz
Clock Input High Frequency Detection Range	$f_{HCLK\ DET}$	100	200	400	kHz

Notes

41. The PWM ratio is measured at V_{OUT} = 50% of V_{BAT} in nominal range of frequency. It is possible to put the device fully on (PWM duty cycle = 100%) and fully off (PWN duty cycle = 0%). Between 4%-96%, $OCLO_{1,2}$, OCLO and open load are available in ON state. See Input Timing Switching Characteristics on page 20.
42. Linear range is defined by output duty cycle to SPI duty cycle configuration +/- LSB. For values outside the linear duty cycle range, a calibration curve is available.
43. Not production tested.
44. Full diagnostic corresponds to the availability of the following features: output current sensing, output status and openload detection. Not production tested.
45. This time is measured from the $V_{BAT(UV)}$ level to the fault reporting. Parameter guaranteed in testmode.
46. OLLEDn bit (where “n” corresponds to respective outputs 1 through 5) in SI data is set to logic [1]. Refer to Table 9, Serial Input Address and Configuration Bit Map.

Table 5. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI INTERFACE CHARACTERISTICS					
Maximum Frequency of SPI Operation	f_{SPI}	–	–	3.0	MHz
Rising Edge of $\overline{CS}$ to Falling Edge of $\overline{CS}$ (Required Setup Time)(47)	$t_{\overline{CS}}$	–	–	1.0	us
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (Required Setup Time)(47)	t_{LEAD}	–	–	500	ns
Required High State Duration of SCLK (Required Setup Time)(47)	t_{WSCLKH}	–	–	167	ns
Required Low State Duration of SCLK (Required Setup Time)(47)	t_{WSCLKI}	–	–	167	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ (Required Setup Time)(47)	t_{LAG}	–	50	167	ns
SI to Falling Edge of SCLK (Required Setup Time)(48)	t_{SISU}	–	25	83	ns
Falling Edge of SCLK to SI (Required Setup Time)(48)	t_{SIHOLD}	–	25	83	ns
SO Rise Time C_L = 80 pF	t_{RSO}	–	25	50	ns
SO Fall Time C_L = 80 pF	t_{FSO}	–	25	50	ns
SI, $\overline{CS}$, SCLK, Incoming Signal Rise Time(49)	t_{RSI}	–	–	50	ns
SI, $\overline{CS}$, SCLK, Incoming Signal Fall Time(49)	t_{FSI}	–	–	50	ns
Time from Falling Edge of $\overline{CS}$ to SO Low-impedance(50)	$t_{SO(EN)}$	–	–	145	ns
Time from Rising Edge of $\overline{CS}$ to SO High-impedance(51)	$t_{SO(DIS)}$	–	65	145	ns

Notes
47. Maximum setup time required for the 35XS3500 is the minimum guaranteed time needed from the microcontroller.
48. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
49. Time required for output status data to be available for use at SO. 1.0 kΩ on pull-up on $\overline{CS}$.
50. Time required for output status data to be terminated at SO. 1.0 kΩ on pull-up on $\overline{CS}$.
51. Time required to obtain valid data out from SO following the rise of SCLK.

TIMING DIAGRAMS

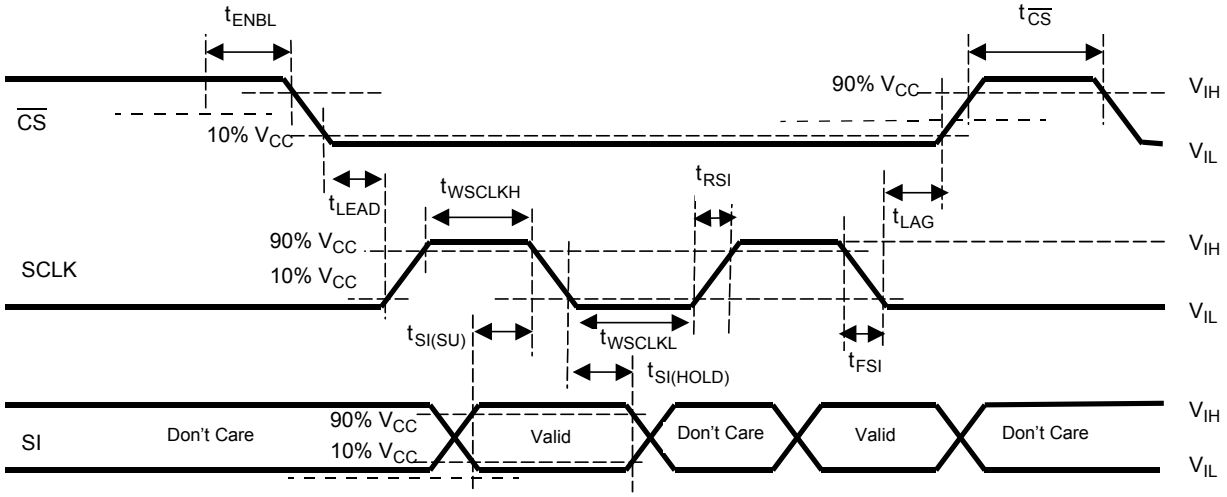


Figure 4. Input Timing Switching Characteristics

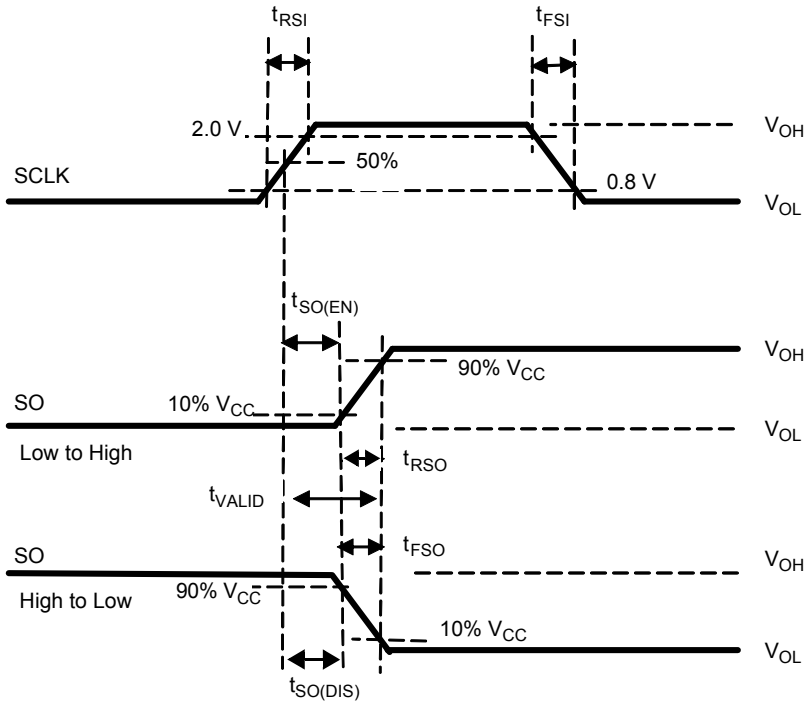


Figure 5. SCLK Waveform and Valid SO Data Delay Time

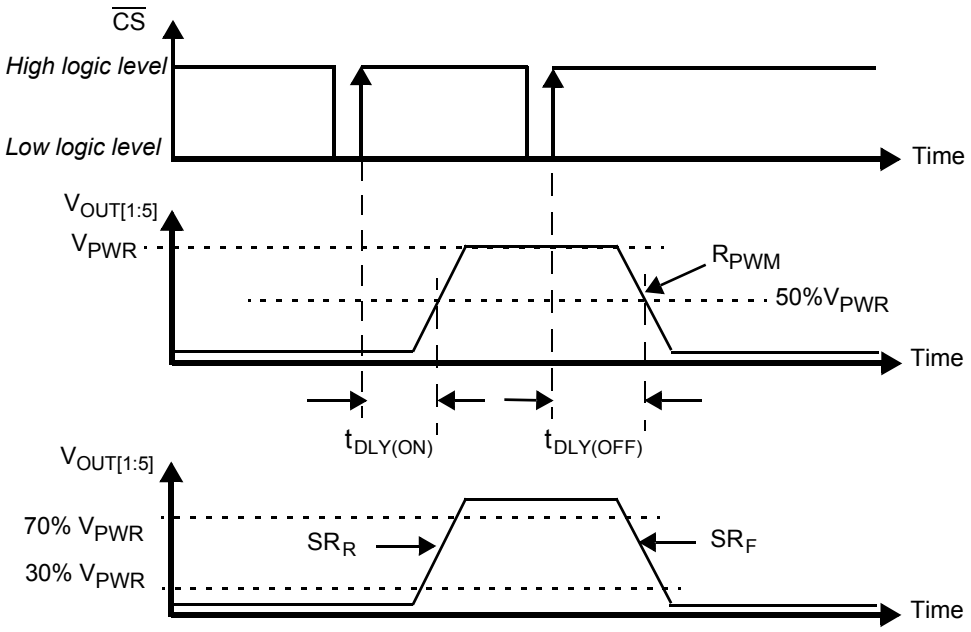


Figure 6. Output Slew Rate and Time Delays

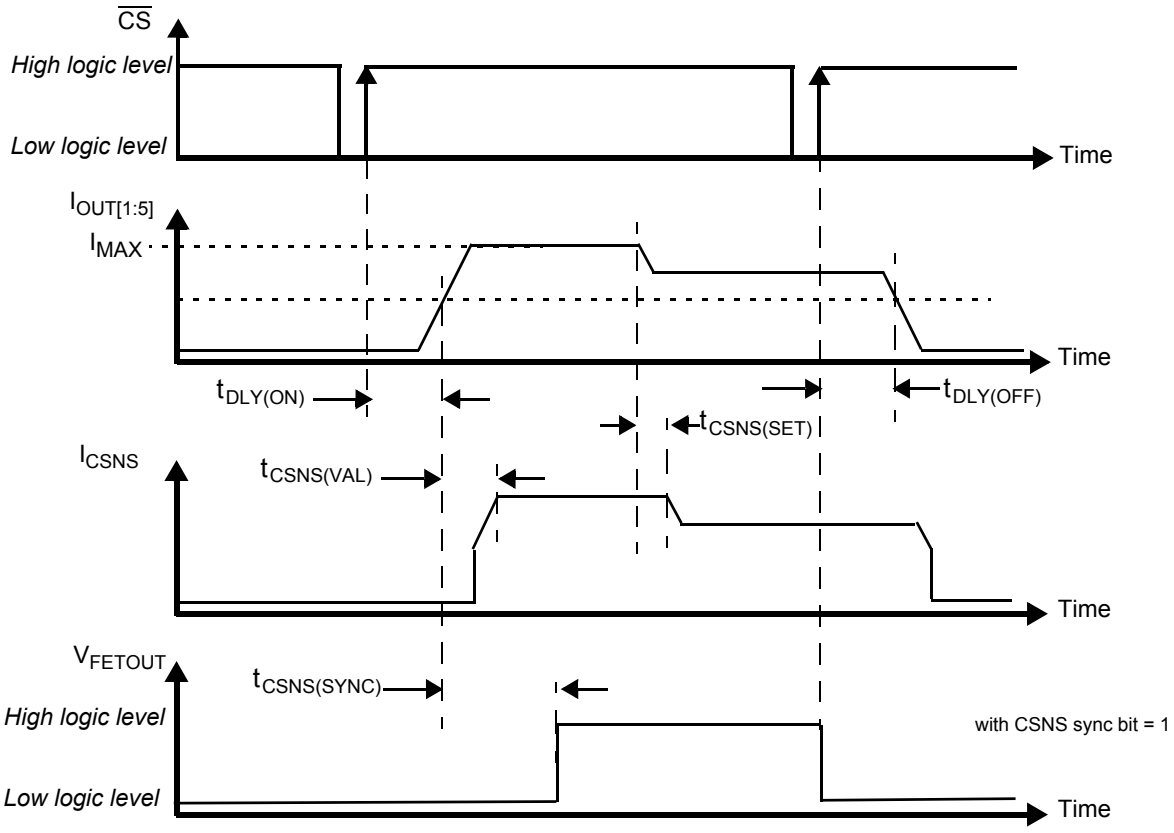


Figure 7. Current Sensing Time Delays

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 35XS3500 is designed for low-voltage automotive and industrial lighting applications. Its five low $R_{DS(ON)}$ MOSFETs (five 35 mΩ) can control the high sides of five separate resistive loads (bulbs). Programming, control, and diagnostics are accomplished using a 16-bit SPI interface.

FUNCTIONAL PIN DESCRIPTION

Supply Voltage (VBAT)

The VBAT pin of the 35XS3500 is the power supply of the device. In addition to its supply function, this tab contributes to the thermal behavior of the device by conducting the heat from the switching MOSFETs to the printed circuit board.

Supply Voltage (VCC)

This is an external voltage input pin used to supply the SPI digital portion of the circuit and the gate driver of the external SMART MOSFET.

Ground (GND)

This pin is the ground of the device.

Clock Input (CLOCK) and PWM Module

When the part is in Normal Mode ($\overline{RST}$=1), the PWM frequency and timing are generated from the rising edge of clock input by the PWM module. The clock input frequency is the selectable factor 2^7 = 128 or 2^8 = 256 of the PWM frequency per output, depending PR bit value.

The OUT1:6 can be controlled in the range of 4% to 96% with a resolution of 7 bits of duty cycle (bits D[6:0]).

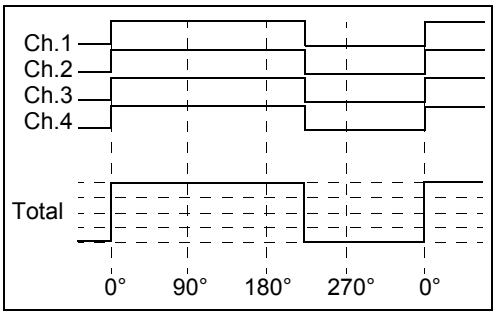
The following table describes the PWM resolution.

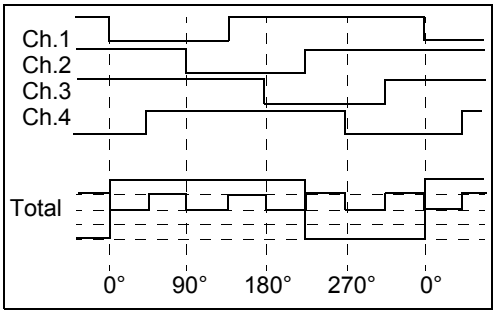
On/Off (Bit D7)	Duty cycle (7 bits resolution)	Output state
0	**X**	**OFF**
1	0000000	PWM (1/128 duty cycle)
1	0000001	PWM (2/128 duty cycle)
1	0000010	PWM (3/128 duty cycle)
1	1111111	fully ON

Table 6. PWM Resolution

The timing includes four programmable PWM switching phases (0°, 90°, 180°, and 270°) to improve overall EMC behavior of the light module.

The amplitude of the input current is divided by four while the frequency is four times the original one. The two following pictures illustrate the behavior.





The synchronization of the switching phases between different corner light IC is provided by a SPI command in combination with the $\overline{CS}$ input. The bit in the SPI is called PWM sync (initialization register).

In Normal mode, No PWM feature (100% duty cycle) is provided in the following instances:

- with the following SPI configuration: D7:D0=FF.
- In case of clock input signal failure (out of f_{PWM}), the outputs state depends on the D7 bit value (D7=1+ON) in Normal mode.

In Fail mode. The outputs state depends on the IGN, STOP and Flasher pins.

If $\overline{RST}$=0, this pin reports the wake-up event for wake=1 when VBAT and VCC are in operational voltage range.

Limp Home (LIMP)

The Limp Home mode of the component can be activated by this digital input port. The signal is “high active”, meaning the Fail mode can be activated by a logic high signal at the input.

Ignition Input (IGN)

The Ignition input wakes the device. It also controls the Fail Home mode activation. The signal is “high active”, meaning the component is active in case of a logic high at the input.

Flasher Input (FLASHER)

The Flasher input wakes the device. It also controls the Fail mode activation. The signal is “high active”, meaning the component is active in case of a logic high at the input.

Reset Input ($\overline{\text{RST}}$)

This input wakes the device when the $\overline{\text{RST}}$ pin is at logic [1]. It is also used to initialize the device configuration and the SPI fault registers when the signal is low. All SI/SO registers described in Table 9 and Table are reset. The fault management is not affected by $\overline{\text{RST}}$ (see Figure 2).

Current Sense Output (CSNS)

The current sense output pin is an analog current output or a voltage proportional to the temperature on the GND flag. The routing to the common resistor is SPI programmable.

This current sense monitoring may be synchronized in case of the OUT6 is not used. So, the current sense monitoring can be synchronized with a rising edge on the FETOUT pin ($t_{CSNS(SYNC)}$) if CSNS sync SPI bit is set to logic [1]. Connection of the FETOUT pin to a MCU input pin allows the MCU to sample the CSNS pin during a valid time-slot. Since this falling edge is generated at the end of this timeslot, upon a switch-off command, this feature may be used to implement maximum current control.

Charge Pump (CP)

An external capacitor is connected between this pin and the VBAT pin. It is used as a tank for the internal charge pump. Its typical value is 100 nF ±20%, 25 V maximum.

FETOUT Output (FETOUT)

This output pin is used to control an external MOSFET (OUT6).

The high level of the FETOUT Output is VCC if V_{BAT} and V_{CC} are available in case of FETOUT is controlled ON.

FETOUT is not protected in case of a short-circuit or under-voltage on V_{BAT}.

In case of a reverse battery, OUT6 is OFF.

FETIN Input (FETIN)

This input pin gives the current recopy of the external MOSFET. It can be routed on the CSNS output by a SPI command.

SPI Protocol Description

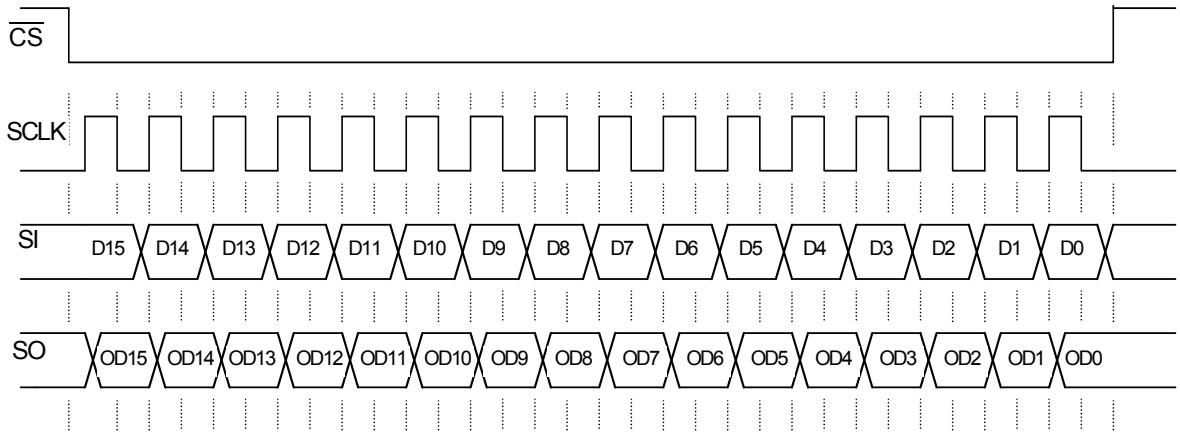
The SPI interface has a full-duplex, three-wire synchronous data transfer with four I/O lines associated with it: Serial Clock (SCLK), Serial Input (SI), Serial Output (SO), and Chip Select ($\overline{\text{CS}}$).

The SI/SO pins of the 35XS3500 device follow a first-in, first-out (D15 to D0) protocol, with both input and output words transferring the most significant bit (MSB) first. All inputs are compatible with 5.0 V CMOS logic levels supplied by V_{CC}.

The SPI lines perform the following functions:

Serial Clock (SCLK)

The SCLK pin clocks the internal shift registers of the 35XS3500 device. The SI pin accepts data into the input shift register on the falling edge of the SCLK signal, while the SO pin shifts data information out of the SO line driver on the rising edge of the SCLK signal. It is important that the SCLK pin be in a logic low state whenever $\overline{\text{CS}}$ makes any transition. For this reason, it is recommended that the SCLK pin be in a logic [0] whenever the device is not accessed ($\overline{\text{CS}}$ logic [1] state). SCLK has a passive pull-down, R_{DWN}. When $\overline{\text{CS}}$ is logic [1], signals at the SCLK and SI pins are ignored and SO is tri-stated (high-impedance) (see Figure 8).



Notes
1. D15:D0 relate to the most recent ordered entry of data into the device.
2. OD15:OD0 relate to the first 16 bits of ordered fault and status data out of the device.

Figure 8. Single 16-Bit Word SPI Communication

Serial Input (SI)

The SI pin is a serial interface command data input pin. Each SI bit is read on the falling edge of SCLK. A 16-bit stream of serial data is required on the SI pin, starting with D15 to D0. SI has a passive pull-down, R_{DOWN}.

Serial Output (SO)

The SO data pin is a tri-state output from the shift register. The SO pin remains in a high-impedance state until the $\overline{CS}$ pin is put into a logic [0] state. The SO data is capable of reporting the status of the output, the device configuration, and the state of the key inputs. The SO pin changes state on the rising edge of SCLK and reads out on the falling edge of SCLK.

Chip Select ($\overline{CS}$)

The $\overline{CS}$ pin enables communication with the master device. When this pin is in a logic [0] state, the device is capable of transferring information to, and receiving information from, the master device. The 35XS3500 device latches in data from the Input Shift registers to the addressed registers on the rising edge of $\overline{CS}$. The device transfers status information from the power output to the Shift register on the falling edge of $\overline{CS}$. The SO output driver is enabled when $\overline{CS}$ is logic [0]. $\overline{CS}$ should transition from a logic [1] to a logic [0] state only when SCLK is a logic [0]. $\overline{CS}$ has a passive pull-up, R_{UP}.

STOP Input (STOP)

The STOP input wakes the device. It also controls the Fail mode activation. The signal is “high active“, meaning the component is active in case of a logic high at the input.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

Sleep Mode

The Sleep mode is the default mode of the 35XS3500. This is the state of the device after first applying battery voltage (V_{BAT}) and prior to any I/O transitions. This is also the state of the device when IGN, $\overline{RST}$, FLASHER, and STOP are logic [0]. In the Sleep mode, the output and all internal circuitry are OFF to minimize current draw. In addition, all SPI-configurable features of the device are reset. The 35XS3500 will transit to two modes (Normal and Fail) depending on wake and fail signals (see Table 18).

The transition to the other modes is according to the following signals:

- Wake = IGN or IGN_ON or FLASHER or $\overline{FLASHER\_ON}$ or STOP or STOP_ON or $\overline{RST}$
- Fail = VCC fail or SPI fail or External limp

Normal Mode

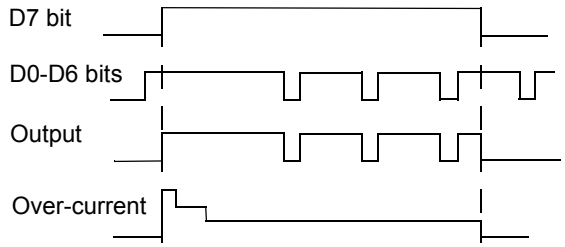
The 35XS3500 is in Normal mode when:

- Wake = 1
- Fail = 0

In Normal operating mode the power outputs are under full control of the SPI as follows:

- The outputs 1 to 6, including multiphase timing, and selectable slew-rate, are controlled by the programmable PWM module.
- The output 4 is activated directly by the STOP external pin in case the STOP_en bit is set to a logic [1].
- The outputs 1 to 5 are switched OFF in case of under-voltage on VBAT.
- The outputs 1 to 5 are protected by the selectable over-current double window and over-temperature shutdown circuit.
- The digital diagnosis feature transfers status of the smart outputs via the SPI.
- The analog current sense output (current recopy feature) can be rerouted by the SPI.
- The outputs can be configured to control LED loads: $R_{DS(ON)}$ is increased by a factor of 2 and the current recopy ratio is scaled by a factor of 4.
- The SPI reports NM=1 in this mode.

The following figure describes the PWM, outputs and over-current behavior in Normal mode.



Fail Mode

The 35XS3500 is in Fail mode when:

- Wake = 1
- Fail = 1

In Fail mode:

- The outputs are under control of the external pins (see Table 6).
- The outputs are fully protected in case of overload, over-temperature and under-voltage (on B_{VAT} or on V_{CC}).
- The SPI reports continuously the content of address 11, disregard to previous requested output data word.
- Neither digital diagnosis feature (SPI) nor analog current sense are available.
- In case of overload (OCHI2 or OCLO) conditions or under-voltage on VBAT, the outputs are under control of the autorestart feature.
- In case of a serious overload condition (OCHI1 or OT) the corresponding output is latched OFF until a new wake-up event (wake = 0 then 1)

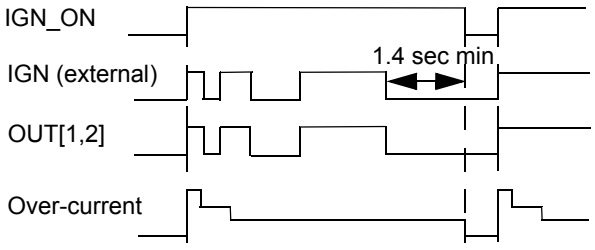


Table 7. Limp Home Output State

Output 1 Tail Light	Output 2 License Light	Output 3 Rear Drive Light	Output 4 Stop Light	Output 5 Flasher	External Switch Rear Fog Light
IGN Pin	OFF	OFF	STOP Pin	FLASHER Pin	OFF