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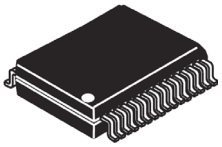
Document Number: MC50XSD200
Rev. 2.0, 8/2016

Dual 24 V, 50 mOhm high-side switch

50XSD200

HIGH-SIDE SWITCH



EK SUFFIX (PB-FREE)
98ASA00368D
32 PIN SOIC (10 mm X11 mm)

The 50XSD200 device is part of a 24 V dual high-side switch product family with integrated control, and a high number of protective and diagnostic functions. It is designed for industrial applications. The low $R_{DS(on)}$ channels (<50 mΩ) can control different load types; bulbs, solenoids, or DC motors. Control, device configuration, and diagnostics are performed through a 16-bit serial peripheral interface (SPI), allowing easy integration into existing applications. This device is powered by SMARTMOS technology.

Both channels can be controlled individually by external/internal clock signals, or by direct inputs. Using the internal clock allows fully autonomous device operation. Programmable output voltage slew- rates (individually programmable) helps improve electromagnetic compatibility (EMC) performance. To avoid shutting off the device upon inrush current, while still being able to closely track the load current, a dynamic overcurrent threshold profile is featured. Switching current of each channel can be sensed with a programmable sensing ratio. Whenever communication with the external microcontroller is lost, the device enters a Fail-safe operation mode, but remains operational, controllable, and protected.

Features

- Two fully-protected 50 mΩ (at 25 °C) high-side switches
- Up to 1.2 A steady-state current per channel
- Separate bulb and DC motor latched overcurrent handling
- Individually programmable internal/external PWM clock signals
- Overcurrent, short-circuit, and overtemperature protection with programmable autoretry functions
- Accurate temperature and current sensing
- Open load detection (channel in OFF and ON state), also for LED applications (7.0 mA typ.)
- Normal operating range: 8.0 - 36 V, extended range: 6.0 - 58 V
- 3.3 V and 5.0 V compatible 16-bit SPI port for device control, configuration and diagnostics at rates up to 8.0 MHz

Applications

- 24 V industrial systems
- Resistive, capacitive, and inductive loads

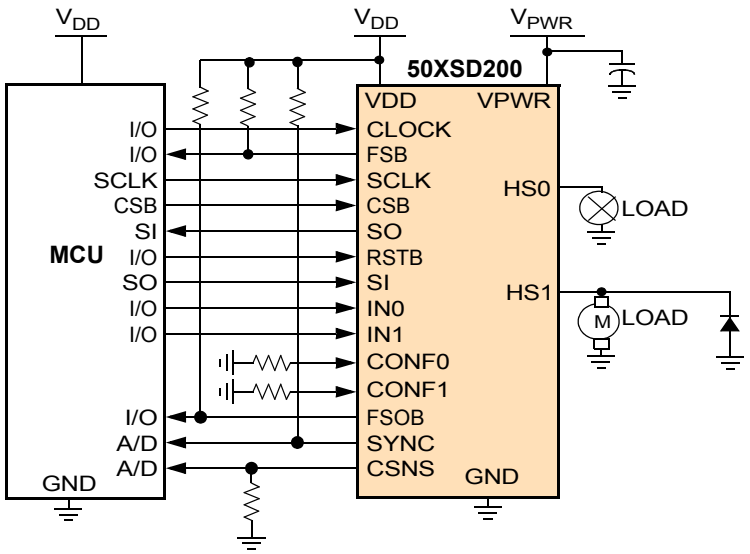


Figure 1. Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Orderable parts

Table 1. Orderable part variations

Part number	Temperature (T_A)	Package
MC50XSD200BEK [(1)]	-40 °C to 125 °C	32 SOIC-EP

Notes
1. To Order parts in Tape & Reel, add the R2 suffix to the part number.

Internal block diagram

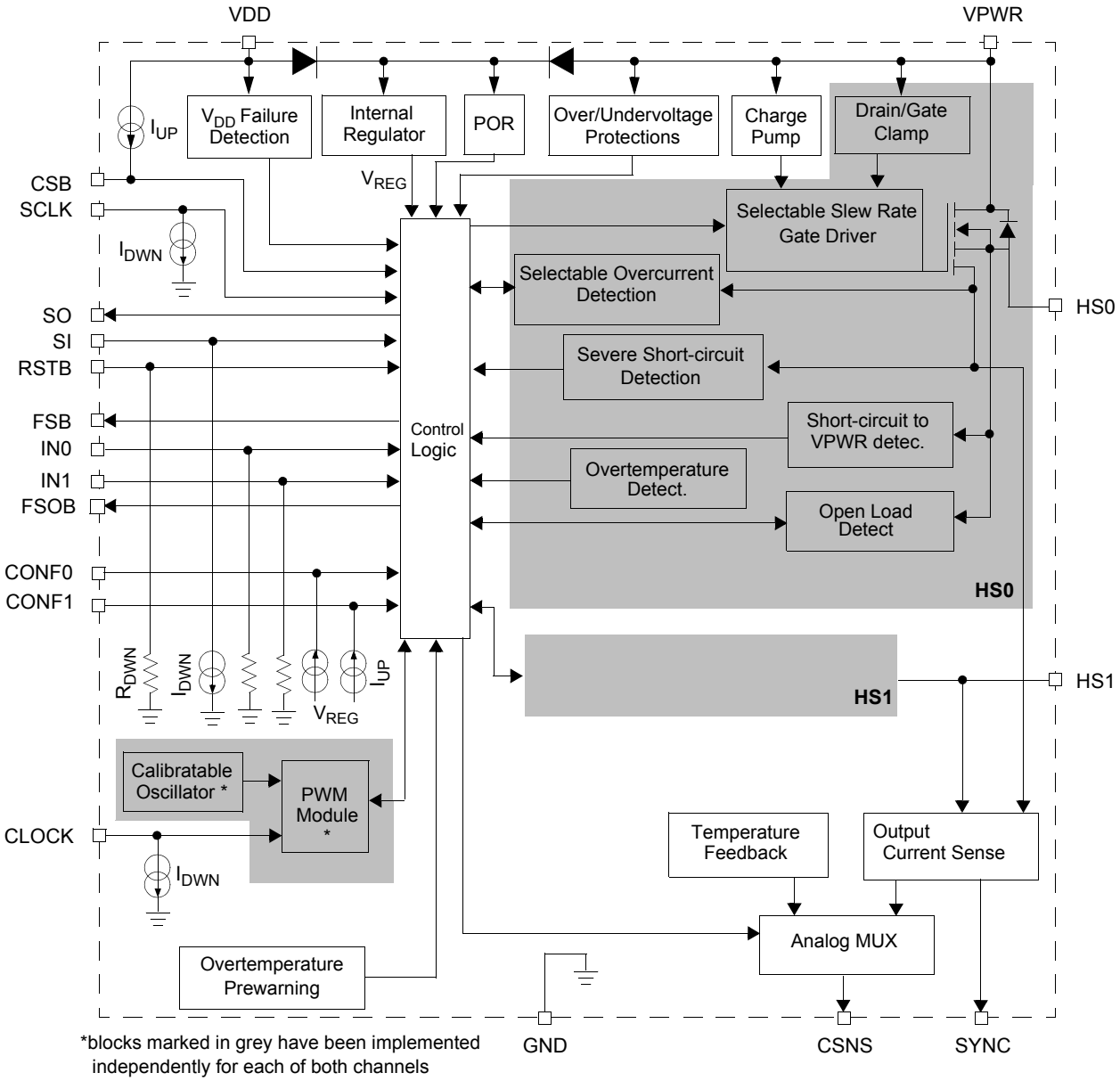


Figure 2. Internal block diagram

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Pin assignment

Transparent Top View

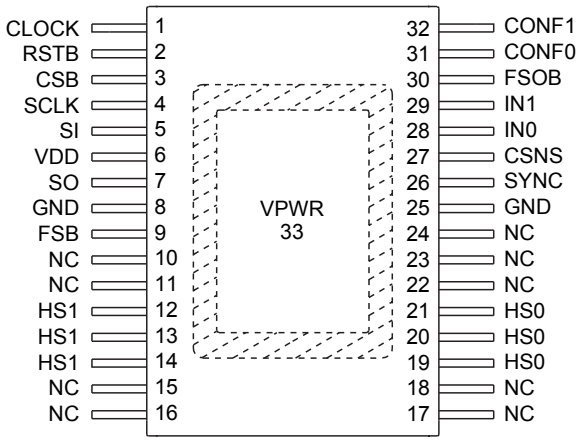


Figure 3. Device pin assignments

The function of each pin is described in the section Functional description

Table 2. 50XSD200 pin description

Pin number	Pin name	Function	Formal name	Definition
1	CLOCK	Input	PWM Clock	The clock input gives the time-base when the device is operated in external clock/ internal PWM mode. This pin has an internal pull-down current source.
2	RSTB	Input	Reset	This input pin is used to initialize the device's configuration - and fault registers. Reset puts the device in Sleep mode (low current consumption) provided it is not stimulated by direct input signals. This pin is connected to GND by an internal pull-down resistor.
3	CSB	Input	Chip Select (Active Low)	This input pin is connected to the SPI chip-select output of an external microcontroller. CSB is internally pulled up to V_{DD} by a current source I_{UP}.
4	SCLK	Input	Serial Clock	This input pin is to be connected to an external SPI Clock signal. The SCLK pin is internally connected to a pull-down current source I_{DWN}.
5	SI	Input	Serial Input	This input pin receives the SPI input data from an external device (microcontroller or another extreme switch device in case of daisy-chaining). The SI pin is internally connected to a pull-down current source I_{DWN}.
6	VDD	Power	Digital Drain Voltage	This is the positive supply pin of the SPI interface.
7	SO	Output	Serial Output	This output pin transmits SPI data to an external device (external microcontroller or the SI pin of the next SPI device in case of daisy-chaining). The pin doesn't require external pull-up or pull-down resistors, but a series resistor is recommended to limit current consumption in case of GND disconnection.
8, 25	GND	Ground	Ground	These pins are the ground for the logic and analog circuitries of the device. For ESD and electrical parameter accuracy purpose, the ground pins must be shorted in the board.
9	FSB	Output	Fault Status (Active Low)	This open drain output pin (external pull-up resistor to V_{DD} required) is set when the device enters Fault mode (see Fault mode).
10, 11, 15, 16, 17, 18, 22, 23, 24	NC	N/A	Not connected	These pins may not be connected.
12, 13, 14, 19, 20, 21	HS1 HS0	Output	Power Switch Outputs	Output pins of the switches, to be connected to the load.
26	SYNC	Output	Output Current Monitoring Synchronization	This output pin is asserted (active low) when the Current Sense (CS) output signal is within the specified accuracy range. Reading the SYNC pin allows the external microprocessor to synchronize to the SPI device when operating in autonomous operating mode. SYNC is open drain and requires a pull-up resistor to V_{DD}.

Table 2. 50XSD200 pin description (continued)

Pin number	Pin name	Function	Formal name	Definition
27	CSNS	Output	Output Current/ Temperature Monitoring	This pin either outputs a current proportional to the channel's output current or a voltage proportional to the temperature of the die. Selection between current and temperature sensing, as well as setting the current sensing sensitivity are performed through the SPI interface. An external pull-down resistor must be connected between CSNS and GND.
28, 29	IN0 IN1	Input	Direct Inputs	The IN[0: 1] input pins are used to directly control the switching state of both switches and consequently the voltage on the HS0: HS1 output pins. The pins are connected to GND by internal pull-down resistors.
30	FSOB	Output	Fail-safe Output (Active Low)	FSOB is asserted (active-low) upon entering Fail-safe mode (see Functional description) This open drain output requires an external pull-up resistor to V_{PWR}.
31, 32	CONF0 CONF1	Input	Configuration Input	The CONF[0: 1] input pins are used to select the appropriate overcurrent detection profile (bulb/DC motor) for each of both channels. CONF requires a pull-down resistor to GND.
33	VPWR	Power	Positive Power Supply	This exposed pad connects to the positive power supply and is the drain of both internal MOSFET switches.

Electrical characteristics

Maximum ratings

Table 3. Maximum ratings

All voltages are relative to ground unless mentioned otherwise. Exceeding these ratings may cause permanent damage.

Symbol	Parameter	Maximum ratings	Unit	Notes
Electrical ratings				
V_{PWR}	VPWR Supply Voltage Range Voltage Transient at 25 °C (500 ms) Reverse Voltage at 25 °C Fast Negative Transient Pulses (ISO 7637-2 pulse #1, V_{PWR}=14V & Ri=10Ω)	 58 -32 -60	V	
V_{DD}	VDD Supply Voltage Range	-0.3 to 5.5	V	
$V_{MAX,LOGIC}$	Voltage on Input pins (except IN[0:1]) and Output pins) (except HS[0:1])	-0.3 to 5.5	V	(2) (3)
V_{FSO}	Voltage on Fail-safe Output (FSOB)	-0.3 to 58	V	
V_{SO}	Voltage on SO pin	-0.3 to V_{DD}+0.3	V	
$V_{IN,MAX}$	Voltage (continuous, max. allowable) on IN[0:1] Inputs	58	V	
$V_{HS[0:1]}$	Voltage (continuous, max. allowable) on output pins (HS [0:1]),	-32 to 58	V	
$I_{HS[0:1]}$	Rated Continuous Output Current per channel	1.2	A	(4)
$E_{CL[0:1]\_SING}$	Maximum allowable energy dissipation per channel and two parallel channels, single-pulse method	17	mJ	(5)
V_{ESD1} V_{ESD2} V_{ESD3} V_{ESD4}	ESD Voltage Human Body Model (HBM) for HS[0:1], VPWR and GND Human Body Model (HBM) for other pins Charge Device Model (CDM) Package Corner pins (1, 13, 19, 20) All Other pins	 ±8000 ±2000 ±750 ±500	V	(6)

Notes:

2. Concerned Input pins are: CONF[0:1], RSTB, SI, SCLK, Clock, and CSB.
3. Concerned Output pins are: CSNS, SYNC, and FSB.
4. Output current rating valid as long as maximum junction temperature is not exceeded. For computation of the maximum allowable output current, the thermal resistance of the package & the underlying heatsink must be taken into account
5. Single pulse Energy dissipation, Single-pulse short-circuit method (L_L = 0.5 mH, R = 48 mΩ V_{PWR} = 28 V, T_J = 150°C initial).
6. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).

Table 3. Maximum ratings *(continued)*

All voltages are relative to ground unless mentioned otherwise. Exceeding these ratings may cause permanent damage.

Symbol	Parameter	Maximum ratings	Unit	Notes
Thermal ratings				
T_A T_J	Operating Temperature Ambient Junction	 -40 to 125 -40 to 150	°C	(7)
T_{STG}	Storage Temperature	-55 to 150	°C	
$R_{\theta JC}$	Thermal Resistance Bottom to Case (Exposed pad)	2.7	°C/W	
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	24	°C/W	(8)
T_{PPRT}	Peak package reflow temperature during reflow	Note 10	°C	(9),(10)

Notes:

7. To achieve high reliability over 10 years of continuous operation, the device's continuous operating junction temperature should not exceed 125 °C.
8. Four layer board (2s2p), per JEDEC JESD51-6 with the board (JESD51-7) horizontal
9. Pin soldering temperature limit is for 40 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
10. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.nxp.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

Static electrical characteristics

Table 4. Static electrical characteristics

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Supply electrical characteristics						
V_{PWR}	Supply Voltage Range: Full Specification compliant Extended Mode	 8.0 6.0	 24 –	 36 58	V	(11)
$I_{PWR(ON)}$	V_{PWR} Supply Current, device in wake-up mode, channel On, Open Load Outputs in ON-state, HS[0:1] open, IN[0:1] > V_{IH}	–	6.5	8.5	mA	
$I_{PWR(SBY)}$	V_{PWR} Supply Current, device in wake-up mode (Standby), channel Off Open Load in OFF-state detection disabled, HS[0:1] shorted to ground with V_{DD} = 5.5 V and RSTB > V_{WAKE}	–	6.5	8.5	mA	
$I_{PWR(SLEEP)}$	Sleep State Supply Current V_{PWR} = 24 V, RSTB = IN[0:1] < V_{WAKE}, HS[0:1] connected to ground T_A = 25 °C T_A = 125 °C	 – –	 3.0 –	 10.0 60.0	µA	
$V_{DD(ON)}$	V_{DD} Supply Voltage	3.0	–	5.5	V	
$I_{DD(ON)}$	V_{DD} Supply Current at V_{DD} = 5.5 V No SPI Communication 8.0 MHz SPI Communication	 – –	 – 5.0	 2.2 –	mA	(12)
$I_{DD(SLEEP)}$	V_{DD} Sleep State Current at V_{DD} = 5.5 V with or without V_{PWR}	–	–	5.0	µA	
$V_{PWR(OV)}$	Overvoltage Shutdown Threshold	39	42	45.5	V	
$V_{PWR(OVHYS)}$	Overvoltage Shutdown Hysteresis	0.2	0.8	1.5	V	
$V_{PWR(UV)}$	Undervoltage Shutdown Threshold	5.0	–	6.0	V	(13)

Table 4. Static electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
$V_{PWR(POR)}$	V_{PWR} Power-On-Reset (POR) Voltage Threshold	2.2	2.6	4.0	V	(13)
$V_{DD(POR)}$	V_{DD} Power-On-Reset (POR) Voltage Threshold	1.5	2.0	2.5	V	(13)
$V_{DD(FAIL)}$	V_{DD} Supply Failure Voltage Threshold (assumed V_{PWR} > $V_{PWR(UV)}$)	2.2	2.5	2.8	V	

Notes

11. In extended mode, availability of several device functions (channel control, value of $R_{DS(on)}$, overtemperature protection) is guaranteed, but compliance with the specified values in this document is not. Below 6.0 V, the device is only protected from overheating (thermal shutdown). Above $V_{PWR(OV)}$, the channels can only be turned ON when the overvoltage detection function has been disabled.
12. Typical value guaranteed per design.
13. When the device recovers from undervoltage and returns to normal mode (6.0 V < V_{PWR} < 58 V) before the end of the auto-retry period (see Auto-retry), the device performs normally. When V_{PWR} drops below $V_{PWR(UV)}$, undervoltage is detected (see Undervoltage fault (latchable fault) and EMC performances).

Table 4. Static electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Electrical characteristics of the output stage (HS0 and HS1)						
$R_{DS(on)25}$	ON-Resistance, Drain-to-Source (I_{HS} = 1.0 A, T_J = 25 °C) CSNS_ratio = 0 V_{PWR} = 8.0 V V_{PWR} = 28 V V_{PWR} = 36 V	 – – –	 41 41 41	 – – –	mΩ	
$R_{DS(on)150}$	ON-Resistance, Drain-to-Source (I_{HS} = 1.0 A,T_J = 150 °C) CSNS_ratio = 0 V_{PWR} = 8.0 V V_{PWR} = 28 V V_{PWR} = 36 V	 – – –	 – – –	 100 100 100	mΩ	
$\Delta R_{DS(on)150}$	ON-Resistance, Drain-to-Source difference from one channel to the other in parallel mode (I_{HS} = 1.0 A,T_J = 150 °C) CSNS_ratio = X	-2.0	–	2.0	mΩ	
$R_{SD(on)150}$	ON-Resistance, Source-Drain (I_{HS} = -1.0 A, T_J = 150 °C, V_{PWR} = -24 V)	–	–	100	mΩ	
L_{SHORT}	Max. detectable wiring length (2.5 mm²) for severe short-circuit detection (see Severe short-circuit fault (latchable fault)): High slew rate selected Medium slew rate selected Low slew rate selected	 12 63 175	 40 210 580	 70 350 990	cm	
$I_{\_OCH1\_0}$ $I_{\_OCH2\_0}$ $I_{\_OCM1\_0}$ $I_{\_OCM2\_0}$ $I_{\_OCL1\_0}$ $I_{\_OCL2\_0}$ $I_{\_OCL3\_0}$	Overcurrent Detection thresholds with CSNS_ratio bit = 0 (CSR0)	10.3 6.6 4.1 2.5 1.7 1.1 0.6	13.20 8.40 5.20 3.20 2.16 1.44 0.72	16.1 10.2 6.3 3.9 2.6 1.8 0.9	A	
$I_{\_OCH1\_1}$ $I_{\_OCH2\_1}$ $I_{\_OCM1\_1}$ $I_{\_OCM2\_1}$ $I_{\_OCL1\_1}$ $I_{\_OCL2\_1}$ $I_{\_OCL3\_1}$	Overcurrent Detection thresholds with CSNS_ratio bit = 1(CSR1)	3.43 2.18 1.35 0.83 0.56 0.37 0.19	4.40 2.80 1.73 1.07 0.72 0.48 0.24	5.37 3.42 2.11 1.31 0.88 0.59 0.29	A	
I_{OUT_LEAK}	Output (HS[x]) leakage Current in sleep state (positive value = outgoing) $V_{HS,OFF}$ = 0 V ($V_{HS,OFF}$ = output voltage in OFF state) $V_{HS,OFF}$ = V_{PWR}, device in sleep state (V_{PWR} = 24 V) $V_{HS,OFF}$ = V_{PWR}, device in sleep state (V_{PWR} = 36 V)	 – -120 -1400	 – – –	 +2.0 +5.0 +5.0	µA	
I_{OUT_OFF}	Output biasing current in off-state (positive value = outgoing) with OL_OFF disabled (worst case for V_{PWR} = 36 V, $V_{HS,OFF}$ = 34 V) Fast slew rate selected Medium slew rate selected Slow slew rate selected With OL_OFF disabled and ECU ground disconnected (V_{PWR} = 32 V)	 -500 -370 -300 0	 -400 -300 -250 -	 -300 -230 -200 -1000	µA	
$V_{D\_GND(CLAMP)}$	Switch Turn-on threshold for Supply overvoltage (V_{PWR} -GND)	58	–	67	V	
$V_{DS(CLAMP)}$	Switch turn-on threshold for Drain-Source overvoltage (measured at I_{OUT} = 500 mA	58	–	66	V	

Table 4. Static electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Electrical characteristics of the output stage (HS0 and HS1) (continued)						
$\Delta V_{DS(CLAMP)}$	Switch turn-on threshold for Drain-Source overvoltage difference from one channel to the other in parallel mode (at I_{HS} = 500 mA)	-2.0	–	+2.0	V	
C_{SR0} C_{SR1}	Current Sensing Ratio CSNS_ratio bit = 0 (high current mode) CSNS_ratio bit = 1 (low current mode)	 – –	 1/600 1/200	 – –	 – 	(14)
$I_{\_LOAD\_MIN}$	Minimum measurable load current with compensated error	–	–	20	mA	(15)
I_{CSR_LEAK}	CSNS leakage current in OFF state (CSNSx_en = 0, CSNS_ratio bit_x = 0)	-4.0	–	+4.0	µA	
$I_{\_LOAD\_ERR\_SYS}$	Systematic offset error (see Current sense errors)	–	-1.6	–	mA	
$I_{\_LOAD\_ERR\_RAND}$	Random offset error	-30	–	30	mA	
$I_{CSNS,MAX}$	CSNS pin current sourcing capability, absolute upper limit	5.15	–	–	mA	
E_{SR0_ERR}	E_{SR0} Output Current Sensing Error (%), uncompensated at output Current level (Sense ratio C_{SR0} selected): T_J = -40 °C 1.2 A 0.6 A 0.3 A 0.15 A T_J = 125 °C 1.2 A 0.6 A 0.3 A 0.15 A T_J = 25 °C to 125 °C 1.2 A 0.6 A 0.3 A 0.15 A	 -12 -12 -15 -25 -10 -9.0 -12 -12 -10 -9.0 -12 -15	 – – – – – – – – – – – –	 12 12 15 25 10 9.0 12 12 10 9.0 12 15	 % 	 (16)

Notes:

14. Current Sense Ratio C_{SRx} = I_{CSNS} / ($I_{HS[x]}$ + $I_{\_LOAD\_ERR\_SYS}$)
15. See note (16), but with I_{CSNS_MEAS} obtained after compensation of $I_{\_LOAD\_ERR\_RAND}$ (see Activation and use of offset compensation). Further accuracy improvements can be obtained by performing a 1 or 2 point calibration (see Application Note)
16. E_{SRx_ERR}=(I_{CSNS_MEAS} / I_{CSNS_MODEL}) -1, with I_{CSNS_MODEL} = (I(HS[x])+ $I_{\_LOAD\_ERR\_SYS}$) * C_{SRx} , ($I_{\_LOAD\_ERR\_SYS}$ defined above, see section Current sense error model). With this model, load current becomes: I(HS[x]) = I_{CSNS} / C_{SRx} - $I_{\_LOAD\_ERR\_SYS}$

Table 4. Static electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Electrical characteristics of the output stage (HS0 and HS1) (continued)						
E_{SR0_ERR}(Comp)	E_{SR0} Output Current Sensing Error (%) after offset compensation at output Current level (Sense ratio C_{SR0} selected):					
	T_J = -40 °C					
	1.2 A	-11	–	11		
	0.6 A	-11	–	11		
	0.3 A	-11	–	11		
	0.15 A	-11	–	11		
	T_J = 125 °C					
	1.2 A	-9.0	–	9.0	%	(17)
	0.6 A	-8.0	–	8.0		
	0.3 A	-8.0	–	8.0		
	0.15 A	-9.0	–	9.0		
	T_J = 25 °C to 125 °C					
	1.2 A	-9.0	–	9.0		
	0.6 A	-8.0	–	8.0		
	0.3 A	-9.0	–	9.0		
	0.15 A	-9.0	–	9.0		
E_{SR1_ERR}	E_{SR1} Output Current Sensing Error (%), uncompensated at output Current level (Sense ratio C_{SR1} selected):					
	T_J = -40 °C					
	0.3 A	-15	–	15	%	(17)
	T_J = 125 °C					
	0.3 A	-12	–	12		
	T_J = 25 °C to 125 °C					
	0.3 A	-12	–	12		
E_{SR1_ERR}(Comp)	E_{SR1} Output Current Sensing Error (%) after offset compensation at output Current level (Sense ratio C_{SR1} selected):					
	T_J = -40 °C					
	0.3 A	-11	–	11		
	0.1 A	-13	–	13		
	0.05 A	-18	–	18		
	0.03 A	-29	–	29		
	T_J = 125 °C					
	0.3 A	-9.0	–	9.0	%	(18)
	0.1 A	-10	–	10		
	0.05 A	-12	–	12		
	0.03 A	-12	–	12		
	T_J = 25 °C to 125 °C					
	0.3 A	-9.0	–	9.0		
	0.1 A	-10	–	10		
	0.05 A	-13	–	13		
	0.03 A	-16	–	16		

Notes:

17. E_{SRx_ERR}=(I_{CSNS_MEAS} / I_{CSNS_MODEL}) -1, with I_{CSNS_MODEL} = (I(HS[x])+ $I_{\_LOAD\_ERR\_SYS}$) * C_{SRx} , ($I_{\_LOAD\_ERR\_SYS}$ defined above, see section Current sense error model). With this model, load current becomes: I(HS[x]) = I_{CSNS} / C_{SRx} - $I_{\_LOAD\_ERR\_SYS}$

18. See note (19), but with I_{CSNS_MEAS} obtained after compensation of $I_{\_LOAD\_ERR\_RAND}$ (see Activation and use of offset compensation). Further accuracy improvements can be obtained by performing a 1 or 2 point calibration

Table 4. Static electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Electrical characteristics of the output stage (HS0 and HS1) (continued)						
$E_{SR0\_ERR\_PAR}$	E_{SR0} Output Current Sensing Error in parallel mode (%), uncompensated) at outputs Current level (Sense ratio C_{SR0} selected): T_J = -40 °C 1.2 A 0.6 A T_J = 125 °C 1.2 A 0.6 A T_J = 25 °C to 125 °C 1.2 A 0.6 A	 -10 -11 -8.0 -8.0 -9.0 -9.0	 – – – – – –	 10 11 8.0 8.0 9.0 9.0	%	(19)
$V_{CL(CSNS)}$	Current Sense Clamping Voltage (condition: R(CSNS) > 10 kOhm)	5.5	–	7.5	V	
$I_{OLD(OFF)}$	Open Load Detection Current threshold in OFF state	30	–	100	µA	(19)
$V_{OLD(THRES)}$	Open Load Fault Detection Voltage Threshold	4.0	–	5.5	V	(19)
$I_{OLD(ON)}$	Open Load Detection Current threshold in ON state (see Open load detection in on state (OL_ON)): CSNS_ratio bit = 0 CSNS_ratio bit = 1 (fast slew rate SR[1:0] = 10 mandatory for this function)	 20 4.0	 60 7.0	 100 10	mA	
t_{OLLED}	Time period of the periodically activated Open Load in ON state detection for CSNS_ratio bit = 1	105	150	195	ms	
$V_{OSD(THRES)}$	Output Shorted-to-V_{PWR} Detection Voltage Threshold (channel in OFF state)	V_{PWR}-1.2	V_{PWR}-0.8	V_{PWR}-0.4	V	
V_{CL}	Switch turn-on threshold for Negative Output Voltages (protects against negative transients) - (measured at I_{OUT} = 100mA, Channel in OFF state)	-38	–	-32	V	
ΔV_{CL}	Switch turn-on threshold for Negative Output Voltages difference from one channel to the other in parallel mode - (measured at I_{OUT} = 100 mA, Channel in OFF state)	-2.0	–	+2.0	V	
V_{HS_TH}	Switching State (On/Off) discrimination thresholds	0.45*V_{PWR}	0.5*V_{PWR}	0.55*V_{PWR}	V	
T_{SD}	Shutdown temperature (Power MOSFET junction; 6.0 V < V_{PWR} < 58 V)	160	175	190	°C	

Notes:

19. Minimum required value of open load impedance for detection of open load in OFF-state: 200 kΩ.($V_{OLD(THRES)}$ = V_{HS} at $I_{OLD(OFF)}$)

Table 4. Static electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Electrical characteristics of the control interface pins						
V_{IH}	Logic Input Voltage, High	2.0	–	5.5	V	(20)
V_{IL}	Logic Input Voltage, Low	-0.3	–	0.8	V	(20)
V_{WAKE}	Wake-up Threshold Voltage (IN[0:1] and RSTB)	1.0	–	2.2	V	(21)
I_{DWN}	Internal Pull-down Current Source (on Inputs: CLOCK, SCLK and SI)	5.0	–	20	µA	(22)
I_{UP_CSB}	Internal Pull-up Current Source (input CSB)	5.0	–	20	µA	(23)
I_{UP_CONF}	Internal Pull-up Current Source (input CONF[0:1])	25	–	100	µA	(24)
C_{SO}	Capacitance of SO, FSB and FSOB pins in Tri-state	–	–	20	pF	
R_{DWN}	Internal Pull-down Resistance (RSTB and IN[0:1])	125	250	500	kΩ	
C_{IN}	Input Capacitance	–	4.0	12	pF	(25)
V_{SOH}	SO High-state Output Voltage (I_{OH} = 1.0 mA)	V_{DD}-0.4	–	–	V	
V_{SOL}	SYNC, SO, FSOB and FSB Low-state Output Voltage (I_{OL} = -1.0 mA)	–	–	0.4	V	
$I_{SO(LEAK)}$	SYNC, SO, CSNS, FSOB and FSB Tri-state Leakage Current: (0.0 V < V(SO) < V_{DD}, or V(FS) or V(SYNC) = 5.5 V, or V(FSO) = 36 V or V(CSNS) = 0.0 V	-2.0	0.0	2.0	µA	
R_{CONF}	CONF[0:1]: Required values of the External Pull-down Resistor Lighting applications DC motor applications	 1.0 50	 – –	 10 Infinite	kΩ	

Notes

20. High and low voltage ranges apply to SI, CSB, SCLK, RSTB, IN[0:1] and CLOCK input signals. The IN[0:1] signals may be derived from V_{PWR} and can tolerate voltages up to 58 V.
21. Voltage above which the device wakes up
22. Valid for V_{SI} ≥ 0.8 V and V_{SCLK} ≥ 0.8 V and V_{CLOCK} ≥ 0.8 V.
23. Valid for V_{CSB} ≤ 2.0 V. CSB has an internal pull-up current source derived from V_{DD}
24. Pins CONF[0:1] are connected to an internal current source, derived from an internal voltage regulator (V_{REG} ~ 3.0 V).
25. Input capacitance of SI, CSB, SCLK, RSTB, IN[0:1], CONF[0:1], and CLOCK pins. This parameter is guaranteed by the manufacturing process but is not tested in production.

Dynamic electrical characteristics

Table 5. Dynamic electrical characteristics

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Symbol	Parameter	Min.	Typ.	Max.	Unit	
Output voltage switching characteristics						
SR_{R_00} SR_{F_00}	Rising and Falling edges medium slew rate (SR[1:0] = 00) V_{PWR} = 16 V V_{PWR} = 28 V V_{PWR} = 36 V	 0.5 0.6 0.7	 – – –	 2.0 2.4 2.8	V/µs	(26)
SR_{R_01} SR_{F_01}	Rising and Falling edges low slew rate (SR[1:0] = 01) V_{PWR} = 16 V V_{PWR} = 28 V V_{PWR} = 36 V	 0.2 0.3 0.35	 – – –	 1.0 1.2 1.4	V/µs	(26)
SR_{R_10} SR_{F_10}	Rising and Falling edges high slew rate / SR[1:0] = 10) V_{PWR} = 16 V V_{PWR} = 28 V V_{PWR} = 36 V	 1.0 1.2 1.4	 – – –	 4.0 4.8 5.6	V/µs	(26)
ΔSR	Rising/Falling edge slew rate matching (SR_R /SR_F) 16 V < V_{PWR} < 36 V	0.75	–	1.25		
ΔSR	Edge slew rate difference from one channel to the other in parallel mode 16 V < V_{PWR} < 36 V SR[1:0] = 00 SR[1:0] = 01 SR[1:0] = 10	 -0.24 -0.13 -0.48	 0.0 0.0 0.0	 0.24 0.13 0.48	V/µs	(26)
t_{DLY_00}	Output Turn-ON and Turn-OFF Delays (medium slew rate: SR[1:0] = 00) 16 V < V_{PWR} < 36 V	6.0	–	60	µs	(27)
t_{DLY_01}	Output Turn-ON and Turn-OFF Delays (low slew rate/SR[1:0] = 01) 16 V < V_{PWR} < 36 V	10	–	120	µs	(27)
t_{DLY_10}	Output Turn-ON and Turn-OFF Delays (high slew rate/SR[1:0] = 10) 16 V < V_{PWR} < 36 V	4.0	–	35	µs	(27)
Δt_{RF_00}	Turn-ON and Turn-OFF Delay time matching ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$) f_{PWM} = 400 Hz, 16 V < V_{PWR} < 36 V, duty cycle on IN[x] = 50 %, SR[1:0] = 00	-15	0.0	15	µs	
Δt_{RF_01}	Turn-ON and Turn-OFF Delay time matching ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$) f_{PWM} = 200 Hz, 16 V < V_{PWR} < 36 V, duty cycle on IN[x] = 50 %, SR[1:0] = 01	-30	–	30	µs	
Δt_{RF_10}	Turn-ON and Turn-OFF Delay time matching ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$) f_{PWM} = 1.0 kHz, 16 V < V_{PWR} < 36 V, duty cycle on IN[x] = 50 %, SR[1:0] = 10	-7.0	0.0	7.0	µs	

Notes

26. Rising and Falling edge slew rates specified for a 20% to 80% voltage variation on a 25.0 Ω resistive load (see Output voltage slew rate and delay).
27. Turn-on delay time measured as delay between a rising edge of the channel control signal (IN[0:1] = 1) and the associated rising edge of the output voltage up to: $V_{HS[0:1]} = V_{PWR} / 2$ (where R_L = 25 Ω). Turn-OFF delay time is measured as time between a falling edge of the channel control signal (IN[0:1] = 0) and the associated falling edge of the output voltage up to the instant at which: $V_{HS[0:1]} = V_{PWR} / 2$ (R_L = 25 Ω)

Table 5. Dynamic electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Symbol	Parameter	Min.	Typ.	Max.	Unit	
Output voltage switching characteristics (continued)						
$\Delta t_{(DLY)}$	Delay time difference from one channel to the other in parallel mode 16 V < V_{PWR} < 36 V SR[1:0] = 00 SR[1:0] = 01 SR[1:0] = 10	 -10 -25 -6.0	 – – –	 10 25 6.0	µs	(28)
t_{FAULT}	Fault Detection Delay Time	–	5.0	8.0	µs	(29)
t_{DETECT}	Output Shutdown Delay Time	–	10	15	µs	(30)
$t_{CSNSVAL\_00}$	Current sense output settling Time for SR[1:0] = 00 (medium slew rate) 16 V < V_{PWR} < 36 V	0.0	–	200	µs	(31)
$t_{CSNSVAL\_01}$	Current sense output settling Time for SR[1:0] = 01(low slew rate) 16 V < V_{PWR} < 36 V	0.0	–	315	µs	(31)
$t_{CSNSVAL\_10}$	Current sense output settling Time for SR[1:0] = 10 (high slew rate) 16 V < V_{PWR} < 36 V	0.0	–	165	µs	(31)
$t_{SYNCVAL\_00}$	SYNC output signal delay for SR[1:0] = 00 (medium SR)	20	–	120	µs	(31)
$t_{SYNCVAL\_01}$	SYNC output signal delay for SR[1:0] = 01 (low SR)	40	–	240	µs	(31)
$t_{SYNCVAL\_10}$	SYNC output signal delay for SR[1:0] = 10 (high SR)	10	–	60	µs	(31)
$t_{SYNREAD\_00}$	Recommended sync_to_read delay SR[1:0] = 00 (medium slew rate)	0.0	–	150	µs	(31)
$t_{SYNREAD\_01}$	Recommended sync_to_read delay SR[1:0] = 01 (low slew rate)	0.0	–	150	µs	(31)
$t_{SYNREAD\_10}$	Recommended sync_to_read delay SR[1:0] = 10 (high slew rate)	0.0	–	150	µs	(31)
t_{OCH1} t_{OCH2}	Upper overcurrent threshold duration	6.0 12.0	8.6 17.2	11.2 22.4	ms	
t_{OCM1_L} t_{OCM2_L}	Medium overcurrent threshold duration (CONF = 0; Lighting Profile)	48 96	67 137	87 178	ms	
t_{OCM1_M} t_{OCM2_M}	Medium overcurrent threshold duration (CONF = 1; DC motor Profile)	48 96	67 137	87 178	ms	

Notes

28. Rising and Falling edge slew rates specified for a 20% to 80% voltage variation on a 10.0 Ω resistive load (see Output voltage slew rate and delay).
29. Time required to detect and report the fault to the FSB pin.
30. Time required to switch off the channel after detection of overtemperature (OT), overcurrent (OC), SC or UV error (time measured between start of the negative edge on the FSB pin and the falling edge on the output voltage until V(HS[0:1)) = 50% of V_{PWR}
31. Settling time (= $t_{CSNSVAL\_XX}$), SYNC output signal delay (= $t_{SYNCVAL\_XX}$) and Read-out delay (= $t_{SYNREAD\_XX}$) are defined for a stepped load current (100 mA< I(LOAD)<IOCLx A FOR CSNS_RATIO_S = 1, AND 300 mA< I(LOAD)<IOCLx A_0 FOR CSNS_RATIO_S = 0). (see Figure 9 and Output current monitoring (CSNS))

Table 5. Dynamic electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Symbol	Parameter	Min.	Typ.	Max.	Unit	
Frequency and PWM duty cycle ranges (protections fully operational, see Protective functions) (32)						
$f_{CONTROL}$	Switching Frequency range - Direct Inputs	0.0	–	1000	Hz	
f_{PWM_EXT}	Switching Frequency range - External clock with internal PWM (recommended)	20	–	1000	Hz	
f_{PWM_INT}	Switching Frequency range - Internal clock with internal PWM (recommended)	60	–	1000	Hz	
$R_{CONTROL}$	Duty Cycle range	0.0	–	100	%	
Availability diagnostic functions over duty cycle and switching frequency (protections & diagnostics both fully operational, see Diagnostic features for the exact boundary values)						
$R_{PWM\_1K\_H}$	Available Duty Cycle Range, f_{PWM} = 1.0 kHz high slew rate, PWM mode OL_OFF OL_ON OS	 0.0 35 0.0	 – – –	 62 100 90	%	(33)
$R_{PWM\_400\_M}$	Available Duty Cycle Range, f_{PWM} = 400 Hz, medium slew rate, PWM mode OL_OFF OL_ON OS	 0.0 21 0.0	 – – –	 81 100 88	%	(33)
$R_{PWM\_400\_H}$	Available Duty Cycle Range, f_{PWM} = 400 Hz, high slew rate, PWM mode OL_OFF OL_ON OS	 0.0 14 0.0	 – – –	 84 100 95	%	(33)
$R_{PWM\_200\_L}$	Available Duty Cycle Range, f_{PWM} = 200 Hz, low slew rate mode, PWM mode OL_OFF OL_ON OS	 0.0 15 0.0	 – – –	 86 100 93	%	(33)
$R_{PWM\_200\_M}$	Available Duty Cycle Range, f_{PWM} = 200 Hz, medium slew rate, PWM mode OL_OFF OL_ON OS	 0.0 11 0.0	 – – –	 90 100 94	%	(33)
$R_{PWM\_100\_L}$	Available Duty Cycle Range, f_{PWM} = 100 Hz in low slew rate, PWM mode OL_OFF OL_ON OS	 0.0 8.0 0.0	 – – –	 93 100 96	%	(33)
$A_{FPWM(CAL)}$	Deviation of the internal clock PWM frequency after Calibration	-10	–	+10	%	(34)
$f_{PWM(0)}$	Default output frequency when using an uncalibrated oscillator	280	400	520	Hz	

Notes

32. In Direct Input mode, the lower frequency limit is 0 Hz with RSTB=5.0 V and 4.0 Hz with RSTB=0.0 V. Duty cycle applies to instants at which V_{HS} = 50 % V_{PWR}. For low duty cycle values, the effective value also depends on the value of the selected slew rate.
33. The device can be operated outside the specified duty cycle and frequency ranges (basic protective functions OC, SC, UV, OV, OT remain active) but the availability of the diagnostic functions OL_ON, OL_OFF, OS is affected.
34. Values guaranteed from 60 Hz to 1.0 kHz (recommended switching frequency range for internal clock operation).

Table 5. Dynamic electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Symbol	Parameter	Min.	Typ.	Max.	Unit	
Availability diagnostic functions over duty cycle and switching frequency (continued) (protections & diagnostics both fully operational, see Diagnostic features for the exact boundary values)						
$t_{CSB(MIN)}$	Minimal required Low Time during Calibration of the Internal Clock through CSB	1.0	1.5	2.0	µs	
$t_{CSB(MAX)}$	Maximal allowed Low Time during Calibration of the Internal Clock through CSB	70	100	130	µs	
f_{CLOCK}	Recommended external Clock Frequency Range (external clock/PWM Module)	15	–	512	kHz	
$f_{CLOCK(MAX)}$	Upper detection threshold for external Clock frequency monitoring	512	730	930	kHz	
$f_{CLOCK(MIN)}$	Lower detection threshold for external Clock frequency monitoring	5.0	7.0	10	kHz	
Timing: SPI port, IN[0]/ IN[1] signals and autoretry						
t_{IN}	Required Low time allowing delatching or triggering sleep mode (direct input mode)	175	250	325	ms	
t_{WDTO}	Watchdog Timeout for entering Fail-safe Mode due to loss of SPI contact	217	310	400	ms	(35)
t_{AUTO_00} t_{AUTO_01} t_{AUTO_10} t_{AUTO_11}	Auto-Retry Repetition Period (when activated): Auto_period bits = 00 Auto_period bits = 01 Auto_period bits = 10 Auto_period bits = 11	 105 52.5 26.2 13.1	 150 75 37.5 17.7	 195 97.5 47.8 24.4	ms	
GND pin temperature sensing function						
T_{OTWAR}	Thermal Prewarning Detection Threshold	110	125	140	°C	(36)
T_{FEED}	Temperature Sensing output voltage at T_A = 25 °C (470 Ω < R_{CSNS} < 10 kΩ)	918	1078	1238	mV	
DT_{FEED}	Gain Temperature Sensing output at T_A = 25 °C (470 Ω < R_{CSNS} < 10 kΩ)	10.7	11.1	11.5	mV/°C	(36)
T_{FEED_ERROR}	Temperature Sensing Error, range [-40 °C, 150 °C], default	-15	–	+15	°C	(36)
$T_{FEED\_ERROR\_CAL}$	Temperature Sensing Error, [-40 °C, 150 °C] after 1 point calibration at 25 °C	-5.0	–	+5.0	°C	(36)

Notes

35. Only when the WD_dis bit set to logic [0] (default). Watchdog timeout defined from the rising edge on RST to rising edge HS[0,1]
36. Values were obtained by lab. characterization

Table 5. Dynamic electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Symbol	Parameter	Min.	Typ.	Max.	Unit	
SPI interface electrical characteristics (37)						
f_{SPI}	Maximum Operating Frequency of the Serial Peripheral Interface (SPI)	–	–	8.0	MHz	(43)
t_{WRSTB}	Required Low-state Duration for reset RSTB	10	–	–	µs	(38)
t_{CSB}	Required duration from the Rising to the Falling Edge of CSB (Required Setup Time)	1.0	–	–	µs	(39)
t_{ENBL}	Rising Edge of RSTB to Falling Edge of CSB (Required Setup Time)	5.0	–	–	µs	(39)
t_{LEAD}	Falling Edge of CSB to Rising Edge of SCLK (Required Setup Time)	500	–	–	ns	(39)
t_{LAG}	Falling Edge of SCLK to Rising Edge of CSB (Required Setup lag Time)	60	–	–	ns	(39)
t_{WSCLKh}	Required High State Duration of SCLK (Required Setup Time)	50	–	–	ns	(39)
t_{WSCLKl}	Required Low State Duration of SCLK (Required Setup Time)	50	–	–	ns	(39)
$t_{SI(SU)}$	SI to Falling Edge of SCLK (Required Setup Time)	15	–	–	ns	(40)
$t_{SI(H)}$	Falling Edge of SCLK to SI (Required hold Time of the SI signal)	30	–	–	ns	(40)
t_{RSO}	SO Rise Time C_L = 80 pF	–	–	20	ns	
t_{FSO}	SO Fall Time C_L = 80 pF	–	–	20	ns	
t_{RSI}	SI, CSB, SCLK, Max. Rise Time allowing operation at f_{SPI} = 8.0 MHz	–	–	11	ns	(40)
t_{FSI}	SI, CSB, SCLK, Max. Fall Time allowing operation at f_{SPI} = 8.0 MHz	–	–	11	ns	(40)
t_{VALID}	Time from Rising Edge of SCLK to reach a valid level at the SO pin	–	–	44	ns	(41)
t_{SOEN}	Time from Falling Edge of CSB to reach low-impedance on SO (access time)	–	–	30	ns	(42)
t_{SODIS}	Time from Falling Edge of CSB to reach high-impedance on SO pin (turn off time)	–	–	30	ns	

Notes:

37. Parameters guaranteed by design. It is recommended to tie unused SPI-pins to GND by resistors 1.0 k <R <10 k
38. RSTB low duration is defined as the minimum time required to switch off the channel when previously put ON in SPI mode (direct inputs inactive).
39. Minimum setup time required for the device is the minimum required time that the microcontroller must wait or remain in a given state.
40. Rise and Fall time of incoming SI, CSB, and SCLK signals.
41. Time required for output data to be available for use at SO, measured with a 1.0 kΩ series resistor connected CSB.
42. Time required for output data to be terminated at SO measured with a 1.0 kΩ series resistor connected CSB.
43. For clock frequencies > 4.0 MHz, series resistors on the SPI pins should preferably be removed. Otherwise, 470 pF ($V_{MAX.}$ > 40 V) ceramic speed-up capacitors in parallel with the >8.0 kΩ input resistors are required on pins SCLK, SI, SO, CS

Timing diagrams

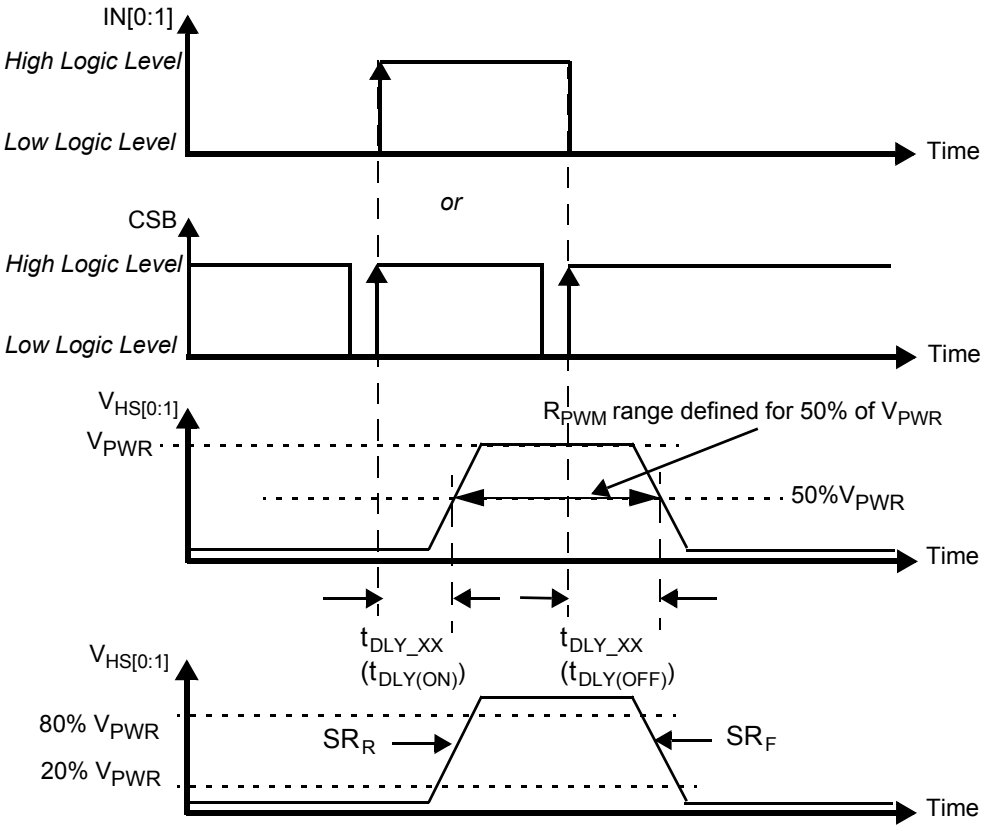


Figure 4. Output voltage slew rate and delay

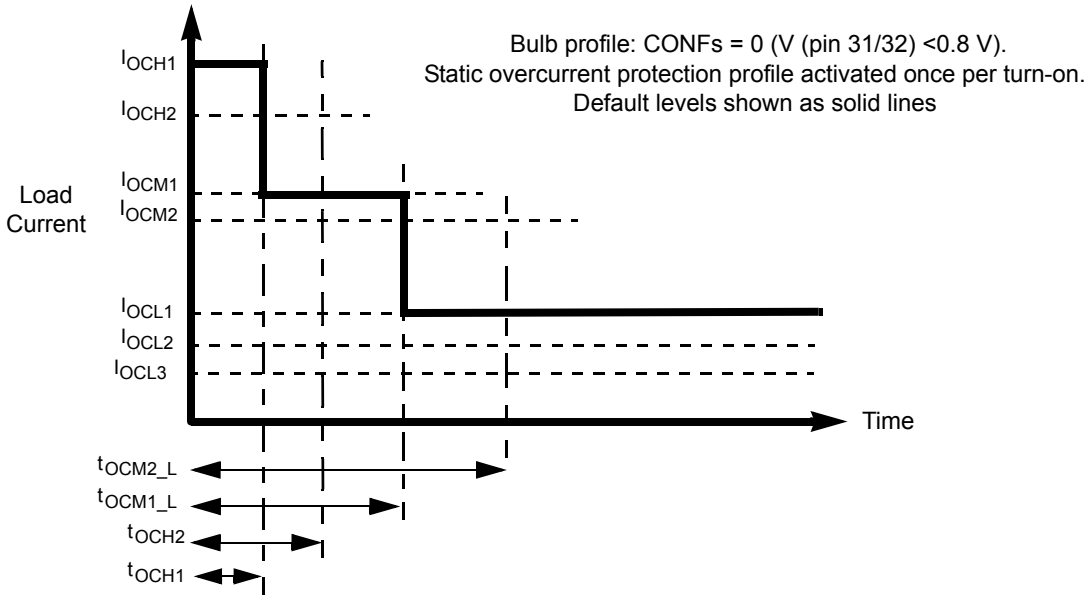


Figure 5. Overcurrent protection profile for bulb applications

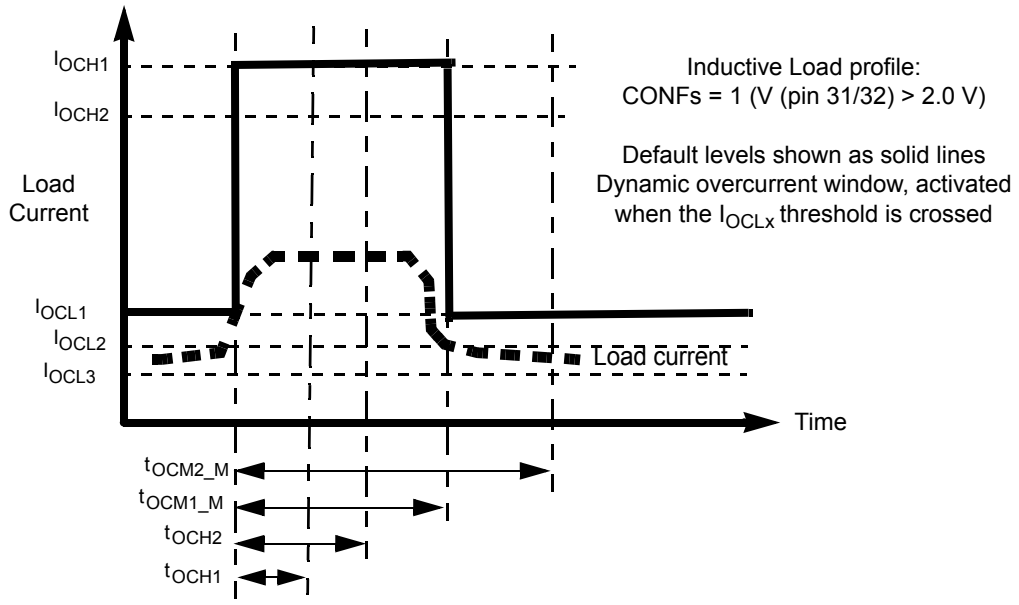


Figure 6. Overcurrent protection profile for applications with inductive loads (DC motors, solenoids)

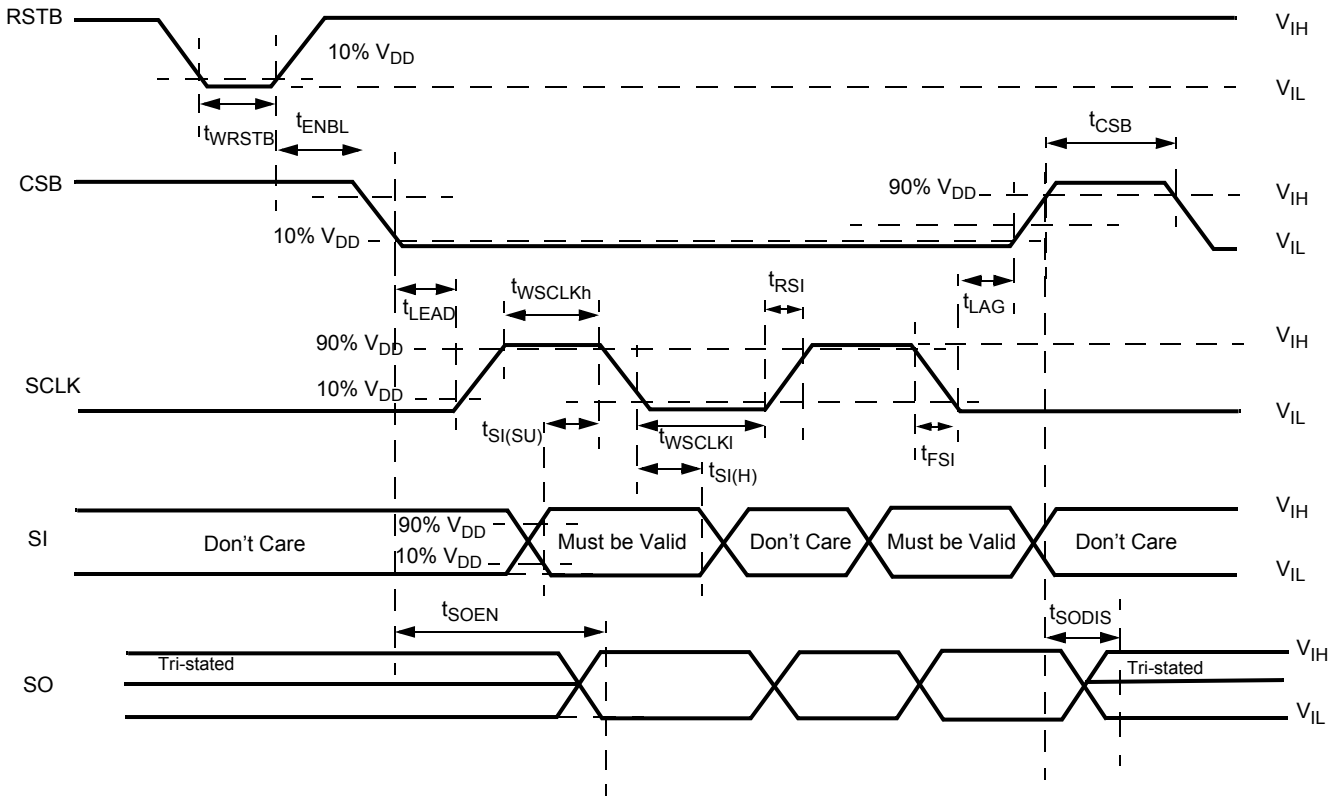


Figure 7. Timing requirements during SPI communication

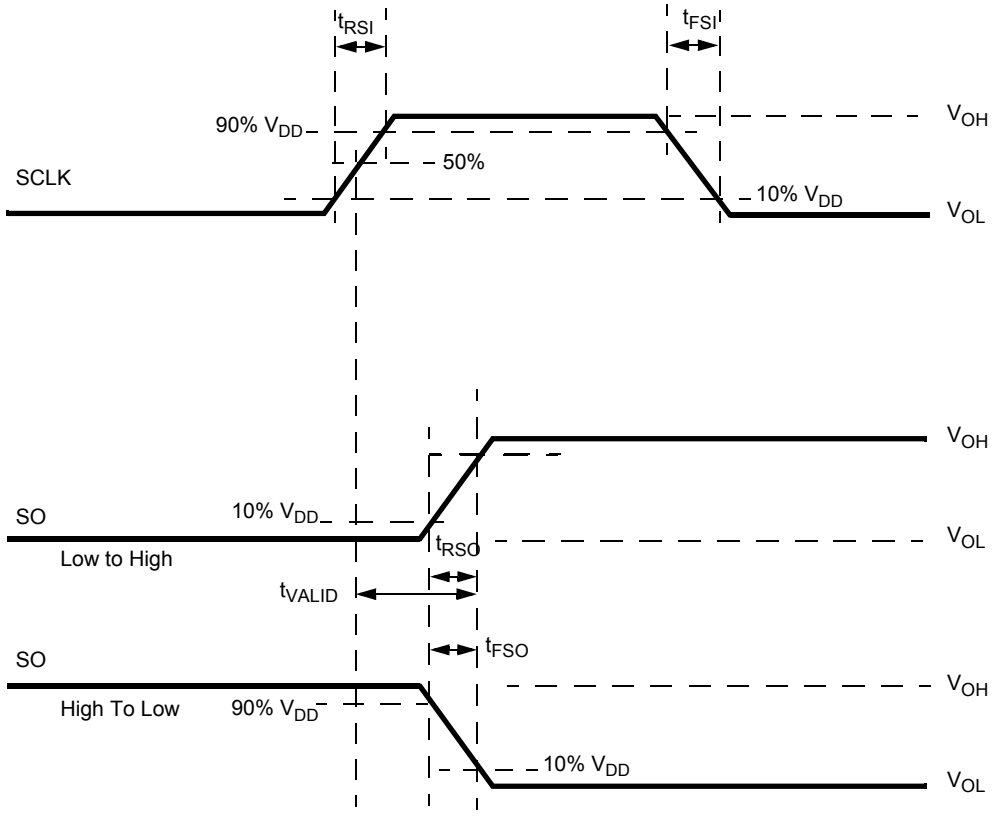


Figure 8. Timing diagram for serial output (SO) data communication

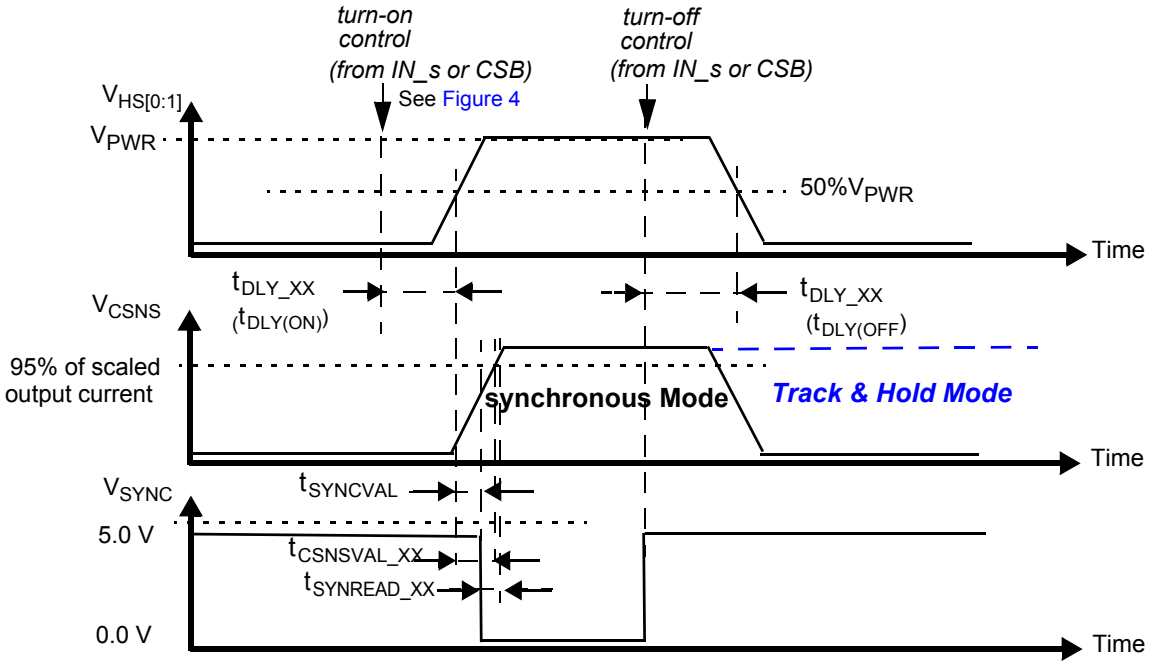


Figure 9. Synchronous and track-and-hold current sensing modes: associated delay and settling times

Functional description

Introduction

The 50XSD200 is a two-channel, 24 V high-side switch with integrated control and diagnostics designed for industrial applications. The device provides a high number of protective functions. Both low $R_{DS(on)}$ channels (<50 mΩ) can independently drive various load types like light bulbs, solenoid actuators, or DC motors. Device control and diagnostics are configured through a 16-bit SPI port with daisy chain capability.

Independently programmable output voltage slew rates allow satisfying electromagnetic compatibility (EMC) requirements.

Both channels can independently be operated in three different switching modes: internal clock and internal PWM mode (fully autonomous operation), external clock and internal PWM mode, and direct control switching mode.

Current sensing with an adjustable ratio is available on both channels, allowing both high current (bulbs) and low current (LED) monitoring. By activating the Track & Hold Mode, current monitoring can be performed during the switch-Off phase. This allows random access to the current sense functionality. A patented offset compensation technique further enhances current sense accuracy.

To avoid turning off upon inrush current, while being able to monitor it, the device features a dynamic overcurrent threshold profile. For bulbs, this profile is a stair function with stages of which the height and width are programmable through the SPI port. DC motors can be protected from overheating by activating a specific window-shaped overcurrent profile that allow stall currents of limited duration.

Whenever communication with the external micro-controller is lost, the device enters Fail-safe operation mode, but remains operational, controllable, and protected.

Pin assignment and functions

Functions and register bits that are implemented independently for both channels have extension "_s". Max. ratings of the pins are given in Table 3.

Output current monitoring (CSNS)

The CS pin allows independent current monitoring of channel 0 or channel 1 up to the steady-state overcurrent threshold. It can also be used to sense the device temperature. The different functions are selected by setting bits CSNS1_en and CSNS0_en to the appropriate value (Table 23). When the CSNS pin is sensed during switch-off in the (optional) track & hold mode (see Figure 9), it outputs the scaled value of the load current as it was just before turn-Off. When several devices share the same pull-down resistor, the CSNS pins of devices the current of which is not monitored must be tri-stated. This is accomplished by setting CSNS0_en = 0 and CSNS1_en = 0 in the GCR register (Table 10). Settling time ($t_{CSNSVAL\_XX}$) is defined as the time between the instant at the middle of the output voltage's rising edge (HS[0:1] = 50% of V_{PWR}), and the instant at which the voltage on the CSNS-pin has settled to ±5.0% of its final value. Anytime an overcurrent window is active, the CSNS pin is disabled (see Overcurrent detection on resistive and inductive loads). The current and temperature sensing functions are unavailable in Fail-safe mode and in Normal mode when operating without the V_{DD} supply voltage. In order to generate a voltage output, a pull-down resistor is required (R(CSNS)=1.0 kΩ typ. and 470 < R(CSNS) < 10 k). When the current sense resistor connected to the CSNS pin is disconnected, the CSNS voltage is clamped to $V_{CL(CSNS)}$. The CSNS pin can source currents up to about 5.6 mA.

Current sense synchronization (SYNC)

To synchronize current sensing with an external process, the SYNC signal can be connected to a digital input of an external MCU. SYNC is asserted logic low when the current sense signal is accurate and ready to be read. The current sense signal on the CSNS pin has the specified accuracy $t_{SYNREAD\_XX}$ seconds after the falling edge on the SYNC pin (Figure 9) and remains valid until a rising edge is generated. The rising edge that is generated by the SYNC pin at the turn-OFF instant (internal or external) may also be used to implement synchronization with the external MCU. Parameter $t_{SYNCVAL\_XX}$ is defined as the time between the instant at the middle of the output-voltage rising edge (HS[0:1] = 50% of VPWR), and the instant at which the voltage on the SYNC-pin drops below 0.4 V (V_{SOL}). The SYNC pins of different devices can be connected together to save µ-controller input channels. However, in this configuration, the CSNS function of only one device should be active at a time. Otherwise, the MCU does not determine the origin of the SYNC signal. The SYNC pin is open drain and requires an external pull-up resistor to VDD.

Direct control inputs (IN0 and IN1)

The IN[0:1] pins allow direct control of both channels. A logic [0] level turns off the channel and a logic[1] level turns it on (Channel control in normal mode). When the device is in Sleep mode, a transition from logic 0 to logic 1 on any of these pins wake it up (Sleep mode). If it is desired to automatically turn on the channels after a transition to Fail-safe mode, inputs IN[0] and IN[1] must be externally connected to the VPWR pin by a pull-up resistor (e.g. 10 kΩ typ.). However, this prevents the device from going into Sleep mode. Both IN pins are internally connected to a pull-down resistor.

Configuration inputs (conf0 and conf1)

The CONF[0:1] input pins allow configuring both channels for the appropriate load type. CONF = 0 activates the bulb overcurrent protection profile, and CONF = 1 the DC motor profile. These inputs are connected to an internal voltage regulator of 3.3 V by an internal pull-up current source I_{UP}. Therefore, CONF = 1 is the default value when these pins are disconnected. Details on how to configure the channels are given in Table 9.

Fault status (FSB)

This open drain output is asserted low when any of the following faults occurs (see Fault mode): overcurrent (OC), overtemperature (OT), Output connected to V_{PWR}, Severe short-circuit (SC), open load in ON state (OL_ON), open load in OFF state (OL_OFF), External Clock-fail (CLOCK_fail), overvoltage (OV), undervoltage (UV). Each fault type has its own assigned bit inside the STATR, FAULTR_s, or DIAGR_s register. Fault type identification and fault bit reset are accomplished by reading out these registers. They are part of the SO register (Fault mode) and are accessed through the SPI port.

Pwm clock (clock)

This pin is the input for an external clock signal that controls the internal PWM module.The clock signal is monitored by the device. The PWM module controls ON-time and turn-ON delay of the selected channels. The CLOCK pin should not be confused with the SCLK pin, which is the clock pin of the SPI interface. CLOCK has an internal pull-down current source (I_{DWN}) to GND.

Reset (RSTB)

All SPI register contents are reset when RSTB = 0. When RSTB = 0, the device returns to Sleep mode t_{IN} sec. after the last falling edge of the last active IN[0:1] signal. As long as the Reset input (RSTB pin) is at logic 0 and both direct input states are low, the device remains in Sleep mode (Channel configuration through the SPI). A 0-to-1 transition on RSTB wakes up the device and starts a watchdog timer to check the continuous presence of the SPI signals. To do this, the device monitors the contents of the first bit (WDIN bit) of all SPI words following that transition (regardless the register it is contained in). When this contents is not alternated within a duration t_{WDTO}, SPI communication is considered lost, and Fail-safe mode is entered (Entering fail-safe mode). RSTB is internally pulled-down to GND by resistor R_{DWN}.

Chip select (CSB)

Data communication over the SPI port is enabled when the CSB pin is in the logic [0] state. Data from the Input Shift registers are locked in the addressed SI registers on the rising edge of CSB. The device transfers the contents of one of the eight internal registers to the SO register on the falling edge of CSB. The SO output driver is enabled when CSB is logic [0]. CSB should transition from a logic [1] to a logic [0] state only when SCLK is at logic [0] (Figure 7 and Figure 8). CSB is internally pulled up to V_{DD} through I_{UP}.

SPI serial clock (SCLK)

The SCLK pin clocks the SPI data communication of the device. The serial input pin (SI) transfers data to the SI shift registers on the falling edge of the SCLK signal while data in the SO registers are transferred to the SO pin on the rising edge of the SCLK signal. The SCLK pin must be in low state when CSB makes any transition. For this reason, it is recommended to have the SCLK pin in the logic [0] state when the device is not accessed (CSB is at logic [1]). When CSB is set to logic [1], the signals at the SCLK and SI pins are ignored and the SO output is tri-stated (high-impedance). The SCLK pin is connected to an internal pull-down current source I_{DWN}.

Serial input (SI)

Serial input (SI) data bits are shifted in at this pin. SI data is read on the falling edge of SCLK. 16-bit data packages are required on the SI pin (see Figure 7), starting with bit D15 (MSB) and ending with D0 (LSB). All the internal device registers are addressed and controlled by a 4-bit address (D9-D12) described in Table 14. Register addresses and function attribution are described in Table 15. The SI pin is internally connected to a pull-down current source, I_{DWN}.

Supply of the digital circuitry (VDD)

This pin supplies the SPI circuit (3.3 V or 5.0 V). When lost, all circuitry becomes supplied by a V_{PWR} derived voltage, except the SPI's SO shift-register that can no longer be read.

Ground (GND)

This is the GND pin common for both the SPI and the other circuitry.

Positive supply pin (VPWR)

This pin is the positive supply and the common input pin of both switches. A 100 nF ceramic capacitor must be connected between VPWR and GND, close to the device. In addition, it is recommended to put a ceramic capacitor of at least 1.0 µF in parallel with this 100 nF capacitor.

Serial output (SO)

The SO pin is a tri-stateable output pin that conveys data from one of the 13 internal SO registers or from the previous SI register to the outside world. The SO pin remains in a high-impedance state (tri-state) until the CSB pin becomes logic [0]. It then transfers the SPI data (device state, configuration, fault information). The SO pin changes state at the rising edge of the SCLK signal. For daisy-chaining, it can be read out on the falling edge of SCLK. V_{DD} must be present before the SO registers can be read. The SO register assignment is described in Table 13.

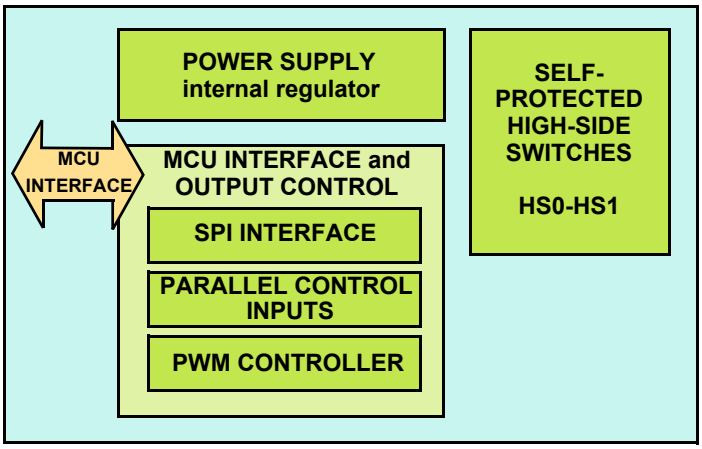
Power switch output pins (HS0 and HS1)

HS0 and HS1 are the output pins of the power switches, to be connected to the loads. A ceramic capacitor (<= 22 nF (+/- 20%) is recommended between these pins and GND for optimal EMC performances.

Fail-safe output (FSOB)

This pin (active low) is used to indicate loss of SPI communication or loss of SPI supply voltage, V_{DD}. This open drain output requires an external pull-up resistor to VPWR.

Functional internal block description



Power supply

The device operates with supply voltages from 6.0 V to 58 V (V_{PWR}), but is full spec. compliant between 8.0 V and 36 V. The VPWR pin supplies power to the internal regulator, analog, and logic circuit blocks. The VDD pin (5.0 V typ.) supplies the output register of the serial peripheral interface (SPI). Consequently, the SPI registers cannot be read without presence of V_{DD}. The employed IC architecture guarantees a low quiescent current in Sleep mode.

Switch output pins HS0 & HS1

HS0 and HS1 are the output pins of the power switches. Both channels are protected against various kinds of short-circuits and have active clamp circuitry that may be activated when switching off inductive loads. Many protective and diagnostic functions are available. For large inductive loads, it is recommended to use a freewheeling diode. The device can be configured to control the output switches in parallel, which guarantees good switching synchronization.

Communication interface and device control

In Normal mode the output channels can either be controlled by the direct inputs or by the internal PWM module, which is configured by the SPI register settings. For bidirectional SPI communication, V_{DD} has to be in the authorized range. Failure diagnostics and configuration are also performed through the SPI port. The reported failure types are: open load, short-circuit to supply, severe short-circuit to ground, overcurrent, overtemperature, clock-fail, undervoltage, and overvoltage. The SPI port can be supplied either by a 5.0 V or by a 3.3 V voltage supply. For direct input control, V_{DD} is not required.

A Pulse Width Modulation (PWM) circuit allows driving loads at frequencies up to 1.0 kHz from an external or an internal clock. SPI communication is required to set these options.