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Freescale Semiconductor
Technical Data

Document Number: MC56F8006
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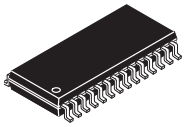
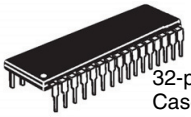
MC56F8006/MC56F8002





MC56F8006/MC56F8002 Digital Signal Controller

This document applies to parts marked with 2M53M.

The 56F8006/56F8002 is a member of the 56800E core-based family of digital signal controllers (DSCs). It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create a cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56F8006/56F8002 is well-suited for many applications. It includes many peripherals that are especially useful for cost-sensitive applications, including:

- Industrial control
- Home appliances
- Smart sensors
- Fire and security systems
- Switched-mode power supply and power management
- Power metering
- Motor control (ACIM, BLDC, PMSM, SR, and stepper)
- Handheld power tools
- Arc detection
- Medical device/equipment
- Instrumentation
- Lighting ballast

The 56800E core is based on a dual Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The 56F8006/56F8002 supports program execution from internal memories. Two data operands can be accessed from the on-chip data RAM per instruction cycle. The 56F8006/56F8002 also offers up to 40 general-purpose input/output (GPIO) lines, depending on peripheral configuration.

The 56F8006/56F8002 digital signal controller includes up to 16 KB of program flash and 2 KB of unified data/program RAM. Program flash memory can be independently bulk erased or erased in small pages of 512 bytes (256 words).

On-chip features include:

- Up to 32 MIPS at 32 MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- On-chip memory
  - 56F8006: 16 KB (8K x 16) flash memory
  - 56F8002: 12 KB (6K x 16) flash memory
  - 2 KB (1K x 16) unified data/program RAM
- One 6-channel PWM module
- Two 28-channel, 12-bit analog-to-digital converters (ADCs)
- Two programmable gain amplifiers (PGA) with gain up to 32x
- Three analog comparators
- One programmable interval timer (PIT)
- One high-speed serial communication interface (SCI) with LIN slave functionality
- One serial peripheral interface (SPI)
- One 16-bit dual timer (2 x 16 bit timers)
- One programmable delay block (PDB)
- One SMBus compatible inter-integrated circuit (I^2C) port
- One real time counter (RTC)
- Computer operating properly (COP)/watchdog
- Two on-chip relaxation oscillators — 1 kHz and 8 MHz (400 kHz at standby mode)
- Crystal oscillator
- Integrated power-on reset (POR) and low-voltage interrupt (LVI) module
- JTAG/enhanced on-chip emulation (OnCE™) for unobtrusive, real-time debugging
- Up to 40 GPIO lines
- 28-pin SOIC, 32-pin LQFP, 32-pin PSDIP, and 48-pin LQFP packages

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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Table of Contents

1 MC56F8006/MC56F8002 Family Configuration

MC56F8006/MC56F8002 device comparison in Table 1.

Table 1. MC56F8006 Series Device Comparison

Feature	MC56F8006			MC56F8002
	28-pin	32-pin	48-pin	28-pin
Flash memory size (Kbytes)	16			12
RAM size (Kbytes)	2			
Analog comparators (ACMP)	3			
Analog-to-digital converters (ADC)	2			
Unshielded ADC inputs	6	7	7	6
Shielded ADC inputs	9	11	17	9
Total number of ADC input pins[1]	15	18	24	15
Programmable gain amplifiers (PGA)	2			
Pulse-width modulator (PWM) outputs	6			
PWM fault inputs	3	4	4	3
Inter-integrated circuit (IIC)	1			
Serial peripheral interface (SPI)	1			
High speed serial communications interface (SCI)	1			
Programmable interrupt timer (PIT)	1			
Programmable delay block (PDB)	1			
16-bit multi-purpose timers (TMR)	2			
Real-time counter (RTC)	1			
Computer operating properly (COP) timer	Yes			
Phase-locked loop (PLL)	Yes			
1 kHz on-chip oscillator	Yes			
8 MHz (400 kHz at standby mode) on-chip ROSC	Yes			
Crystal oscillator	Yes			
Power management controller (PMC)	Yes			
IEEE 1149.1 Joint Test Action Group (JTAG) interface	Yes			
Enhanced on-chip emulator (EOnCE) IEEE 1149.1 Joint Test Action Group (JTAG) interface	Yes			

[1] Some ADC inputs share the same pin. See Table 4.

2 Block Diagram

Figure 1 shows a top-level block diagram of the MC56F8006/MC56F8002 digital signal controller. Package options for this family are described later in this document. Italics indicate a 56F8002 device parameter.

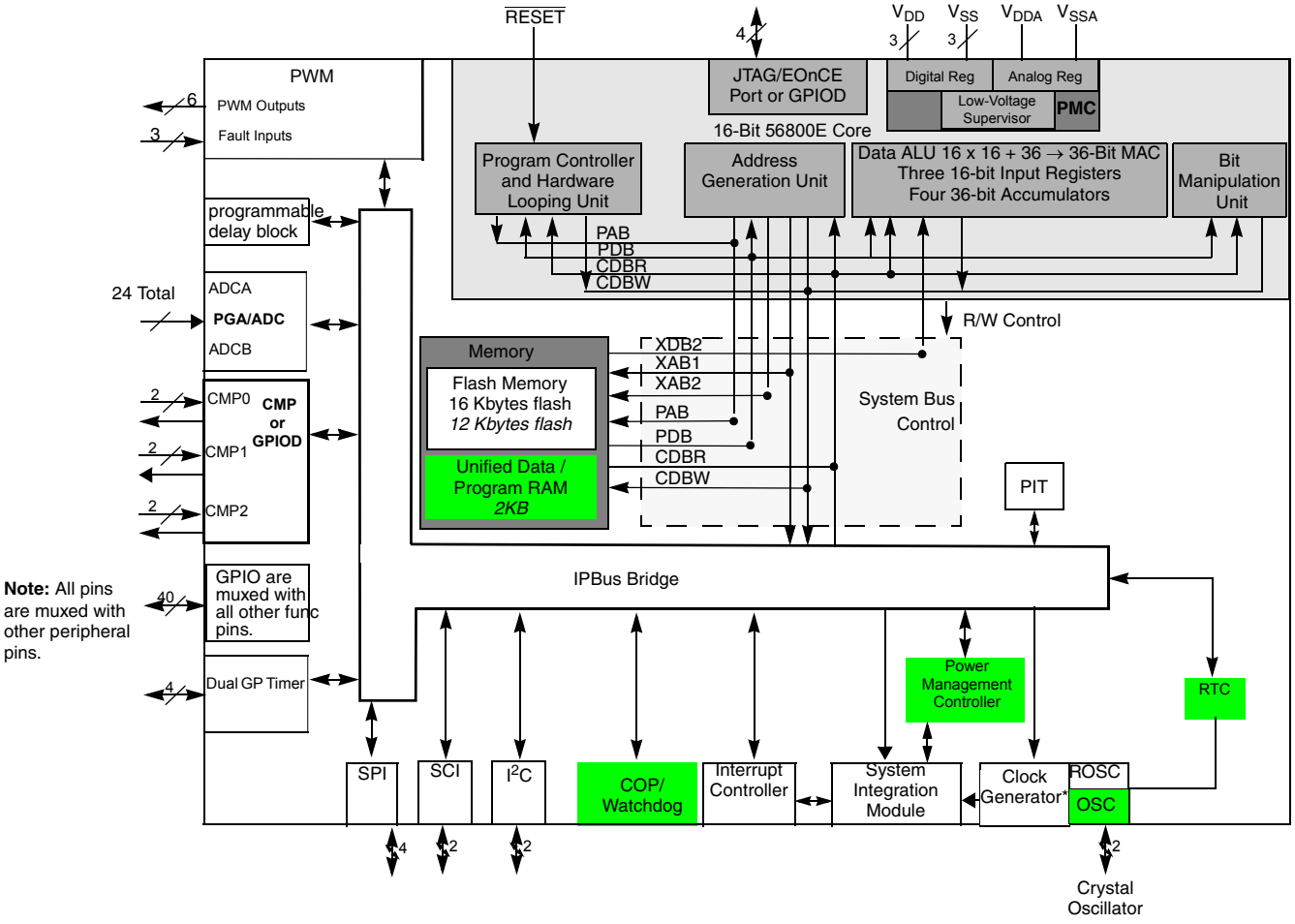

Figure 1. MC56F8006/MC56F8002 Block Diagram

3 Overview

3.1 56F8006/56F8002 Features

3.1.1 Core

- Efficient 16-bit 56800E family digital signal controller (DSC) engine with dual Harvard architecture
- As many as 32 million instructions per second (MIPS) at 32 MHz core frequency
- 155 basic instructions in conjunction with up to 20 address modes
- Single-cycle 16 × 16-bit parallel multiplier-accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 32-bit arithmetic and logic multi-bit shifter

- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses
- Four internal data buses
- Instruction set supports DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/enhanced on-chip emulation (EOnCE) for unobtrusive, processor speed–independent, real-time debugging

3.1.2 Operation Range

- 1.8 V to 3.6 V operation (power supplies and I/O)
- From power-on-reset: approximately 1.9 V to 3.6 V
- Ambient temperature operating range:
  - –40 °C to 125 °C

3.1.3 Memory

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Flash security and protection that prevent unauthorized users from gaining access to the internal flash
- On-chip memory
  - 16 KB of program flash for 56F8006 and 12 KB of program flash for 56F8002
  - 2 KB of unified data/program RAM
- EEPROM emulation capability using flash

3.1.4 Interrupt Controller

- Five interrupt priority levels
  - Three user programmable priority levels for each interrupt source: Level 0, 1, 2
  - Unmaskable level 3 interrupts include: illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction. Maskable level 3 interrupts include: EOnCE step counter, EOnCE breakpoint unit, EOnCE trace buffer
  - Lowest-priority software interrupt: level LP
- Allow nested interrupt that higher priority level interrupt request can interrupt lower priority interrupt subroutine
- The masking of interrupt priority level is managed by the 56800E core
- One programmable fast interrupt that can be assigned to any interrupt source
- Notification to system integration module (SIM) to restart clock out of wait and stop states
- Ability to relocate interrupt vector table

3.1.5 Peripheral Highlights

- One multi-function, six-output pulse width modulator (PWM) module
  - Up to 96 MHz PWM operating clock
  - 15 bits of resolution
  - Center-aligned and edge-aligned PWM signal mode
  - Phase shifting PWM pulse generation

  - Four programmable fault inputs with programmable digital filter
  - Double-buffered PWM registers
  - Separate deadtime insertions for rising and falling edges
  - Separate top and bottom pulse-width correction by means of software
  - Asymmetric PWM output within both Center Aligned and Edge Aligned operation
  - Separate top and bottom polarity control
  - Each complementary PWM signal pair allows selection of a PWM supply source from:
    - PWM generator
    - Internal timers
    - Analog comparator outputs
- Two independent 12-bit analog-to-digital converters (ADCs)
  - 2 x 14 channel external inputs plus seven internal inputs
  - Support simultaneous and software triggering conversions
  - ADC conversions can be synchronized by PWM and PDB modules
  - Sampling rate up to 400 KSPS for 10- or 12-bit conversion result; 470 KSPS for 8-bit conversion result
  - Two 16-word result registers
- Two programmable gain amplifier (PGAs)
  - Each PGA is designed to amplify and convert differential signals to a single-ended value fed to one of the ADC inputs
  - 1X, 2X, 4X, 8X, 16X, or 32X gain
  - Software and hardware triggers are available
  - Integrated sample/hold circuit
  - Includes additional calibration features:
    - Offset calibration eliminates any errors in the internal reference used to generate the VDDA/2 output center point
    - Gain calibration can be used to verify the gain of the overall datapath
    - Both features require software correction of the ADC result
- Three analog comparators (CMPs)
  - Selectable input source includes external pins, internal DACs
  - Programmable output polarity
  - Output can drive timer input, PWM fault input, PWM source, external pin output, and trigger ADCs
  - Output falling and rising edge detection able to generate interrupts
- One dual channel 16-bit multi-purpose timer module (TMR)
  - Two independent 16-bit counter/timers with cascading capability
  - Up to 96 MHz operating clock
  - Each timer has capture and compare and quadrature decoder capability
  - Up to 12 operating modes
  - Four external inputs and two external outputs
- One serial communication interface (SCI) with LIN slave functionality
  - Up to 96 MHz operating clock
  - Full-duplex or single-wire operation
  - Programmable 8- or 9- bit data format
  - Two receiver wakeup methods:
    - Idle line
    - Address mark

  - 1/16 bit-time noise detection
- One serial peripheral interface (SPI)
  - Full-duplex operation
  - Master and slave modes
  - Programmable length transactions (2 to 16 bits)
  - Programmable transmit and receive shift order (MSB as first or last bit transmitted)
  - Maximum slave module frequency = module clock frequency/2
- One inter-integrated Circuit (I^2C) port
  - Operates up to 400 kbps
  - Supports master and slave operation
  - Supports 10-bit address mode and broadcasting mode
  - Supports SMBus, Version 2
- One 16-bit programmable interval timer (PIT)
  - 16 bit counter with programmable counter modulo
  - Interrupt capability
- One 16-bit programmable delay block (PDB)
  - 16 bit counter with programmable counter modulo and delay time
  - Counter is initiated by positive transition of internal or external trigger pulse
  - Supports two independently controlled delay pulses used to synchronize PGA and ADC conversions with input trigger event
  - Two PDB outputs can be ORed together to schedule two conversions from one input trigger event
  - PDB outputs can be can be used to schedule precise edge placement for a pulsed output that generates the control signal for the CMP windowing comparison
  - Supports continuous or single shot mode
  - Bypass mode supported
- Computer operating properly (COP)/watchdog timer capable of selecting different clock sources
  - Programmable prescaler and timeout period
  - Programmable wait, stop, and partial powerdown mode operation
  - Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
  - Choice of clock sources from four sources in support of EN60730 and IEC61508:
    - On-chip relaxation oscillator
    - External crystal oscillator/external clock source
    - System clock (IPBus up to 32 MHz)
    - On-chip low power 1 kHz oscillator
- Real-timer counter (RTC)
  - 8-bit up-counter
  - Three software selectable clock sources
    - External crystal oscillator/external clock source
    - On-chip low-power 1 kHz oscillator
    - System bus (IPBus up to 32 MHz)
  - Can signal the device to exit power down mode
- Phase lock loop (PLL) provides a high-speed clock to the core and peripherals
  - Provides 3x system clock to PWM and dual timer and SCI
  - Loss of lock interrupt
  - Loss of reference clock interrupt

- Clock sources
  - On-chip relaxation oscillator with two user selectable frequencies: 400 kHz for low speed mode, 8 MHz for normal operation
  - On-chip low-power 1 kHz oscillator can be selected as clock source to the RTC and/or COP
  - External clock: crystal oscillator, ceramic resonator, and external clock source
- Power management controller (PMC)
  - On-chip regulator for digital and analog circuitry to lower cost and reduce noise
  - Integrated power-on reset (POR)
  - Low-voltage interrupt with a user selectable trip voltage of 1.81 V or 2.31 V
  - User selectable brown-out reset
  - Run, wait, and stop modes
  - Low-power run, wait, and stop modes
  - Partial power down mode
- Up to 40 general-purpose I/O (GPIO) pins
  - Individual control for each pin to be in peripheral or GPIO mode
  - Individual input/output direction control for each pin in GPIO mode
  - Hysteresis and configurable pullup device on all input pins
  - Configurable slew rate and drive strength and optional input low pass filters on all output pins
  - 20 mA sink/source current
- JTAG/EOnCE debug programming interface for real-time debugging
  - IEEE 1149.1 Joint Test Action Group (JTAG) interface
  - EOnCE interface for real-time debugging

3.1.6 Power Saving Features

- Three low power modes
  - Low-speed run, wait, and stop modes: 200 kHz IP bus clock provided by ROSC
  - Low-power run, wait, and stop modes: clock provided by external 32–38.4 kHz crystal
  - Partial power down mode
- Low power external oscillator can be used in any low-power mode to provide accurate clock to active peripherals
- Low power real time counter for use in run, wait, and stop modes with internal and external clock sources
- 32 µs typical wakeup time from partial power down modes
- Each peripheral can be individually disabled to save power

3.2 Award-Winning Development Environment

Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs), demonstration board kit, and development system cards support concurrent engineering. Together, PE, CodeWarrior, and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

A full set of programmable peripherals — PWM, PGAs, ADCs, SCI, SPI, I^2C, PIT, timers, and analog comparators — supports various applications. Each peripheral can be independently shut down to save power. Any pin in these peripherals can also be used as general-purpose input/outputs (GPIOs).

3.3 Architecture Block Diagram

The 56F8006/56F8002's architecture is shown in Figure 2 and Figure 3. Figure 2 illustrates how the 56800E system buses communicate with internal memories and the IPBus interface and the internal connections among each unit of the 56800E core. Figure 3 shows the peripherals and control blocks connected to the IPBus bridge. Please see the system integration module (SIM) section in the *MC56F8006 Reference Manual* for information about which signals are multiplexed with those of other peripherals.

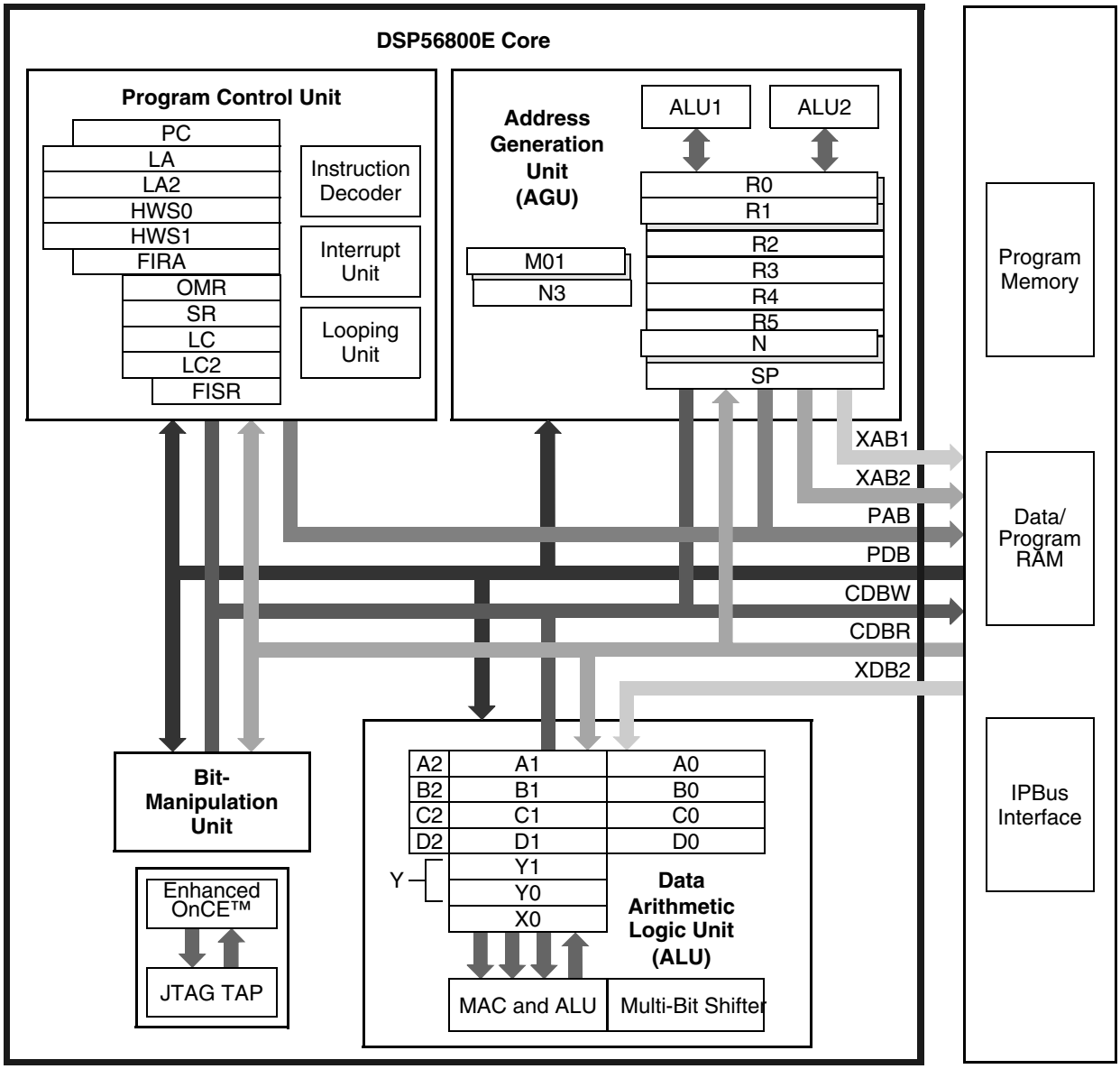

Figure 2. 56800E Core Block Diagram

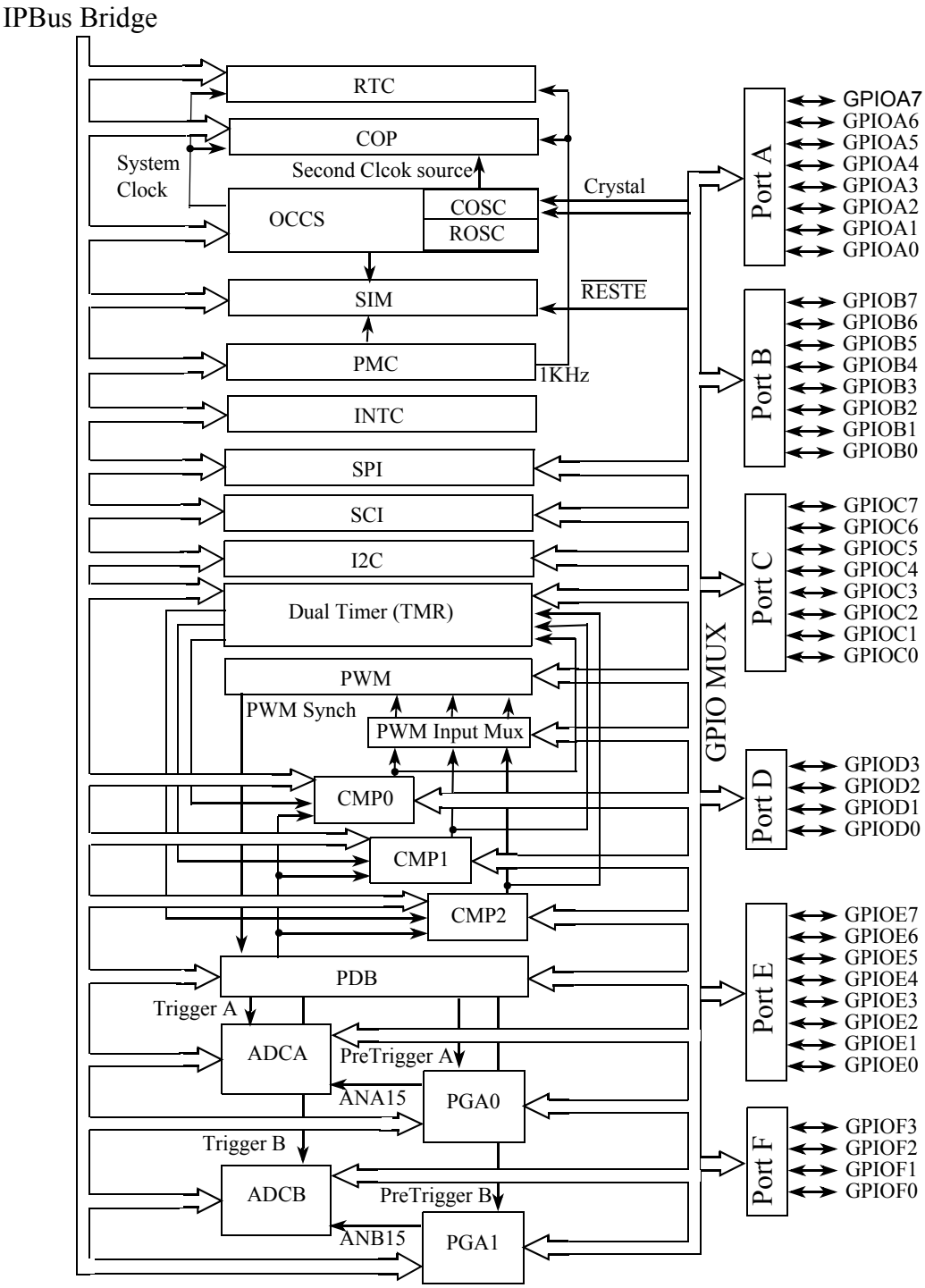

Figure 3. Peripheral Subsystem

3.4 Product Documentation

The documents listed in Table 2 are required for a complete description and proper design with the 56F8006/56F8002. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at http://www.freescale.com.

Table 2. 56F8006/56F8002 Device Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, 16-bit digital signal controller core processor, and the instruction set	DSP56800ERM
56F800x Peripheral Reference Manual	Detailed description of peripherals of the 56F8006 and 56F8002 devices	MC56F8006RM
56F80x Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the 56F800x family of devices	TBD
56F8006/56F8002 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	MC56F8006
56F8006/56F8002 Errata	Details any chip issues that might be present	MC56F8006E

4 Signal/Connection Descriptions

4.1 Introduction

The input and output signals of the 56F8006/56F8002 are organized into functional groups, as detailed in Table 3. Table 4 summarizes all device pins. In Table 4, each table row describes the signal or signals present on a pin, sorted by pin number.

Table 3. Functional Group Pin Allocations

Functional Group	Number of Pins in 28 SOIC	Number of Pins in 32 LQFP	Number of Pins in 32 PSDIP	Number of Pins in 48 LQFP
Power Inputs (V_{DD}, V_{DDA})	2	2	2	4
Ground (V_{SS}, V_{SSA})	3	3	3	4
Reset[1]	1	1	1	1
Pulse Width Modulator (PWM) Ports[1]	10	12	12	12
Serial Peripheral Interface (SPI) Ports[1]	5	7	7	7
Serial Communications Interface 0 (SCI) Ports[1]	4	5	5	5
Inter-Integrated Circuit Interface (I^2C) Ports[1]	6	7	7	7
Analog-to-Digital Converter (ADC) Inputs[1]	16	18	18	24
High Speed Analog Comparator Inputs[1]	13	15	15	25
Programmable Gain Amplifiers (PGA)[1]	4	4	4	4
Dual Timer Module (TMR) Ports[1]	8	10	10	10
Programmable Delay Block (PDB)[1]	—	—	—	1
Clock[1]	5	5	5	5
JTAG/Enhanced On-Chip Emulation (EOnCE[1])	4	4	4	4

[1] Pins may be shared with other peripherals. See Table 4.

In Table 4, peripheral pins in bold identify reset state.

Table 4. 56F8006/56F8002 Pins

Pin Number				Pin Name	Peripherals												
28 SOIC	32 LQFP	32 PSDIP	48 LQFP		GPIO	I^2C	SCI	SPI	ADC	PGA	COMP	Dual Timer	PWM	Power and Ground	JTAG	Misc.
26	1	29	1	GPIOB6/*RXD/SDA/ANA13 and CMP0_P2/CLKIN*	B6	SDA	RXD		ANA13[1]		CMP0_P2					CLKIN
27	2	30	2	GPIOB1/*$\overline{SS}$/SDA/ANA12 andCMP2_P3*	B1	SDA		$\overline{SS}$	ANA12[1]		CMP2_P3					
	3	31	3	GPIOB7/*TXD/SCL/ANA11 and CMP2_M3*	B7	SCL	TXD		ANA11[1]		CMP2_M3					
	4	32	4	GPIOB5/*T1/FAULT3/SCLK*	B5			SCLK				T1	FAULT3			
			5	GPIOE0	E0											
			6	GPIOE1/*ANB9 and CMP0_P1*	E1				ANB9[1]		CMP0_P1					
28	5	1	7	ANB8 and PGA1+ and CMP0_M2/*GPIOC4*	C4				ANB8[1]	PGA1+	CMP0_M2					
			8	GPIOE2/*ANB7 and CMP0_M1*	E2				ANB7[1]		CMP0_M1					
1	6	2	9	ANB6 and PGA1– and CMP0_P4/*GPIOC5*	C5				ANB6[1]	PGA1–	CMP0_P4					
			10	GPIOC7/*ANB5 and CMP1_M2*	C7				ANB5[1]		CMP1_M2					
2	7	3	11	ANB4 and CMP1_P1/*GPIOC6/PWM2*	C6				ANB4[1]		CMP1_P1		PWM2			
3	8	4	12	V_{DDA}										V_{DDA}		
4	9	5	13	V_{SSA}										V_{SSA}		
			14	GPIOE3/*ANA10 and CMP2_M1*	E3				ANA10[1]		CMP2_M1					
5	10	6	15	ANA9 and PGA0– and CMP2_P4/*GPIOC2*	C2				ANA9[1]	PGA0–	CMP2_P4					
			16	GPIOE5/*ANA8 and CMP2_P1*	E5				ANA8[1]		CMP2_P1					
6	11	7	17	ANA7 and PGA0+ and CMP2_M2/*GPIOC1*	C1				ANA7[1]	PGA0+	CMP2_M2					
			18	GPIOE4/ANA6 and CMP2_P2	E4				ANA6[1]		CMP2_P2					
7	12	8	19	ANA5 and CMP1_M1/*GPIOC0/FAULT0*	C0				ANA5[1]		CMP1_M1		FAULT0			
8	13	9	20	V_{SS}										V_{SS}		
			21	V_{DD}										V_{DD}		
9	14	10	22	TCK/*GPIOD2/ANA4 and CMP1_P2/CMP2_OUT*	D2				ANA4[1]		CMP1_P2, CMP2_OUT				TCK	
10	15	11	23	$\overline{RESET}$/*GPIOA7*	A7											$\overline{RESET}$
11	16	12	24	GPIOB3/*MOSI/TIN3/ANA3 and ANB3/PWM5/CMP1_OUT*	B3			MOSI	ANA3[1] and ANB3[1]		CMP1_OUT	TIN3	PWM5			
	17	13	25	GPIOB2/*MISO/TIN2/ANA2 and ANB2/CMP0_OUT*	B2			MISO	ANA2 and ANB2		CMP0_OUT	TIN2				
12	18	14	26	GPIOA6/*FAULT0/ANA1 and ANB1/SCL/TXD/CLKO_1*	A6	SCL	TXD		ANA1 and ANB1				FAULT0			CLKO_1
13	19	15	27	GPIOB4/*T0/CLKO_0/MISO/ SDA/RXD/ANA0 and ANB0*	B4	SDA	RXD	MISO	ANA0 and ANB0			T0				CLKO_0

Table 4. 56F8006/56F8002 Pins (continued)

Pin Number				Pin Name	Peripherals												
28 SOIC	32 LQFP	32 PSDIP	48 LQFP		GPIO	I^2C	SCI	SPI	ADC	PGA	COMP	Dual Timer	PWM	Power and Ground	JTAG	Misc.
			28	GPIOE6	E6											
14	20	16	29	GPIOA5/*PWM5/FAULT2 or EXT_SYNC/TIN3*	A5							TIN3	PWM5, FAULT2 or EXT_ SYNC			
			30	V_{SS}										V_{SS}		
			31	V_{DD}										V_{DD}		
15	21	17	32	GPIOB0/*SCLK/SCL/ANB13/ PWM3/T1*	B0	SCL		SCLK	ANB13			T1	PWM3			
16	22	18	33	GPIOA4/*PWM4/SDA/FAULT1 /TIN2*	A4	SDA						TIN2	PWM4, FAULT1			
			34	GPIOE7/*CMP1_M3*	E7						CMP1_M3					
	23	19	35	GPIOA2/*PWM2*	A2								PWM2			
17	24	20	36	GPIOA3/*PWM3/TXD/EXTAL*	A3		TXD						PWM3			EXTAL
18	25	21	37	GPIOF0/*XTAL*	F0											XTAL
19	26	22	38	V_{DD}										V_{DD}		
20	27	23	39	V_{SS}										V_{SS}		
			40	GPIOF1/*CMP1_P3*	F1						CMP1_P3					
			41	GPIOF2/*CMP0_M3*	F2						CMP0_M3					
			42	GPIOF3/*CMP0_P3*	F3						CMP0_P3					
21	28	24	43	GPIOA1/*PWM1*	A1								PWM1			
22	29	25	44	GPIOA0/*PWM0*	A0								PWM0			
23	30	26	45	TDI/*GPIOD0/ANB12/$\overline{SS}$/ TIN2/CMP0_OUT*	D0			$\overline{SS}$	ANB12		CMP0_OUT	TIN2			TDI	
			46	GPIOC3/*EXT_TRIGGER*	C3											EXT_ TRGGER
24	31	27	47	TMS/*GPIOD3/ANB11/T1/ CMP1_OUT*	D3				ANB11		CMP1_OUT	T1			TMS	
25	32	28	48	**TDO**/*GPIOD1/ANB10/T0/ CMP2_OUT*	D1				ANB10		CMP2_OUT	T0			TDO	

1 Shielded ADC input.

4.2 Pin Assignment

MC56F8006 and MC56F8002 28-pin small outline IC (28SOIC) assignment is shown in Figure 4; MC56F8006 32-pin low-profile quad flat pack (32LQFP) is shown in Figure 5; MC56F8006 32-pin plastic shrink dual in-line package (PSDIP) is shown in Figure 6; MC56F8006 48-pin low-profile quad flat pack (48LQFP) is shown in Figure 7.

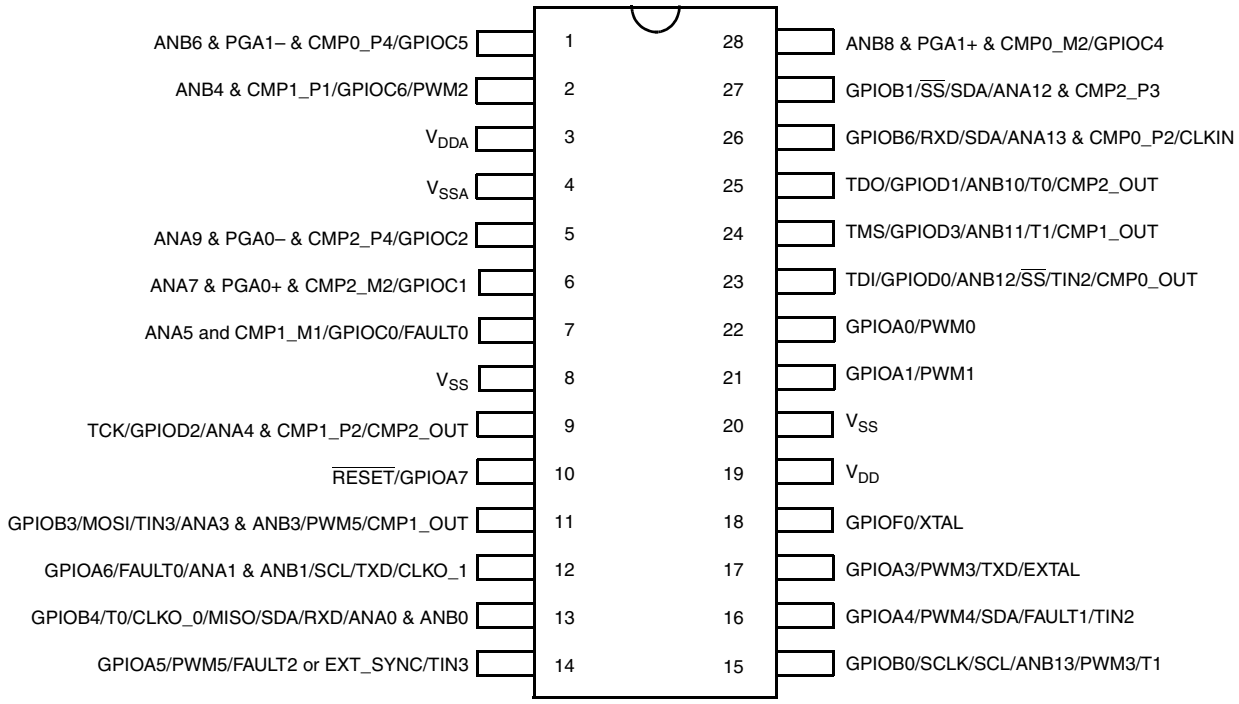

Figure 4. Top View, MC56F8006/MC56F8002 28-Pin SOIC Package

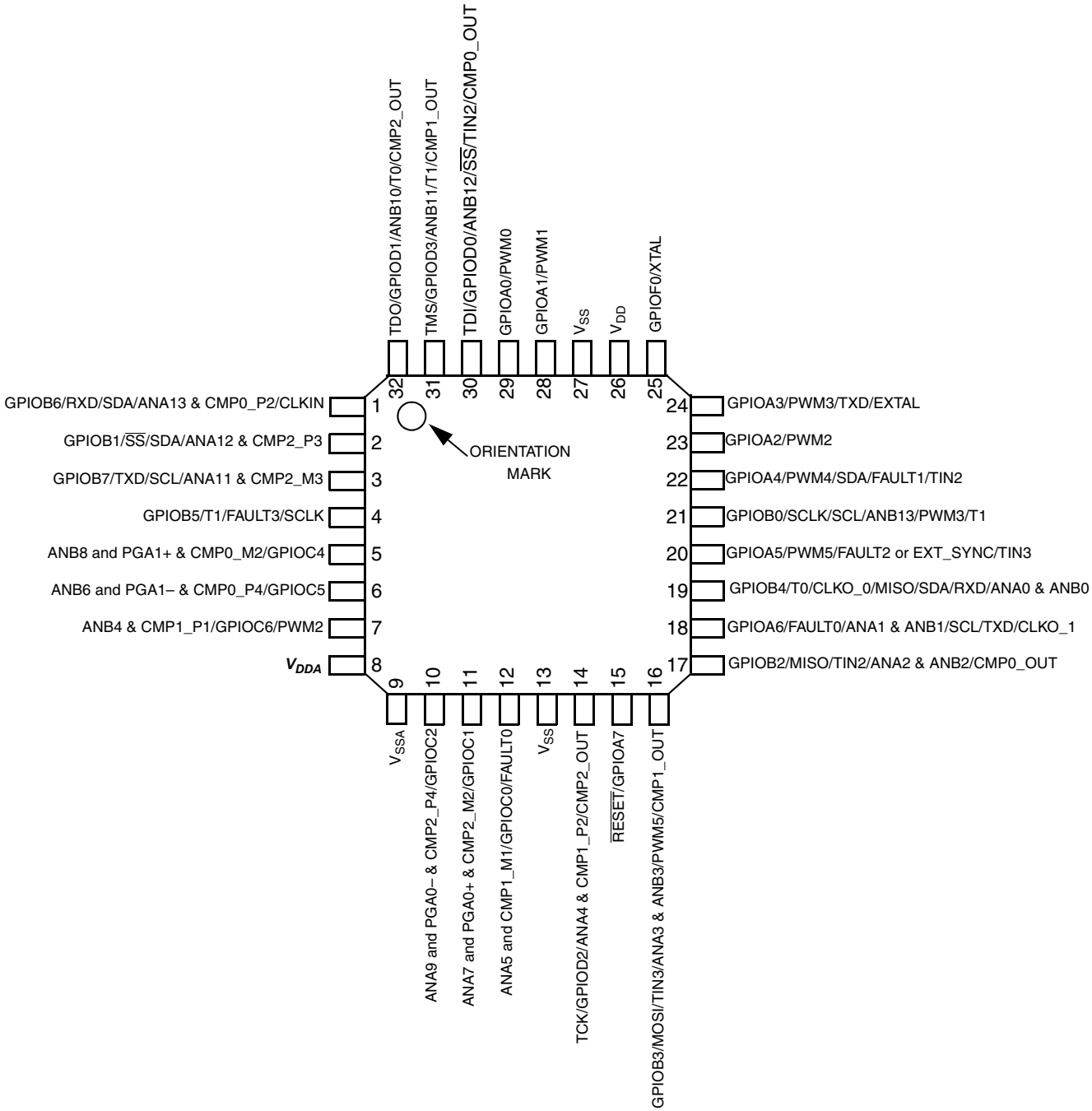

Figure 5. Top View, MC56F8006 32-Pin LQFP Package

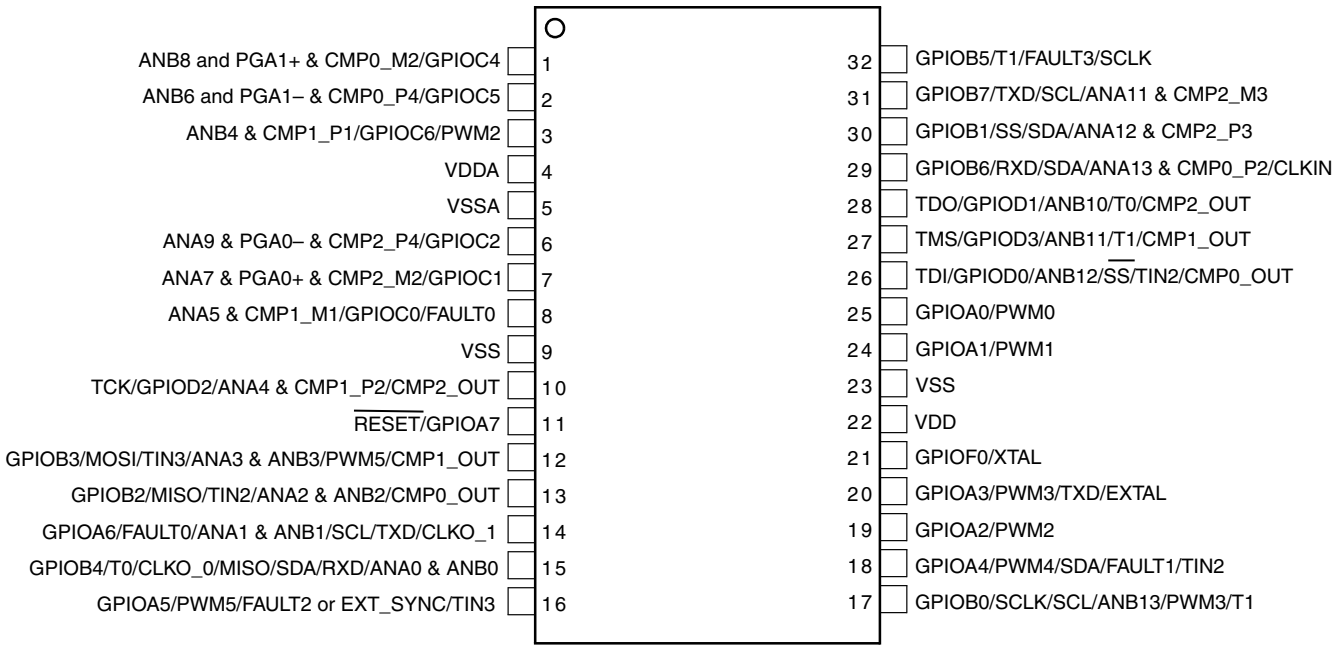

Figure 6. Top View, MC56F8006 32-Pin PSDIP Package

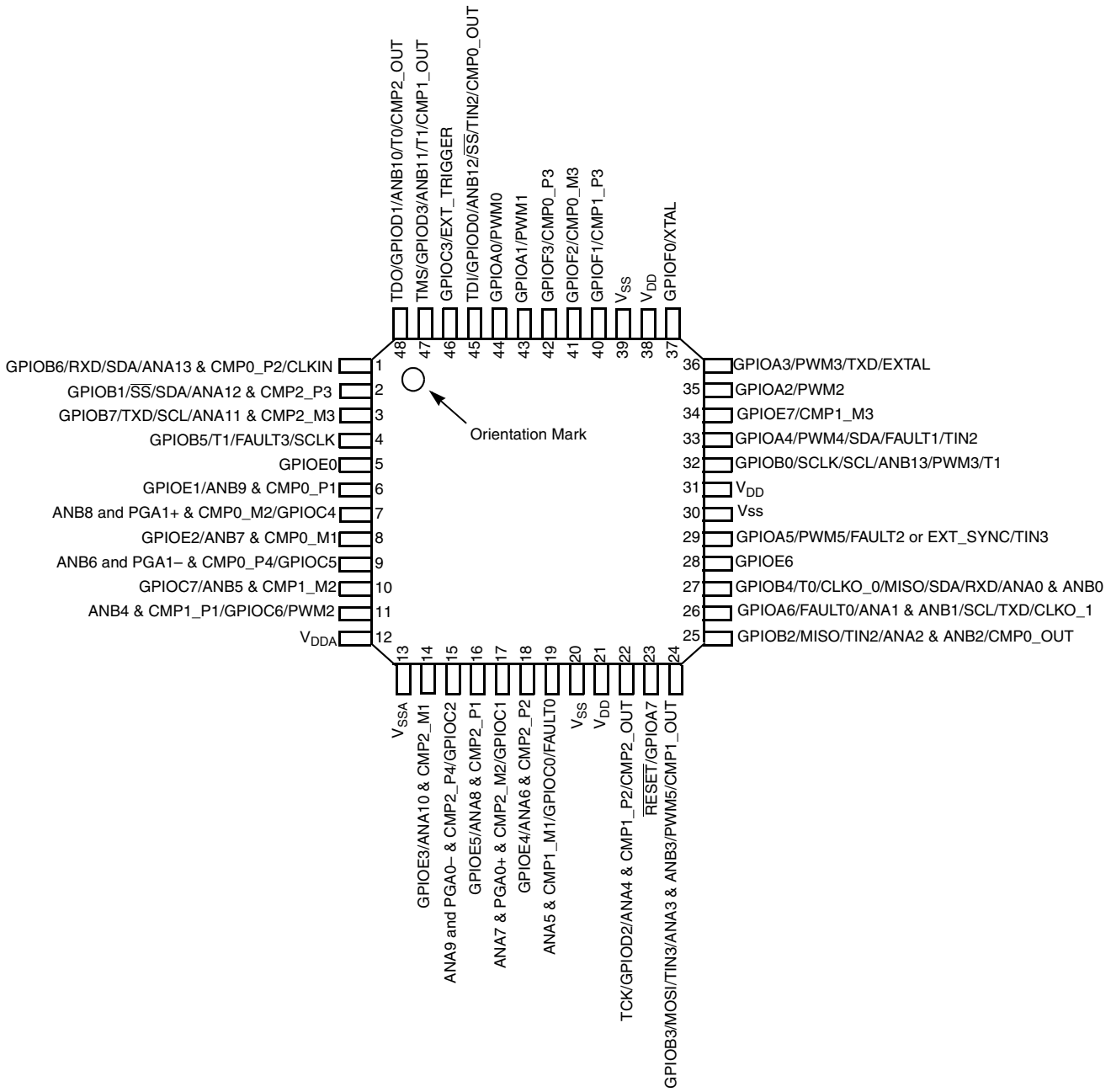

Figure 7. Top View, MC56F8006 48-Pin LQFP Package

4.3 56F8006/56F8002 Signal Pins

After reset, each pin is configured for its primary function (listed first). Any alternate functionality must be programmed via the GPIO module's peripheral enable registers (GPIO_x_PER) and SIM module's (GPS_xn) GPIO peripheral select registers. If CLKIN or XTAL is selected as device external clock input, the CLK_MOD bit in the OCCS oscillator control register (OSCTL) needs to be set too. EXT_SEL bit in OSCTL selects CLKIN or XTAL.

Table 5. 56F8006/56F8002 Signal and Package Information

Signal Name	28 SOIC	32 LQFP	32 PSDIP	48 LQFP	Type	State During Reset	Signal Description
V_{DD}				21	Supply	Supply	I/O Power — This pin supplies 3.3 V power to the chip I/O interface.
V_{DD}				31			
V_{DD}	19	26	22	38			
V_{SS}	8	13	9	20	Supply	Supply	I/O Ground — These pins provide ground for chip I/O interface.
V_{SS}				30			
V_{SS}	20	27	23	39			
V_{DDA}	3	8	4	12	Supply	Supply	Analog Power — This pin supplies 3.3 V power to the analog modules. It must be connected to a clean analog power supply.
V_{SSA}	4	9	5	13	Supply	Supply	Analog Ground — This pin supplies an analog ground to the analog modules. It must be connected to a clean power supply.
$\overline{\text{RESET}}$ (GPIOA7)	10	15	11	23	Input Input/ Output	Input, internal pullup enabled	Reset — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the reset state. A Schmitt-trigger input is used for noise immunity. The internal reset signal is deasserted synchronous with the internal clocks after a fixed number of internal clocks. Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. $\overline{\text{RESET}}$ functionality is disabled in this mode and the chip can be reset only via POR, COP reset, or software reset. After reset, the default state is $\overline{\text{RESET}}$.
GPIOA0 (PWM0)	22	29	25	44	Input/ Output Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM0 — The PWM channel 0. After reset, the default state is GPIOA0.
GPIOA1 (PWM1)	21	28	24	43	Input/ Output Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM1 — The PWM channel 1. After reset, the default state is GPIOA1.
GPIOA2 (PWM2)		23	19	35	Input/ Output Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM2 — The PWM channel 2. After reset, the default state is GPIOA2.

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

Signal Name	28 SOIC	32 LQFP	32 PSDIP	48 LQFP	Type	State During Reset	Signal Description
GPIOA3	17	24	20	36	Input/ Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin.
(PWM3)					Output		PWM3 — The PWM channel 3.
(TXD)					Output		TXD — The SCI transmit data output or transmit/receive in single wire operation.
(EXTAL)					Analog Input		EXTAL — External Crystal Oscillator Input. This input can be connected to a 32.768 kHz or 1–16 MHz external crystal or ceramic resonator. When used to supply a source to the internal PLL, the crystal/resonator must be in the 4 MHz to 8 MHz range. Tie this pin low or configure as GPIO if XTAL is being driven by an external clock source. If using a 32.768 kHz crystal, place the crystal as close as possible to device pins to speed startup. After reset, the default state is GPIOA3.
GPIOA4	16	22	18	33	Input/ Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin.
(PWM4)					Output		PWM4 — The PWM channel 4.
(SDA)					Input/Open-drain Output		SDA — The I^2C serial data line.
(FAULT1)					Input		FAULT1 — PWM fault input 1used for disabling selected PWM outputs in cases where fault conditions originate off-chip.
(TIN2)					Input		TIN2 — Dual timer module channel 2 input After reset, the default state is GPIOA4.
GPIOA5	14	20	16	29	Input/ Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin.
(PWM5)					Output		PWM5 — The PWM channel 5.
(FAULT2/ EXT_SYNC)					Input/ Output		FAULT2 — PWM fault input 2 used for disabling selected PWM outputs in cases where fault conditions originate off-chip. EXT_SYNC — When not being used as a fault input, this pin can be used to receive a pulse to reset the PWM counter or to generate a positive pulse at the start of every PWM cycle.
(TIN3)					Input		TIN3 — Dual timer module channel 3 input After reset, the default state is GPIOA5.

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

Signal Name	28 SOIC	32 LQFP	32 PSDIP	48 LQFP	Type	State During Reset	Signal Description
GPIOA6	12	18	14	26	Input/ Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin.
(FAULT0)					Input		FAULT0 — PWM fault input 0 used for disabling selected PWM outputs in cases where fault conditions originate off-chip.
(ANA1 & ANB1)					Analog Input		ANA1 and ANB1 — Analog input to channel 1 of ADCA and ADCB.
(SCL)					Input/Open-drain Output		SCL — The I^2C serial clock
(TXD)					Output		TXD — The SCI transmit data output or transmit/receive in single wire operation.
(CLKO_1)					Output		CLKO_1 — This is a buffered clock output; the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) in the SIM. When used as an analog input, the signal goes to the ANA1 and ANB1. After reset, the default state is GPIOA6.
GPIOB0	15	21	17	32	Input/ Output	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin.
(SCLK)					Input/ Output		SCLK — The SPI serial clock. In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input.
(SCL)					Input/Open-drain Output		SCL — The I^2C serial clock.
(ANB13)					Analog Input		ANB13 — Analog input to channel 13 of ADCB
(PWM3)					Output		PWM3 — The PWM channel 3.
(T1)					Input/ Output		T1 — Dual timer module channel 1 input/output. After reset, the default state is GPIOB0.

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

Signal Name	28 SOIC	32 LQFP	32 PSDIP	48 LQFP	Type	State During Reset	Signal Description
GPIOB1 ($\overline{SS}$) (SDA) (ANA12 and CMP2_P3)	27	2	30	2	Input/ Output Input/ Output Input/Open-drain Output Analog input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. $\overline{SS}$ — $\overline{SS}$ is used in slave mode to indicate to the SPI module that the current transfer is to be received. SDA — The I^2C serial data line. ANA12 and CMP2_P3 — Analog input to channel 12 of ADCA and Positive input 3 of analog comparator 2. When used as an analog input, the signal goes to the ANA12 and CMP2_P3. After reset, the default state is GPIOB1.
GPIOB2 (MISO) (TIN2) (ANA2 and ANB2) (CMP0_ OUT)		17	13	25	Input/ Output Input/ Output Input/ Output Analog Input Output	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. MISO — Master in/slave out. In master mode, this pin serves as the data input. In slave mode, this pin serves as the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. TIN2 — Dual timer module channel 2 input. ANA2 and ANB2 — Analog input to channel 2 of ADCA and ADCB. CMP0_OUT— Analog comparator 0 output. When used as an analog input, the signal goes to the ANA2 and ANB2. After reset, the default state is GPIOB2.

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

Signal Name	28 SOIC	32 LQFP	32 PSDIP	48 LQFP	Type	State During Reset	Signal Description
GPIOB3	11	16	12	24	Input/ Output	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin.
(MOSI)					Input/ Output		MOSI — Master out/slave in. In master mode, this pin serves as the data output. In slave mode, this pin serves as the data input.
(TIN3)					Input/ Output		TIN3 — Dual timer module channel 3 input.
(ANA3 and ANB3)					Input		ANA3 and ANB3 — Analog input to channel 3 of ADCA and ADCB.
(PWM5)					Output		PWM5 — The PWM channel 5.
(CMP1_ OUT					Output		CMP1_OUT— Analog comparator 1 output.
							When used as an analog input, the signal goes to the ANA3 and ANB3.
							After reset, the default state is GPIOB3.
GPIOB4	13	19	15	27	Input/ Output	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin.
(T0)					Input/ Output		T0 — Dual timer module channel 0 input/output.
(CLKO_0)					Output		CLKO_0 — This is a buffered clock output; the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.
(MISO)					Input/ Output		MISO — Master in/slave out. In master mode, this pin serves as the data input. In slave mode, this pin serves as the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
(SDA)					Input/Open-drain Output		SDA — The I^2C serial data line.
(RXD)					Input		RXD — The SCI receive data input.
(ANA0 and ANB0)					Analog Input		ANA0 and ANB0 — Analog input to channel 0 of ADCA and ADCB.
							When used as an analog input, the signal goes to the ANA0 and ANB0.
							After reset, the default state is GPIOB4.

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

Signal Name	28 SOIC	32 LQFP	32 PSDIP	48 LQFP	Type	State During Reset	Signal Description
GPIOB5 (T1) (FAULT3) (SCLK)		4	32	4	Input/ Output Input/ Output Input Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. T1 — Dual timer module channel 1 input/output. FAULT3 — PWM fault input 3 used for disabling selected PWM outputs in cases where fault conditions originate off-chip. SCLK — SPI serial clock. In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. After reset, the default state is GPIOB5.
GPIOB6 (SDA) (ANA13 and CMP0_P2) (CLKIN)	26	1	29	1	Input/ Output Input/Open-drain Output Analog Input Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. SDA — The I^2C serial data line. ANA13 and CMP0_P2 — Analog input to channel 13 of ADCA and positive input 2 of analog comparator 0. External Clock Input — This pin serves as an external clock input. When used as an analog input, the signal goes to the ANA13 and CMP0_P2. After reset, the default state is GPIOB6.
GPIOB7 (TXD) (SCL) (ANA11 and CMP2_M3)		3	31	3	Input/ Output Input/ Output Input/Open-drain Output Analog Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. TXD — The SCI transmit data output or transmit/receive in single wire operation. SCL — The I^2C serial clock. ANA11 and CMP2_M3 — Analog input to channel 11 of ADCA and negative input 3 of analog comparator 2. When used as an analog input, the signal goes to the ANA11 and CMP2_M3. After reset, the default state is GPIOB7.

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

Signal Name	28 SOIC	32 LQFP	32 PSDIP	48 LQFP	Type	State During Reset	Signal Description
ANA5 and CMP1_M1 (GPIOC0) (FAULT0)	7	12	8	19	Analog Input Analog Input Input	Analog Input	ANA5 and CMP1_M1— Analog input to channel 5 of ADCA and negative input 1 of analog comparator 1. Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. FAULT0 — PWM fault input 0 is used for disabling selected PWM outputs in cases where fault conditions originate off-chip. When used as an analog input, the signal goes to the ANA5 and CMP1_M1. After reset, the default state is ANA5 and CMP1_M1.
ANA7 and PGA0+ and CMP2_M2 (GPIOC1)	6	11	7	17	Analog Input Input/ Output	Analog Input	ANA7 and PGA0+ and CMP2_M2 — Analog input to channel 7 of ADCA and PGA0 positive input and negative input 2 of analog comparator 2. Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. When used as an analog input, The signal goes to the ANA7 and PGA0+ and CMP2_M2. After reset, the default state is ANA7 and PGA0+ and CMP2_M2.
ANA9 and PGA0– and CMP2_P4 (GPIOC2)	5	10	6	15	Analog Input Input/ Output	Analog Input	ANA9 and PGA0– and CMP2_P4 — Analog input to channel 9 of ADCA and PGA0 negative input and positive input 4 of analog comparator 2. Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. When used as an analog input, The signal goes to the ANA9 and PGA0– and CMP2_P4. After reset, the default state is ANA9 and PGA0– and CMP2_P4.
GPIOC3 (EXT_ TRIGGER)				46	Input/ Output Input	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. EXT_TRIGGER — PDB external trigger input. After reset, the default state is GPIOC3.

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

Signal Name	28 SOIC	32 LQFP	32 PSDIP	48 LQFP	Type	State During Reset	Signal Description
ANB8 and PGA1+ and CMP0_M2 (GPIOC4)	28	5	1	7	Analog Input Input/ Output	Analog Input	ANB8 and PGA1+ and CMP0_M2 — Analog input to channel 8 of ADCB and PGA1 positive input and negative input 2 of analog comparator 0. Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. When used as an analog input, the signal goes to the ANB8 and PGA1+ and CMP0_M2. After reset, the default state is ANB8 and PGA1+ and CMP0_M2.
ANB6 and PGA1– and CMP0_P4 (GPIOC5)	1	6	2	9	Input/ Output Analog Input	Analog Input	ANB6 and PGA1– and CMP0_P4 — Analog input to channel 6 of ADCB and PGA1 negative input and positive input 4 of analog comparator 0. Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. When used as an analog input, the signal goes to the ANB6 and PGA1– and CMP0_P4. After reset, the default state is ANB6 and PGA1– and CMP0_P4.
ANB4 and CMP1_P1 (GPIOC6) (PWM2)	2	7	3	11	Analog Input Input/ Output Output	Analog Input	ANB4 and CMP1_P1 — Analog input to channel 4 of ADCB and positive input 1 of analog comparator 1. Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM2 — The PWM channel 2. When used as an analog input, the signal goes to the ANB4 and CMP1_P1. After reset, the default state is ANB4 and CMP1_P1.
GPIOC7 (ANB5 and CMP1_M2)				10	Input/ Output Analog Input	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB5 and CMP1_M2 — Analog input to channel 5 of ADCB and negative input 2 of analog comparator 1. After reset, the default state is GPIOC7.