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56F8037/56F8027

Data Sheet

Technical Data

56F8000
16-bit Digital Signal Controllers

MC56F8037
Rev. 8
04/2012

freescale.com

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semiconductor

Document Revision History

Version History	Description of Change
Rev. 0	Initial public release.
Rev. 1	• In Table 10-4, added an entry for flash data retention with less than 100 program/erase cycles (minimum 20 years). • In Table 10-6, changed the device clock speed in STOP mode from 8MHz to 4MHz. • In Table 10-12, changed the typical relaxation oscillator output frequency in Standby mode from 400kHz to 200kHz. • Changed input propagation delay values in Table 10-21 as follows: Old values: 1 µs typical, 2 µs maximum New values: 35 ns typical, 45 ns maximum
Rev. 2	In Table 10-20, changed the maximum ADC internal clock frequency from 8MHz to 5.33MHz.
Rev. 3	• Added the following note to the description of the TMS signal in Table 2-3: **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor. • Changed the description of the GPIOC4 signal in Table 2-3 (was "*...the signal goes to both the ANA0 and CMPAI3*", is "*...the signal goes to both ANB0 and CMPB13*").
Rev. 4	• Changed the ITCN_BASE address In **Table 5-3** (was $00 F060, is $00 F0E0). • In **Figure 5-10**, moved the footnote marker (superscript 1) from bit 4 to "RESET". • Changed the STANDBY > STOP I_{DD} values in **Table 10-6** as follows: Typical: was 290µA, is 540µA Maximum: was 390µA, is 650µA • Changed the POWERDOWN I_{DD} values in **Table 10-6** as follows: Typical: was 190µA, is 440µA Maximum: was 250µA, is 550µA • Changed footnote 1 in **Table 10-12** (was "Output frequency after application of 8MHz trim value, at 125°C.", is "Output frequency after application of factory trim"). • Deleted the text "at 125°C" from **Figure 10-5**. • Changed the maximum input offset voltage in **Table 10-21** (was +/- 20 mV, is ±35 mV).
Rev. 5	• In **Table 2-3**, changed V_{CAP} value from 4.7µF to 2.2µF. • Revised **Section 7, Security Features**. • Added information for 56F8027 device throughout document. • Fixed miscellaneous typos.

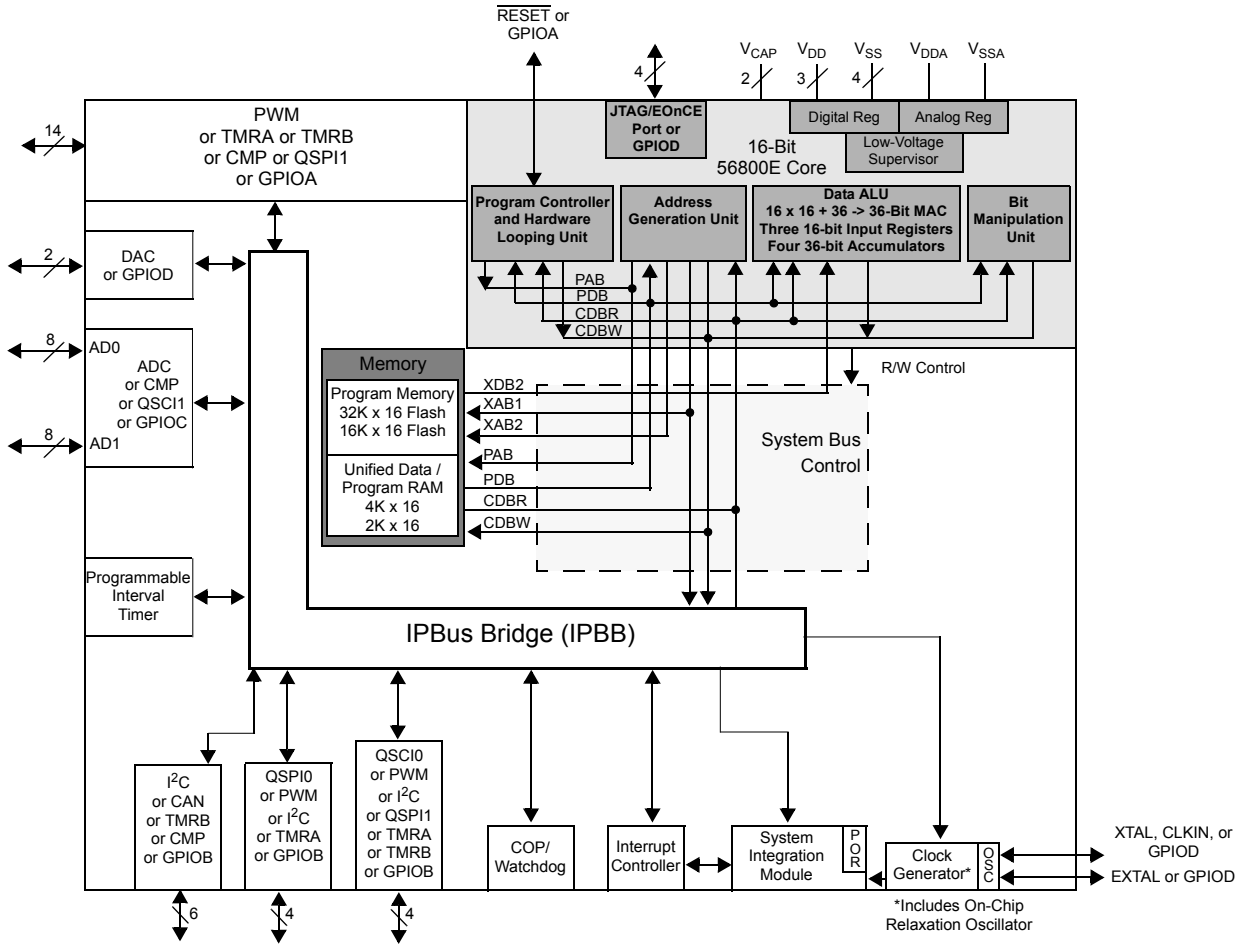
Document Revision History

Version History	Description of Change
Rev. 6	In the table **Recommended Operating Conditions**, removed the line “XTAL not driven by an external clock“ from the characteristic: “Oscillator Input Voltage High XTAL not driven by an external clock XTAL driven by an external clock source” In the table **56F8037/56F8027 Ordering Information**, changed “MC56F8027VLD“ to “MC56F8027VLH“ Removed “Preliminary” from data sheet In the **Select Peripheral Input Source for PWM2/PWM3 Pair Source Bits**, fixed typos Added new part number to ordering information: MC56F8027MLH
Rev. 7	Added MC56F8037MLH to the part ordering table.
Rev. 8	• In section **Section 5.6.18**, changed bit15 from “PENDING” to reserved. • Added section **Section 5.6.18.2** to describe the reserved bit.

Please see http://www.freescale.com for the most current data sheet revision.

56F8037/56F8027 General Description

- Up to 32 MIPS at 32MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- 56F8037 offers 64KB (32K x 16) Program Flash
- 56F8027 offers 32KB (16K x 16) Program Flash
- 56F8037 offers 8KB (4K x 16) Unified Data/Program RAM
- 56F8027 offers 4KB (2K x 16) Unified Data/Program RAM
- One 6-channel PWM module
- Two 8-channel 12-bit Analog-to-Digital Converters (ADCs)
- Two 12-bit Digital-to-Analog Converters (DACs)
- Two Analog Comparators
- Three Programmable Interval Timers (PITs)
- Two Queued Serial Communication Interfaces (QSCIs) with LIN slave functionality
- Two Queued Serial Peripheral Interfaces (QSPIs)
- Freescale's scalable controller area network (MSCAN) 2.0 A/B Module
- Two 16-bit Quad Timers
- One Inter-Integrated Circuit (I^2C) port
- Computer Operating Properly (COP)/Watchdog
- On-Chip Relaxation Oscillator
- Integrated Power-On Reset (POR) and Low-Voltage Interrupt (LVI) module
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging



56F8037/56F8027 Block Diagram

56F8037/56F8027 Data Sheet Table of Contents

Part 1 Overview

1.1 56F8037/56F8027 Features

1.1.1 Digital Signal Controller Core

- Efficient 16-bit 56800E family Digital Signal Controller (DSC) engine with dual Harvard architecture
- As many as 32 Million Instructions Per Second (MIPS) at 32MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 32-bit arithmetic and logic multi-bit shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses
- Four internal data buses
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, processor speed-independent, real-time debugging

1.1.2 Difference Between Devices

Table 1-1 outlines the key differences between the 56F8037 and 56F8027 devices.

Table 1-1 Device Differences

Feature	56F8037	56F8027
Program Flash	64KB	32KB
Unified Data/Program RAM	8KB	4KB

1.1.3 Memory

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Flash security and protection that prevent unauthorized users from gaining access to the internal Flash
- On-chip memory
  - 64KB of Program Flash (56F8037 device)
    32KB of Program Flash (56F8027 device)
  - 8KB of Unified Data/Program RAM (56F8037 device)
    4KB of Unified Data/Program RAM (56F8027 device)
- EEPROM emulation capability using Flash

1.1.4 Peripheral Circuits for 56F8037/56F8027

- One multi-function six-output Pulse Width Modulator (PWM) module
  - Up to 96MHz PWM operating clock
  - 15 bits of resolution
  - Center-aligned and Edge-aligned PWM signal mode
  - Four programmable fault inputs with programmable digital filter
  - Double-buffered PWM registers
  - Each complementary PWM signal pair allows selection of a PWM supply source from:
    - PWM generator
    - External GPIO
    - Internal timers
    - Analog comparator outputs
    - ADC conversion result which compares with values of ADC high- and low-limit registers to set PWM output
- Two independent 12-bit Analog-to-Digital Converters (ADCs)
  - 2 x 8 channel inputs
  - Supports both simultaneous and sequential conversions
  - ADC conversions can be synchronized by both PWM and timer modules
  - Sampling rate up to 2.67MSPS
  - 16-word result buffer registers
- Two 12-bit Digital-to-Analog Converters (DACs)
  - 2 microsecond settling time when output swing from rail to rail
  - Automatic waveform generation generates square, triangle and sawtooth waveforms with programmable period, update rate, and range
- Two 16-bit multi-purpose Quad Timer modules (TMRs)
  - Up to 96MHz operating clock
  - Eight independent 16-bit counter/timers with cascading capability
  - Each timer has capture and compare capability
  - Up to 12 operating modes
- Two Queued Serial Communication Interfaces (QSCIs) with LIN Slave functionality
  - Full-duplex or single-wire operation
  - Two receiver wake-up methods:
    - Idle line
    - Address mark
  - Four-bytes-deep FIFOs are available on both transmitter and receiver
- Two Queued Serial Peripheral Interfaces (QSPIs)

- Full-duplex operation
- Master and slave modes
- Four-words-deep FIFOs available on both transmitter and receiver
- Programmable Length Transactions (2 to 16 bits)

- One Inter-Integrated Circuit (I^2C) port
  - Operates up to 400kbps
  - Supports both master and slave operation
  - Supports both 10-bit address mode and broadcasting mode
- One Freescale scalable controller area network (MSCAN) module
  - Fully compliant with CAN protocol - Version 2.0 A/B
  - Supports standard and extended data frames
  - Supports data rate up to 1Mbps
  - Five receive buffers and three transmit buffers
- Three 16-bit Programmable Interval Timers (PITs)
- Two analog Comparators (CMPs)
  - Selectable input source includes external pins, DACs
  - Programmable output polarity
  - Output can drive Timer input, PWM fault input, PWM source, external pin output and trigger ADCs
  - Output falling and rising edge detection able to generate interrupts
- Computer Operating Properly (COP)/Watchdog timer capable of selecting different clock sources
- Up to 53 General-Purpose I/O (GPIO) pins with 5V tolerance
- Integrated Power-On Reset and Low-Voltage Interrupt Module
- Phase Lock Loop (PLL) to provide high-speed clock to the core and peripherals
- Clock sources:
  - On-chip relaxation oscillator
  - External clock: crystal oscillator, ceramic resonator and external clock source
- JTAG/EOnCE debug programming interface for real-time debugging

1.1.5 Energy Information

- Fabricated in high-density CMOS with 5V tolerance
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available
- ADC smart power management
- Each peripheral can be individually disabled to save power

1.2 56F8037/56F8027 Description

The 56F8037/56F8027 is a member of the 56800E core-based family of Digital Signal Controllers (DSCs). It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost,

configuration flexibility, and compact program code, the 56F8037/56F8027 is well-suited for many applications. The 56F8037/56F8027 includes many peripherals that are especially useful for industrial control, motion control, home appliances, general purpose inverters, smart sensors, fire and security systems, switched-mode power supply, power management, and medical monitoring applications.

The 56800E core is based on a dual Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The 56F8037/56F8027 supports program execution from internal memories. Two data operands can be accessed from the on-chip data RAM per instruction cycle. The 56F8037/56F8027 also offers up to 53 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The 56F8037 Digital Signal Controller includes 64KB of Program Flash and 8KB of Unified Data/Program RAM. The 56F8027 Digital Signal Controller includes 32KB of Program Flash and 4KB of Unified Data/Program RAM. Program Flash memory can be independently bulk erased or erased in pages. Program Flash page erase size is 512 Bytes (256 Words).

A full set of programmable peripherals—PWM, ADCs, QSCIs, QSPIs, I2C, PITs, Quad Timers, DACs and analog comparators—supports various applications. Each peripheral can be independently shut down to save power. Any pin in these peripherals can also be used as General Purpose Input/Outputs (GPIOs).

1.3 Award-Winning Development Environment

Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs), demonstration board kit and development system cards will support concurrent engineering. Together, PE, CodeWarrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Architecture Block Diagram

The 56F8037/56F8027's architecture is shown in **Figures 1-1**, **1-2**, **1-3**, **1-4**, **1-5**, **1-6**, and **1-7**. **Figure 1-1** illustrates how the 56800E system buses communicate with internal memories and the IPBus Bridge and the internal connections between each unit of the 56800E core. **Figure 1-2** shows the peripherals and control blocks connected to the IPBus Bridge. **Figures 1-3**, **1-4**, **1-5**, **1-6** and **1-7** detail how the device's I/O pins are muxed. The figures do not show the on-board regulator and power and ground signals. Please see **Part 2, Signal/Connection Descriptions**, for information about which signals are multiplexed with those of other peripherals.

1.4.1 PWM, TMR and ADC Connections

Figure 1-6 shows the over-limit and under-limit connections from the ADC to the PWM and the

connections to the PWM from the TMR and GPIO. These signals can control the PWM outputs in a similar manner as the PWM generator. See the **56F802x and 56F803x Peripheral Reference Manual** for additional information.

The PWM_reload_sync output can be connected to Timer A's (TMRA) Channel 3 input; TMRA's Channels 2 and 3 outputs are connected to the ADC sync inputs. TMRA Channel 3 output is connected to SYNC0 and TMRA Channel 2 is connected to SYNC1. SYNC0 is the master ADC sync input that is used to trigger ADCA and ADCB in sequence and parallel mode. SYNC1 is used to trigger ADCB in parallel independent mode. These are controlled by bits in the SIM Control Register; see **Section 6.3.1**.

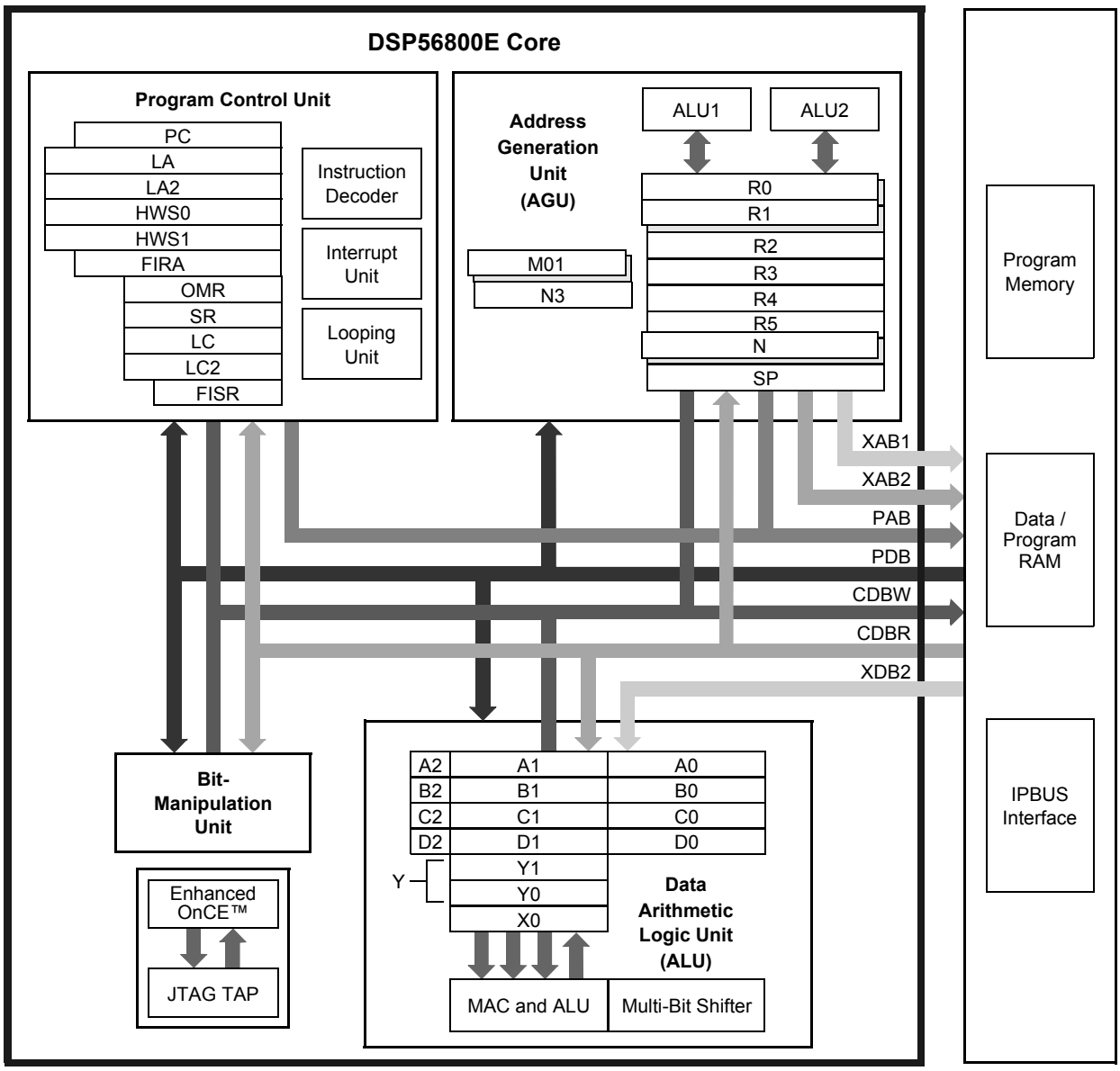


Figure 1-1 56800E Core Block Diagram

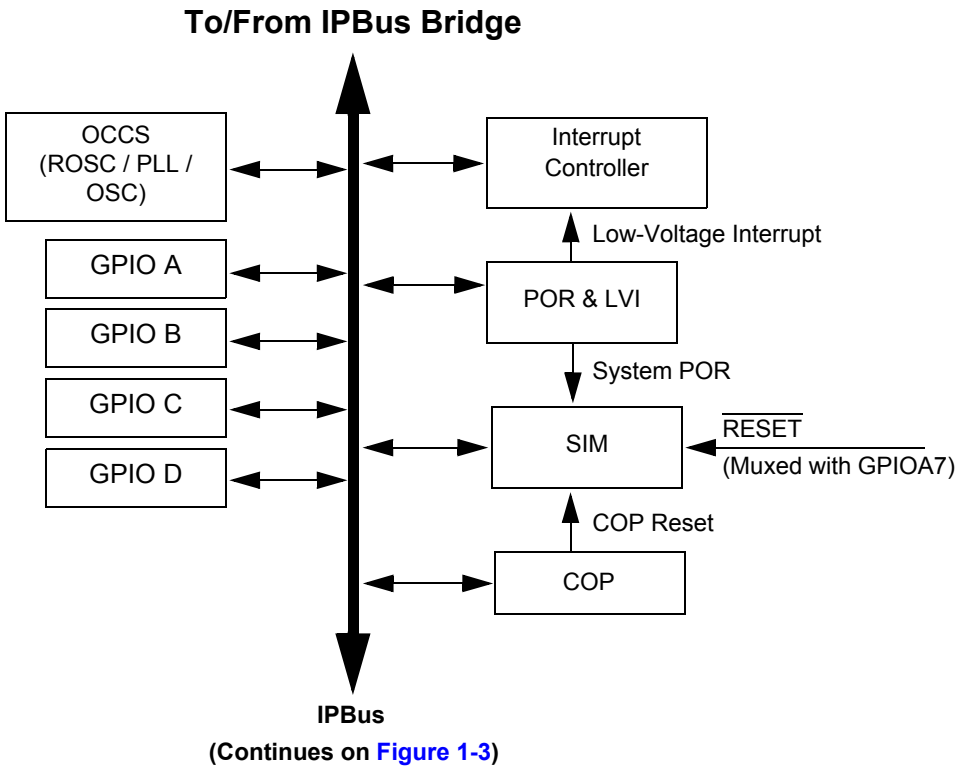


Figure 1-2 Peripheral Subsystem

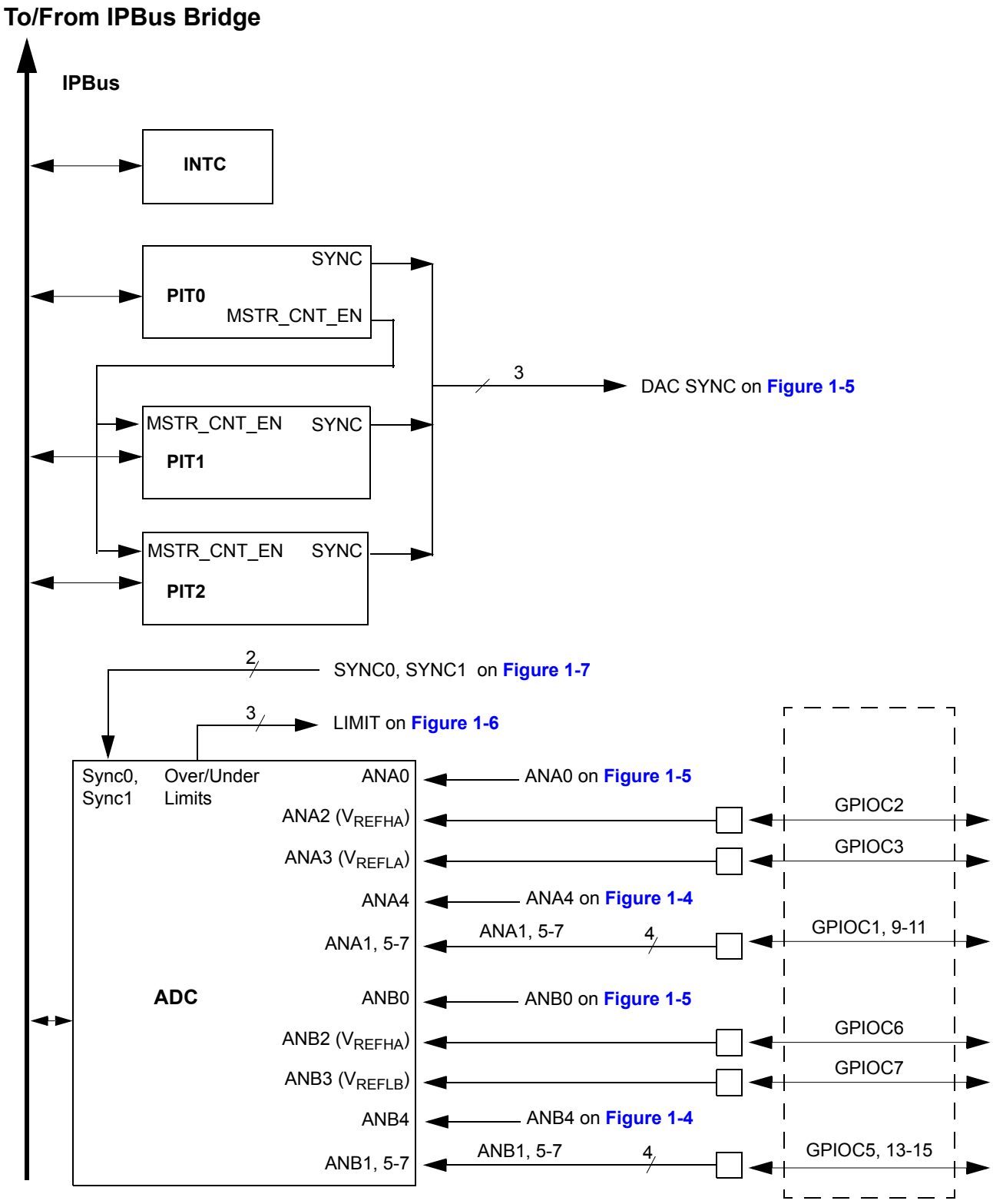


Figure 1-3 56F8037/56F8027 I/O Pin-Out Muxing (Part 1/5)

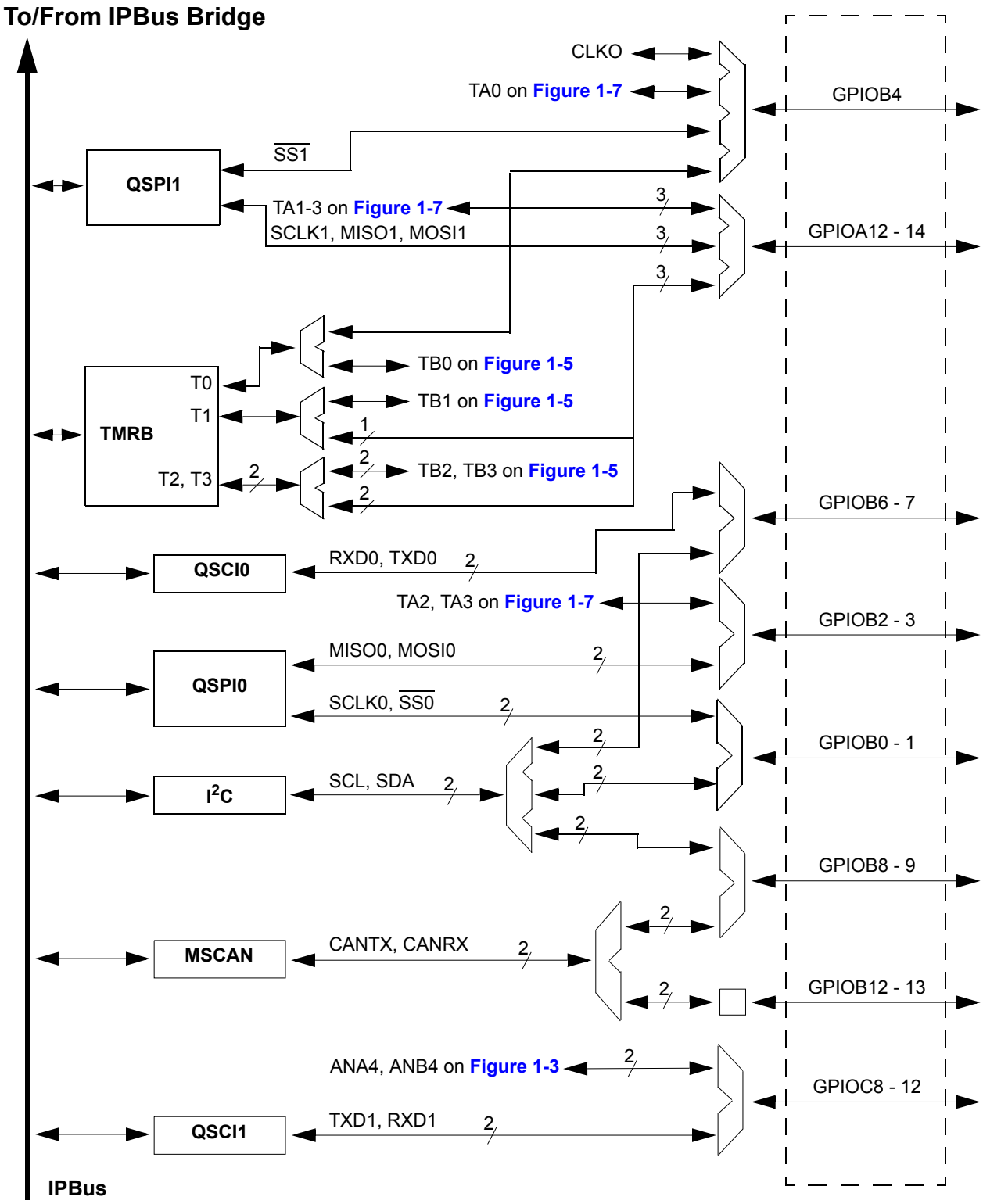


Figure 1-4 56F8037/56F8027 I/O Pin-Out Muxing (Part 2/5)

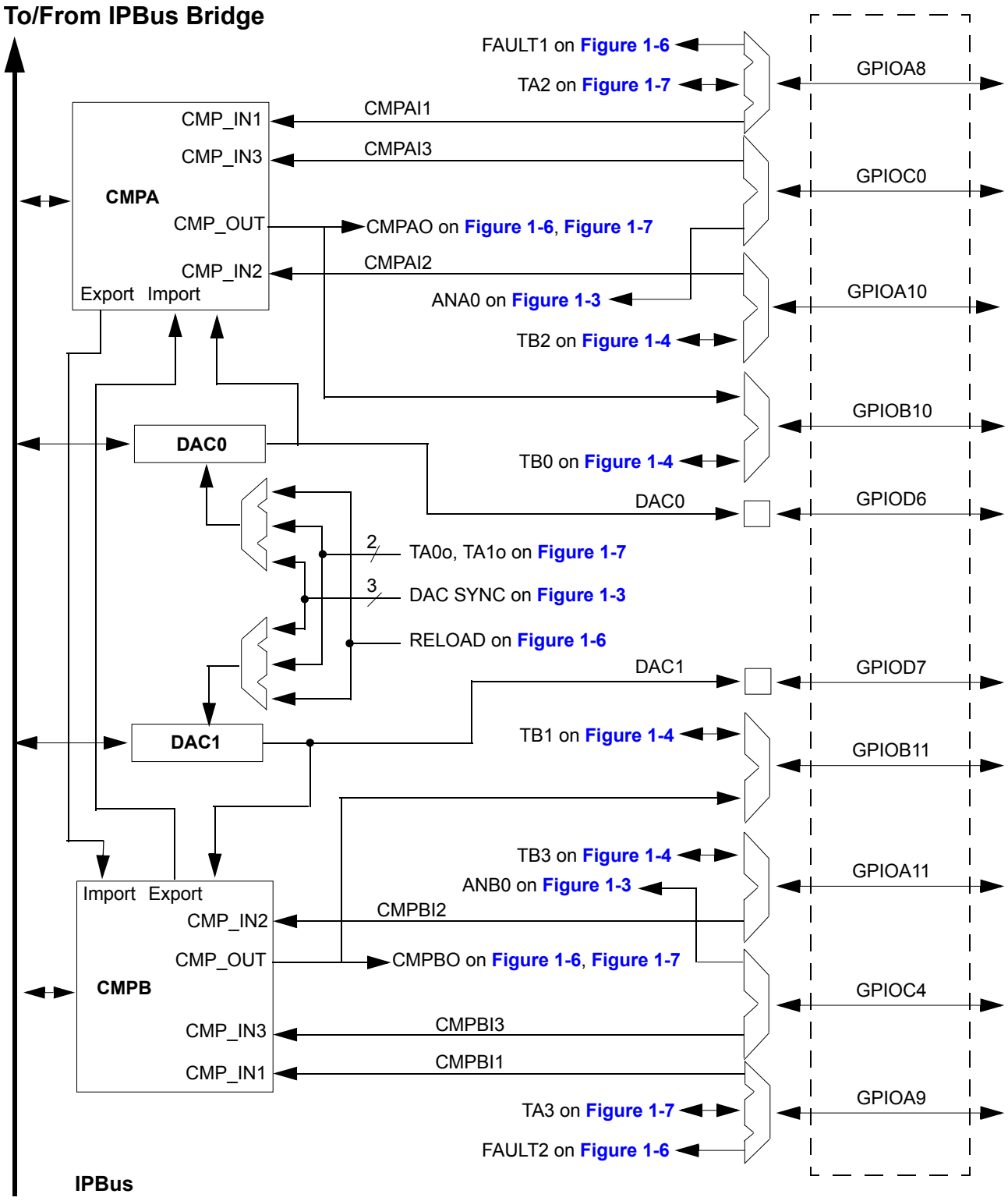


Figure 1-5 56F8037/56F8027 I/O Pin-Out Muxing (Part 3/5)

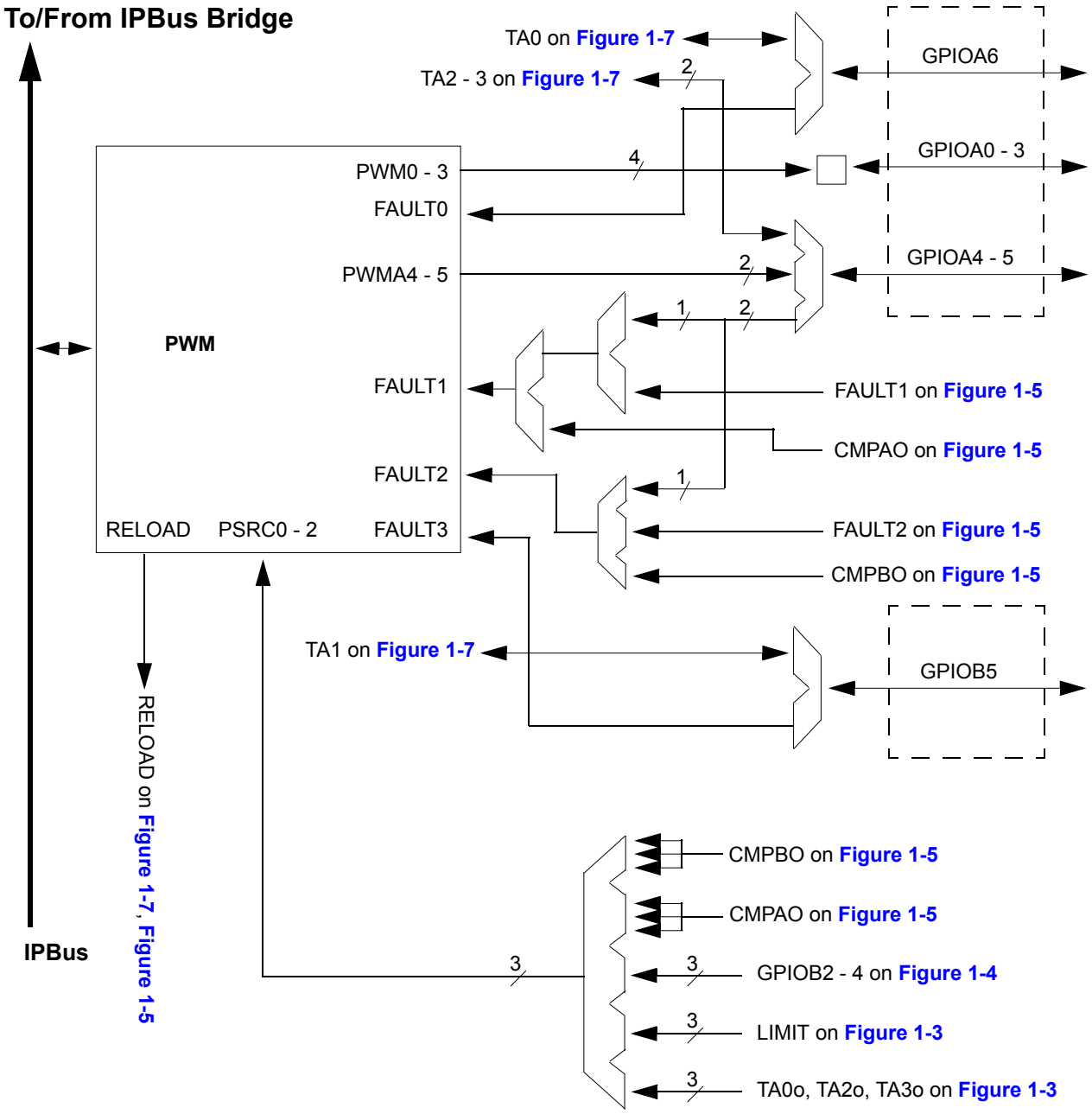


Figure 1-6 56F8037/56F8027 I/O Pin-Out Muxing (Part 4/5)

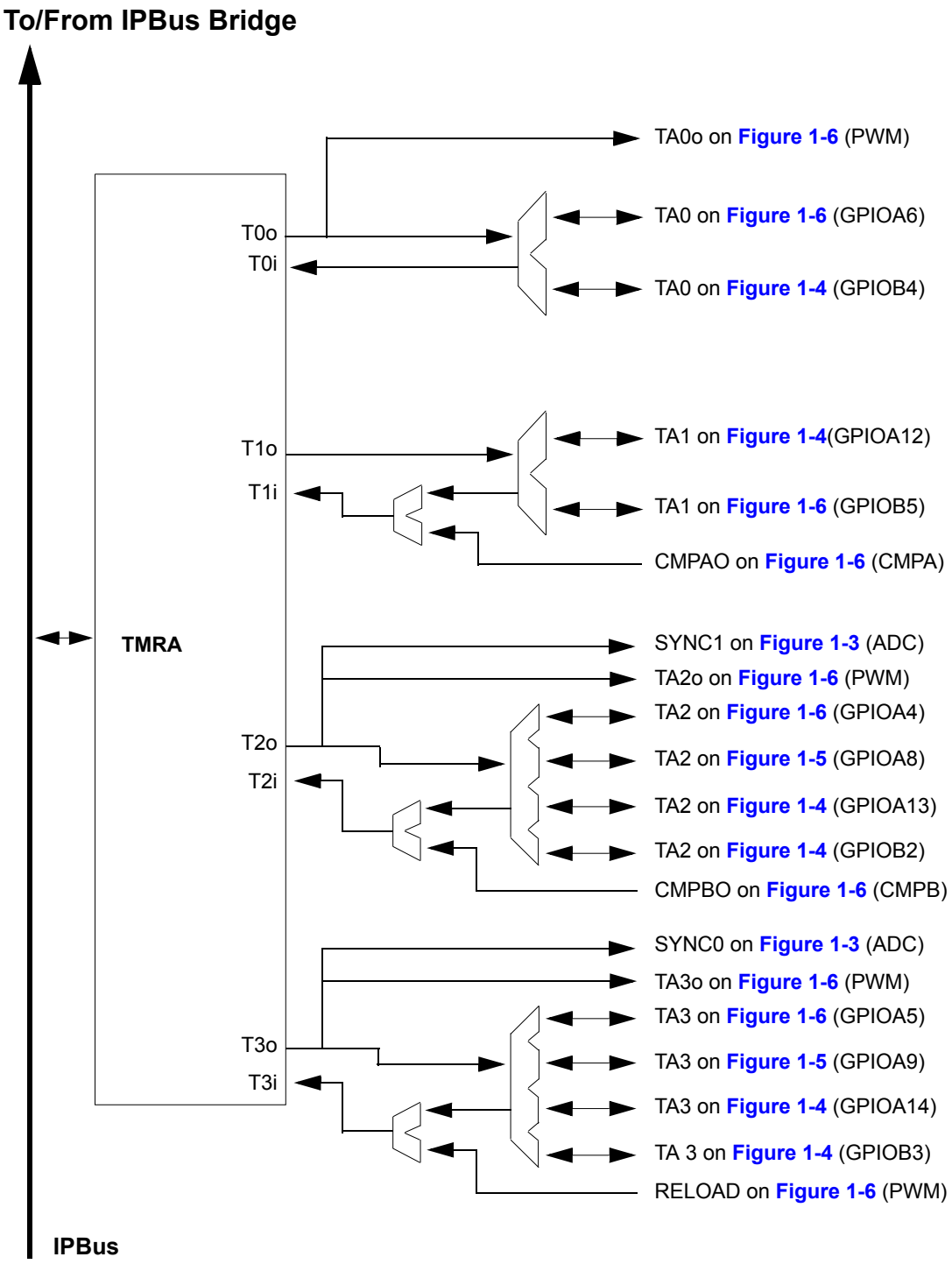


Figure 1-7 56F8037/56F8027 I/O Pin-Out Muxing (Part 5/5)

1.5 Product Documentation

The documents listed in **Table 1-2** are required for a complete description and proper design with the 56F8037/56F8027. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at:
http://www.freescale.com

Table 1-2 56F8037/56F8027 Chip Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, 16-bit Digital Signal Controller core processor, and the instruction set	DSP56800ERM
56F802x and 56F803x Peripheral Reference Manual	Detailed description of peripherals of the 56F802x and 56F803x family of devices	MC56F80xxRM
56F802x and 56F803x Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the 56F802x and 56F803x family of devices	56F80xxBLUG
56F8037/56F8027 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	MC56F8037/56F8027
56F8037/56F8027 Errata	Details any chip issues that might be present	MC56F8037/56F8027E

1.6 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
“asserted”	A high true (active high) signal is high or a low true (active low) signal is low.
“deasserted”	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:	Signal/Symbol	Logic State	Signal State	Voltage[1]
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the 56F8037/56F8027 are organized into functional groups, as detailed in Table 2-1. Table 2-2 summarizes all device pins. In Table 2-2, each table row describes the signal or signals present on a pin, sorted by pin number.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins
Power Inputs (V_{DD}, V_{DDA})	4
Ground (V_{SS}, V_{SSA})	5
Supply Capacitors	2
Reset[1]	1
Pulse Width Modulator (PWM) Ports[1]	13
Queued Serial Peripheral Interface 0 (QSPI0) Ports[1]	4
Queued Serial Peripheral Interface 1 (QSPI1) Ports[1]	4
Timer Module A (TMRA) Ports[1]	4
Timer Module B (TMRB) Ports[1]	4
Analog-to-Digital Converter (ADC) Ports[1]	16
Digital-to-Analog Converter (DAC) Ports[1]	2
Queued Serial Communications Interface 0 (QSCI0) Ports[1]	2
Queued Serial Communications Interface 1 (QSCI1) Ports[1]	2
Inter-Integrated Circuit Interface (I^2C) Ports[1]	2
MSCAN Ports[1]	2
Oscillator Signals[1]	2
JTAG/Enhanced On-Chip Emulation (EOnCE)[1]	4

1. Pins may be shared with other peripherals. See Table 2-2.

In **Table 2-2**, peripheral pins in bold identify reset state.

Table 2-2 56F8037/56F8027 Pins

			Peripherals:												
Pin #	**Pin Name**	**Signal Name**	**GPIO**	**I2C**	**QSCI**	**QSPI**	**ADC**	**PWM**	**Quad Timer**	**DAC**	**Comp**	**MSCAN**	**Power & Ground**	**JTAG**	**Misc.**
1	**GPIOB6**	GPIOB6, RXD0, SDA, CLKIN	**B6**	SDA	RXD0										CLKIN
2	**GPIOB1**	GPIOB1, $\overline{SS0}$, SDA	**B1**	SDA		$\overline{SS0}$									
3	**GPIOB7**	GPIOB7, TXD0, SCL	**B7**	SCL	TXD0										
4	**GPIOB5**	GPIOB5, TA1, FAULT3, CLKIN	**B5**					FAULT3	TA1						CLKIN
5	**GPIOA9**	GPIOA9, FAULT2, TA3, CMPBI1	**A9**					FAULT2	TA3		CMPBI1				
6	**GPIOA11**	GPIOA11, TB3, CMPBI2	**A11**						TB3		CMPBI2				
7	**VDD**	V_{DD}											V_{DD}		
8	**VSS**	V_{SS}											V_{SS}		
9	**GPIOC12**	GPIOC12, ANB4, RXD1	**C12**		RXD1		ANB4								
10	**GPIOC4**	GPIOC4, ANB0, CMPBI3	**C4**				ANB0				CMPBI3				
11	**GPIOC5**	GPIOC5, ANB1	**C5**				ANB1								
12	**GPIOC13**	GPIOC13, ANB5	**C13**				ANB5								
13	**GPIOC6**	ANB2, V_{REFHB}	**C6**				ANB2 V_{REFHB}								
14	**GPIOC7**	GPIOC7, ANB3, V_{REFLB}	**C7**				ANB3 V_{REFLB}								
15	**GPIOD7**	GPIOD7, DAC1	**D7**							DAC1					
16	**VDDA**	V_{DDA}											V_{DDA}		
17	**VSSA**	V_{SSA}											V_{SSA}		
18	**GPIOD6**	GPIOD6, DAC0	**D6**							DAC0					
19	**GPIOC3**	GPIOC3, ANA3, V_{REFLA}	**C3**				ANA3 V_{REFLA}								
20	**GPIOC2**	GPIOC2, ANA2, V_{REFHA}	**C2**				ANA2 V_{REFHA}								
21	**GPIOC9**	GPIOC9, ANA5	**C9**				ANA5								
22	**GPIOC1**	GPIOC1, ANA1	**C1**				ANA1								
23	**GPIOC10**	GPIOC10, ANA6	**C10**				ANA6								
24	**GPIOC0**	GPIOC0, ANA0, CMPAI3	**C0**				ANA0				CMPAI3				
25	**GPIOC11**	GPIOC11, ANA7	**C11**				ANA7								
26	**GPIOC8**	GPIOC8, ANA4, TXD1	**C8**		TXD1		ANA4								
27	**VSS**	V_{SS}											**V_{SS}**		

Table 2-2 56F8037/56F8027 Pins (Continued)

			Peripherals:												
Pin #	**Pin Name**	**Signal Name**	**GPIO**	**I2C**	**QSCI**	**QSPI**	**ADC**	**PWM**	**Quad Timer**	**DAC**	**Comp**	**MSCAN**	**Power & Ground**	**JTAG**	**Misc.**
28	**VCAP**	V_{CAP}											**V_{CAP}**		
29	**TCK**	TCK, GPIOD2	D2											**TCK**	
30	**GPIOB10**	GPIOB10, CMPAO, TB0	**B10**						TB0		CMPAO				
31	**RESET**	$\overline{\text{RESET}}$, GPIOA7	A7												**$\overline{\text{RESET}}$**
32	**GPIOB3**	GPIOB3, MOSI0, TA3, PSRC1	**B3**			MOSI0		PSRC1	TA3						
33	**GPIOB2**	GPIOB2, MISO0, TA2, PSRC0	**B2**			MISO0		PSRC0	TA2						
34	**GPIOA6**	GPIOA6, FAULT0, TA0	**A6**					FAULT0	TA0						
35	**GPIOA10**	GPIOA10, TB2, CMPAI2	**A10**						TB2		CMPAI2				
36	**GPIOA8**	GPIOA8, FAULT1, TA2, CMPAI1	**A8**					FAULT1	TA2		CMPAI1				
37	**GPIOA12**	GPIOA12, TB1, SCLK1, TA1	**A12**			SCLK1			TB1 TA1						
38	**GPIOB4**	GPIOB4, $\overline{\text{SS1}}$, TB0, TA0, PSRC2, CLKO	**B4**			$\overline{\text{SS1}}$		PSRC2	TA0 TB0						CLKO
39	**GPIOA5**	GPIOA5, PWM5, TA3, FAULT2	**A5**					PWM5 FAULT2	TA3						
40	**VSS**	V_{SS}											**V_{SS}**		
41	**VDD**	V_{DD}											**V_{DD}**		
42	**GPIOB0**	GPIOB0, SCLK0, SCL	**B0**	SCL		SCLK0									
43	**GPIOA4**	GPIOA4, PWM4, TA2, FAULT1	**A4**					PWM4 FAULT1	TA2						
44	**GPIOA13**	GPIOA13, TB2, MISO1, TA2	**A13**			MISO1			TB2 TA2						
45	**GPIOA14**	GPIOA14, TB3, MOSI1, TA3	**A14**			MOSI1			TB3 TA3						
46	**GPIOB9**	GPIOB9, SDA, CANRX	**B9**	SDA								CANRX			
47	**GPIOA2**	GPIOA2, PWM2	**A2**					PWM2							
48	**GPIOA3**	GPIOA3, PWM3	**A3**					PWM3							
49	**VCAP**	V_{CAP}											**V_{CAP}**		
50	**VDD**	V_{DD}											**V_{DD}**		
51	**VSS**	V_{SS}											**V_{SS}**		
52	**GPIOD5**	GPIOD5, XTAL, CLKIN	**D5**												XTAL CLKIN
53	**GPIOD4**	GPIOD4, EXTAL	**D4**												EXTAL
54	**GPIOB8**	GPIOB8, SCL, CANTX	**B8**	SCL								CANTX			
55	**GPIOA1**	GPIOA1, PWM1	**A1**					PWM1							

Table 2-2 56F8037/56F8027 Pins (Continued)

			Peripherals:												
Pin #	**Pin Name**	**Signal Name**	**GPIO**	**I2C**	**QSCI**	**QSPI**	**ADC**	**PWM**	**Quad Timer**	**DAC**	**Comp**	**MSCAN**	**Power & Ground**	**JTAG**	**Misc.**
56	**GPIOA0**	GPIOA0, PWM0	**A0**					PWM0							
57	**GPIOB12**	GPIOB12, CANTX	**B12**									CANTX			
58	**GPIOB13**	GPIOB13, CANRX	**B13**									CANRX			
59	**TDI**	TDI, GPIOD0	D0											**TD1**	
60	**GPIOB11**	GPIOB11, CMPBO, TB1	**B11**						TB1		CMPBO				
61	**GPIOC15**	GPIOC15, ANB7	**C15**				ANB7								
62	**GPIOC14**	GPIOC14, ANB6	**C14**				ANB6								
63	**TMS**	TMS, GPIOD3	D3											**TMS**	
64	**TDO**	TDO, GPIOD1	D1											**TDO**	

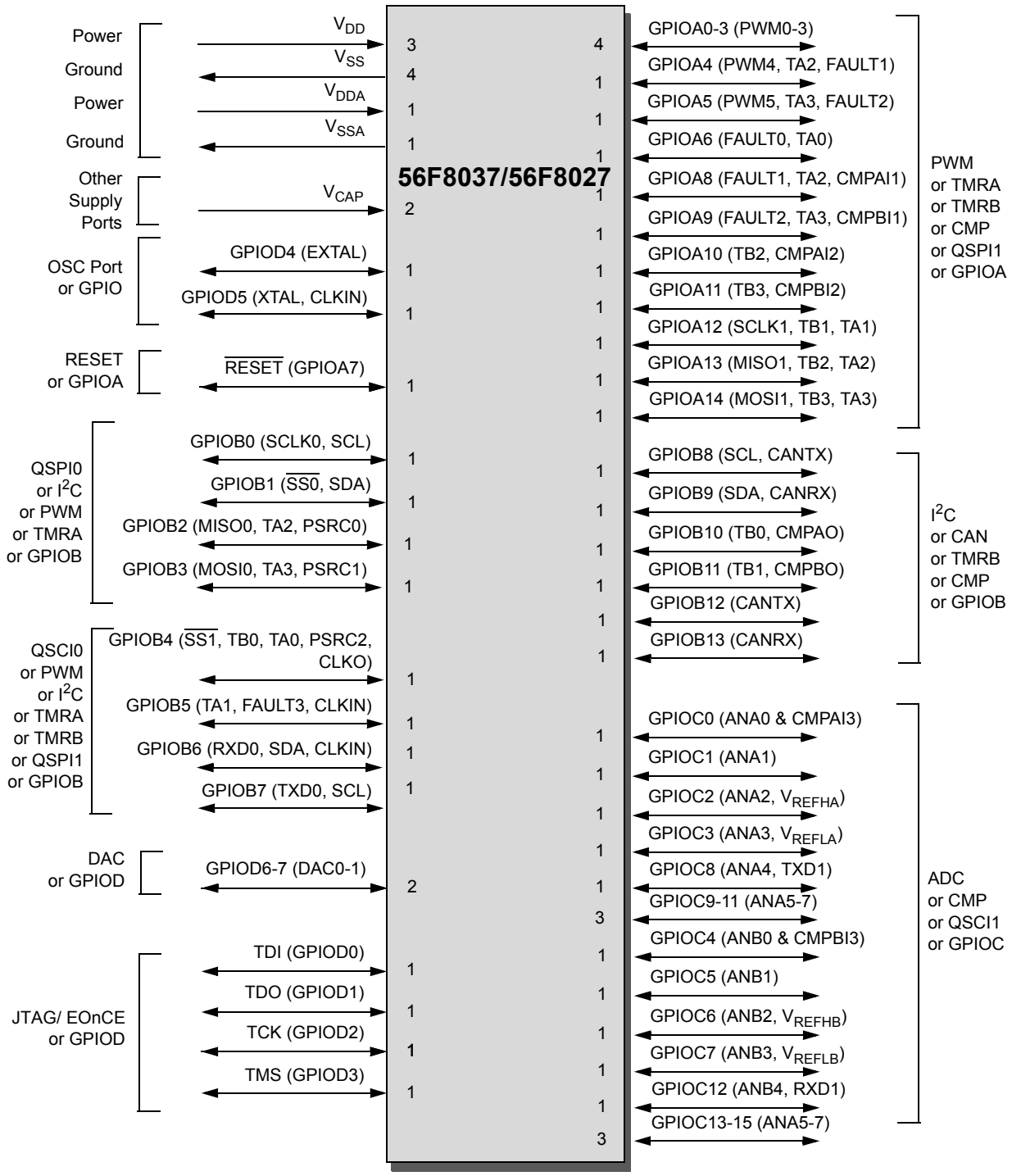


Figure 2-1 56F8037/56F8027 Signals Identified by Functional Group

2.2 56F8037/56F8027 Signal Pins

After reset, each pin is configured for its primary function (listed first). Any alternate functionality must be programmed.

Table 2-3 56F8037/56F8027 Signal and Package Information for the 64-Pin LQFP

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
V_{DD}	7	Supply	Supply	**I/O Power** — This pin supplies 3.3V power to the chip I/O interface.
V_{DD}	41			
V_{DD}	50			
V_{SS}	8	Supply	Supply	V_{SS} — These pins provide ground for chip logic and I/O drivers.
V_{SS}	27			
V_{SS}	40			
V_{SS}	51			
V_{DDA}	16	Supply	Supply	**ADC Power** — This pin supplies 3.3V power to the ADC modules. It must be connected to a clean analog power supply.
V_{SSA}	17	Supply	Supply	**ADC Analog Ground** — This pin supplies an analog ground to the ADC modules.
V_{CAP}	28	Supply	Supply	V_{CAP} — Connect this pin to a 2.2µF or greater bypass capacitor in order to bypass the core voltage regulator, required for proper chip operation. See Section 10.2.1.
V_{CAP}	49			
$\overline{\text{RESET}}$ (GPIOA7)	31	Input Input/Open Drain Output	Input, internal pull-up enabled	**Reset** — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the chip is initialized and placed in the reset state. A Schmitt trigger input is used for noise immunity. The internal reset signal will be deasserted synchronous with the internal clocks after a fixed number of internal clocks. **Port A GPIO** — This GPIO pin can be individually programmed as an input or open drain output pin. Note that $\overline{\text{RESET}}$ functionality is disabled in this mode and the chip can only be reset via POR, COP reset, or software reset. After reset, the default state is $\overline{\text{RESET}}$.

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Table 2-3 56F8037/56F8027 Signal and Package Information for the 64-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOA0 **(PWM0)**	56	Input/ Output Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. **PWM0** — This is one of the six PWM output pins. After reset, the default state is GPIOA0.
GPIOA1 **(PWM1)**	55	Input/ Output Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. **PWM1** — This is one of the six PWM output pins. After reset, the default state is GPIOA1.
GPIOA2 **(PWM2)**	47	Input/ Output Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. **PWM2** — This is one of the six PWM output pins. After reset, the default state is GPIOA2.
GPIOA3 **(PWM3)**	48	Input/ Output Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. **PWM3** — This is one of the six PWM output pins. After reset, the default state is GPIOA3.

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