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Freescale Semiconductor
Technical Data

Document Number: MC56F825X
Rev. 3, 04/2011

RoHS

MC56F825x/MC56F824x


44-pin LQFP
Case:
10 x 10 mm^2


48-pin LQFP
Case:
7 x 7 mm^2


64-pin LQFP
Case:
10 x 10 mm^2

MC56F825x/MC56F824x Digital Signal Controller

The MC56F825x/MC56F824x is a member of the 56800E core-based family of digital signal controllers (DSCs). It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create a cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, it is well-suited for many applications. The MC56F825x/MC56F824x includes many peripherals that are especially useful for cost-sensitive applications, including:

- Industrial control
- Home appliances
- Smart sensors
- Fire and security systems
- Solar inverters
- Battery chargers and management
- Switched-mode power supplies and power management
- Power metering
- Motor control (ACIM, BLDC, PMSM, SR, and stepper)
- Handheld power tools
- Arc detection
- Medical devices/equipment
- Instrumentation
- Lighting ballast

The 56800E core is based on a modified Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The MC56F825x/MC56F824x supports program execution from internal memories. Two data operands per instruction cycle can be accessed from the on-chip data RAM. A full set of programmable peripherals supports various applications. Each peripheral can be independently shut down to save power. Any pin, except Power pins and the Reset pin, can also be configured as General Purpose Input/Outputs (GPIOs).

On-chip features include:

- 60 MHz operation frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- On-chip memory
  - 56F8245/46: 48 KB (24K x 16) flash memory; 6 KB (3K x 16) unified data/program RAM
  - 56F8247: 48 KB (24K x 16) flash memory; 8 KB (4K x 16) unified data/program RAM
  - 56F8255/56/57: 64 KB (32K x 16) flash memory; 8 KB (4K x 16) unified data/program RAM
- eFlexPWM with up to 9 channels, including 6 channels with high (520 ps) resolution NanoEdge placement
- Two 8-channel, 12-bit analog-to-digital converters (ADCs) with dynamic x2 and x4 programmable amplifier, conversion time as short as 600 ns, and input current-injection protection
- Three analog comparators with integrated 5-bit DAC references
- Cyclic Redundancy Check (CRC) Generator
- Two high-speed queued serial communication interface (QSCI) modules with LIN slave functionality
- Queued serial peripheral interface (QSPI) module
- Two SMBus-compatible inter-integrated circuit (I^2C) ports
- Freescale's scalable controller area network (MSCAN) 2.0 A/B module
- Two 16-bit quad timers (2 x 4 16-bit timers)
- Computer operating properly (COP) watchdog module
- On-chip relaxation oscillator: 8 MHz (400 kHz at standby mode)
- Crystal/resonator oscillator
- Integrated power-on reset (POR) and low-voltage interrupt (LVI) and brown-out reset module
- Inter-module crossbar connection
- Up to 54 GPIOs
- 44-pin LQFP, 48-pin LQFP, and 64-pin LQFP packages
- Single supply: 3.0 V to 3.6 V

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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Table of Contents

1 MC56F825x/MC56F824x Family Configuration

Table 1 compares the MC56F825x/MC56F824x devices.

Table 1. MC56F825x/MC56F824x Device Comparison

Feature		56F8245	56F8246	56F8247	56F8255	56F8256	56F8257
Operation Frequency (MHz)		60					
High Speed Peripheral Clock (MHz)		120					
Flash memory size (KB) with 1024 words per page		48	48	48	64	64	64
RAM size (KB)		6	6	8	8	8	8
Enhanced Flex PWM (eFlexPWM)	High resolution NanoEdge PWM (520 ps res.)	6	6	6	6	6	6
	Enhanced Flex PWM with Input Capture	0	0	3	0	0	3
	PWM Fault Inputs (from Crossbar Input)	4	4	4	4	4	4
12-bit ADC with x1, 2x, 4x Programmable Gain		2 x 4Ch	2 x 5Ch	2 x 8Ch	2 x 4Ch	2 x 5 Ch	2 x 8 Ch
Analog comparators (ACMP) each with integrated 5-bit DAC		3					
12-bit DAC		1					
Cyclic Redundancy Check (CRC)		Yes					
Inter-Integrated Circuit (I^2C) / SMBus		2					
Queued Serial peripheral Interface (QSPI)		1					
High speed Queued Serial Communications Interface (QSCI)[1]		2					
Controller Area Network (MSCAN)		0			1		
High Speed 16-bit multi-purpose timers (TMR)[2]		8					
Computer operating properly (COP) watchdog timer		Yes					
Integrated Power-On Reset and low voltage detection		Yes					
Phase-locked loop (PLL)		Yes					
8 MHz (400 kHz at standby mode) on-chip ROSC		Yes					
Crystal/resonator oscillator		Yes					
Crossbar	Input pins	6	6	6	6	6	6
	Output pins	2	2	6	2	2	6
General purpose I/O (GPIO)[3]		35	39	54	35	39	54
IEEE 1149.1 Joint Test Action Group (JTAG) interface		Yes					
Enhanced on-chip emulator (EOnCE)		Yes					
Operating temperature range		-40 °C to 105 °C					
Package		44LQFP	48LQFP	64LQFP	44LQFP	48LQFP	64LQFP

1 Can be clocked by high speed peripheral clock up to 120 MHz

2 Can be clocked by high speed peripheral clock up to 120 MHz

3 Shared with other function pins

2 Overview

2.1 MC56F825x/MC56F824x Features

2.1.1 Core

- Efficient 56800E digital signal processor (DSP) engine with modified Harvard architecture
  - Three internal address buses
  - Four internal data buses
- As many as 60 million instructions per second (MIPS) at 60 MHz core frequency
- 155 basic instructions in conjunction with up to 20 address modes
- 32-bit internal primary data buses supporting 8-bit, 16-bit, and 32-bit data movement, addition, subtraction, and logical operation
- Single-cycle 16 × 16-bit parallel multiplier-accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 32-bit arithmetic and logic multi-bit shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Instruction set supports DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/enhanced on-chip emulation (EOnCE) for unobtrusive, processor speed–independent, real-time debugging

2.1.2 Operation Range

- 3.0 V to 3.6 V operation (power supplies and I/O)
- From power-on-reset: approximately 2.7 V to 3.6 V
- Ambient temperature operating range: –40 °C to +105 °C

2.1.3 Memory

- Dual Harvard architecture that permits as many as three simultaneous accesses to program and data memory
- 48 KB (24K x 16) to 64 KB (32K x 16) on-chip flash memory with 2048 bytes (1024 x 16) page size
- 6 KB (3K x 16) to 8 KB (4K x 16) on-chip RAM with byte addressable
- EEPROM emulation capability using flash
- Support for 60 MHz program execution from both internal flash and RAM memories
- Flash security and protection that prevent unauthorized users from gaining access to the internal flash

2.1.4 Interrupt Controller

- Five interrupt priority levels
  - Three user programmable priority levels for each interrupt source: Level 0, 1, 2
  - Unmaskable level 3 interrupts include: illegal instruction, hardware stack overflow, misaligned data access, and SWI3 instruction
  - Maskable level 3 interrupts include: EOnCE step counter, EOnCE breakpoint unit, and EOnCE trace buffer

  - Lowest-priority software interrupt: level LP
- Nested interrupts: higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to system integration module (SIM) to restart clock out of wait and stop states
- Ability to relocate interrupt vector table

The masking of interrupt priority level is managed by the 56800E core.

2.1.5 Peripheral Highlights

- One Enhanced Flex Pulse Width Modulator (eFlexPWM) module
  - Up to nine output channels
  - 16-bit resolution for center aligned, edge aligned, and asymmetrical PWMs
  - Each complementary pair can operate with its own PWM frequency based and deadtime values
    - 4 Time base
    - Independent top and bottom deadtime insertion
  - PWM outputs can operate as complimentary pairs or independent channels
  - Independent control of both edges of each PWM output
  - 6-channel NanoEdge high resolution PWM
    - Fractional delay for enhanced resolution of the PWM period and edge placement
    - Arbitrary eFlexPWM edge placement - PWM phase shifting
    - NanoEdge implementation: 520 ps PWM frequency resolution
  - 3 Channel PWM with full Input Capture features
    - Three PWM Channels - PWMA, PWMB, and PWMX
    - Enhanced input capture functionality
  - Support for synchronization to external hardware or other PWM
  - Double buffered PWM registers
    - Integral reload rates from 1 to 16
    - Half cycle reload capability
  - Multiple output trigger events can be generated per PWM cycle via hardware
  - Support for double switching PWM outputs
  - Up to four fault inputs can be assigned to control multiple PWM outputs
    - Programmable filters for fault inputs
  - Independently programmable PWM output polarity
  - Individual software control for each PWM output
  - All outputs can be programmed to change simultaneously via a FORCE_OUT event
  - PWMX pin can optionally output a third PWM signal from each submodule
  - Channels not used for PWM generation can be used for buffered output compare functions
  - Channels not used for PWM generation can be used for input capture functions
  - Enhanced dual edge capture functionality
  - Option to supply the source for each complementary PWM signal pair from any of the following:
    - Crossbar module outputs
    - External ADC input, taking into account values set in ADC high and low limit registers
- Two independent 12-bit analog-to-digital converters (ADCs)
  - 2 x 8 channel external inputs
  - Built-in x1, x2, x4 programmable gain pre-amplifier

  - Maximum ADC clock frequency: up to 10 MHz
    - Single conversion time of 8.5 ADC clock cycles (8.5 x 100 ns = 850 ns)
    - Additional conversion time of 6-ADC clock cycles (6 x 100 ns = 600 ns)
  - Sequential, parallel, and independent scan mode
  - First 8 samples have Offset, Limit and Zero-crossing calculation supported
  - ADC conversions can be synchronized by eFlexPWM and timer modules via internal crossbar module
  - Support for simultaneous and software triggering conversions
  - Support for multi-triggering mode with a programmable number of conversions on each trigger
- Inter-module Crossbar Switch (XBAR)
  - Programmable internal module connections among the eFlexPWM, ADCs, Quad Timers, 12-bit DAC, HSCMPs, and package pins
  - User-defined input/output pins for PWM fault inputs, Timer input/output, ADC triggers, and Comparator outputs
- Three analog comparators (CMPs)
  - Selectable input source includes external pins, internal DACs
  - Programmable output polarity
  - Output can drive timer input, eFlexPWM fault input, eFlexPWM source, external pin output, and trigger ADCs
  - Output falling and rising edge detection able to generate interrupts
  - 32-tap programmable voltage reference per comparator
- One 12-bit digital-to-analog converter (12-bit DAC)
  - 12-bit resolution
  - Power down mode
  - Output can be routed to internal comparator, or off chip
- Two four-channel 16-bit multi-purpose timer (TMR) modules
  - Four independent 16-bit counter/timers with cascading capability per module
  - Up to 120 MHz operating clock
  - Each timer has capture and compare and quadrature decoder capability
  - Up to 12 operating modes
  - Four external inputs and two external outputs
- Two queued serial communication interface (QSCI) modules with LIN slave functionality
  - Up to 120 MHz operating clock
  - Four-byte-deep FIFOs available on both transmit and receive buffers
  - Full-duplex or single-wire operation
  - Programmable 8- or 9-bit data format
  - 13-bit integer and 3-bit fractional baud rate selection
  - Two receiver wakeup methods:
    - Idle line
    - Address mark
  - 1/16 bit-time noise detection
  - Support LIN slave operation
- One queued serial peripheral interface (QSPI) module
  - Full-duplex operation
  - Four-word deep FIFOs available on both transmit and receive buffers
  - Master and slave modes
  - Programmable length transactions (2 to 16 bits)
  - Programmable transmit and receive shift order (MSB as first or last bit transmitted)

  - Maximum slave module frequency = module clock frequency/2
  - 13-bit baud rate divider for low speed communication
- Two inter-integrated circuit (I^2C) ports
  - Operation at up to 100 kbps
  - Support for master and slave operation
  - Support for 10-bit address mode and broadcasting mode
  - Support for SMBus, Version 2
- One Freescale Scalable Controller Area Network (MSCAN) module
  - Fully compliant with CAN protocol Version 2.0 A/B
  - Support for standard and extended data frames
  - Support for data rate up to 1 Mbit/s
  - Five receive buffers and three transmit buffers
- Computer operating properly (COP) watchdog timer capable of selecting different clock sources
  - Programmable prescaler and timeout period
  - Programmable wait, stop, and partial powerdown mode operation
  - Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
  - Choice of clock sources from four sources in support of EN60730 and IEC61508:
    - On-chip relaxation oscillator
    - External crystal oscillator/external clock source
    - System clock (IP bus to 60 MHz)
- Power supervisor (PS)
  - On-chip linear regulator for digital and analog circuitry to lower cost and reduce noise
  - Integrated low voltage detection to generate warning interrupt if VDD is below low voltage detection (LVI) threshold
  - Integrated power-on reset (POR)
    - Reliable reset process during power-on procedure
    - POR is released after VDD passes low voltage detection (LVI) threshold
  - Integrated brown-out reset
  - Run, wait, and stop modes
- Phase lock loop (PLL) providing a high-speed clock to the core and peripherals
  - 2x system clock provided to Quad Timers and SCIs
  - Loss of lock interrupt
  - Loss of reference clock interrupt
- Clock sources
  - On-chip relaxation oscillator with two user selectable frequencies: 400 kHz for low speed mode, 8 MHz for normal operation
  - External clock: crystal oscillator, ceramic resonator, and external clock source
- Cyclic Redundancy Check (CRC) Generator
  - Hardware CRC generator circuit using 16-bit shift register
  - CRC16-CCITT compliancy with x16 + x12 + x5 + 1 polynomial
  - Error detection for all single, double, odd, and most multi-bit errors
  - Programmable initial seed value
  - High-speed hardware CRC calculation
  - Optional feature to transpose input data and CRC result via transpose register, required on applications where bytes are in LSb (Least Significant bit) format.

- Up to 54 general-purpose I/O (GPIO) pins
  - 5 V tolerant I/O
  - Individual control for each pin to be in peripheral or GPIO mode
  - Individual input/output direction control for each pin in GPIO mode
  - Individual control for each output pin to be in push-pull mode or open-drain mode
  - Hysteresis and configurable pullup device on all input pins
  - Ability to generate interrupt with programmable rising or falling edge and software interrupt
  - Configurable drive strength: 4 mA / 8 mA sink/source current
- JTAG/EOnCE debug programming interface for real-time debugging
  - IEEE 1149.1 Joint Test Action Group (JTAG) interface
  - EOnCE interface for real-time debugging

2.1.6 Power Saving Features

- Low-speed run, wait, and stop modes: as low as 781 Hz clock provided by OCCS and internal ROSC
- Large regulator standby mode available for reducing power consumption at low-speed mode
- Less than 30 µs typical wakeup time from stop modes
- Each peripheral can be individually disabled to save power

2.2 Award-Winning Development Environment

Processor Expert (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior Integrated Development Environment (IDE) is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs), demonstration board kit, and development system cards supports concurrent engineering. Together, PE, CodeWarrior, and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

2.3 Architecture Block Diagram

The MC56F825x/MC56F824x's architecture appears in Figure 1 and Figure 2. Figure 1 illustrates how the 56800E system buses communicate with internal memories and the IP bus interface as well as the internal connections among the units of the 56800E core.

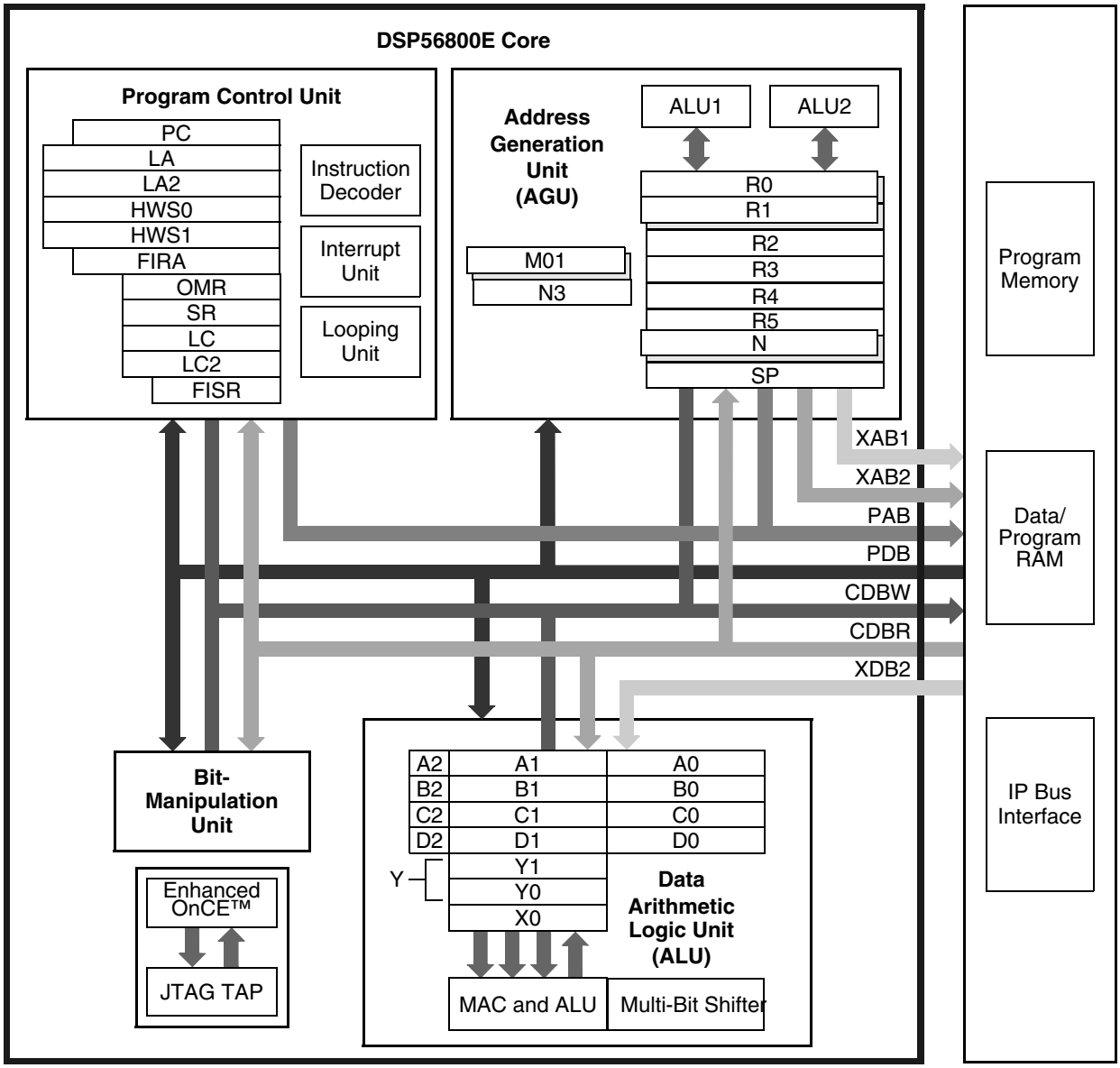

Figure 1. 56800E Core Block Diagram

Figure 2 shows the peripherals and control blocks connected to the IP bus bridge. Refer to the system integration module (SIM) section in the device's reference manual for information about which signals are multiplexed with those of other peripherals.

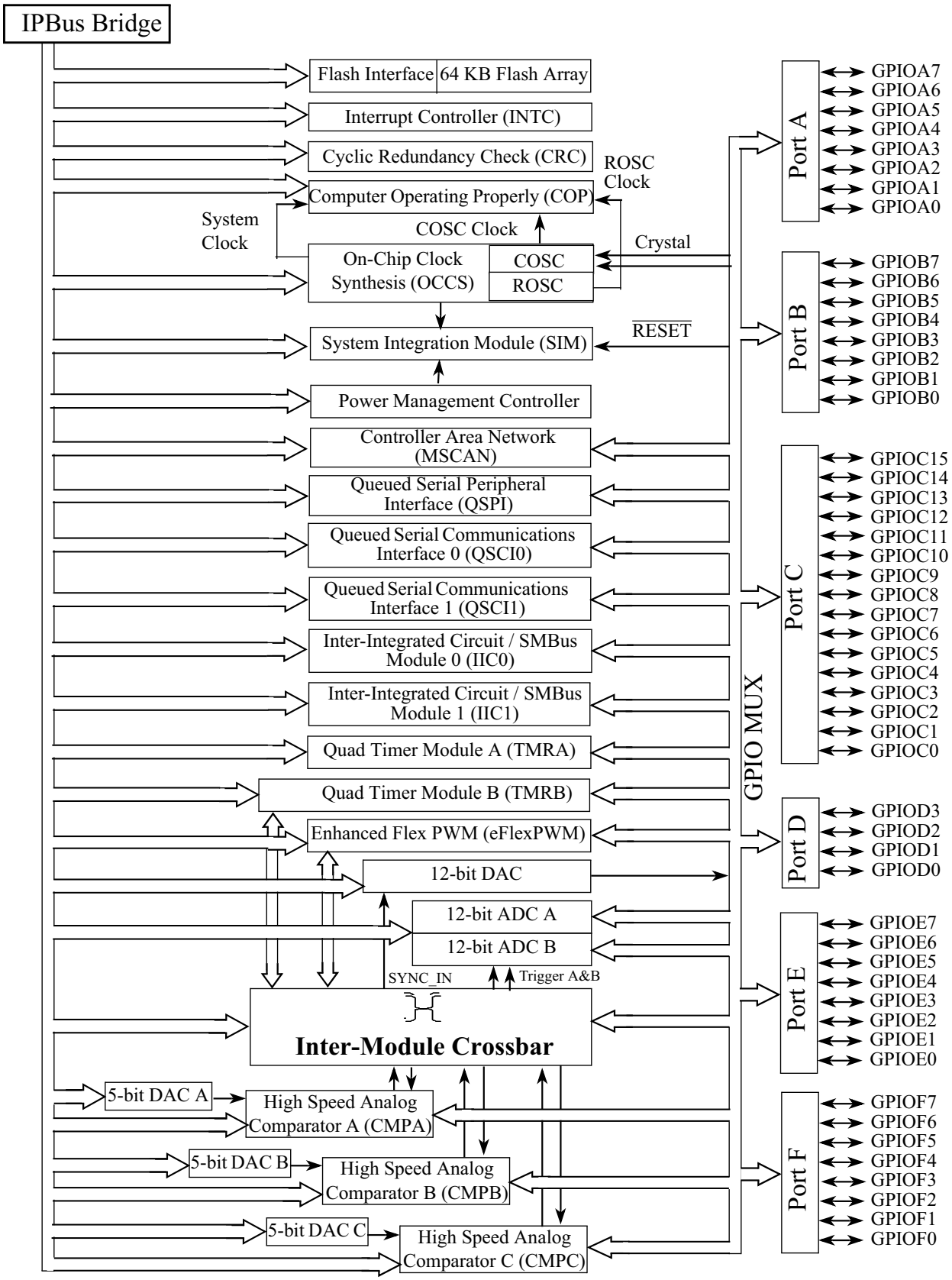

Figure 2. Peripheral Subsystem

2.4 Product Documentation

The documents listed in Table 2 are required for a complete description and proper design with the MC56F825x/MC56F824x. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at http://www.freescale.com.

Table 2. MC56F825x/MC56F824x Device Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, 16-bit digital signal controller core processor, and the instruction set	DSP56800ERM
MC56F825x Reference Manual	Detailed description of peripherals of the MC56F825x/MC56F824x devices	MC56F825XRM
MC56F824x/5x Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the 56F800x family of devices	TBD
MC56F825x Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	MC56F825X
MC56F825x Errata	Detailed description of any chip issues that might be present	MC56F825XE

3 Signal/Connection Descriptions

3.1 Introduction

The input and output signals of the MC56F825x/MC56F824x are organized into functional groups, as detailed in Table 3.

Table 3. Functional Group Pin Allocations

Functional Group	Number of Pins in 44 LQFP	Number of Pins in 48 LQFP	Number of Pins in 64 LQFP
Power inputs (V_{DD}, V_{DDA}, V_{CAP})	5	5	6
Ground (V_{SS}, V_{SSA})	4	4	4
Reset[1]	1	1	1
Enhanced Flex Pulse Width Modulator (eFlexPWM) ports[1]	6	6	9
Queued Serial Peripheral Interface (SPI) ports[1]	4	4	4
Queued Serial Communications Interface 0&1 (QSCI0 & QSCI1) ports[1]	6	6	9
Inter-Integrated Circuit Interface 0&1 (I^2C0 & I^2C0) ports[1]	4	4	6
Analog-to-Digital Converter (ADC) inputs[1]	8	10	16
High Speed Analog Comparator inputs/outputs[1]	11	12	15
12-bit Digital-to-Analog Converter (DAC_12B) output	1	1	1
Quad Timer Module (TMRA & TMRB) ports[1]	5	5	8
Freescale's Scalable Controller-Area-Network (MSCAN)[1, 2]	2	2	2
Inter-Module Cross Bar package inputs/outputs[1]	10	12	17
Clock[1]	3	4	4
JTAG/Enhanced On-Chip Emulation (EOnCE)[1]	4	4	4

1 Pins may be shared with other peripherals. See Table 4.

2 Exclude MC56F824x.

Table 4 summarizes all device pins. Each table row describes the signal or signals present on a pin, sorted by pin number. Peripheral pins in bold identify reset state.

Table 4. MC56F825x/MC56F824x Pins

Pin Number			Pin Name	Peripherals													
44 LQFP	48 LQFP	64 LQFP		GPIO	I^2C	SCI	SPI	MS CAN[1]	ADC	Cross Bar	COMP	Quad Timer	eFlex PWM	Power	JTAG	Misc.
1	1	1	TCK/*GPIOD2*	*GPIOD2*											**TCK**	
2	2	2	$\overline{\text{RESET}}$ / *GPIOD4*	*GPIOD4*												**$\overline{\text{RESET}}$**
3	3	3	GPIOC0/*XTAL/CLKIN*	**GPIOC0**												*XTAL/ CLKIN*
4	4	4	GPIOC1/*EXTAL*	**GPIOC1**												*EXTAL*
5	5	5	GPIOC2/*TXD0/TB0/XB_IN2/ CLKO*	**GPIOC2**		*TXD0*				*XB_IN2*		*TB0*				*CLKO*
		6	GPIOF8/*RXD0/TB1*	**GPIOF8**		*RXD0*						*TB1*				
6	6	7	GPIOC3/*TA0/CMPA_O/RXD0*	**GPIOC3**		*RXD0*					*CMPA_O*	*TA0*				
7	7	8	GPIOC4/*TA1/CMPB_O*	**GPIOC4**							*CMPB_O*	*TA1*				
		9	GPIOA7/*ANA7*	**GPIOA7**					*ANA7*							
		10	GPIOA6/*ANA6*	**GPIOA6**					*ANA6*							
		11	GPIOA5/*ANA5*	**GPIOA5**					*ANA5*							
	8	12	GPIOA4/*ANA4*	**GPIOA4**					*ANA4*							
8	9	13	GPIOA0/*ANA0& CMPA_P2/CMPC_O*	**GPIOA0**					*ANA0*		*CMPA_P2/ CMPC_O*					
9	10	14	GPIOA1/ *ANA1&CMPA_M0*	**GPIOA1**					*ANA1*		*CMPA_M0*					
10	11	15	GPIOA2/*ANA2&VREFHA& CMPA_M1*	**GPIOA2**					*ANA2& VREFHA*		*CMPA_M1*					
11	12	16	GPIOA3/*ANA3&VREFLA& CMPA_M2*	**GPIOA3**					*ANA3& VREFLA*		*CMPA_M2*					
		17	GPIOB7/*ANB7&CMPB_M2*	**GPIOB7**					*ANB7*		*CMPB_M2*					
12	13	18	GPIOC5/*DACO/XB_IN7*	**GPIOC5**						*XB_IN7*						*DACO*
		19	GPIOB6/*ANB6&CMPB_M1*	**GPIOB6**					*ANB6*		*CMPB_M1*					
		20	GPIOB5/*ANB5&CMPC_M2*	**GPIOB5**					*ANB5*		*CMPC_M2*					
	14	21	GPIOB4/*ANB4&CMPC_M1*	**GPIOB4**					*ANB4*		*CMPC_M1*					
13	15	22	V_{DDA}											**V_{DDA}**		
14	16	23	V_{SSA}											**V_{SSA}**		
15	17	24	GPIOB0/ *ANB0&CMPB_P2*	**GPIOB0**					*ANB0*		*CMPB_P2*					
16	18	25	GPIOB1/ *ANB1&CMPB_M0*	**GPIOB1**					*ANB1*		*CMPB_M0*					
17	19	26	V_{CAP}											**V_{CAP}**		
18	20	27	GPIOB2/ *ANB2&VREFHB&CMPC_P2*	**GPIOB2**					*ANB2& VREFHB*		*CMPC_P2*					

Table 4. MC56F825x/MC56F824x Pins (continued)

Pin Number			Pin Name	Peripherals													
44 LQFP	48 LQFP	64 LQFP		GPIO	I^2C	SCI	SPI	MSCAN[1]	ADC	Cross Bar	COMP	Quad Timer	eFlex PWM	Power	JTAG	Misc.
19	21	28	GPIOB3/ *ANB3&VREFLB&CMPC_M0*	**GPIOB3**					*ANB3& VREFLB*		*CMPC_M0*					
		29	V_{DD}											**V_{DD}**		
20	22	30	V_{SS}											**V_{SS}**		
21	23	31	GPIOC6/*TA2/XB_IN3/ CMP_REF*	**GPIOC6**						*XB_IN3*	*CMP_REF*	*TA2*				
22	24	32	GPIOC7/$\overline{SS}$/*TXD0*	**GPIOC7**		*TXD0*	$\overline{SS}$									
23	25	33	GPIOC8/*MISO/RXD0*	**GPIOC8**		*RXD0*	*MISO*									
24	26	34	GPIOC9/*SCLK/XB_IN4*	**GPIOC9**			*SCLK*			*XB_IN4*						
25	27	35	GPIOC10/MOSI/XB_IN5/MISO	**GPIOC10**			MOSI/ MISO			XB_IN5						
	28	36	GPIOF0/*XB_IN6*	**GPIOF0**						*XB_IN6*						
26	29	37	GPIOC11/*CANTX/SCL1/TXD1*	**GPIOC11**	*SCL1*	*TXD1*		*CANTX*								
27	30	38	GPIOC12/*CANRX/SDA1/RXD1*	**GPIOC12**	*SDA1*	*RXD1*		*CANRX*								
		39	GPIOF2/*SCL1/XB_OUT2*	**GPIOF2**	*SCL1*					*XB_OUT2*						
		40	GPIOF3/*SDA1/XB_OUT3*	**GPIOF3**	*SDA1*					*XB_OUT3*						
		41	GPIOF4/*TXD1/XB_OUT4*	**GPIOF4**		*TXD1*				*XB_OUT4*						
		42	GPIOF5/*RXD1/XB_OUT5*	**GPIOF5**		*RXD1*				*XB_OUT5*						
28	31	43	V_{SS}											**V_{SS}**		
29	32	44	V_{DD}											**V_{DD}**		
30	33	45	GPIOE0/*PWM0B*	**GPIOE0**									*PWM0B*			
31	34	46	GPIOE1/*PWM0A*	**GPIOE1**									*PWM0A*			
32	35	47	GPIOE2/*PWM1B*	**GPIOE2**									*PWM1B*			
33	36	48	GPIOE3/*PWM1A*	**GPIOE3**									*PWM1A*			
34	37	49	GPIOC13/*TA3/XB_IN6*	**GPIOC13**						*XB_IN6*		TA3				
	38	50	GPIOF1/*CLKO/XB_IN7*	**GPIOF1**						*XB_IN7*						*CLKO*
35	39	51	GPIOE4/*PWM2B/XB_IN2*	**GPIOE4**						*XB_IN2*			*PWM2B*			
36	40	52	GPIOE5/*PWM2A/XB_IN3*	**GPIOE5**						*XB_IN3*			*PWM2A*			
		53	GPIOE6/*PWM3B/XB_IN4*	**GPIOE6**						*XB_IN4*			*PWM3B*			
		54	GPIOE7/*PWM3A/XB_IN5*	**GPIOE7**						*XB_IN5*			*PWM3A*			
37	41	55	GPIOC14/*SDA0/XB_OUT0*	**GPIOC14**	*SDA0*					*XB_OUT0*						
38	42	56	GPIOC15/*SCL0/XB_OUT1*	**GPIOC15**	*SCL0*					*XB_OUT1*						
39	43	57	V_{CAP}											**V_{CAP}**		
		58	GPIOF6/*TB2/PWM3X*	**GPIOF6**								*TB2*	*PWM3X*			
		59	GPIOF7/*TB3*	**GPIOF7**								*TB3*				
40	44	60	V_{DD}											**V_{DD}**		

Table 4. MC56F825x/MC56F824x Pins (continued)

Pin Number			Pin Name	Peripherals												
44 LQFP	48 LQFP	64 LQFP		GPIO	I^2C	SCI	SPI	MS CAN[1]	ADC	Cross Bar	COMP	Quad Timer	eFlex PWM	Power	JTAG	Misc.
41	45	61	V_{SS}											V_{SS}		
42	46	62	TDO/*GPIOD1*	***GPIOD1***											**TDO**	
43	47	63	TMS/*GPIOD3*	***GIPOD3***											**TMS**	
44	48	64	TDI/*GPIOD0*	***GPIOD0***											**TDI**	

[1] The MSCAN module is not available on the MC56F824x devices.

3.2 Pin Assignment

Figure 3 shows the pin assignments of the 56F8245 and 56F8255's 44-pin low-profile quad flat pack (44LQFP). Figure 4 shows the pin assignments of the 56F8246 and 56F8256's 48-pin low-profile quad flat pack (48LQFP). Figure 5 shows the pin assignments of the 56F8247 and 56F8257's 64-pin low-profile quad flat pack (64LQFP).

NOTE

The CANRX and CANTX signals of the MSCAN module are not available on the MC56F824x devices.

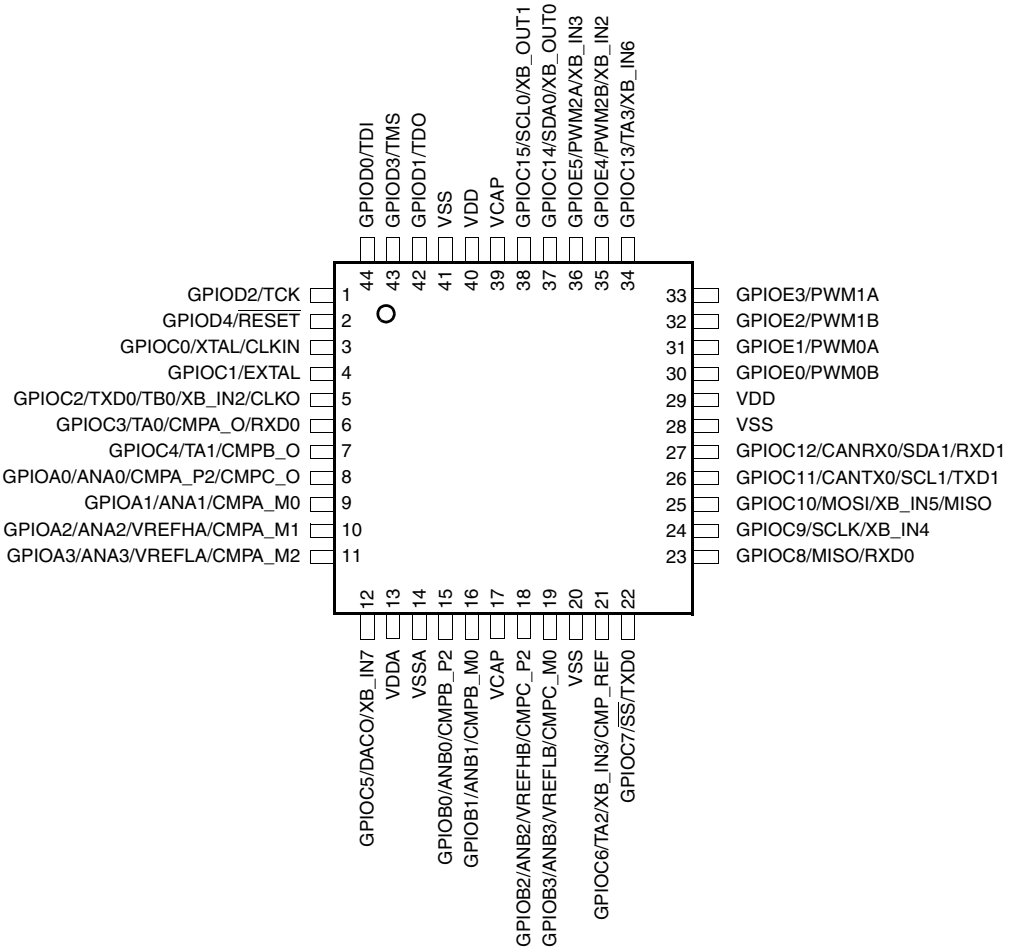

Figure 3. Top View: 56F8245 and 56F8255 44-Pin LQFP Package

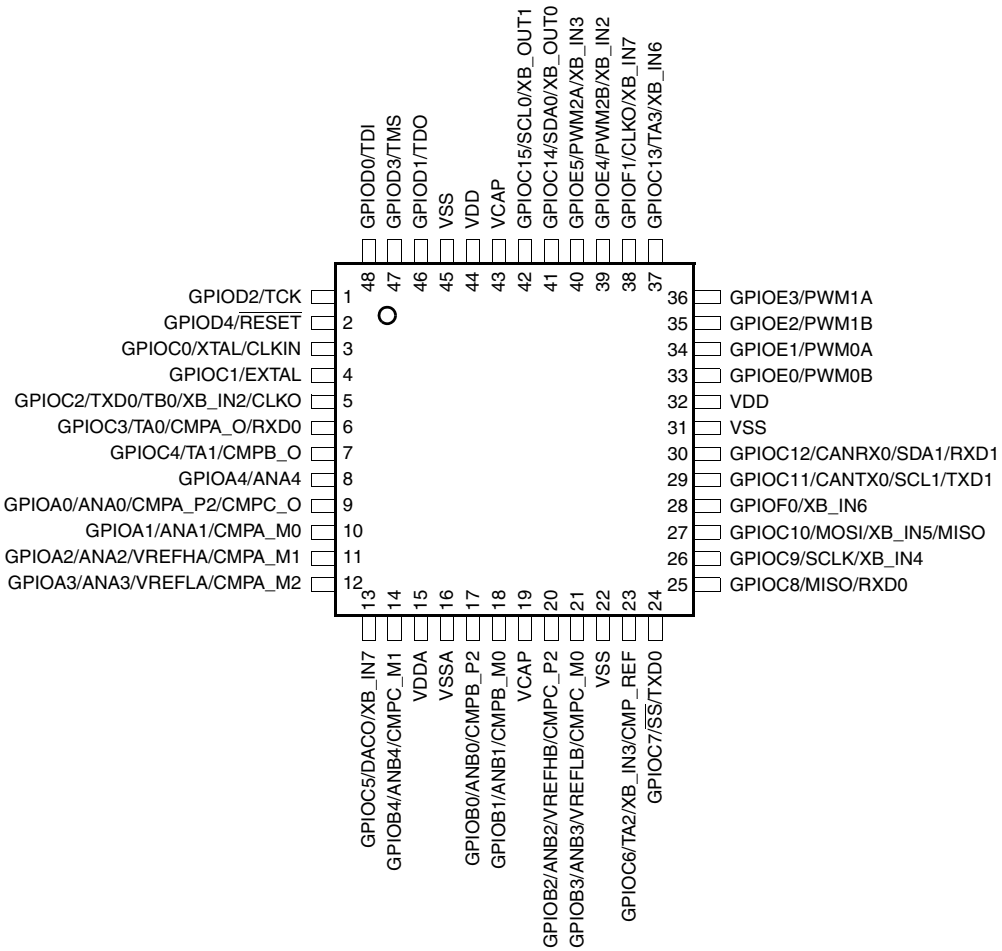

Figure 4. Top View: 56F8246 and 56F8256 48-Pin LQFP Package

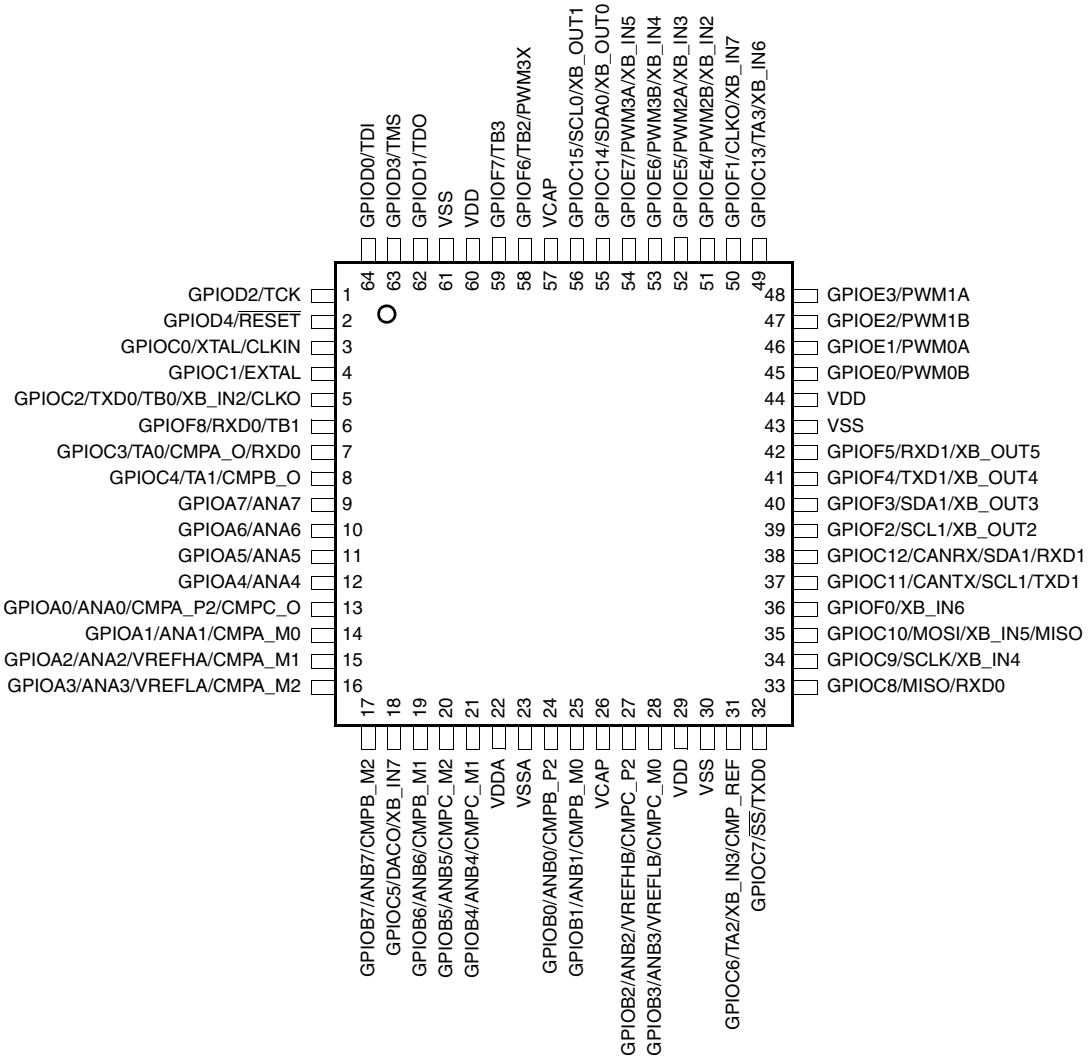

Figure 5. Top View: 56F8247 and 56F8257 64-Pin LQFP Package

3.3 MC56F825x/MC56F824x Signal Pins

After reset, each pin is configured for its primary function (listed first). Any alternative functionality, shown in parentheses and as *italic*, must be programmed via the GPIO module's peripheral enable registers (GPIO_x_PER) and the SIM module's GPIO peripheral select (GPSx) registers.

Table 5. MC56F825x/MC56F824x Signal and Package Information

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
V_{DD}			29	Supply	Supply	I/O Power — This pin supplies 3.3 V power to the chip I/O interface.
V_{DD}	29	32	44			
V_{DD}	40	44	60			
V_{SS}	20	22	30	Supply	Supply	I/O Ground — These pins provide ground for chip I/O interface.
V_{SS}	28	31	43			
V_{SS}	41	45	61			
V_{DDA}	13	15	22	Supply	Supply	Analog Power — This pin supplies 3.3 V power to the analog modules. It must be connected to a clean analog power supply.
V_{SSA}	14	16	23	Supply	Supply	Analog Ground — This pin supplies an analog ground to the analog modules. It must be connected to a clean power supply.
V_{CAP}	17	19	26	Supply	Supply	V_{CAP} — Connect a bypass capacitor of 2.2 µF or greater between this pin and V_{SS} to stabilize the core voltage regulator output required for proper device operation. See Section 8.2, "Electrical Design Considerations," on page 73.
V_{CAP}	39	43	57			
TDI *(GPIOD0)*	44	48	64	Input Input/ Output	Input, internal pullup enabled	Test Data Input — This input pin provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an on-chip pullup resistor. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDI.
TDO *(GPIOD1)*	42	46	62	Output Input/ Output	Output	Test Data Output — This tri-stateable output pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and changes on the falling edge of TCK. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDO.
TCK *(GPIOD2)*	1	1	1	Input Input/ Output	Input, internal pullup enabled	Test Clock Input — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pullup resistor. A Schmitt-trigger input is used for noise immunity. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TCK

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
TMS *(GPIOD3)*	43	47	63	input Input/ Output	Input, internal pullup enabled	Test Mode Select Input — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pullup resistor. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TMS **Note**: Always tie the TMS pin to VDD through a 2.2K resistor if need to keep on-board debug capability. Otherwise directly tie to VDD
$\overline{\text{RESET}}$ *(GPIOD4)*	2	2	2	Input Input/ Open-drain Output	Input, internal pullup enabled	Reset — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the reset state. A Schmitt-trigger input is used for noise immunity. The internal reset signal is deasserted synchronous with the internal clocks after a fixed number of internal clocks. Port D GPIO — This GPIO pin can be individually programmed as an input or open-drain output pin.If $\overline{\text{RESET}}$ functionality is disabled in this mode and the chip can be reset only via POR, COP reset, or software reset. After reset, the default state is $\overline{\text{RESET}}$.
GPIOA0 *(ANA0& CMPA_P2)* *(CMPC_O)*	8	9	13	Input/ Output Input Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA0 and CMPA_P2 — Analog input to channel 0 of ADCA and positive input 2 of analog comparator A. CMPC_O— Analog comparator C output When used as an analog input, the signal goes to the ANA0 and CMPA_P2. After reset, the default state is GPIOA0.
GPIOA1 *(ANA1& CMPA_M0)*	9	10	14	Input/ Output Input	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA1 and CMPA_M0 — Analog input to channel 1of ADCA and negative input 0 of analog comparator A. When used as an analog input, the signal goes to the ANA1 and CMPA_M0. After reset, the default state is GPIOA1.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOA2 *(ANA2& VREFHA& CMPA_M1)*	10	11	15	Input/ Output Input	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA2 and VREFHA and CMPA_M1 — Analog input to channel 2 of ADCA and analog references high of ADCA and negative input 1 of analog comparator A. When used as an analog input, the signal goes to ANA2 and VREFHA and CMPA_M1. ADC control register configures this input as ANA2 or VREFHA. After reset, the default state is GPIOA2.
GPIOA3 *(ANA3& VREFLA& CMPA_M2)*	11	12	16	Input/ Output Input	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA3 and VREFLA and CMPA_M2 — Analog input to channel 3 of ADCA and analog references low of ADCA and negative input 2 of analog comparator A. When used as an analog input, the signal goes to ANA3 and VREFLA and CMPA_M2. ADC control register configures this input as ANA3 or VREFLA. After reset, the default state is GPIOA3.
GPIOA4 *(ANA4)*		8	12	Input/ Output Input	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA4 — Analog input to channel 4 of ADCA. After reset, the default state is GPIOA4.
GPIOA5 *(ANA5)*			11	Input/ Output Input	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA5 — Analog input to channel 5 of ADCA. After reset, the default state is GPIOA5.
GPIOA6 *(ANA6)*			10	Input/ Output Input	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA6 — Analog input to channel 5 of ADCA. After reset, the default state is GPIOA6.
GPIOA7 *(ANA7)*			9	Input/ Output Input	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA7 — Analog input to channel 7 of ADCA. After reset, the default state is GPIOA7.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOB0 *(ANB0& CMPB_P2)*	15	17	24	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB0 and CMPB_P2 — Analog input to channel 0 of ADCB and positive input 2 of analog comparator B. When used as an analog input, the signal goes to ANB0 and CMPB_P2. After reset, the default state is GPIOB0.
GPIOB1 *(ANB1& CMPB_M0)*	16	18	25	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB1 and CMPB_M0— Analog input to channel 1 of ADCB and negative input 0 of analog comparator B. When used as an analog input, the signal goes to ANB1 and CMPB_M0. After reset, the default state is GPIOB1.
GPIOB2 *(ANB2& VREFHB& CMPC_P2)*	18	20	27	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB2 and VREFHB and CMPC_P2 — Analog input to channel 2 of ADCB and analog references high of ADCB and positive input 2 of analog comparator C. When used as an analog input, the signal goes to ANB2 and VREFHB and CMPC_P2. ADC control register configures this input as ANB2 or VREFHB. After reset, the default state is GPIOB2.
GPIOB3 *(ANB3& VREFLB& CMPC_M0)*	19	21	28	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB3 and VREFLB and CMPC_M0 — Analog input to channel 3 of ADCB and analog references low of ADCB and negative input 0 of analog comparator C. When used as an analog input, the signal goes to ANB3 and VREFLB and MPC_M0. ADC control register configures this input as ANB3 or VREFLB. After reset, the default state is GPIOB3.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOB4 *(ANB4& CMPC_M1)*		14	21	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB4 and CMPC_M1 — Analog input to channel 4 of ADCB and negative input 1 of analog comparator C. After reset, the default state is GPIOB4.
GPIOB5 *(ANB5& CMPC_M2)*			20	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB5 and CMPC_M2 — Analog input to channel 5 of ADCB and negative input 2 of analog comparator C. After reset, the default state is GPIOB5.
GPIOB6 *(ANB6& CMPB_M1)*			19	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB6 and CMPB_M1 — Analog input to channel 6 of ADCB and negative input 1 of analog comparator B. After reset, the default state is GPIOB6.
GPIOB7 *(ANB7& CMPB_M2)*			17	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB7 and CMPB_M2 — Analog input to channel 7 of ADCB and negative input 2 of analog comparator B. After reset, the default state is GPIOB7.
GPIOC0 *XTAL* *CLKIN*	3	3	3	Input/ Output Analog Output Input	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. XTAL — External Crystal Oscillator Output. This output connects the internal crystal oscillator output to an external crystal or ceramic resonator. CLKIN — This pin serves as an external clock input.[1] After reset, the default state is GPIOC0.
GPIOC1 *(EXTAL)*	4	4	4	Input/ Output Analog Input	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. EXTAL — External Crystal Oscillator Input. This input connects the internal crystal oscillator input to an external crystal or ceramic resonator. After reset, the default state is GPIOC1.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOC2	5	5	5	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TXD0)				Output		TXD0 — The SCI0 transmit data output or transmit/receive in single wire operation.
(TB0)				Input/ Output		TB0 — Quad timer module B channel 0 input/output.
(XB_IN2)				Input		XB_IN2 — Crossbar module input 2
(CLKO)				Output		CLKO — This is a buffered clock output; the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM. After reset, the default state is GPIOC2.
GPIOC3	6	6	7	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA0)				Input/ Output		TA0 — Quad timer module A channel 0 input/output.
(CMPA_O)				Output		CMPA_O— Analog comparator A output
(RXD0)				Input		RXD0 — The SCI0 receive data input. After reset, the default state is GPIOC3.
GPIOC4	7	7	8	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA1)				Input/ Output		TA1 — Quad timer module A channel 1input/output
(CMPB_O)				Output		CMPB_O — Analog comparator B output After reset, the default state is GPIOC4.
GPIOC5	12	13	18	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(DACO)				Analog Output		DACO — 12-bit Digital-to-Analog Controller output
(XB_IN7)				Input		XB_IN7 — Crossbar module input 7 After reset, the default state is GPIOC5.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOC6	21	23	31	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA2)				Input/ Output		TA2 — Quad timer module A channel 2 input/output
(XB_IN3)				Input		XB_IN3 — Crossbar module input 3
(CMP_REF)				Analog Input		CMP_REF— Positive input 3 of analog comparator A and B and C
						After reset, the default state is GPIOC6
GPIOC7	22	24	32	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
($\overline{SS}$)				Input/ Output		$\overline{SS}$ — $\overline{SS}$ is used in slave mode to indicate to the SPI module that the current transfer is to be received.
(TXD0)				Output		TXD0 — SCI0 transmit data output or transmit/receive in single wire operation
						After reset, the default state is GPIOC7.
GPIOC8	23	25	33	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(MISO)				Input/ Output		MISO — Master in/slave out. In master mode, this pin serves as the data input. In slave mode, this pin serves as the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
(RXD0)				Input		RXD0 — SCI0 receive data input
						After reset, the default state is GPIOC8.
GPIOC9	24	26	34	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(SCLK)				Input/ Output		SCLK — The SPI serial clock. In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input.
(XB_IN4)				Input		XB_IN4 — Crossbar module input 4
						After reset, the default state is GPIOC9.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOC10	25	27	35	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(MOSI)				Input/ Output		MOSI — Master out/slave in. In master mode, this pin serves as the data output. In slave mode, this pin serves as the data input.
(XB_IN5)				Input		XB_IN5 — Crossbar module input 5
(MISO)				Input/ Output		MISO — Master in/slave out. In master mode, this pin serves as the data input. In slave mode, this pin serves as the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. After reset, the default state is GPIOC10.
GPIOC11	26	29	37	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(CANTX)				Open-drain Output		CANTX — CAN transmit data output (not available on 56F8245/46/47)
(SCL1)				Input/ Open-drain Output		SCL1 — I^2C1 serial clock
(TXD1)				Output		TXD1 — SCI1 transmit data output or transmit/receive in single wire operation After reset, the default state is GPIOC11.
GPIOC12	27	30	38	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(CANRX)				Input		CANRX — CAN receive data input (not available on 56F8245/46/47)
(SDA1)				Input/ Open-drain Output		SDA1 — I^2C1 serial data line
(RXD1)				Input		RXD1 — SCI1 receive data input After reset, the default state is GPIOC12.
GPIOC13	34	37	49	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA3)				Input/ Output		TA3 — Quad timer module A channel 3input/output.
(XB_IN6)				Input		XB_IN6 — Crossbar module input 6 After reset, the default state is GPIOC13.