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NXP Semiconductors
Data Sheet: Technical Data

Document Number MC56F827XXDS
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MC56F827XXDS

MC56F827xx

Supports MC56F82748VLH, MC56F82746VLF, MC56F82746MLF, MC56F82743VLC, MC56F82743VFM, MC56F82738VLH, MC56F82736VLF, MC56F82733VLC, MC56F82733VFM, MC56F82733MFM, MC56F82728VLH, MC56F82726VLF, MC56F82723VLC, MC56F82723VFM

Features

- This family of digital signal controllers (DSCs) is based on the 32-bit 56800EX core. On a single chip, each device combines the processing power of a DSP and the functionality of an MCU, with a flexible set of peripherals to support many target applications:
  - Industrial control
  - Home appliances
  - Smart sensors
  - Wireless charging
  - Switched-mode power supply and power management
  - Power distribution systems
  - Motor control (ACIM, BLDC, PMSM, SR, stepper)
  - Photovoltaic systems
  - Circuit breaker
  - Medical device/equipment
  - Instrumentation
  - Uninterruptible power supplies (UPSs)
  - Lighting
- DSC based on 32-bit 56800EX core
  - Up to 100 MIPS at 100 MHz core frequency in fast mode
  - DSP and MCU functionality in a unified, C-efficient architecture
- On-chip memory
  - Up to 64 KB flash memory
  - Up to 8 KB data/program RAM
  - On-chip flash memory and RAM can be mapped into both program and data memory spaces
- Analog
  - Two high-speed, 8-channel, 12-bit ADCs with dynamic x1, x2, and x4 programmable amplifier
  - Four analog comparators with integrated 6-bit DAC references
  - Up to two 12-bit digital-to-analog converters (DAC)
- One eFlexPWM module with up to 8 PWM outputs, including 8 channels with high resolution NanoEdge placement
- Communication interfaces
  - Up to two high-speed queued SCI (QSCI) modules with LIN slave functionality
  - Up to two queued SPI (QSPI) modules
  - One I2C/SMBus port
  - One Modular/Scalable Controller Area Network (MSCAN) module
- Timers
  - One 16-bit quad timer (1 x 4 16-bit timer)
  - Two Periodic Interval Timers (PITs)
- Security and integrity
  - Cyclic Redundancy Check (CRC) generator
  - Windowed Computer operating properly (COP) watchdog
  - External Watchdog Monitor (EWM)
- Clocks
  - Two on-chip relaxation oscillators: 8 MHz (400 kHz at standby mode) and 200 kHz
  - Crystal / resonator oscillator

- System
  - DMA controller
  - Integrated power-on reset (POR) and low-voltage interrupt (LVI) and brown-out reset module
  - Inter-module crossbar connection
  - JTAG/enhanced on-chip emulation (EOnCE) for unobtrusive, real-time debugging
- Operating characteristics
  - Single supply: 3.0 V to 3.6 V
  - 5 V–tolerant I/O (except for RESETB pin which is a 3.3 V pin only)
  - Operation ambient temperature: V temperature option: -40°C to 105°C
  - Operation ambient temperature: M temperature option: -40°C to 125°C
- 64-pin LQFP, 48-pin LQFP, 32-pin QFN, and 32-pin LQFP packages

Table of Contents

1 Overview

1.1 MC56F827xx Product Family

The following table is the comparsion of features among members of the family.

Table 1. MC56F827xx Family

Feature	MC56F82											
Part Number[1]	748V LH	746V LF 746M LF	743V LC	743V FM	738V LH	736V LF	733V LC	733V FM 733M FM	728V LH	726V LF	723V LC	723V FM
Core frequency (MHz)	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50
Flash memory (KB)	64	64	64	64	48	48	48	48	32	32	32	32
RAM (KB)	8	8	8	8	8	8	8	8	6	6	6	6
Interrupt Controller	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Windowed Computer Operating Properly (WCOP)	1	1	1	1	1	1	1	1	1	1	1	1
External Watchdog Monitor (EWM)	1	1	1	1	1	1	1	1	1	1	1	1
Periodic Interrupt Timer (PIT)	2	2	2	2	2	2	2	2	2	2	2	2
Cyclic Redundancy Check (CRC)	1	1	1	1	1	1	1	1	1	1	1	1
Quad Timer (TMR)	1x4	1x4	1x4	1x4	1x4	1x4	1x4	1x4	1x4	1x4	1x4	1x4
12-bit Cyclic ADC channels	2x8	2x5	2x3	2x3	2x8	2x5	2x3	2x3	2x8	2x5	2x3	2x3
PWM Module:												
Input capture channels[2]	12	6	6	6	12	6	6	6	12	6	6	6
High-resolution channels	8	6	6	6	8	6	6	6	8	6	6	6
Standard channels	4	0	0	0	4	0	0	0	4	0	0	0
12-bit DAC	2	2	2	2	2	2	2	2	2	2	2	2
DMA	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Table continues on the next page...

Table 1. MC56F827xx Family (continued)

Feature	MC56F82											
Part Number[1]	748V LH	746V LF 746M LF	743V LC	743V FM	738V LH	736V LF	733V LC	733V FM 733M FM	728V LH	726V LF	723V LC	723V FM
Analog Comparators (CMP)	4	4	3	3	4	4	3	3	4	4	3	3
QSCI	2	2	1	1	2	2	1	1	2	2	1	1
QSPI	2	1	1	1	2	1	1	1	2	1	1	1
I2C/SMBus	1	1	1	1	1	1	1	1	1	1	1	1
MSCAN	1	1	0	0	1	1	0	0	1	1	0	0
GPIO	54	39	26	26	54	39	26	26	54	39	26	26
Package pin count	64 LQFP	48 LQFP	32 LQFP	32 QFN	64 LQFP	48 LQFP	32 LQFP	32 QFN	64 LQFP	48 LQFP	32 LQFP	32 QFN
AEC-Q100[3]	Yes	Yes	No	No	Yes	Yes	No	No	Yes	Yes	No	No

1. Temperature options
   V: -40°C to 105°C
   M: -40°C to 125°C
2. Input capture shares the pin with cooresponding PWM channels.
3. Qualification aligned to AEC-Q100

1.2 56800EX 32-bit Digital Signal Controller (DSC) core

- Efficient 32-bit 56800EX Digital Signal Processor (DSP) engine with modified dual Harvard architecture:
  - Three internal address buses
  - Four internal data buses: two 32-bit primary buses, one 16-bit secondary data bus, and one 16-bit instruction bus
  - 32-bit data accesses
  - Supports concurrent instruction fetches in the same cycle, and dual data accesses in the same cycle
  - 20 addressing modes
- As many as 100 million instructions per second (MIPS) at 100 MHz core frequency
- 162 basic instructions
- Instruction set supports both fractional arithmetic and integer arithmetic
- 32-bit internal primary data buses support 8-bit, 16-bit, and 32-bit data movement, plus addition, subtraction, and logical operations
- Single-cycle 16 × 16-bit -> 32-bit and 32 x 32-bit -> 64-bit multiplier-accumulator (MAC) with dual parallel moves
- 32-bit arithmetic and logic multi-bit shifter
- Four 36-bit accumulators, including extension bits

- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Bit reverse address mode, which effectively supports DSP and Fast Fourier Transform algorithms
- Full shadowing of the register stack for zero-overhead context saves and restores: nine shadow registers correspond to nine address registers (R0, R1, R2, R3, R4, R5, N, N3, M01)
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions enable compact code
- Enhanced bit manipulation instruction set
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack, with the stack's depth limited only by memory
- Priority level setting for interrupt levels
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging that is independent of processor speed

1.3 Operation Parameters

- Up to 50 MHz operation in normal mode and 100 MHz operation in fast mode
- Operation ambient temperature:
  V Temperature option:-40 ºC to 105ºC
  M Temperature option:-40 ºC to 125ºC
- Single 3.3 V power supply
- Supply range: V_{DD} - V_{SS} = 2.7 V to 3.6 V, V_{DDA} - V_{SSA} = 2.7 V to 3.6 V

1.4 On-Chip Memory and Memory Protection

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Internal flash memory with security and protection to prevent unauthorized access
- Memory resource protection (MRP) unit to protect supervisor programs and resources from user programs
- Programming code can reside in flash memory during flash programming
- The dual-port RAM controller supports concurrent instruction fetches and data accesses, or dual data accesses by the core.
  - Concurrent accesses provide increased performance.
  - The data and instruction arrive at the core in the same cycle, reducing latency.
- On-chip memory

- Up to 64 KB program/data flash memory
- Up to 8 KB dual port data/program RAM

1.5 Interrupt Controller

- Five interrupt priority levels
  - Three user-programmable priority levels for each interrupt source: level 0, level 1, level 2
  - Unmaskable level 3 interrupts include illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction
  - Interrupt level 3 is highest priority and non-maskable. Its sources include:
    - Illegal instructions
    - Hardware stack overflow
    - SWI instruction
    - EOnce interrupts
    - Misaligned data accesses
  - Lowest-priority software interrupt: level LP
- Support for nested interrupts, so that a higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Masking of interrupt priority level is managed by the 56800EX core
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to System Integration Module (SIM) to restart clock when in wait and stop states
- Ability to relocate interrupt vector table

1.6 Peripheral highlights

1.6.1 Enhanced Flex Pulse Width Modulator (eFlexPWM)

- 16 bits of resolution for center, edge-aligned, and asymmetrical PWMs
- PWM outputs can be configured as complementary output pairs or independent outputs
- Dedicated time-base counter with period and frequency control per submodule
- Independent top and bottom deadtime insertion for each complementary pair
- Independent control of both edges of each PWM output
- Enhanced input capture and output compare functionality on each input:
  - Channels not used for PWM generation can be used for buffered output compare functions.

    - Channels not used for PWM generation can be used for input capture functions.
    - Enhanced dual edge capture functionality
- Synchronization of submodule to external hardware (or other PWM) is supported.
- Double-buffered PWM registers
    - Integral reload rates from 1 to 16
    - Half-cycle reload capability
- Multiple output trigger events can be generated per PWM cycle via hardware.
- Support for double-switching PWM outputs
- Up to eight fault inputs can be assigned to control multiple PWM outputs
    - Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Individual software control of each PWM output
- All outputs can be programmed to change simultaneously via a FORCE_OUT event.
- PWMX pin can optionally output a third PWM signal from each submodule
- Option to supply the source for each complementary PWM signal pair from any of the following:
    - Crossbar module outputs
    - External ADC input, taking into account values set in ADC high and low limit registers

1.6.2 12-bit Analog-to-Digital Converter (Cyclic type)

- Two independent 12-bit analog-to-digital converters (ADCs):
    - 2 x 8-channel external inputs
    - Built-in x1, x2, x4 programmable gain pre-amplifier
    - Maximum ADC clock frequency up to 10 MHz, having period as low as 100-ns
    - Single conversion time of 10 ADC clock cycles
    - Additional conversion time of 8 ADC clock cycles
- Support of analog inputs for single-ended and differential, including unipolar differential, conversions
- Sequential, parallel, and independent scan mode
- First 8 samples have offset, limit and zero-crossing calculation supported
- ADC conversions can be synchronized by *any* module connected to the internal crossbar module, such as PWM, timer, GPIO, and comparator modules.
- Support for simultaneous triggering and software-triggering conversions
- Support for a multi-triggering mode with a programmable number of conversions on each trigger
- Each ADC has ability to scan and store up to 8 conversion results.
- Current injection protection

1.6.3 Periodic Interrupt Timer (PIT) Modules

- 16-bit counter with programmable count modulo
- PIT0 is master and PIT1 is slave (if synchronizing both PITs)
- The output signals of both PIT0 and PIT1 are internally connected to a peripheral crossbar module
- Can run when the CPU is in Wait/Stop modes. Can also wake up the CPU from Wait/Stop modes.
- In addition to its existing bus clock (up to 50 MHz), 3 alternate clock sources for the counter clock are available:
  - Crystal oscillator output
  - 8 MHz / 400 kHz ROSC (relaxation oscillator output)
  - On-chip low-power 200 kHz oscillator

1.6.4 Inter-Module Crossbar and AND-OR-INVERT logic

- Provides generalized connections between and among on-chip peripherals: ADCs, 12-bit DAC, comparators, quad-timers, eFlexPWMs, EWM, and select I/O pins
- User-defined input/output pins for all modules connected to the crossbar
- DMA request and interrupt generation from the crossbar
- Write-once protection for all registers
- AND-OR-INVERT function provides a universal Boolean function generator that uses a four-term sum-of-products expression, with each product term containing true or complement values of the four selected inputs (A, B, C, D).

1.6.5 Comparator

- Full rail-to-rail comparison range
- Support for high and low speed modes
- Selectable input source includes external pins and internal DACs
- Programmable output polarity
- 6-bit programmable DAC as a voltage reference per comparator
- Three programmable hysteresis levels
- Selectable interrupt on rising-edge, falling-edge, or toggle of a comparator output

1.6.6 12-bit Digital-to-Analog Converter

- 12-bit resolution
- Powerdown mode

- Automatic mode allows the DAC to automatically generate pre-programmed output waveforms, including square, triangle, and sawtooth waveforms (for applications like slope compensation)
- Programmable period, update rate, and range
- Output can be routed to an internal comparator, ADC, or optionally to an off-chip destination

1.6.7 Quad Timer

- Four 16-bit up/down counters, with a programmable prescaler for each counter
- Operation modes: edge count, gated count, signed count, capture, compare, PWM, signal shot, single pulse, pulse string, cascaded, quadrature decode
- Programmable input filter
- Counting start can be synchronized across counters
- Up to 100 MHz operation clock

1.6.8 Queued Serial Communications Interface (QSCI) modules

- Operating clock can be up to two times the CPU operating frequency
- Four-word-deep FIFOs available on both transmit and receive buffers
- Standard mark/space non-return-to-zero (NRZ) format
- 16-bit integer and 3-bit fractional baud rate selection
- Full-duplex or single-wire operation
- Programmable 8-bit or 9-bit data format
- Error detection capability
- Two receiver wakeup methods:
  - Idle line
  - Address mark
- 1/16 bit-time noise detection
- Up to 6.25 Mbit/s baud rate at 100 MHz operation clock

1.6.9 Queued Serial Peripheral Interface (QSPI) modules

- Maximum 12.5 Mbit/s baud rate
- Selectable baud rate clock sources for low baud rate communication
- Baud rate as low as Baudrate_Freq_in / 8192
- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four-word-deep FIFOs available on transmit and receive buffers

- Programmable length transmissions (2 bits to 16 bits)
- Programmable transmit and receive shift order (MSB as first bit transmitted)

1.6.10 Inter-Integrated Circuit (I2C)/System Management Bus (SMBus) modules

- Compatible with I2C bus standard
- Support for System Management Bus (SMBus) specification, version 2
- Multi-master operation
- General call recognition
- 10-bit address extension
- Start/Repeat and Stop indication flags
- Support for dual slave addresses or configuration of a range of slave addresses
- Programmable glitch input filter with option to clock up to 100 MHz

1.6.11 Modular/Scalable Controller Area Network (MSCAN) Module

- Clock source from PLL or oscillator.
- Implementation of the CAN protocol Version 2.0 A/B
- Standard and extended data frames
- 0-to-8 bytes data length
- Programmable bit rate up to 1 Mbit/s
- Support for remote frames
- Individual Rx Mask Registers per Message Buffer
- Internal timer for time-stamping of received and transmitted messages
- Listen-only mode capability
- Programmable loopback mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Low power modes, with programmable wakeup on bus activity

1.6.12 Windowed Computer Operating Properly (COP) watchdog

- Programmable windowed timeout period
- Support for operation in all power modes: run mode, wait mode, stop mode
- Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
- Selectable reference clock source in support of EN60730 and IEC61508
- Selectable clock sources:
    - External crystal oscillator/external clock source

  - On-chip low-power 200 kHz oscillator
  - System bus (IPBus up to 50 MHz)
  - 8 MHz / 400 kHz ROSC
- Support for interrupt triggered when the counter reaches the timeout value

1.6.13 External Watchdog Monitor (EWM)

- Monitors external circuit as well as the software flow
- Programmable timeout period
- Interrupt capability prior to timeout
- Independent output (EWM_OUT_b) that places external circuit (but not CPU and peripheral) in a safe mode when EWM timeout occurs
- Selectable reference clock source in support of EN60730 and IEC61508
- Wait mode and Stop mode operation is not supported.
- Selectable clock sources:
  - External crystal oscillator/external clock source
  - On-chip low-power 200 kHz oscillator
  - System bus (IPBus up to 50 MHz)
  - 8 MHz / 400 kHz ROSC

1.6.14 Power supervisor

- Power-on reset (POR) to reset CPU, peripherals, and JTAG/EOnCE controllers (V_{DD} > 2.1 V)
- Brownout reset (V_{DD} < 1.9 V)
- Critical warn low-voltage interrupt (LVI2.0)
- Peripheral low-voltage interrupt (LVI2.7)

1.6.15 Phase-locked loop

- Wide programmable output frequency: 200 MHz to 400 MHz
- Input reference clock frequency: 8 MHz to 16 MHz
- Detection of loss of lock and loss of reference clock
- Ability to power down

1.6.16 Clock sources

1.6.16.1 On-chip oscillators

- Tunable 8 MHz relaxation oscillator with 400 kHz at standby mode (divide-by-two output)
- 200 kHz low frequency clock as secondary clock source for COP, EWM, PIT

1.6.16.2 Crystal oscillator

- Support for both high ESR crystal oscillator (ESR greater than 100 Ω) and ceramic resonator
- Operating frequency: 4–16 MHz

1.6.17 Cyclic Redundancy Check (CRC) Generator

- Hardware CRC generator circuit with 16-bit shift register
- High-speed hardware CRC calculation
- Programmable initial seed value
- CRC16-CCITT compliancy with $x^{16} + x^{12} + x^5 + 1$ polynomial
- Error detection for all single, double, odd, and most multibit errors
- Option to transpose input data or output data (CRC result) bitwise, which is required for certain CRC standards

1.6.18 General Purpose I/O (GPIO)

- 5 V tolerance (except RESETB pin)
- Individual control of peripheral mode or GPIO mode for each pin
- Programmable push-pull or open drain output
- Configurable pullup or pulldown on all input pins
- All pins (except JTAG and RESETB) default to be GPIO inputs
- 2 mA / 9 mA source/sink capability
- Controllable output slew rate

1.7 Block diagrams

The 56800EX core is based on a modified dual Harvard-style architecture, consisting of three execution units operating in parallel, and allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set

enable straightforward generation of efficient and compact code for the DSP and control functions. The instruction set is also efficient for C compilers, to enable rapid development of optimized control applications.

The device's basic architecture appears in Figure 1 and Figure 2. Figure 1 shows how the 56800EX system buses communicate with internal memories, and the IPBus interface and the internal connections among the units of the 56800EX core. Figure 2 shows the peripherals and control blocks connected to the IPBus bridge. See the specific device's Reference Manual for details.

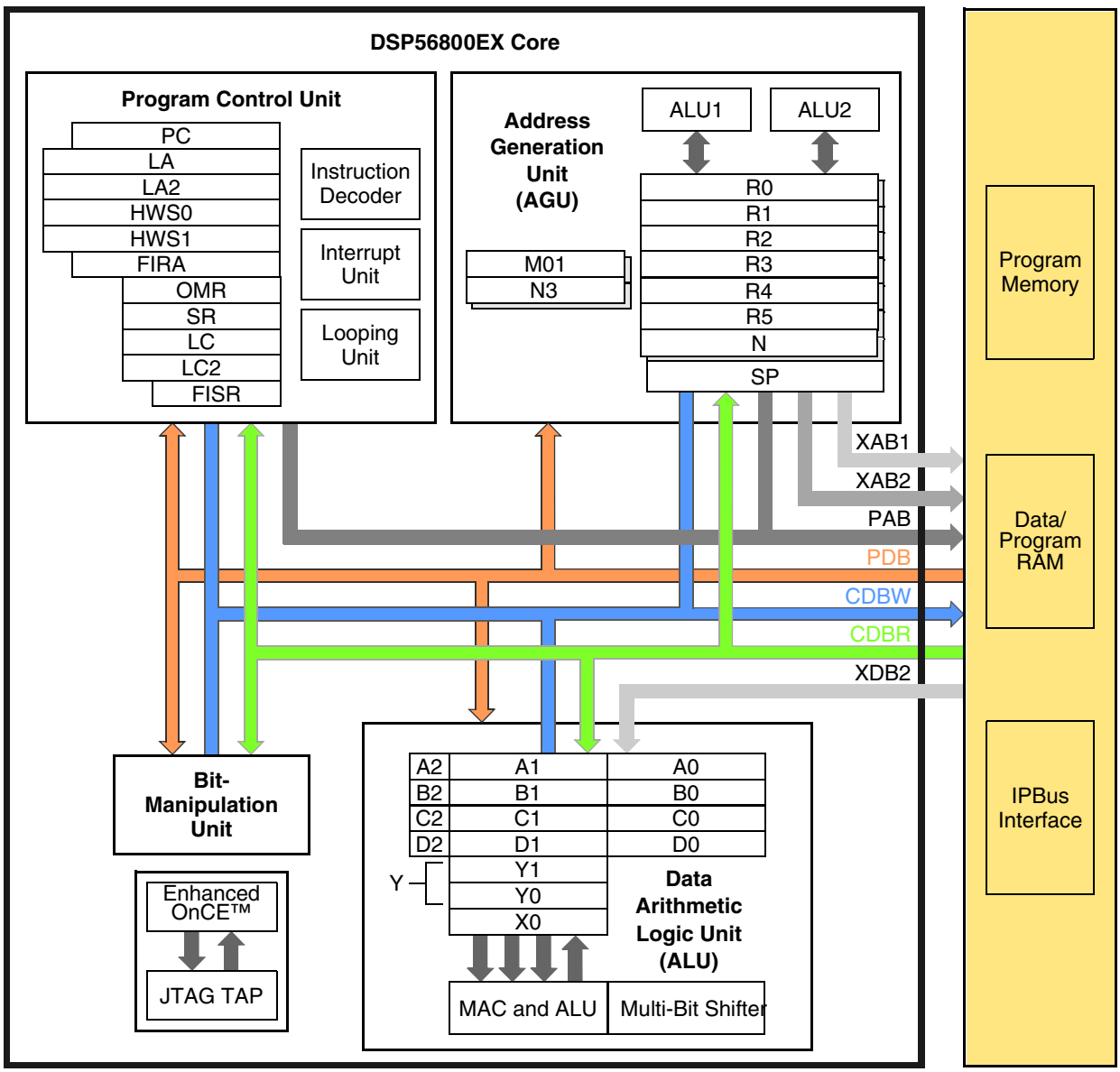

Figure 1. 56800EX basic block diagram

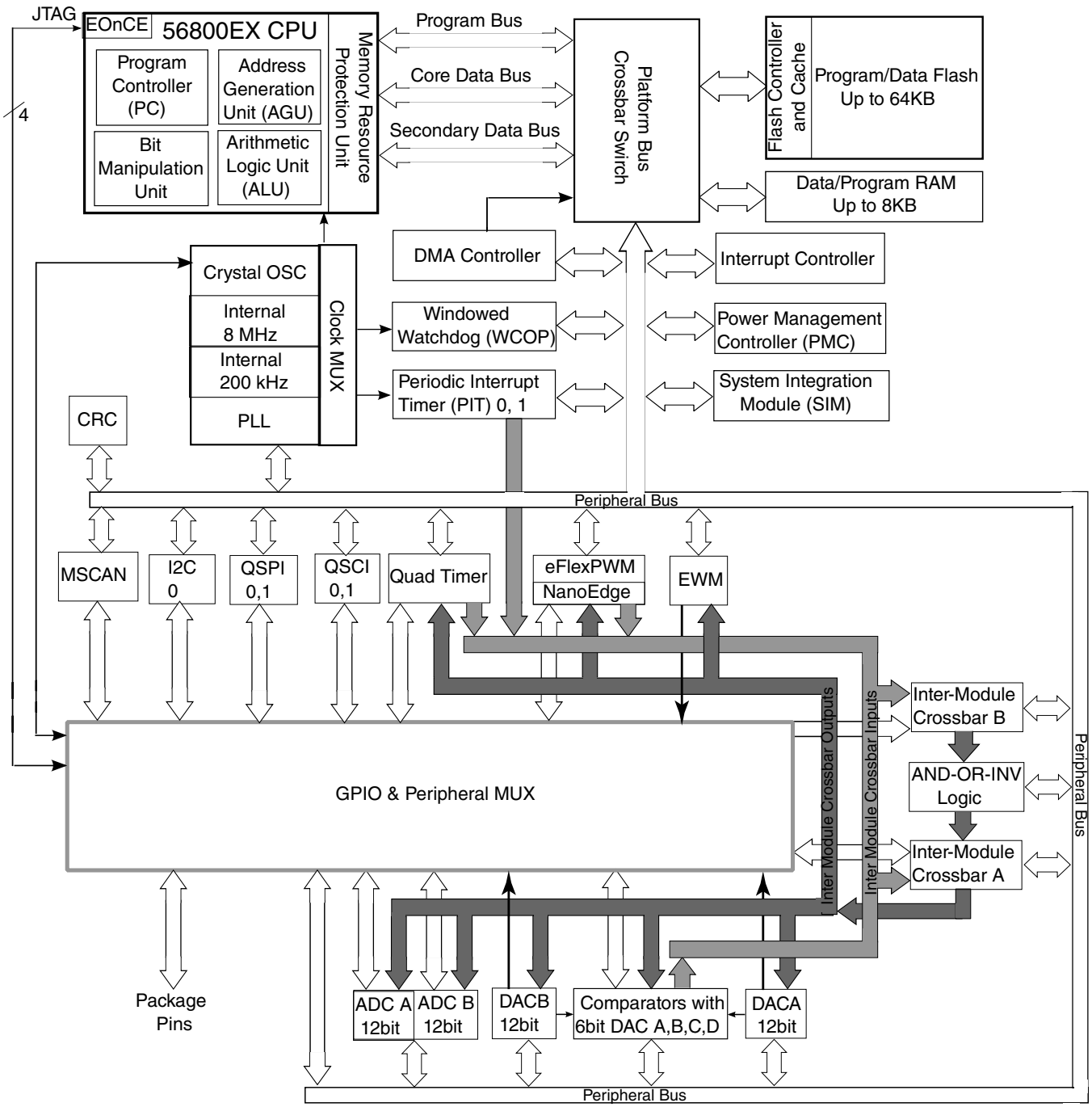

Figure 2. System diagram

2 MC56F827xx signal and pin descriptions

After reset, each pin is configured for its primary function (listed first). Any alternative functionality, shown in parentheses, must be programmed through the GPIO module peripheral enable registers (GPIOx_PER) and the SIM module GPIO peripheral select (GPSx) registers. All GPIO ports can be individually programmed as an input or output (using bit manipulation).

- PWMA_FAULT0, PWMA_FAULT1, and similar signals are inputs used to disable selected PWMA outputs, in cases where the fault conditions originate off-chip.

For the MC56F827xx products, which use 64-pin LQFP, 48-pin LQFP and 32-pin packages:

Table 2. Signal descriptions

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
V_{DD}	29	—	—	Supply	Supply	I/O Power — Supplies 3.3 V power to the chip I/O interface.
	44	32	—			
	60	44	28			
V_{SS}	30	22	14	Supply	Supply	I/O Ground — Provide ground for the device I/O interface.
	43	31	—			
	61	45	29			
V_{DDA}	22	15	9	Supply	Supply	Analog Power — Supplies 3.3 V power to the analog modules. It must be connected to a clean analog power supply.
V_{SSA}	23	16	10	Supply	Supply	Analog Ground — Supplies an analog ground to the analog modules. It must be connected to a clean power supply.
V_{CAP}	26	19	—	On-chip regulator output	On-chip regulator output	Connect a 2.2 µF or greater bypass capacitor between this pin and V_{SS} to stabilize the core voltage regulator output required for proper device operation.
	57	43	27			
TDI	64	48	32	Input	Input, internal pullup enabled	Test Data Input — It is sampled on the rising edge of TCK and has an internal pullup resistor. After reset, the default state is TDI.
(GPIOD0)				Input/Output		GPIO Port D0
TDO	62	46	30	Output	Output	Test Data Output — It is driven in the shift-IR and shift-DR controller states, and it changes on the falling edge of TCK. After reset, the default state is TDO
(GPIOD1)				Input/Output	Output	GPIO Port D1

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
TCK	1	1	1	Input	Input, internal pullup enabled	Test Clock Input — The pin is connected internally to a pullup resistor. A Schmitt-trigger input is used for noise immunity. After reset, the default state is TCK
(GPIOD2)				Input/Output		GPIO Port D2
TMS	63	47	31	Input	Input, internal pullup enabled	Test Mode Select Input — It is sampled on the rising edge of TCK and has an internal pullup resistor. After reset, the default state is TMS. **NOTE:** Always tie the TMS pin to V_{DD} through a 2.2 kΩ resistor if need to keep on-board debug capability. Otherwise, directly tie to V_{DD}.
(GPIOD3)				Input/Output		GPIO Port D3
$\overline{\text{RESET}}$ or RESETB	2	2	2	Input	Input, internal pullup enabled	Reset — A direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the reset state. A Schmitt-trigger input is used for noise immunity. The internal reset signal is deasserted synchronous with the internal clocks after a fixed number of internal clocks. After reset, the default state is $\overline{\text{RESET}}$. Recommended a capacitor of up to 0.1 µF for filtering noise.
(GPIOD4)				Input/ Opendrain Output		GPIO Port D4 $\overline{\text{RESET}}$ functionality is disabled in this mode and the device can be reset only through POR, COP reset, or software reset.
GPIOA0	13	9	6	Input/Output	Input, internal pullup enabled	GPIO Port A0
(ANA0&CMPA_IN3)				Input		ANA0 is analog input to channel 0 of ADCA; CMPA_IN3 is positive input 3 of analog comparator A. After reset, the default state is GPIOA0.
(CMPC_O)				Output		Analog comparator C output
GPIOA1	14	10	7	Input/Output	Input, internal pullup enabled	GPIO Port A1: After reset, the default state is GPIOA1.
(ANA1&CMPA_IN0)				Input		ANA1 is analog input to channel 1 of ADCA; CMPA_IN0 is negative input 0 of analog comparator A. When used as an analog input, the signal goes to ANA1 and CMPA_IN0. The ADC control register configures this input as ANA1 or CMPA_IN0.
GPIOA2	15	11	8	Input/Output	Input, internal pullup enabled	GPIO Port A2: After reset, the default state is GPIOA2.
(ANA2&VREFHA &CMPA_IN1)				Input		ANA2 is analog input to channel 2 of ADCA; VREFHA is analog reference

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
						high of ADCA; CMPA_IN1 is negative input 1 of analog comparator A. When used as an analog input, the signal goes to both ANA2, VREFHA, and CMPA_IN1.
GPIOA3	16	12	—	Input/Output	Input, internal pullup enabled	GPIO Port A3: After reset, the default state is GPIOA3.
(ANA3&VREFLA&CMPA_IN2)				Input		ANA3 is analog input to channel 3 of ADCA; VREFLA is analog reference low of ADCA; CMPA_IN2 is negative input 2 of analog comparator A.
GPIOA4	12	8	—	Input/Output	Input, internal pullup enabled	GPIO Port A4: After reset, the default state is GPIOA4.
(ANA4&CMPD_IN0)				Input		ANA4 is Analog input to channel 4 of ADCA; CMPD_IN0 is input 0 to comparator D.
GPIOA5	11	—	—	Input/Output	Input, internal pullup enabled	GPIO Port A5: After reset, the default state is GPIOA5.
(ANA5&CMPD_IN1)				Input		ANA5 is analog input to channel 5 of ADCA; ANC9 is analog input to channel 9 of ADCC; CMPD_IN1 is negative input 1 of analog comparator D.
GPIOA6	10	—	—	Input/Output	Input, internal pullup enabled	GPIO Port A6: After reset, the default state is GPIOA6.
(ANA6&CMPD_IN2)				Input		ANA6 is analog input to channel 5 of ADCA; CMPD_IN2 is negative input 2 of analog comparator D.
GPIOA7	9	—	—	Input/Output	Input, internal pullup enabled	GPIO Port A7: After reset, the default state is GPIOA7.
(ANA7&CMPD_IN3)				Input		ANA7 is analog input to channel 7 of ADCA; CMPD_IN3 is negative input 3 of analog comparator D.
GPIOB0	24	17	11	Input/Output	Input, internal pullup enabled	GPIO Port B0: After reset, the default state is GPIOB0.
(ANB0&CMPB_IN3)				Input		ANB0 is analog input to channel 0 of ADCB; CMPB_IN3 is positive input 3 of analog comparator B. When used as an analog input, the signal goes to ANB0 and CMPB_IN3. The ADC control register configures this input as ANB0.
GPIOB1	25	18	12	Input/Output	Input, internal pullup enabled	GPIO Port B1: After reset, the default state is GPIOB1.
(ANB1&CMPB_IN0)				Input		ANB1 is analog input to channel 1 of ADCB; CMPB_IN0 is negative input 0 of analog comparator B. When used as an analog input, the signal goes to ANB1 and CMPB_IN0. The ADC control register configures this input as ANB1.

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Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
DACB_O				Analog Output		12-bit digital-to-analog output
GPIOB2	27	20	13	Input/Output	Input, internal pullup enabled	GPIO Port B2: After reset, the default state is GPIOB2.
(ANB2&VERFHB &CMPC_IN3)				Input		ANB2 is analog input to channel 2 of ADCB; VREFHB is analog reference high of ADCB; CMPC_IN3 is positive input 3 of analog comparator C. When used as an analog input, the signal goes to both ANB2 and CMPC_IN3.
GPIOB3	28	21	—	Input/Output	Input, internal pullup enabled	GPIO Port B3: After reset, the default state is GPIOB3.
(ANB3&VREFLB& CMPC_IN0)				Input		ANB3 is analog input to channel 3 of ADCB; VREFLB is analog reference low of ADCB; CMPC_IN0 is negative input 0 of analog comparator C.
GPIOB4	21	14	—	Input/Output	Input, internal pullup enabled	GPIO Port B4: After reset, the default state is GPIOB4.
(ANB4&CMPC_IN 1)				Input		ANB4 is analog input to channel 4 of ADCB; CMPC_IN1 is negative input 1 of analog comparator C.
GPIOB5	20	—	—	Input/Output	Input, internal pullup enabled	GPIO Port B5: After reset, the default state is GPIOB5.
(ANB5&CMPC_IN 2)				Input		ANB5 is analog input to channel 5 of ADCB; CMPC_IN2 is negative input 2 of analog comparator C.
GPIOB6	19	—	—	Input/Output	Input, internal pullup enabled	GPIO Port B6: After reset, the default state is GPIOB6.
(ANB6&CMPB_IN 1)				Input		ANB6 is analog input to channel 6 of ADCB; CMPB_IN1 is negative input 1 of analog comparator B.
GPIOB7	17	—	—	Input/Output	Input, internal pullup enabled	GPIO Port B7: After reset, the default state is GPIOB7.
(ANB7&CMPB_IN 2)				Input		ANB7 is analog input to channel 7 of ADCB; CMPB_IN2 is negative input 2 of analog comparator B.
GPIOC0	3	3	—	Input/Output	Input, internal pullup enabled	GPIO Port C0: After reset, the default state is GPIOC0.
(EXTAL)				Analog Input		The external crystal oscillator input (EXTAL) connects the internal crystal oscillator input to an external crystal or ceramic resonator.
(CLKIN0)				Input		External clock input 0[1]
GPIOC1	4	4	—	Input/Output	Input, internal pullup enabled	GPIO Port C1: After reset, the default state is GPIOC1.
(XTAL)				Input		The external crystal oscillator output (XTAL) connects the internal crystal

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Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
						oscillator output to an external crystal or ceramic resonator.
GPIOC2	5	5	3	Input/Output	Input, internal pullup enabled	GPIO Port C2: After reset, the default state is GPIOC2.
(TXD0)				Output		SCI0 transmit data output or transmit/ receive in single wire operation
(XB_OUT11)				Output		Crossbar module output 11
(XB_IN2)				Input		Crossbar module input 2
(CLKO0)				Output		Buffered clock output 0: the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.
GPIOC3	7	6	4	Input/Output	Input, internal pullup enabled	GPIO Port C3: After reset, the default state is GPIOC3.
(TA0)				Input/Output		Quad timer module A channel 0 input/ output
(CMPA_O)				Output		Analog comparator A output
(RXD0)				Input		SCI0 receive data input
(CLKIN1)				Input		External clock input 1
GPIOC4	8	7	5	Input/Output	Input, internal pullup enabled	GPIO Port C4: After reset, the default state is GPIOC4.
(TA1)				Input/Output		Quad timer module A channel 1 input/ output
(CMPB_O)				Output		Analog comparator B output
(XB_IN6)				Input		Crossbar module input 6
(EWM_OUT_B)				Output		External Watchdog Module output
GPIOC5	18	13	—	Input/Output	Input, internal pullup enabled	GPIO Port C5: After reset, the default state is GPIOC5.
(DACA_O)				Analog Output		12-bit digital-to-analog output
(XB_IN7)				Input		Crossbar module input 7
GPIOC6	31	23	15	Input/Output	Input, internal pullup enabled	GPIO Port C6: After reset, the default state is GPIOC6.
(TA2)				Input/Output		Quad timer module A channel 2 input/ output
(XB_IN3)				Input		Crossbar module input 3
(CMP_REF)				Analog Input		Positive input 3 of analog comparator A and B and C.
($\overline{\text{SS0\_B}}$)				Input/Output		In slave mode, $\overline{\text{SS0\_B}}$ indicates to the SPI module 0 that the current transfer is to be received.
GPIOC7	32	24	—	Input/Output	Input, internal pullup enable	GPIO Port C7: After reset, the default state is GPIOC7.

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Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
($\overline{SS0\_B}$)				Input/Output		In slave mode, $\overline{SS0\_B}$ indicates to the SPI module 0 that the current transfer is to be received.
(TXD0)				Output		SCI0 transmit data output or transmit/ receive in single wire operation
(XB_IN8)				Input		Crossbar module input 8
GPIOC8	33	25	16	Input/Output	Input, internal pullup enabled	GPIO Port C8: After reset, the default state is GPIOC8.
(MISO0)				Input/Output		Master in/slave out for SPI0 — In master mode, MISO0 pin is the data input. In slave mode, MISO0 pin is the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
(RXD0)				Input		SCI0 receive data input
(XB_IN9)				Input		Crossbar module input 9
(XB_OUT6)				Output		Crossbar module output 6
GPIOC9	34	26	17	Input/Output	Input, internal pullup enabled	GPIO Port C9: After reset, the default state is GPIOC9.
(SCLK0)				Input/Output		SPI0 serial clock. In master mode, SCLK0 pin is an output, clocking slaved listeners. In slave mode, SCLK0 pin is the data clock input.
(XB_IN4)				Input		Crossbar module input 4
(TXD0)				Output		SCI0 transmit data output or transmit/ receive in single wire operation
(XB_OUT8)				Output		Crossbar module output 8
GPIOC10	35	27	18	Input/Output	Input, internal pullup enabled	GPIO Port C10: After reset, the default state is GPIOC10.
(MOSI0)				Input/Output		Master out/slave in for SPI0 — In master mode, MOSI0 pin is the data output. In slave mode, MOSI0 pin is the data input.
(XB_IN5)				Input		Crossbar module input 4
(MISO0)				Input/Output		Master in/slave out for SPI0 — In master mode, MISO0 pin is the data input. In slave mode, MISO0 pin is the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
(XB_OUT9)				Output		Crossbar module output 9
GPIOC11	37	29	—	Input/Output	Input, internal pullup enabled	GPIO Port C11: After reset, the default state is GPIOC11.
(CANTX)				Open-drain Output		CAN transmit data output
(SCL0)				Input/Open-drain Output		I^2C0 serial clock

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Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
(TXD1)				Output		SCI1 transmit data output or transmit/ receive in single wire operation
GPIOC12	38	30	—	Input/Output	Input, internal pullup enabled	GPIO Port C12: After reset, the default state is GPIOC12.
(CANRX)				Input		CAN receive data input
(SDA0)				Input/Open-drain Output		I^2C0 serial data line
(RXD1)				Input		SCI1 receive data input
GPIOC13	49	37	—	Input/Output	Input, internal pullup enabled	GPIO Port C13: After reset, the default state is GPIOC13.
(TA3)				Input/Output		Quad timer module A channel 3 input/ output
(XB_IN6)				Input		Crossbar module input 6
(EWM_OUT_B)				Output		External Watchdog Module output
GPIOC14	55	41	—	Input/Output	Input, internal pullup enabled	GPIO Port C14: After reset, the default state is GPIOC14.
(SDA0)				Input/ Opendrain Output		I^2C0 serial data line
(XB_OUT4)				Output		Crossbar module output 4
(PWM_FAULT4)				Input		Disable PWMA output 4
GPIOC15	56	42	—	Input/Output	Input, internal pullup enabled	GPIO Port C15: After reset, the default state is GPIOC15.
(SCL0)				Input/Open-drain Output		I^2C0 serial clock
(XB_OUT5)				Output		Crossbar module output 5
(PWM_FAULT5)				Input		Disable PWMA output 5
GPIOE0	45	33	21	Input/Output	Input, internal pullup enabled	GPIO Port E0: After reset, the default state is GPIOE0.
(PWM_0B)				Input/Output		PWM module A (NanoEdge), submodule 0, output B or input capture B
GPIOE1	46	34	22	Input/Output	Input, internal pullup enabled	GPIO Port E1: After reset, the default state is GPIOE1.
(PWM_0A)				Input/Output		PWM module A (NanoEdge), submodule 0, output A or input capture A
GPIOE2	47	35	23	Input/Output	Input, internal pullup enabled	GPIO Port E2: After reset, the default state is GPIOE2.
(PWMA_1B)				Input/Output		PWM module A (NanoEdge), submodule 1, output B or input capture B
GPIOE3	48	36	24	Input/Output	Input, internal pullup enabled	GPIO Port E3: After reset, the default state is GPIOE3.
(PWMA_1A)				Input/Output		PWM module A (NanoEdge), submodule 1, output A or input capture A

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Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
GPIOE4	51	39	25	Input/Output	Input, internal pullup enabled	GPIO Port E4: After reset, the default state is GPIOE4.
(PWMA_2B)				Input/Output		PWM module A (NanoEdge), submodule 2, output B or input capture B
(XB_IN2)				Input		Crossbar module input 2
GPIOE5	52	40	26	Input/Output	Input, internal pullup enabled	GPIO Port E5: After reset, the default state is GPIOE5.
(PWMA_2A)				Input/Output		PWM module A (NanoEdge), submodule 2, output A or input capture A
(XB_IN3)				Input		Crossbar module input 3
GPIOE6	53	—	—	Input/Output	Input, internal pullup enabled	GPIO Port E6: After reset, the default state is GPIOE6.
(PWMA_3B)				Input/Output		PWM module A (NanoEdge), submodule 3, output B or input capture B
(XB_IN4)				Input		Crossbar module input 4
GPIOE7	54	—	—	Input/Output	Input, internal pullup enabled	GPIO Port E7: After reset, the default state is GPIOE7.
(PWMA_3A)				Input/Output		PWM module A (NanoEdge), submodule 3, output A or input capture A
(XB_IN5)				Input		Crossbar module input 5
GPIOF0	36	28	—	Input/Output	Input, internal pullup enabled	GPIO Port F0: After reset, the default state is GPIOF0.
(XB_IN6)				Input		Crossbar module input 6
(SCLK1)				Input/Output		SPI1 serial clock — In master mode, SCLK1 pin is an output, clocking slaved listeners. In slave mode, SCLK1 pin is the data clock input 0.
GPIOF1	50	38	—	Input/Output	Input, internal pullup enabled	GPIO Port F1: After reset, the default state is GPIOF1.
(CLKO1)				Output		Buffered clock output 1: the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.
(XB_IN7)				Input		Crossbar module input 7
(CMPD_O)				Output		Analog comparator D output
GPIOF2	39	—	19	Input/Output	Input, internal pullup enabled	GPIO Port F2: After reset, the default state is GPIOF2.
(SCL0)				Input/Open-drain Output		I^2C0 serial clock
(XB_OUT6)				Output		Crossbar module output 6
(MISO1)				Input/Output		Master in/slave out for SPI1 —In master mode, MISO1 pin is the data input. In slave mode, MISO1 pin is the data output. The MISO line of a slave device

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
						is placed in the high-impedance state if the slave device is not selected.
GPIOF3	40	—	20	Input/Output	Input, internal pullup enabled	GPIO Port F3: After reset, the default state is GPIOF3.
(SDA0)				Input/Open-drain Output		I^2C0 serial data line
(XB_OUT7)				Output		Crossbar module output 7
(MOSI1)				Input/Output		Master out/slave in for SPI1— In master mode, MOSI1 pin is the data output. In slave mode, MOSI1 pin is the data input.
GPIOF4	41	—	—	Input/Output	Input, internal pullup enabled	GPIO Port F4: After reset, the default state is GPIOF4.
(TXD1)				Output		SCI1 transmit data output or transmit/ receive in single wire operation
(XB_OUT8)				Output		Crossbar module output 8
(PWMA_0X)				Input/Output		PWM module A (NanoEdge), submodule 0, output X or input capture X
(PWMA_FAULT6)				Input		Disable PWMA output 6
GPIOF5	42	—	—	Input/Output	Input, internal pullup enabled	GPIO Port F5: After reset, the default state is GPIOF5.
(RXD1)				Input		SCI1 receive data input
(XB_OUT9)				Output		Crossbar module output 9
(PWMA_1X)				Input/Output		PWM module A (NanoEdge), submodule 1, output X or input capture X
(PWMA_FAULT7)				Input		Disable PWMA output 7
GPIOF6	58	—	—	Input/Output	Input, internal pullup enabled	GPIO Port F6: After reset, the default state is GPIOF6.
(PWMA_3X)				Input/Output		PWM module A (NanoEdge), submodule 3, output X or input capture X
(XB_IN2)				Input		Crossbar module input 2
GPIOF7	59	—	—	Input/Output	Input, internal pullup enabled	GPIO Port F7: After reset, the default state is GPIOF7.
(CMPC_O)				Output		Analog comparator C output
(SS1_B)				Input/Output		In slave mode, SS1_B indicates to the SPI1 module that the current transfer is to be received.
(XB_IN3)				Input		Crossbar module input 3
GPIOF8	6	—	—	Input/Output	Input, internal pullup enabled	GPIO Port F8: After reset, the default state is GPIOF8.
(RXD0)				Input		SCI0 receive data input
(XB_OUT10)				Output		Crossbar module output 10
(CMPD_O)				Output		Analog comparator D output
(PWMA_2X)						PWM module A (NanoEdge), submodule 2, output X or input capture X

1. If CLKIN is selected as the device's external clock input, then both the GPS_C0 bit (in GPS1) and the EXT_SEL bit (in OCCS oscillator control register (OSCTL)) must be set. Also, the crystal oscillator should be powered down.

2.1 Signal groups

The input and output signals of the MC56F827xx are organized into functional groups, as detailed in Table 3.

Table 3. Functional Group Pin Allocations

Functional Group	Number of Pins			
	32QFN	32LQFP	48LQFP	64LQFP
Power Inputs (V_{DD}, V_{DDA}), Power output(V_{CAP})	3	3	5	6
Ground (V_{SS}, V_{SSA})	3	3	4	4
Reset	1	1	1	1
eFlexPWM with NanoEdge ports not including fault pins (for 56F827xx)	6	6	6	8
eFlexPWM without NanoEdge ports not including fault pins	0	0	0	4
Queued Serial Peripheral Interface (QSPI0 and QSPI1) ports	4	4	5	9
Queued Serial Communications Interface (QSCI0 and QSCI1) ports	4	4	7	10
Inter-Integrated Circuit Interface (I^2C0) ports	2	2	4	6
12-bit Analog-to-Digital Converter inputs	6	6	10	16
Analog Comparator inputs/outputs	7/3	7/3	11/4	17/5
12-bit Digital-to-Analog output	2	2	2	2
Quad Timer Module (TMRA and TMRB) ports	3	3	4	4
Controller Area Network (MSCAN)	0	0	2	2
Inter-Module Crossbar inputs/outputs	8/4	8/4	12/6	17/11
Clock inputs/outputs	1/1	1/1	2/2	2/2
JTAG / Enhanced On-Chip Emulation (EOnCE)	4	4	4	4

3 Ordering parts

3.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to **freescale.com** and perform a part number search for the following device numbers: MC56F82

4 Part identification