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56F8323/56F8123

Data Sheet

Preliminary Technical Data

56F8300
16-bit Digital Signal Controllers

MC56F8323
Rev. 17
04/2007

freescale.com

freescale™ semiconductor

Document Revision History

Version History	Description of Change
Rev 1.0	Pre-Release version, Alpha customers only
Rev 2.0	Initial Public Release
Rev 3.0	Corrected typo in **Table 10-4**, Flash Endurance is 10,000 cycles. Addressed additional grammar issues.
Rev 4.0	Added Package Pins to GPIO Table in Section 8. Removed reference to pin group 9 in **Table 10-5**. Replacing TBD Typical Min with values in **Table 10-17**. Editing grammar, spelling, consistency of language throughout family. Updated values in Regulator Parameters, **Table 10-9**, External Clock Operation Timing Requirements **Table 10-13**, SPI Timing, **Table 10-18**, ADC Parameters, **Table 10-24**, and IO Loading Coefficients at 10MHz, **Table 10-25**.
Rev 5.0	Updated values in Power-On Reset Low Voltage, **Table 10-6**.
Rev 6.0	Correcting package pin numbers in **Table 2-2**, **PhaseA0** changed from 38 to 52, **PhaseB0** changed from 37 to 51, **Index0** changed from 36 to 50, and **Home0** changed from 35 to 49. All pin changes in Table 2-2 were do to data entry errors - This package pin-out has not changed
Rev 7.0	Added **Part 4.8**, added addition text to **Part 6.9** on POR reset, added the word “access” to FM Error Interrupt in **Table 4-3**, removed min and max numbers; only documenting Typ. numbers for LVI in **Table 10-6**.
Rev 8.0	Updated numbers in **Table 10-7** and **Table 10-8** with more recent data. Corrected typo in **Table 10-3** in Pd characteristics.
Rev 9.0	Replace any reference to Flash Interface Unit with Flash Memory Module; changed example in **Part 2.2**; added note on V_{REFH} and V_{REFLO} in **Table 2-2** and **Table 11-1**; added note to Vcap pin in **Table 2-2**; corrected typo FIVAL1 and FIVAH1 in **Table 4-12**; removed unneccessary notes in **Table 10-12**; corrected temperature range in **Table 10-14**; added ADC calibration information to **Table 10-24** and new graphs in **Figure 10-21**.
Rev 10.0	Clarification to **Table 10-23**, corrected Digital Input Current Low (pull-up enabled) numbers in **Table 10-5**. Removed text and Table 10-2; replaced with note to **Table 10-1**.
Rev. 11.0	Added 56F8123 information; edited to indicate differences in 56F8323 and 56F8123.Reformatted for Freescale look and feel. Updated Temperature Sensor and ADC tables, then updated balance of electrical tables for consistency throughout the family. Clarified I/O power description in **Table 2-2**, added note to **Table 10-7** and clarified **Section 12.3** .
Rev 12.0	Added output voltage maximum value and note to clarify in **Table 10-1**; also removed overall life expectancy note, since life expectancy is dependent on customer usage and must be determined by reliability engineering. Clarified value and unit measure for Maximum allowed P_D in **Table 10-3**. Corrected note about average value for Flash Data Retention in **Table 10-4**. Added new RoHS-compliant orderable part numbers in **Table 13-1**.
Rev 13.0	Deleted formula for Max Ambient Operating Temperature (Automotive) and Max Ambient Operating Temperature (Industrial) in **Table 10-4**. Added RoHS-compliance and “pb-free” language to back cover.

Document Revision History

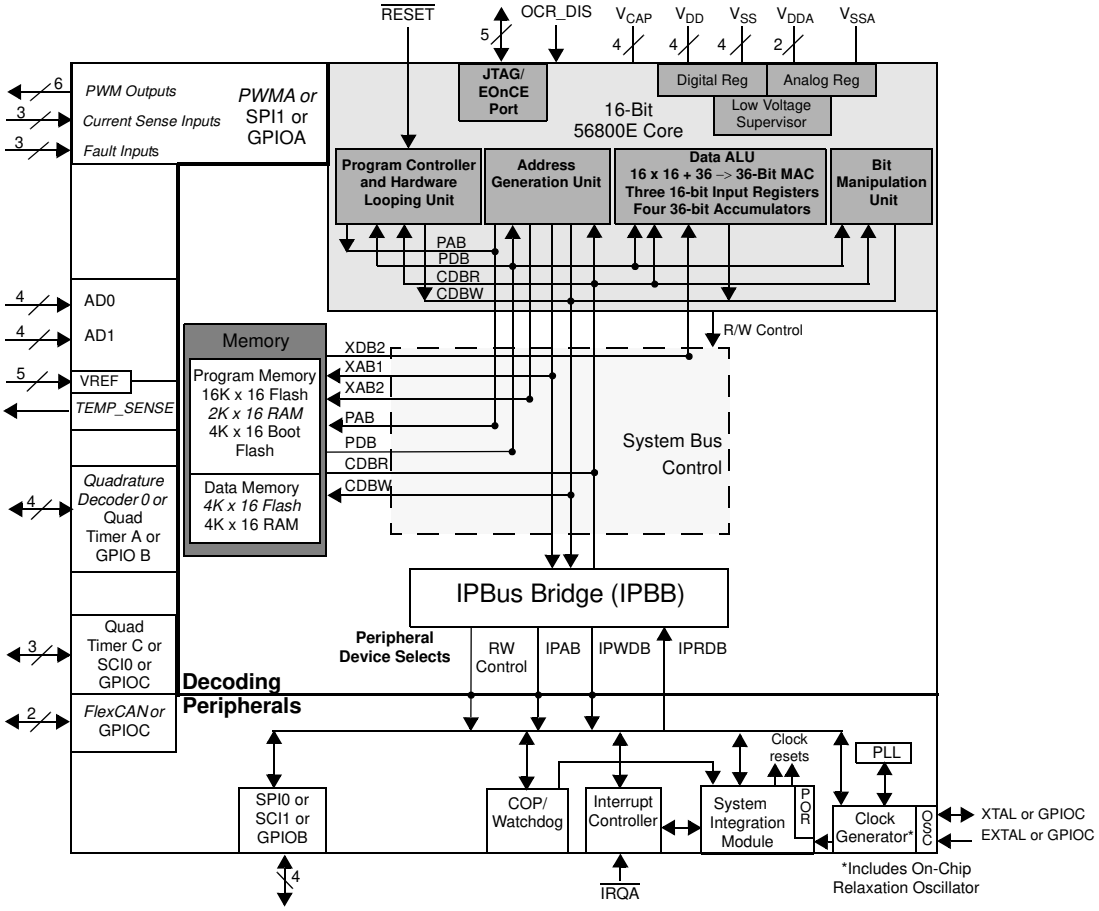
Version History	Description of Change
Rev 14.0	Added information/corrected state during reset in **Table 2-2**. Clarified external reference crystal frequency for PLL in **Table 10-14** by increasing maximum value to 8.4MHz.
Rev 15.0	Replaced “Tri-stated” with an explanation in State During Reset column in **Table 2-2**.
Rev. 16	• Added the following note to the description of the TMS signal in **Table 2-2**: **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor. • Added the following note to the description of the $\overline{\text{TRST}}$ signal in **Table 2-2**: **Note:** For normal operation, connect $\overline{\text{TRST}}$ directly to V_{SS}. If the design is to be used in a debugging environment, $\overline{\text{TRST}}$ may be tied to V_{SS} through a 1K resistor.
Rev. 17	Changed the “Frequency Accuracy” specification in **Table 10-16** (was ±2.0%, is +2 / -3%).

Please see http://www.freescale.com for the most current data sheet revision.

56F8323/56F8123 General Description

Note: *Features in italics are NOT available in the 56F8123 device.*

- Up to 60 MIPS at 60MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- 32KB Program Flash
- *4KB Program RAM*
- *8KB Data Flash*
- 8KB Data RAM
- 8KB Boot Flash
- *One 6-channel PWM module*
- Two 4-channel 12-bit ADCs
- *Temperature Sensor*
- *One Quadrature Decoder*
- *One FlexCAN module*
- Up to two Serial Communication Interfaces (SCIs)
- Up to two Serial Peripheral Interfaces (SPIs)
- Two general-purpose Quad Timers
- Computer Operating Properly (COP)/Watchdog
- On-Chip Relaxation Oscillator
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Up to 27 GPIO lines
- 64-pin LQFP Package



56F8323/56F8123 Block Diagram

Table of Contents

Part 1 Overview

1.1 56F8323/56F8123 Features

1.1.1 Core

- Efficient 16-bit 56800E family engine with dual Harvard architecture
- Up to 60 Million Instructions Per Second (MIPS) at 60MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- Arithmetic and logic multi-bit shifter
- Parallel instruction set with unique addressing modes
- Hardware DO and REP loops
- Three internal address buses
- Four internal data buses
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/EOnCE debug programming interface

1.1.2 Differences Between Devices

Table 1-1 outlines the key differences between the 56F8323 and 56F8123 devices.

Table 1-1 Device Differences

Feature	56F8323	56F8123
Guaranteed Speed	60MHz/60 MIPS	40MHz/40 MIPS
Program RAM	4KB	Not Available
Data Flash	8KB	Not Available
PWM	1 x 6	Not Available
CAN	1	Not Available
Quadrature Decoder	1 x 4	Not Available
Temperature Sensor	1	Not Available
Dedicated GPIO	—	10

1.1.3 Memory

Note: *Features in italics are NOT available in the 56F8123 device.*

- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Flash security protection
- On-chip memory, including a low-cost, high-volume Flash solution
  - 32KB of Program Flash
  - *4KB of Program RAM*
  - *8KB of Data Flash*
  - 8KB of Data RAM
  - 8KB of Boot Flash
- EEPROM emulation capability

1.1.4 Peripheral Circuits

Note: *Features in italics are NOT available in the 56F8123 device.*

- *One Pulse Width Modulator module with six PWM outputs, three Current Sense inputs and three Fault inputs; fault-tolerant design with dead time insertion; supports both center-aligned and edge-aligned modes*
- Two 12-bit, Analog-to-Digital Converters (ADCs), which support two simultaneous conversions with dual, 4-pin multiplexed inputs; ADC *and PWM modules* can be synchronized through Timer C, channel 2
- *Temperature Sensor can be connected, on the board, to any of the ADC inputs to monitor the on-chip temperature*
- Two 16-bit Quad Timer modules (TMR) totaling seven pins:
  - In the 56F8323, Timer A works in conjunction with Quad Decoder 0 and Timer C works in conjunction with the PWMA and ADCA
  - In the 56F8123, Timer C works in conjunction with ADCA
- *One Quadature Decoder which works in conjunction with Quad Timer A*
- *FlexCAN (CAN Version 2.0 B-compliant) module with 2-pin port for transmit and receive*
- Up to two Serial Communication Interfaces (SCIs)
- Up to two Serial Peripheral Interfaces (SPIs)
- Computer Operating Properly (COP)/Watchdog timer
- One dedicated external interrupt pin
- 27 General Purpose I/O (GPIO) pins
- Integrated Power-On Reset and Low-Voltage Interrupt Module
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, processor speed-independent, real-time debugging
- Software-programmable, Phase Lock Loop (PLL)
- On-chip relaxation oscillator

1.1.5 Energy Information

- Fabricated in high-density CMOS with 5V tolerant, TTL-compatible digital inputs
- On-board 3.3V down to 2.6V voltage regulator for powering internal logic and memories
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available
- ADC smart power management
- Each peripheral can be individually disabled to save power

1.2 Device Description

The 56F8323 and 56F8123 are members of the 56800E core-based family of controllers. Each combines, on a single chip, the processing power of a Digital Signal Processor (DSP) and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of their low cost, configuration flexibility, and compact program code, the 56F8323 and 56F8123 are well-suited for many applications. The devices include many peripherals that are especially useful for *automotive* control (56F8323 only); industrial control and networking; motion control; home appliances; general purpose inverters; smart sensors; fire and security systems; power management; and medical monitoring applications.

The 56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C Compilers to enable rapid development of optimized control applications.

The 56F8323 and 56F8123 support program execution from internal memories. Two data operands can be accessed from the on-chip data RAM per instruction cycle. These devices also provide one external dedicated interrupt line and up to 27 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

1.2.1 56F8323 Features

The 56F8323 controller includes 32KB of Program Flash and 8KB of Data Flash, each programmable through the JTAG port, with 4KB of Program RAM and 8KB of Data RAM. A total of 8KB of Boot Flash is incorporated for easy customer inclusion of field-programmable software routines that can be used to program the main Program and Data Flash memory areas. Both Program and Data Flash memories can be independently bulk erased or erased in pages. Program Flash page erase size is 1KB. Boot and Data Flash page erase size is 512 bytes. The Boot Flash memory can also be either bulk or page erased.

A key application-specific feature of the 56F8323 is the inclusion of one Pulse Width Modulator (PWM) module. This module incorporates three complementary, individually programmable PWM signal output pairs and is also capable of supporting six independent PWM functions to enhance motor control functionality. Complementary operation permits programmable dead time insertion, distortion correction via current sensing by software, and separate top and bottom output polarity control. The up-counter value is programmable to support a continuously variable PWM frequency. Edge-aligned and center-aligned

synchronous pulse width control (0% to 100% modulation) is supported. The device is capable of controlling most motor types: ACIM (AC Induction Motors); both BDC and BLDC (Brush and Brushless DC motors); SRM and VRM (Switched and Variable Reluctance Motors); and stepper motors. The PWM incorporates fault protection and cycle-by-cycle current limiting with sufficient output drive capability to directly drive standard optoisolators. A “smoke-inhibit”, write-once protection feature for key parameters is also included. A patented PWM waveform distortion correction circuit is also provided. Each PWM is double-buffered and includes interrupt controls to permit integral reload rates to be programmable from 1/2 (center-aligned mode only) to 16. The PWM module provides reference outputs to synchronize the Analog-to-Digital Converters (ADCs) through Quad Timer C, Channel 2.

The 56F8323 incorporates one Quadrature Decoder capable of capturing all four transitions on the two-phase inputs, permitting generation of a number proportional to actual position. Speed computation capabilities accommodate both fast- and slow-moving shafts. An integrated watchdog timer in the Quadrature Decoder can be programmed with a time-out value to alarm when no shaft motion is detected. Each input is filtered to ensure only true transitions are recorded.

This controller also provides a full set of standard programmable peripherals that include two Serial Communications Interfaces (SCIs), two Serial Peripheral Interfaces (SPIs), two Quad Timers, and FlexCAN. Any of these interfaces can be used as General Purpose Input/Outputs (GPIOs) if that function is not required. A Flex Controller Area Network (FlexCAN) interface (CAN Version 2.0 B-compliant) and an internal interrupt controller are also a part of the 56F8323.

1.2.2 56F8123 Features

The 56F8123 controller includes 32KB of Program Flash, programmable through the JTAG port, and 8KB of Data RAM. A total of 8KB of Boot Flash is incorporated for easy customer inclusion of field-programmable software routines that can be used to program the main Program Flash memory area. The Program Flash memory can be independently bulk erased or erased in pages; Program Flash page erase size is 1KB. The Boot Flash memory can also be either bulk or page erased.

This controller also provides a full set of standard programmable peripherals that include two Serial Communications Interfaces (SCIs), two Serial Peripheral Interfaces (SPIs), and two Quad Timers. Any of these interfaces can be used as General Purpose Input/Outputs (GPIOs) if that function is not required. An internal interrupt controller is also a part of the 56F8123.

1.3 Award-Winning Development Environment

Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs), demonstration board kit and development system cards will support concurrent engineering. Together, PE, CodeWarrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Architecture Block Diagram

Note: *Features in italics are NOT available in the 56F8123 device and are shaded in the following figures.*

The 56F8323/56F8123 architecture is shown in **Figure 1-1** and **Figure 1-2**. **Figure 1-1** illustrates how the 56800E system buses communicate with internal memories and the IPBus Bridge. **Table 1-2** lists the internal buses in the 56800E architecture and provides a brief description of their function. **Figure 1-2** shows the peripherals and control blocks connected to the IPBus Bridge. The figures do not show the on-board regulator and power and ground signals. They also do not show the multiplexing between peripherals or the dedicated GPIOs. Please see **Part 2 Signal/Connection Descriptions**, to see which signals are multiplexed with those of other peripherals.

Also shown in **Figure 1-2** are connections between the *PWM*, Timer C and ADC blocks. These connections allow the *PWM and/or* Timer C to control the timing of the start of ADC conversions. The Timer C, Channel 2, output can generate periodic start (SYNC) signals to the ADC to start its conversions. *In another operating mode, the PWM load interrupt (SYNC output) signal is routed internally to the Timer C, Channel 2, input as indicated. The timer can then be used to introduce a controllable delay before generating its output signal. The timer output then triggers the ADC.* To fully understand this interaction, please see the **56F8300 Peripheral User Manual** for clarification on the operation of all three of these peripherals.

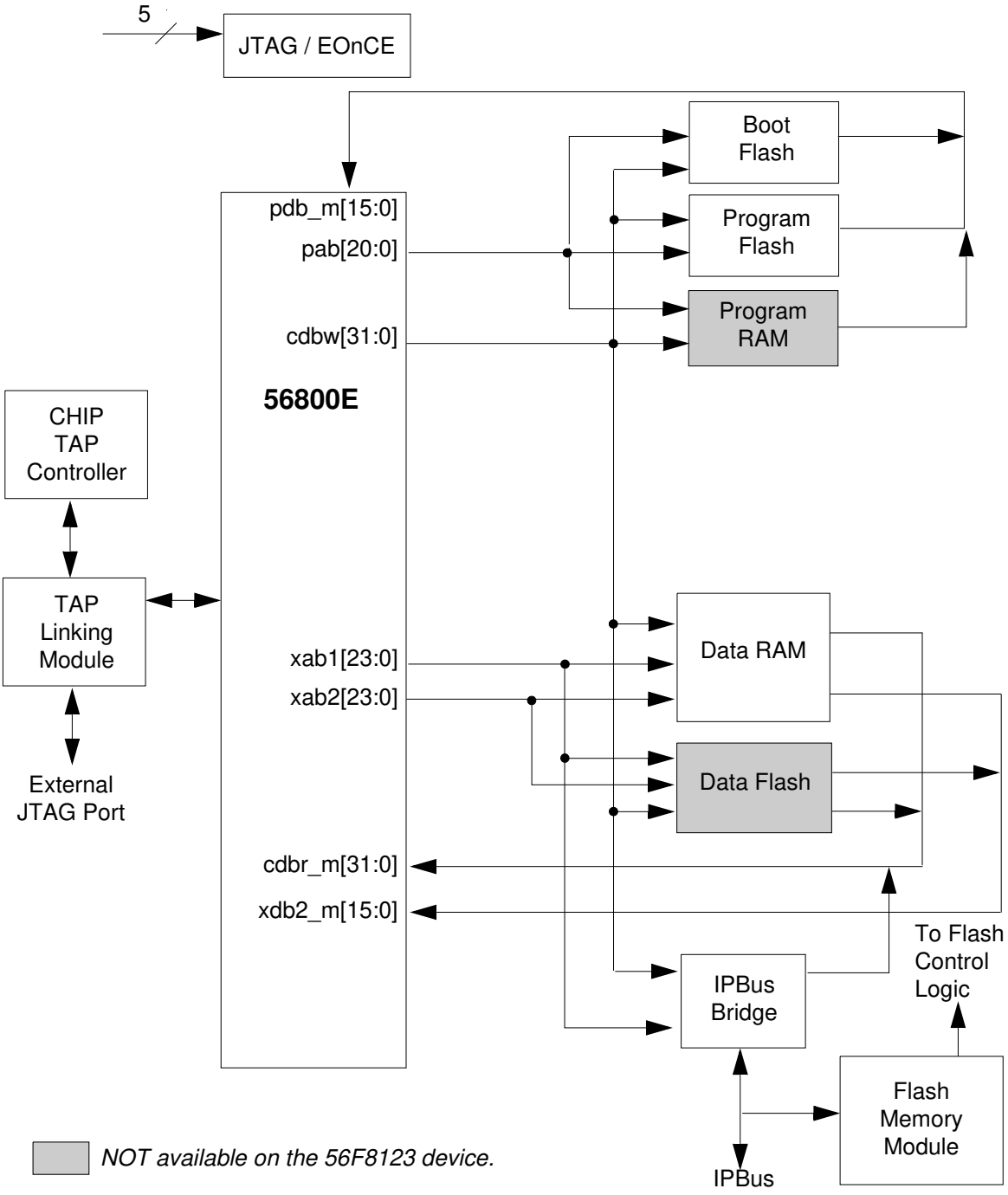


Figure 1-1 System Bus Interfaces

Note: Flash memories are encapsulated within the Flash Memory (FM) Module. Flash control is accomplished by the I/O to the FM over the peripheral bus, while reads and writes are completed between the core and the Flash memories.

Note: The primary data RAM port is 32 bits wide. Other data ports are 16 bits.

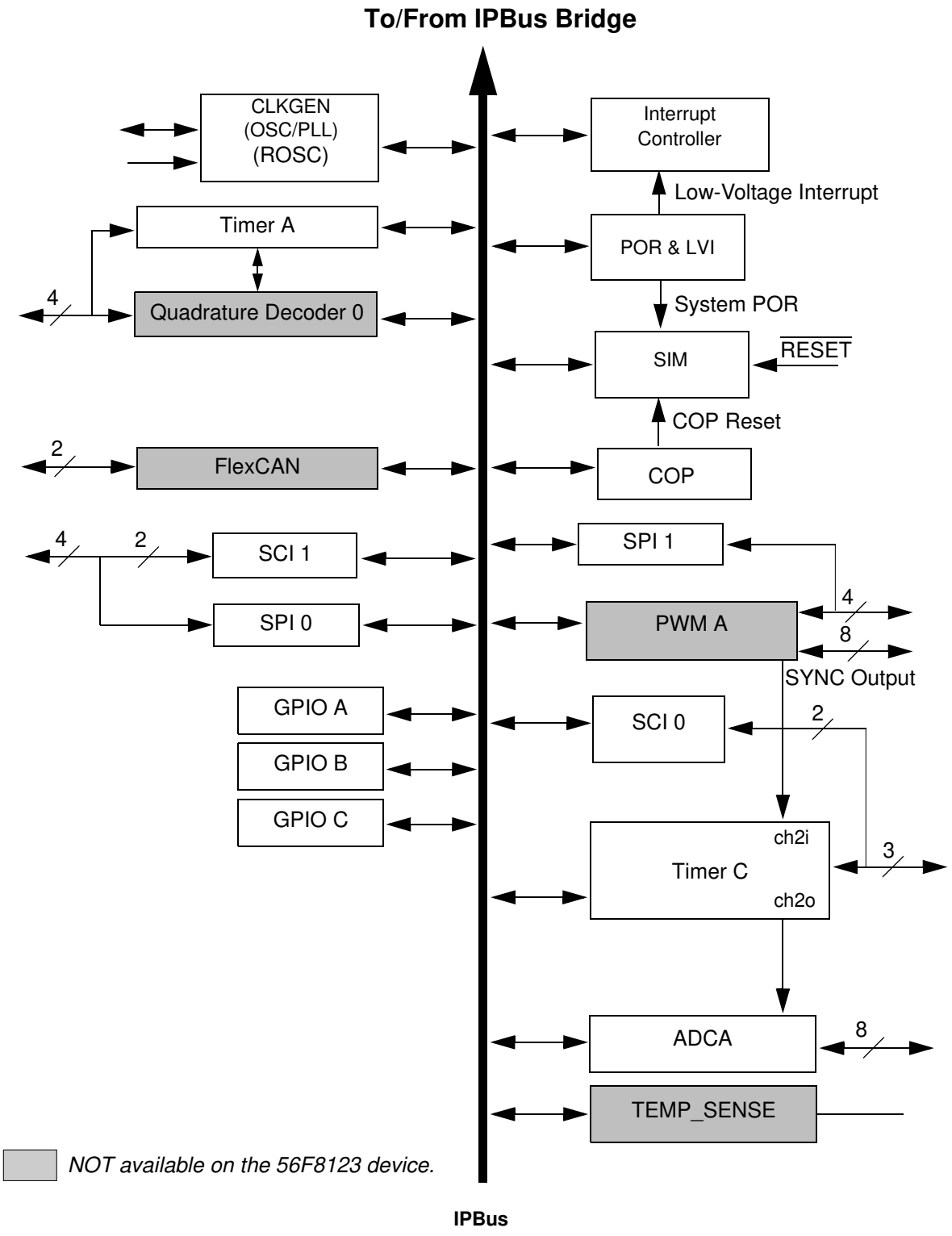


Figure 1-2 Peripheral Subsystem

Table 1-2 Bus Signal Names

Name	Function
Program Memory Interface	
pdb_m[15:0]	Program data bus for instruction word fetches or read operations.
cdbw[15:0]	Primary core data bus used for program memory writes. (Only these 16 bits of the cdbw[31:0] bus are used for writes to program memory.)
pab[20:0]	Program memory address bus. Data is returned on pdb_m bus.
Primary Data Memory Interface Bus	
cdbr_m[31:0]	Primary core data bus for memory reads. Addressed via xab1 bus.
cdbw[31:0]	Primary core data bus for memory writes. Addressed via xab1 bus.
xab1[23:0]	Primary data address bus. Capable of addressing bytes[1], words, and long data types. Data is written on cdbw and returned on cdbr_m. Also used to access memory-mapped I/O.
Secondary Data Memory Interface	
xdb2_m[15:0]	Secondary data bus used for secondary data address bus xab2 in the dual memory reads.
xab2[23:0]	Secondary data address bus used for the second of two simultaneous accesses. Capable of addressing only words. Data is returned on xdb2_m.
Peripheral Interface Bus	
IPBus [15:0]	Peripheral bus accesses all on-chip peripherals registers. This bus operates at the same clock rate as the Primary Data Memory and therefore generates no delays when accessing the processor. Write data is obtained from cdbw. Read data is provided to cdbr_m.

1. Byte accesses can only occur in the bottom half of the memory address space. The MSB of the address will be forced to 0.

1.5 Product Documentation

The documents listed in **Table 1-3** are required for a complete description and proper design with the 56F8323 and 56F8123 devices. Documentation is available from local Freescale distributors, Freescale semiconductor sales offices, Freescale Literature Distribution Centers, or online at **http://www.freescale.com/semiconductors**.

Table 1-3 Chip Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, 16-bit controller core processor, and the instruction set	DSP56800ERM
56F8300 Peripheral User Manual	Detailed description of peripherals of the 56800E family of devices	MC56F8300UM
56F8300 SCI/CAN Bootloader User Manual	Detailed description of the SCI/CAN Bootloaders 56F8300 family of devices	MC56F83xxBLUM
56F8323/56F8123 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	MC56F8323
Errata	Details any chip issues that might be present	MC56F8323E MC56F8123E

1.6 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
“asserted”	A high true (active high) signal is high or a low true (active low) signal is low.
“deasserted”	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:

Signal/Symbol	Logic State	Signal State	Voltage[1]
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the 56F8323 and 56F8123 are organized into functional groups, as detailed in **Table 2-1** and as illustrated in **Figure 2-1** and Figure 2-2. In **Table 2-2**, each table row describes the signal or signals present on a pin.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins in Package	
	56F8323	56F8123
Power (V_{DD} or V_{DDA})	6	6
Power Option Control	1	1
Ground (V_{SS} or V_{SSA})	5	5
Supply Capacitors[1] & V_{PP}[2]	4	4
PLL and Clock	2	2
Interrupt and Program Control	2	2
Pulse Width Modulator (PWM) Ports[3]	12	—
Serial Peripheral Interface (SPI) Port 0[4]	4	8
Quadrature Decoder Port 0[5]	4	—
CAN Ports	2	—
Analog-to-Digital Converter (ADC) Ports	13	13
Timer Module Port C[6]	3	3
Timer Module Port A	—	4
JTAG/Enhanced On-Chip Emulation (EOnCE)	5	5
Temperature Sensse	1	—
Dedicated GPIO	—	10

1. If the on-chip regulator is disabled, the V_{CAP} pins serve as 2.5V V_{DD_CORE} power inputs
2. The V_{PP} input shares the $\overline{IRQA}$ input
3. Pins in this section can function as SPI #1 and GPIO
4. Pins in this section can function as SCI #1 and GPIO
5. Alternately, can function as Quad Timer A pins or GPIO
6. Two pins can function as SCI #0 and GPIO

Note: See **Table 1-1** for 56F8123 functional differences.

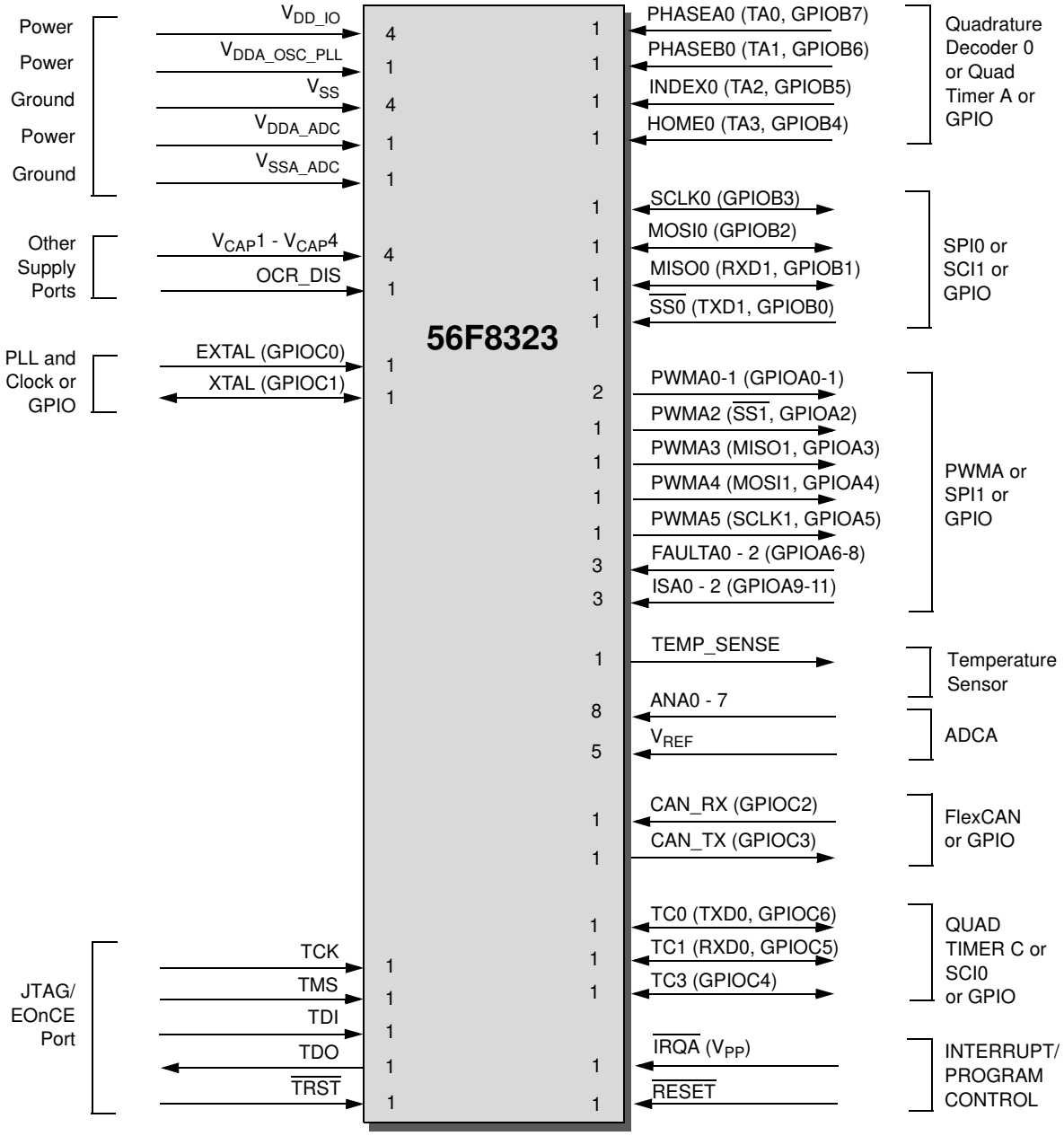


Figure 2-1 56F8323 Signals Identified by Functional Group (64-Pin LQFP)

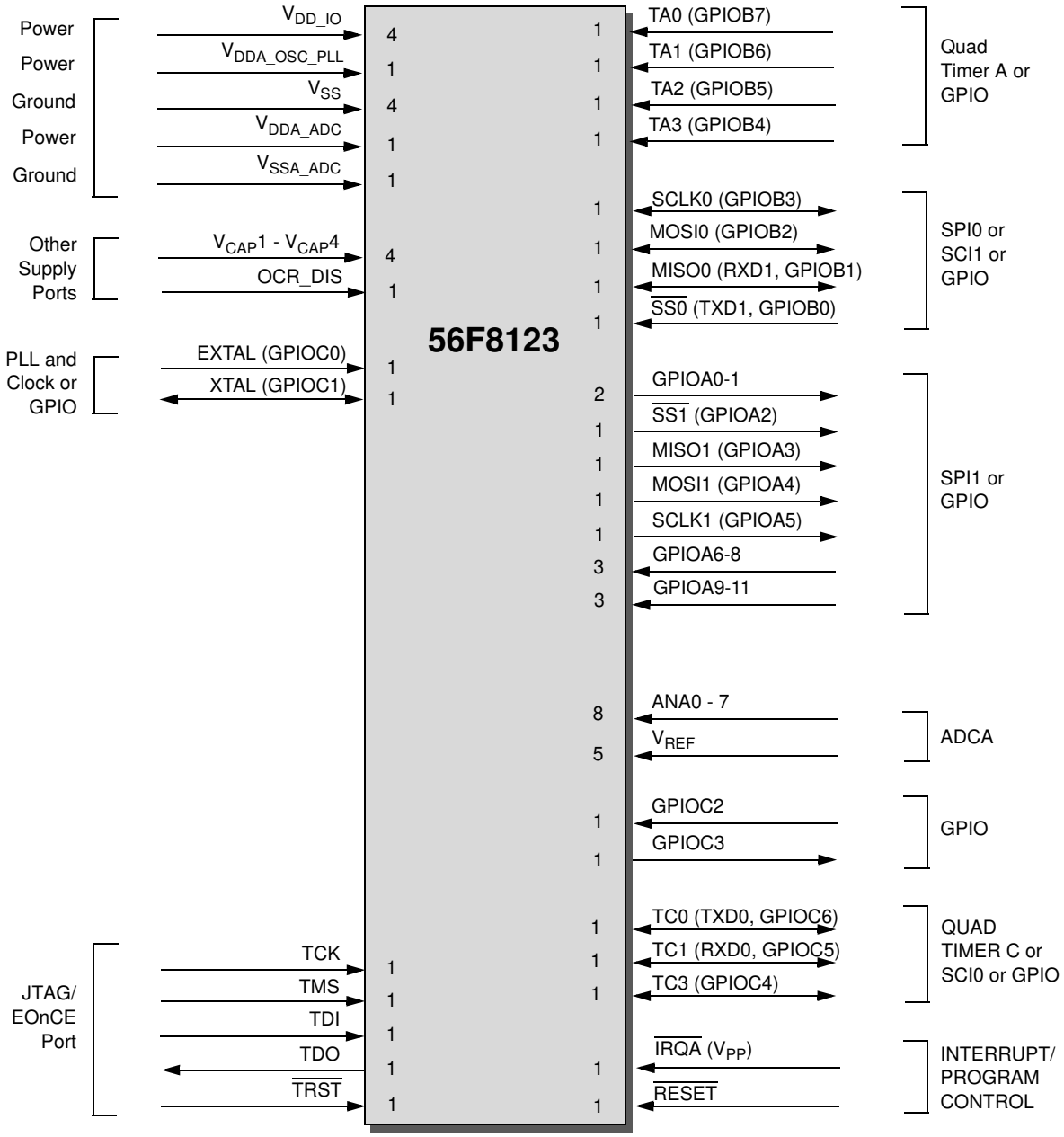


Figure 2-2 56F8123 Signals Identified by Functional Group (64-Pin LQFP)

2.2 Signal Pins

After reset, each pin is configured for its primary function (listed first). In the 56F8123, after reset, each pin must be configured for the desired function. The initialization software will configure each pin for the function listed first for each pin, as shown in Table 2-2. Any alternate functionality must be programmed.

Note: *Signals in italics are not available in the 56F8123 device.*

If the "State During Reset" lists more than one state for a pin, the first state is the actual reset state. Other states show the reset condition of the alternate function, which you get if the alternate pin function is selected without changing the configuration of the alternate peripheral. For example, the SCLK0/GPIOB3 pin shows that it is tri-stated during reset. If the GPIOB_PER is changed to select the GPIO function of the pin, it will become an input if no other registers are changed.

Table 2-2 Signal and Package Information for the 64-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
V_{DD_IO}	6	Supply		**I/O Power** — This pin supplies 3.3V power to the chip I/O interface and also the Processor core throught the on-chip voltage regulator, if it is enabled.
V_{DD_IO}	20			
V_{DD_IO}	48			
V_{DD_IO}	59			
$V_{DDA\_OSC\_PLL}$	42	Supply		**Oscillator and PLL Power** — This pin supplies 3.3V power to the OSC and to the internal regulator that in turn supplies the Phase Locked Loop. It must be connected to a clean analog power supply.
V_{DDA_ADC}	41	Supply		**ADC Power** — This pin supplies 3.3V power to the ADC modules. It must be connected to a clean analog power supply.
V_{SS}	11	Supply		**Ground** — These pins provide ground for chip logic and I/O drivers.
V_{SS}	17			
V_{SS}	44			
V_{SS}	60			
V_{SSA_ADC}	39	Supply		**ADC Analog Ground** — This pin supplies an analog ground to the ADC modules.

Table 2-2 Signal and Package Information for the 64-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
$V_{CAP}1$	57	Supply	Supply	**$V_{CAP}1$ - 4** — When OCR_DIS is tied to V_{SS} (regulator enabled), connect each pin to a 2.2µF or greater bypass capacitor in order to bypass the core logic voltage regulator, required for proper chip operation. When OCR_DIS is tied to V_{DD}, (regulator disabled), these pins become V_{DD_CORE} and should be connected to a regulated 2.5V power supply. **Note: This bypass is required even if the chip is powered with an external supply.**
$V_{CAP}2$	23			
$V_{CAP}3$	5			
$V_{CAP}4$	43			
OCR_DIS	45			**On-Chip Regulator Disable** — Tie this pin to V_{SS} to enable the on-chip regulator Tie this pin to V_{DD} to disable the on-chip regulator **This pin is intended to be a static DC signal from power-up to shut down. Do not try to toggle this pin for power savings during operation.**
EXTAL	46	Input	Input	**External Crystal Oscillator Input** — This input can be connected to an 8MHz external crystal. If an external clock is used, XTAL must be used as the input and EXTAL connected to V_{SS}. The input clock can be selected to provide the clock directly to the core. This input clock can also be selected as the input clock for the on-chip PLL.
(GPIOC0)		Schmitt Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is an EXTAL input with pull-ups disabled.
XTAL	47	Output	Output	**Crystal Oscillator Output** — This output can be connected to an 8MHz external crystal. If an external clock is used, XTAL must be used as the input and EXTAL connected to V_{SS}. The input clock can be selected to provide the clock directly to the core. This input clock can also be selected as the input clock for the on-chip PLL.
(GPIOC1)		Schmitt Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is an XTAL input with pull-ups disabled.
TCK	53	Schmitt Input	Input, pulled low internally	**Test Clock Input** — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pull-down resistor. A Schmitt trigger input is used for noise immunity.

Table 2-2 Signal and Package Information for the 64-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
TMS	54	Schmitt Input	Input, pulled high internally	**Test Mode Select Input** — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
TDI	55	Schmitt Input	Input, pulled high internally	**Test Data Input** — This input pin provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
TDO	56	Output	In reset, output is disabled, pull-up is enabled	**Test Data Output** — This tri-stateable output pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and changes on the falling edge of TCK.
$\overline{\text{TRST}}$	58	Schmitt Input	Input, pulled high internally	**Test Reset** — As an input, a low signal on this pin provides a reset signal to the JTAG TAP controller. To ensure complete hardware reset, $\overline{\text{TRST}}$ should be asserted whenever $\overline{\text{RESET}}$ is asserted. The only exception occurs in a debugging environment when a hardware device reset is required and the EOnCE/JTAG module must not be reset. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$. To deactivate the internal pull-up resistor, set the JTAG bit in the SIM_PUDR register. **Note:** For normal operation, connect $\overline{\text{TRST}}$ directly to V_{SS}. If the design is to be used in a debugging environment, $\overline{\text{TRST}}$ may be tied to V_{SS} through a 1K resistor.
PHASEA0 **(TA0)** **(GPIOB7)** **(oscillator_ clock)**	52	Schmitt Input Schmitt Input/ Output Schmitt Input/ Output Output	Input, pull-up enabled	**Phase A** — Quadrature Decoder 0, PHASEA input **TA0** — Timer A, Channel 0 **Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. **Clock Output** - can be used to monitor the internal oscillator clock signal (see **Part 6.5.7** CLKO Select Register, SIM_CLKOSR). In the 56F8323, the default state after reset is PHASEA0. In the 56F8123, the default state is not one of the functions offered and must be reconfigured.

Table 2-2 Signal and Package Information for the 64-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
PHASEB0	51	Schmitt Input	Input, pull-up enabled	**Phase B** — Quadrature Decoder 0, PHASEB input
(TA1)		Schmitt Input/ Output		**TA1** — Timer A ,Channel 1
(GPIOB6)		Schmitt Input/ Output		**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(SYS_CLK2)		Output		**Clock Output** - can be used to monitor the internal SYS_CLK2 signal (see **Part 6.5.7** CLKO Select Register, SIM_CLKOSR). In the 56F8323, the default state after reset is PHASEB0. In the 56F8123, the default state is not one of the functions offered and must be reconfigured.
INDEX0	50	Schmitt Input	Input, pull-up enabled	**Index** — Quadrature Decoder 0, INDEX input
(TA2)		Schmitt Input/ Output		**TA2** — Timer A, Channel 2
(GPIOB5)		Schmitt Input/ Output		**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(SYS_CLK)		Output		**Clock Output** - can be used to monitor the internal SYS_CLK signal (see **Part 6.5.7** CLKO Select Register, SIM_CLKOSR). In the 56F8323, the default state after reset is INDEX0. In the 56F8123, the default state is not one of the functions offered and must be reconfigured.

Table 2-2 Signal and Package Information for the 64-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
HOME0	49	Schmitt Input	Input, pull-up enabled	**Home** — Quadrature Decoder 0, HOME input
(TA3)		Schmitt Input/ Output		**TA3** — Timer A, Channel 3
(GPIOB4)		Schmitt Input/ Output		**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(prescaler_ clock)		Output		**Clock Output** - can be used to monitor the internal prescaler_clock signal (see **Part 6.5.7** CLKO Select Register, SIM_CLKOSR). In the 56F8323, the default state after reset is HOME0. In the 56F8123, the default state is not one of the functions offered and must be reconfigured.
SCLK0	25	Schmitt Input/ Output	Input, pull-up enabled	**SPI 0 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. A Schmitt trigger input is used for noise immunity.
(GPIOB3)		Schmitt Input/ Output		**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCLK0.
MOSI0	24	Schmitt Input/ Output	In reset, output is disabled, pull-up is enabled	**SPI 0 Master Out/Slave In** — This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data.
(GPIOB2)		Schmitt Input/ Output		**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is MOSI0.

Table 2-2 Signal and Package Information for the 64-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
MISO0	22	Schmitt Input/ Output	Input, pull-up enabled	**SPI 0 Master In/Slave Out** — This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. The slave device places data on the MISO line a half-cycle before the clock edge the master device uses to latch the data.
(RXD1)		Schmitt Input		**Receive Data** — SCI1 receive data input
(GPIOB1)		Schmitt Input/ Output		**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is MISO0.
$\overline{\text{SS0}}$	21	Schmitt Input	Input, pull-up enabled	**SPI 0 Slave Select** — $\overline{\text{SS0}}$ is used in slave mode to indicate to the SPI module that the current transfer is to be received.
(TXD1)		Output		**Transmit Data** — SCI1 transmit data output
(GPIOB0)		Schmitt Input/ Output		**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is $\overline{\text{SS0}}$.
PWMA0	3	Output	In reset, output is disabled, pull-up is enabled	**PWMA0** — This is one of six PWMA output pins.
(GPIOA0)		Schmitt Input/ Output		**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8323, the default state after reset is PWMA0. In the 56F8123, the default state is not one of the functions offered and must be reconfigured.
PWMA1	4	Output	In reset, output is disabled, pull-up is enabled	**PWMA1** — This is one of six PWMA output pins.
(GPIOA1)		Schmitt Input/ Output		**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8323, the default state after reset is PWMA1. In the 56F8123, the default state is not one of the functions offered and must be reconfigured

Table 2-2 Signal and Package Information for the 64-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
PWMA2 **($\overline{\text{SS1}}$)** **(GPIOA2)**	7	Output Schmitt Input Schmitt Input/ Output	In reset, output is disabled, pull-up is enabled	**PWMA2** — This is one of six PWMA output pins. **SPI 1 Slave Select** — $\overline{\text{SS1}}$ is used in slave mode to indicate to the SPI module that the current transfer is to be received. **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8323, the default state after reset is PWMA2. In the 56F8123, the default state is not one of the functions offered and must be reconfigured.
PWMA3 **(MISO1)** **(GPIOA3)**	8	Output Schmitt Input/ Output Schmitt Input/ Output	In reset, output is disabled, pull-up is enabled	**PWMA3** — This is one of six PWMA output pins. **SPI 1 Master In/Slave Out** — This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. The slave device places data on the MISO line a half-cycle before the clock edge the master device uses to latch the data. **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8323, the default state after reset is PWMA3. In the 56F8123, the default state is not one of the functions offered and must be reconfigured.
PWMA4 **(MOSI1)** **(GPIOA4)**	9	Output Schmitt Input/ Output Schmitt Input/ Output	In reset, output is disabled, pull-up is enabled	**PWMA4** — This is one of six PWMA output pins. **SPI 1 Master Out/Slave In** — This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data. **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8323, the default state after reset is PWMA4. In the 56F8123, the default state is not one of the functions offered and must be reconfigured.