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56F8345/56F8145

Data Sheet

Preliminary Technical Data

56F8300
16-bit Digital Signal Controllers

MC56F8345
Rev. 17
01/2007

freescale.com

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semiconductor

Document Revision History

Version History	Description of Change
Rev 1.0	Pre-Release version, Alpha customers only
Rev 2.0	Initial Public Release
Rev 3.0	Corrected typo in **Table 10-4**, Flash Endurance is 10,000 cycles. Addressed additional grammar issues.
Rev 4.0	Added “Typical Min” values to **Table 10-16**. Edited grammar, spelling, consistency of language throughout family. Updated values in Current Consumption per Power Supply Pin, **Table 10-7**, Regulator Parameters, **Table 10-9**, External Clock Operation Timing Requirements **Table 10-13**, SPI Timing, **Table 10-17**, ADC Parameters, **Table 10-23**, and IO Loading Coefficients at 10MHz, **Table 10-24**.
Rev 5.0	Added **Part 4.8**. Added the word “access” to FM Error Interrupt in **Table 4-5**. Removed min and max numbers. Clarified CSBAR 0 and CSBAR 1 reset values in **Table 4-10**. Removed min and max numbers, only documenting Typ. numbers for LVI in **Table 10-6**.
Rev 6.0	Updated numbers in **Table 10-7** and **Table 10-8** with more recent data. Corrected typo in **Table 10-3** in Pd characteristics.
Rev 7.0	Replaced any reference to Flash Interface Unit with Flash Memory Module. Added note to V_{CAP} pin in **Table ?-??????**. Removed unneccessary notes in **Table 10-12**. Corrected temperature range in **Table 10-14**. Added ADC calibration information to **Table 10-23** and new graphs in **Figure 10-21**.
Rev 8.0	Clarified **Table 10-22**. Corrected Digital Input Current Low (pull-up enabled) numbers in **Table 10-5**. Removed text and Table 10-2. Replaced with note to **Table 10-1**.
Rev 9.0	Added 56F8145 information; edited to indicate differences in 56F8345 and 56F8145. Reformatted for Freescale look and feel. Updated Temperature Sensor and ADC tables; updated balance of electrical tables for consistency throughout family. Clarified I/O power description in **Table ?-??????**, added note to **Table 10-7** and clarified **Section 12.3**.
Rev 10.0	Corrected beginning address for On-Chip Data RAM, **Table 4-6**.
Rev 11.0	Corrected addresses in **Table 4-6**.
Rev 12.0	Corrected **Figure 10-21**. Added output voltage maximum value and note to clarify in **Table 10-1**; also removed overall life expectancy note, since life expectancy is dependent on customer usage and must be determined by reliability engineering. Clarified value and unit measure for Maximum allowed P_D in **Table 10-3**. Corrected note about average value for Flash Data Retention in **Table 10-4**. Added new RoHS-compliant orderable part numbers in **Table 13-1**.
Rev 13.0	Updated **Table 10-23** to reflect new value for maximum Uncalibrated Gain Error
Rev 14.0	Deleted RSTO from Pin Group 2 (listed after **Table 10-1**). Deleted formula for Max Ambient Operating Temperature (Automotive) and Max Ambient Operating Temperature (Industrial) in **Table 10-4**. Added RoHS-compliance and “pb-free” language to back cover.

Please see http://www.freescale.com for the most current Data Sheet revision.

Document Revision History (Continued)

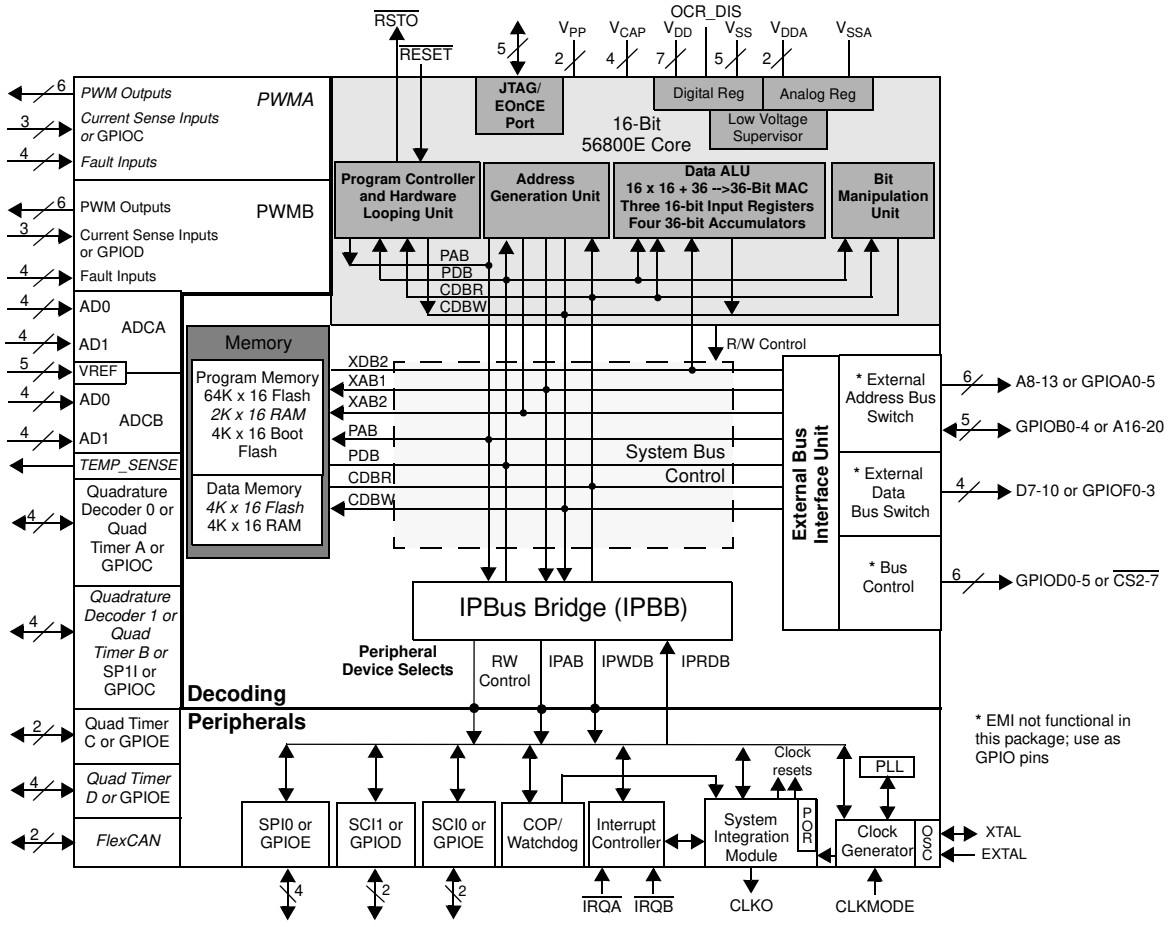
Version History	Description of Change
Rev 15.0	Updated JTAG ID in **Section 6.5.4**. Added information/corrected state during reset in **Table 2-2**. Clarified external reference crystal frequency for PLL in **Table 10-14** by increasing maximum value to 8.4MHz.
Rev 16.0	Replaced “Tri-stated” with an explanation in State During Reset column in **Table 2-2**.
Rev. 17	• Added the following note to the description of the TMS signal in **Table 2-2**: **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor. • Added the following note to the description of the $\overline{\text{TRST}}$ signal in **Table 2-2**: **Note:** For normal operation, connect $\overline{\text{TRST}}$ directly to V_{SS}. If the design is to be used in a debugging environment, $\overline{\text{TRST}}$ may be tied to V_{SS} through a 1K resistor.

Please see http://www.freescale.com for the most current data sheet revision.

56F8345/56F8145 General Description

Note: *Features in italics are NOT available in the 56F8145 device.*

- Up to 60 MIPS at 60MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- 128KB Program Flash
- *4KB Program RAM*
- *8KB Data Flash*
- 8KB Data RAM
- 8KB Boot Flash
- *Up to two* 6-channel PWM modules
- Four 4-channel, 12-bit ADCs
- *Temperature Sensor*
- *Up to two* Quadrature Decoders
- *FlexCAN module*
- Optional On-Chip Regulator
- Two Serial Communication Interfaces (SCIs)
- Up to two Serial Peripheral Interface (SPIs)
- Up to four general-purpose Quad Timers
- Computer Operating Properly (COP)/Watchdog
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Up to 49 GPIO lines
- 128-pin LQFP Package



56F8345/56F8145 Block Diagram - 128 LQFP

Table of Contents

Part 1 Overview

1.1 56F8345/56F8145 Features

1.1.1 Core

- Efficient 16-bit 56800E family controller engine with dual Harvard architecture
- Up to 60 Million Instructions Per Second (MIPS) at 60MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- Arithmetic and logic multi-bit shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses
- Four internal data buses
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/EOnCE debug programming interface

1.1.2 Differences Between Devices

Table 1-1 outlines the key differences between the 56F8345 and 56F8145 devices.

Table 1-1 Device Differences

Feature	56F8345	56F8145
Guaranteed Speed	60MHz/60 MIPS	40MHz/40MIPS
Program RAM	4KB	Not Available
Data Flash	8KB	Not Available
PWM	2 x 6	1 x 6
CAN	1	Not Available
Quad Timer	4	2
Quadrature Decoder	2 x 4	1 x 4
Temperature Sensor	1	Not Available

1.1.3 Memory

Note: *Features in italics are NOT available in the 56F8145 device.*

- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Flash security protection feature
- On-chip memory, including a low-cost, high-volume Flash solution
  - 128KB of Program Flash
  - *4KB of Program RAM*
  - *8KB of Data Flash*
  - 8KB of Data RAM
  - 8KB of Boot Flash
- *EEPROM emulation capability*

1.1.4 Peripheral Circuits

Note: *Features in italics are NOT available in the 56F8145 device.*

- Pulse Width Modulator module:
  - In the 56F8345, two Pulse Width Modulator modules, each with six PWM outputs, three Current Sense inputs, and four Fault inputs; fault-tolerant design with dead time insertion; supports both center-aligned and edge-aligned modes
  - In the 56F8145, one Pulse Width Modulator module with six PWM outputs, three Current Sense inputs and three Fault inputs; fault-tolerant design with dead time insertion; supports both center-aligned and edge-aligned modes
- Four 12-bit, Analog-to-Digital Converters (ADCs), which support four simultaneous conversions with quad, 4-pin multiplexed inputs; ADC and PWM modules can be synchronized through Timer C, channels 2 and 3
- Quadrature Decoder:
  - In the 56F8345, two four-input Quadrature Decoders or two additional Quad Timers
  - In the 56F8145, one four-input Quadrature Decoder, which works in conjunction with Quad Timer A
- *Temperature Sensor can be connected, on the board, to any of the ADC inputs to monitor the on-chip temperature*
- Quad Timer:
  - In the 56F8345, four dedicated general-purpose Quad Timers totaling six dedicated pins: Timer C with two pins and Timer D with four pins
  - In the 56F8145, two Quad Timers; Timer A and Timer C both work in conjunction with GPIO
- Optional On-Chip Regulator
- *FlexCAN (CAN Version 2.0 B-compliant) module with 2-pin port for transmit and receive*
- Two Serial Communication Interfaces (SCIs), each with two pins (or four additional GPIO lines)
- Up to two Serial Peripheral Interfaces (SPIs), both with configurable 4-pin port (or eight additional GPIO lines); SPI 1 can also be used as Quadrature Decoder 1 or Quad Timer B
- Computer Operating Properly (COP)/Watchdog timer

- Two dedicated external interrupt pins
- 49 General Purpose I/O (GPIO) pins; 28 pins dedicated to GPIO
- External reset input pin for hardware reset
- External reset output pin for system reset
- Integrated low-voltage interrupt module
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, processor speed-independent, real-time debugging
- Software-programmable, Phase Lock Loop-based frequency synthesizer for the core clock

1.1.5 Energy Information

- Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
- On-board 3.3V down to 2.6V voltage regulator for powering internal logic and memories; can be disabled
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available
- ADC smart power management
- Each peripheral can be individually disabled to save power

1.2 Device Description

The 56F8345 and 56F8145 are members of the 56800E core-based family of controllers. Each combines, on a single chip, the processing power of a Digital Signal Processor (DSP) and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of their low cost, configuration flexibility, and compact program code, the 56F8345 and 56F8145 are well-suited for many applications. The devices include many peripherals that are especially useful for motion control, smart appliances, steppers, encoders, tachometers, limit switches, power supply and control, *automotive* control (56F8345 only), engine management, noise suppression, remote utility metering, industrial control for power, lighting, and automation applications.

The 56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C/C++ Compilers to enable rapid development of optimized control applications.

The 56F8345 and 56F8145 support program execution from internal memories. Two data operands can be accessed from the on-chip data RAM per instruction cycle. These devices also provide two external dedicated interrupt lines and up to 49 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

1.2.1 56F8345 Features

The 56F8345 controller includes 128KB of Program Flash and 8KB of Data Flash (each programmable through the JTAG port) with 4KB of Program RAM and 8KB of Data RAM. A total of 8KB of Boot Flash is incorporated for easy customer inclusion of field-programmable software routines that can be used to

program the main Program and Data Flash memory areas. Both Program and Data Flash memories can be independently bulk erased or erased in pages. Program Flash page erase size is 1KB. Boot and Data Flash page erase size is 512 bytes. The Boot Flash memory can also be either bulk or page erased.

A key application-specific feature of the 56F8345 is the inclusion of two Pulse Width Modulator (PWM) modules. These modules each incorporate three complementary, individually programmable PWM signal output pairs (each module is also capable of supporting six independent PWM functions, for a total of 12 PWM outputs) to enhance motor control functionality. Complementary operation permits programmable dead time insertion, distortion correction via current sensing by software, and separate top and bottom output polarity control. The up-counter value is programmable to support a continuously variable PWM frequency. Edge-aligned and center-aligned synchronous pulse width control (0% to 100% modulation) is supported. The device is capable of controlling most motor types: ACIM (AC Induction Motors); both BDC and BLDC (Brush and Brushless DC motors); SRM and VRM (Switched and Variable Reluctance Motors); and stepper motors. The PWMs incorporate fault protection and cycle-by-cycle current limiting with sufficient output drive capability to directly drive standard optoisolators. A “smoke-inhibit”, write-once protection feature for key parameters is also included. A patented PWM waveform distortion correction circuit is also provided. Each PWM is double-buffered and includes interrupt controls to permit integral reload rates to be programmable from 1 to 16. The PWM modules provide reference outputs to synchronize the Analog-to-Digital Converters through two channels of Quad Timer C.

The 56F8345 incorporates two Quadrature Decoders capable of capturing all four transitions on the two-phase inputs, permitting generation of a number proportional to actual position. Speed computation capabilities accommodate both fast- and slow-moving shafts. An integrated watchdog timer in the Quadrature Decoder can be programmed with a time-out value to alert when no shaft motion is detected. Each input is filtered to ensure only true transitions are recorded.

This controller also provides a full set of standard programmable peripherals that include two Serial Communications Interfaces (SCIs); two Serial Peripheral Interfaces (SPIs); and four Quad Timers. Any of these interfaces can be used as General Purpose Input/Outputs (GPIOs) if that function is not required. A Flex Controller Area Network (FlexCAN) interface (CAN Version 2.0 B-compliant) and an internal interrupt controller are also a part of the 56F8345.

1.2.2 56F8145 Features

The 56F8145 controller includes 128KB of Program Flash, programmable through the JTAG port, and 8KB of Data RAM. A total of 8KB of Boot Flash is incorporated for easy customer inclusion of field-programmable software routines that can be used to program the main Program Flash memory area. The Program Flash memory can be independently bulk erased or erased in pages; Program Flash page erase size is 1KB. The Boot Flash page erase size is 512 bytes; Boot Flash memory can also be either bulk or page erased.

A key application-specific feature of the 56F8145 is the inclusion of one Pulse Width Modulator (PWM) module. This module incorporates three complementary, individually programmable PWM signal output pairs and can also support six independent PWM functions to enhance motor control functionality. Complementary operation permits programmable dead time insertion, distortion correction via current sensing by software, and separate top and bottom output polarity control. The up-counter value is programmable to support a continuously variable PWM frequency. Edge-aligned and center-aligned

synchronous pulse width control (0% to 100% modulation) is supported. The device is capable of controlling most motor types: ACIM (AC Induction Motors); both BDC and BLDC (Brush and Brushless DC motors); SRM and VRM (Switched and Variable Reluctance Motors); and stepper motors. The PWM incorporates fault protection and cycle-by-cycle current limiting with sufficient output drive capability to directly drive standard optoisolators. A “smoke-inhibit”, write-once protection feature for key parameters is also included. A patented PWM waveform distortion correction circuit is also provided. The PWM is double-buffered and includes interrupt controls to permit integral reload rates to be programmable from 1 to 16. The PWM module provides reference outputs to synchronize the Analog-to-Digital Converters through two channels of Quad Timer C.

The 56F8145 incorporates a Quadrature Decoder capable of capturing all four transitions on the two-phase inputs, permitting generation of a number proportional to actual position. Speed computation capabilities accommodate both fast- and slow-moving shafts. An integrated watchdog timer in the Quadrature Decoder can be programmed with a time-out value to alert when no shaft motion is detected. Each input is filtered to ensure only true transitions are recorded.

This controller also provides a full set of standard programmable peripherals that include two Serial Communications Interfaces (SCIs); two Serial Peripheral Interfaces (SPIs); and two Quad Timers. Any of these interfaces can be used as General Purpose Input/Outputs (GPIOs) if that function is not required. An internal interrupt controller is also a part of the 56F8145.

1.3 Award-Winning Development Environment

Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, CodeWarrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Architecture Block Diagram

Note: *Features in italics are NOT available in the 56F8145 device and are shaded in the following figures.*

The 56F8345/56F8145 architecture is shown in **Figure 1-1** and **Figure 1-2**. **Figure 1-1** illustrates how the 56800E system buses communicate with internal memories and the IPBus Bridge. **Table 1-2** lists the internal buses in the 56800E architecture and provides a brief description of their function. **Figure 1-2** shows the peripherals and control blocks connected to the IPBus Bridge. The figures do not show the on-board regulator and power and ground signals. They also do not show the multiplexing between peripherals or the dedicated GPIOs. Please see **Part 2, Signal/Connection Descriptions,** to see which signals are multiplexed with those of other peripherals.

Also shown in **Figure 1-2** are connections between the PWM, Timer C and ADC blocks. These connections allow the PWM and/or Timer C to control the timing of the start of ADC conversions. The Timer C channel indicated can generate periodic start (SYNC) signals to the ADC to start its conversions. In another operating mode, the PWM load interrupt (SYNC output) signal is routed internally to the Timer C input channel as indicated. The timer can then be used to introduce a controllable delay before generating its output signal. The timer output then triggers the ADC. To fully understand this interaction, please see the **56F8300 Peripheral User's Manual** for clarification on the operation of all three of these peripherals.

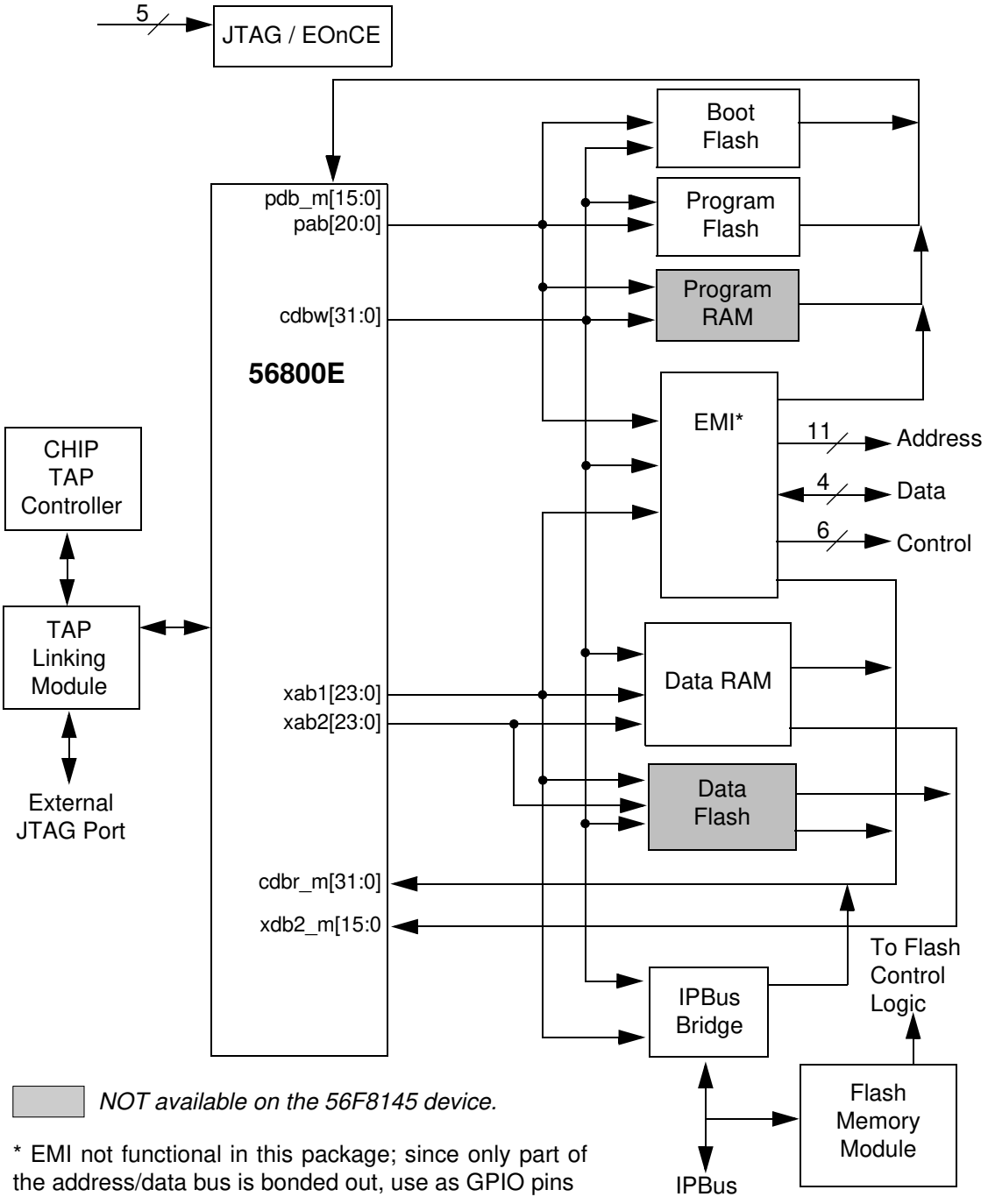


Figure 1-1 System Bus Interfaces

Note: Flash memories are encapsulated within the Flash Memory (FM) Module. Flash control is accomplished by the I/O to the FM over the peripheral bus, while reads and writes are completed between the core and the Flash memories.

Note: The primary data RAM port is 32 bits wide. Other data ports are 16 bits.

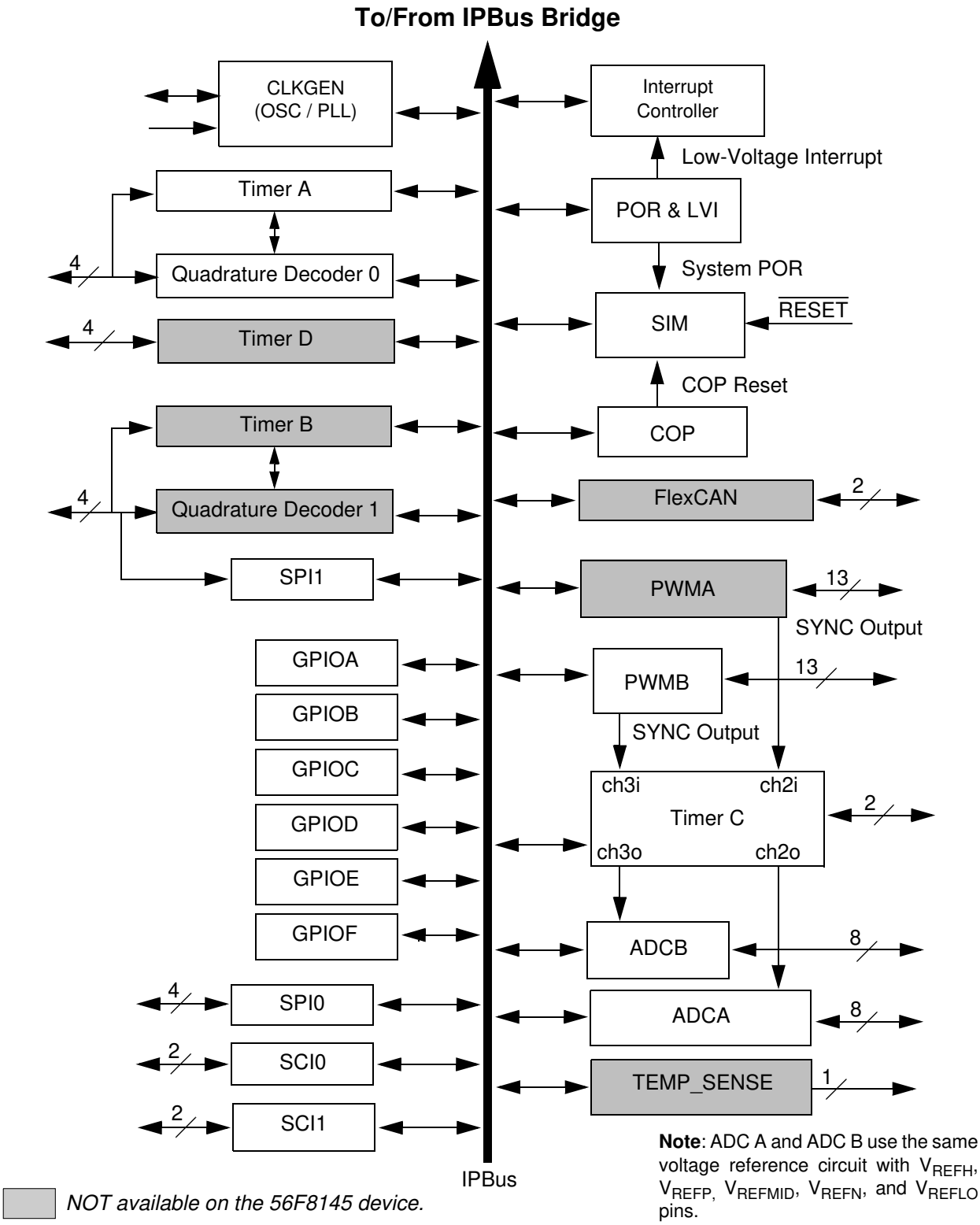


Figure 1-2 Peripheral Subsystem

Table 1-2 Bus Signal Names

Name	Function
Program Memory Interface	
pdb_m[15:0]	Program data bus for instruction word fetches or read operations.
cdbw[15:0]	Primary core data bus used for program memory writes. (Only these 16 bits of the cdbw[31:0] bus are used for writes to program memory.)
pab[20:0]	Program memory address bus. Data is returned on pdb_m bus.
Primary Data Memory Interface Bus	
cdbr_m[31:0]	Primary core data bus for memory reads. Addressed via xab1 bus.
cdbw[31:0]	Primary core data bus for memory writes. Addressed via xab1 bus.
xab1[23:0]	Primary data address bus. Capable of addressing bytes[1], words, and long data types. Data is written on cdbw and returned on cdbr_m. Also used to access memory-mapped I/O.
Secondary Data Memory Interface	
xdb2_m[15:0]	Secondary data bus used for secondary data address bus xab2 in the dual memory reads.
xab2[23:0]	Secondary data address bus used for the second of two simultaneous accesses. Capable of addressing only words. Data is returned on xdb2_m.
Peripheral Interface Bus	
IPBus [15:0]	Peripheral bus accesses all on-chip peripherals registers. This bus operates at the same clock rate as the Primary Data Memory and therefore generates no delays when accessing the processor. Write data is obtained from cdbw. Read data is provided to cdbr_m.

1. Byte accesses can only occur in the bottom half of the memory address space. The MSB of the address will be forced to 0.

1.5 Product Documentation

The documents listed in **Table 1-3** are required for a complete description and proper design with the 56F8345 and 56F8145 devices. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at **http://www.freescale.com**.

Table 1-3 Chip Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, 16-bit controller core processor, and the instruction set	DSP56800EERM
56F8300 Peripheral User Manual	Detailed description of peripherals of the 56F8300 family of devices	MC56F8300UM
56F8300 SCI/CAN Bootloader User Manual	Detailed description of the SCI/CAN Bootloaders 56F8300 family of devices	MC56F83xxBLUM
56F8345/56F8145 Technical Data Sheet	Electrical and timing specifications, pin descriptions, device specific peripheral information and package descriptions (this document)	MC56F8345
Errata	Details any chip issues that might be present	MC56F8345E MC56F8145E

1.6 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
"asserted"	A high true (active high) signal is high or a low true (active low) signal is low.
"deasserted"	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:

Signal/Symbol	Logic State	Signal State	Voltage[1]
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the 56F8345 and 56F8145 are organized into functional groups, as detailed in **Table 2-1** and as illustrated in **Figure 2-1**. In **Table 2-2**, each table row describes the signal or signals present on a pin.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins in Package	
	56F8345	56F8145
Power (V_{DD} or V_{DDA})	9	9
Power Option Control	1	1
Ground (V_{SS} or V_{SSA})	6	6
Supply Capacitors[1] & V_{PP}	6	6
PLL and Clock	4	4
Bus Control	6	6
Interrupt and Program Control	4	4
Pulse Width Modulator (PWM) Ports	26	13
Serial Peripheral Interface (SPI) Port 0	4	4
Serial Peripheral Interface (SPI) Port 1	—	4
Quadrature Decoder Port 0[2]	4	4
Quadrature Decoder Port 1[3]	4	—
Serial Communications Interface (SCI) Ports	4	4
CAN Ports	2	—
Analog-to-Digital Converter (ADC) Ports	21	21
Timer Module Ports	6	4
JTAG/Enhanced On-Chip Emulation (EOnCE)	5	5
Temperature Sense	1	—
Dedicated GPIO (Address Bus = 11; Data Bus = 4[4])	28	28

1. If the on-chip regulator is disabled, the V_{CAP} pins serve as 2.5V V_{DD_CORE} power inputs
2. Alternately, can function as Quad Timer pins or GPIO
3. Pins in this section can function as Quad Timer, SPI 1, orGPIO
4. EMI not functional in these packages; use as GPIO pins.

Note: See **Table 1-1** for 56F8145 functional differences.

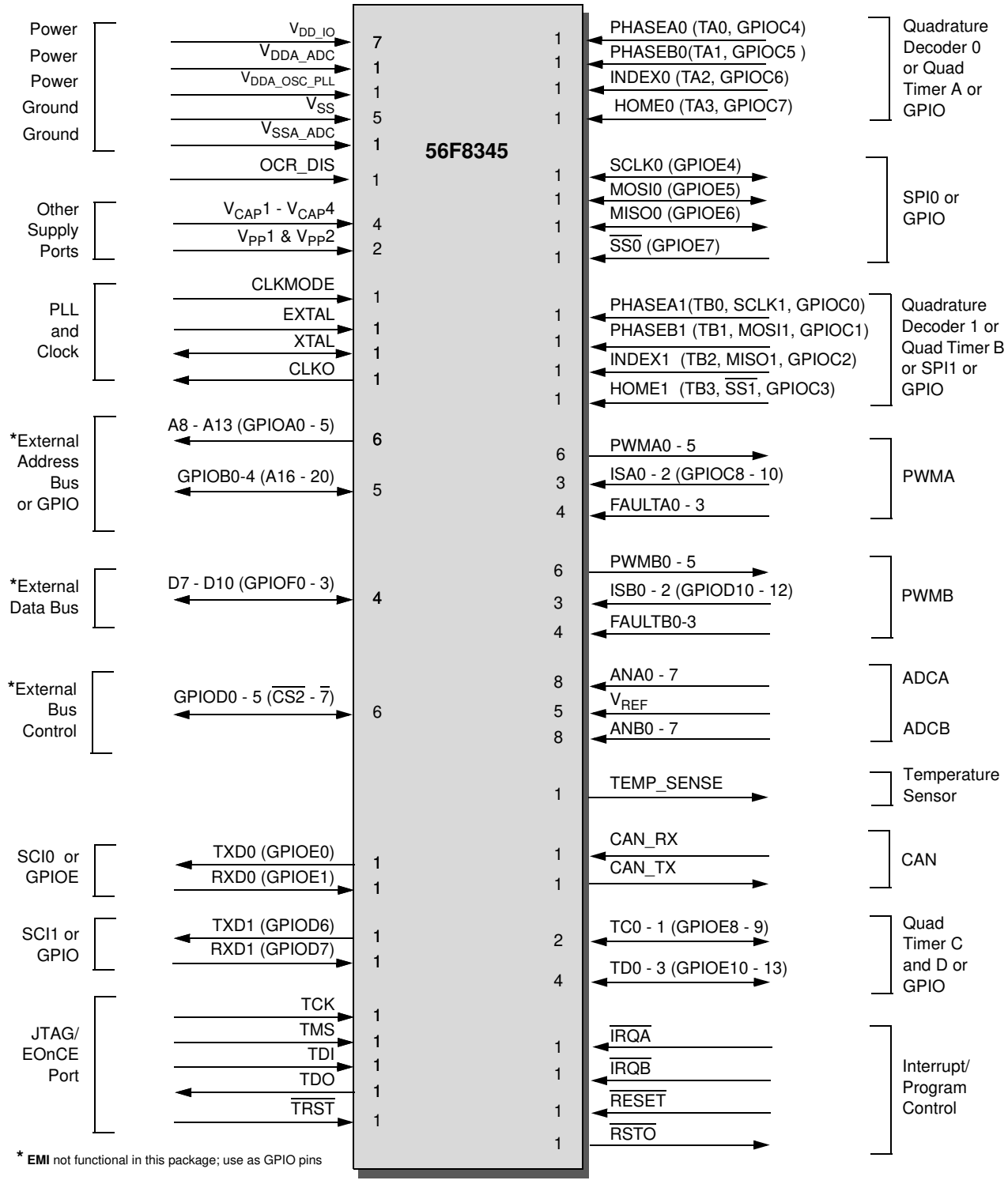


Figure 2-1 56F8345 Signals Identified by Functional Group[1] (128-Pin LQFP)

1. Alternate pin functionality is shown in parenthesis; pin direction/type shown is the default functionality.

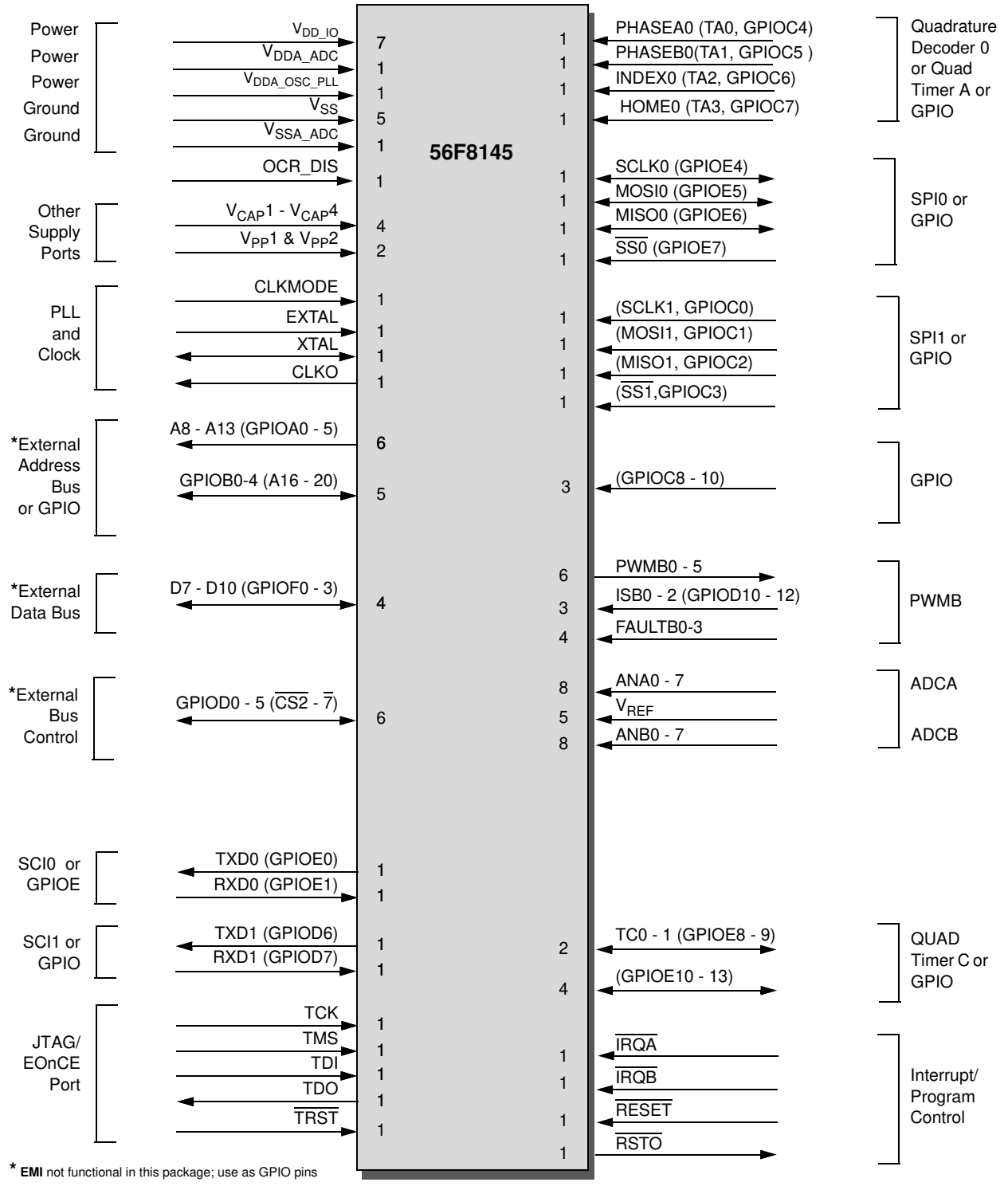


Figure 2-2 56F8145 Signals Identified by Functional Group[1] (128-Pin LQFP)

1. Alternate pin functionality is shown in parenthesis; pin direction/type shown is the default functionality.

2.2 Signal Pins

After reset, each pin is configured for its primary function (listed first). Any alternate functionality must be programmed.

EMI is not functional in this package; since only part of the address/data bus is bonded out, use as GPIO pins.

Note: *Signals in italics are NOT available in the 56F8145 device.*

If the "State During Reset" lists more than one state for a pin, the first state is the actual reset state. Other states show the reset condition of the alternate function, which you get if the alternate pin function is selected without changing the configuration of the alternate peripheral. For example, the A8/GPIOA0 pin shows that it is tri-stated during reset. If the GPIOA_PER is changed to select the GPIO function of the pin, it will become an input if no other registers are changed.

Table 2-2 Signal and Package Information for the 128-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
V_{DD_IO}	4	Supply		**I/O Power** — This pin supplies 3.3V power to the chip I/O interface and also the Processor core throught the on-chip voltage regulator, if it is enabled.
V_{DD_IO}	14			
V_{DD_IO}	25			
V_{DD_IO}	36			
V_{DD_IO}	62			
V_{DD_IO}	76			
V_{DD_IO}	112			
V_{DDA_ADC}	94	Supply		**ADC Power** — This pin supplies 3.3V power to the ADC modules. It must be connected to a clean analog power supply.
$V_{DDA\_OSC\_PLL}$	72	Supply		**Oscillator** and **PLL Power** — This pin supplies 3.3V power to the OSC and to the internal regulator that in turn supplies the Phase Locked Loop. It must be connected to a clean analog power supply.
V_{SS}	3	Supply		**Ground** — These pins provide ground for chip logic and I/O drivers.
V_{SS}	21			
V_{SS}	35			
V_{SS}	59			
V_{SS}	65			

Table 2-2 Signal and Package Information for the 128-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
V_{SSA_ADC}	95	Supply		**ADC Analog Ground** — This pin supplies an analog ground to the ADC modules.
OCR_DIS	71	Input	Input	**On-Chip Regulator Disable** — Tie this pin to V_{SS} to enable the on-chip regulator Tie this pin to V_{DD} to disable the on-chip regulator **This pin is intended to be a static DC signal from power-up to shut down. Do not try to toggle this pin for power savings during operation.**
$V_{CAP}1$	49	Supply	Supply	**$V_{CAP}1$ - 4** — When OCR_DIS is tied to V_{SS} (regulator enabled), connect each pin to a 2.2µF or greater bypass capacitor in order to bypass the core logic voltage regulator, required for proper chip operation. When OCR_DIS is tied to V_{DD} (regulator disabled), these pins become V_{DD_CORE} and should be connected to a regulated 2.5V power supply. **Note: This bypass is required even if the chip is powered with an external supply.**
$V_{CAP}2$	122			
$V_{CAP}3$	75			
$V_{CAP}4$	13			
$V_{PP}1$	119	Input	Input	**$V_{PP}1$ - 2** — These pins should be left unconnected as an open circuit for normal functionality.
$V_{PP}2$	5			
CLKMODE	79	Input	Input	**Clock Input Mode Selection** — This input determines the function of the XTAL and EXTAL pins. 1 = External clock input on XTAL is used to directly drive the input clock of the chip. The EXTAL pin should be grounded. 0 = A crystal or ceramic resonator should be connected between XTAL and EXTAL.
EXTAL	74	Input	Input	**External Crystal Oscillator Input** — This input can be connected to an 8MHz external crystal. Tie this pin low if XTAL is driven by an external clock source.
XTAL	73	Input/ Output	Chip-driven	**Crystal Oscillator Output** — This output connects the internal crystal oscillator output to an external crystal. If an external clock is used, XTAL must be used as the input and EXTAL connected to GND. The input clock can be selected to provide the clock directly to the core. This input clock can also be selected as the input clock for the on-chip PLL.

Table 2-2 Signal and Package Information for the 128-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
CLKO	6	Output	In reset, output is disabled	**Clock Output** — This pin outputs a buffered clock signal. Using the SIM CLKO Select Register (SIM_CLKOSR), this pin can be programmed as any of the following: disabled, CLK_MSTR (system clock), IPBus clock, oscillator output, prescaler clock and postscaler clock. Other signals are also available for test purposes. See **Part 6.5.7** for details.
A8 **(GPIOA0)**	15	Output Schmitt Input/ Output	In reset, output is disabled, pull-up is enabled	**Address Bus** — A8 - A13 specify six of the address lines for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A8 - A13 and EMI control signals are tri-stated when the external bus is inactive. **Port A GPIO** — These six GPIO pins can be individually programmed as input or output pins. After reset, these pins default to address bus functionality and must be programmed as GPIO. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOA_PUR register. Example: GPIOA0, clear bit 0 in the GPIOA_PUR register. **Note:** Primary function is not available in this package configuration; GPIO function must be used instead.
A9 (GPIOA1)	16			
A10 (GPIOA2)	17			
A11 (GPIOA3)	18			
A12 (GPIOA4)	19			
A13 (GPIOA5)	20			
GPIOB0 **(A16)**	27	Schmitt Input/ Output Output	Input, pull-up enabled	**Port B GPIO** — These four GPIO pins can be individually programmed as an input or output pin. **Address Bus** — A16 - A19 specify four of the address lines for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A16 - A19 and EMI control signals are tri-stated when the external bus is inactive. After reset, the default state is GPIO. To deactivate the internal pull-up resistor, clear bit 0 in the GPIOB_PUR register. Example: GPIOB1, clear bit 1 in the GPIOB_PUR register.
GPIOB1 **(A17)**	28			
GPIOB2 **(A18)**	29			
GPIOB3 **(A19)**	30			

Table 2-2 Signal and Package Information for the 128-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
GPIOB4	31	Schmitt Input/ Output	Input, pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(A20)		Output		**Address Bus** — A20 specifies one of the address lines for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A20 and EMI control signals are tri-stated when the external bus is inactive.
(prescaler_ clock)		Output		**Clock Output** — can be used to monitor the prescaler_clock on GPIOB4. After reset, the default state is GPIO. This pin can also be used to view the prescaler_clock. In these cases, the GPIOB_PER can be used to disable the GPIO. The CLKOSR register in the SIM can then be used to choose between address and clock functions; see **Part 6.5.7** for details. To deactivate the internal pull-up resistor, clear bit 4 in the GPIOB_PUR register.
D7	22	Input/ Output	In reset, output is disabled, pull-up is enabled	**Data Bus** — D7 - D10 specify part of the data for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), D7 - D10 are tri-stated when the external bus is inactive
(GPIOF0)		Input/ Output		**Port F GPIO** — These four GPIO pins can be individually programmed as input or output pins. After reset, these pins default to data bus functionality and should be programmed as GPIO. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOF_PUR register. Example: GPIOF0, clear bit 0 in the GPIOF_PUR register. **Note:** Primary function is not available in this package configuration; GPIO function must be used instead.
D8 (GPIOF1)	23			
D9 (GPIOF2)	24			
D10 (GPIOF3)	26			

Table 2-2 Signal and Package Information for the 128-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
GPIOD0 **($\overline{CS2}$)**	42	Input/ Output Output	Input, pull-up enabled	**Port D GPIO** — These six GPIO pins can be individually programmed as input or output pins. **Chip Select** — $\overline{CS2}$ - $\overline{CS7}$ may be programmed within the EMI module to act as chip selects for specific areas of the external memory map. Depending upon the state of the DRV bit in the EMI bus control register (BCR), $\overline{CS2}$ - $\overline{CS7}$ are tri-stated when the external bus is inactive. After reset, these pins are configured as GPIO. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOD_PUR register. Example: GPIOD0, clear bit 0 in the GPIOD_PUR register.
GPIOD1 ($\overline{CS3}$)	43			
GPIOD2 ($\overline{CS4}$)	44			
GPIOD3 ($\overline{CS5}$)	45			
GPIOD4 ($\overline{CS6}$)	46			
GPIOD5 ($\overline{CS7}$)	47			
TXD0 **(GPIOE0)**	7	Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Transmit Data** — SCI0 transmit data output **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCI output. To deactivate the internal pull-up resistor, clear bit 0 in the GPIOE_PUR register.
RXD0 **(GPIOE1)**	8	Input Input/ Output	Input, pull-up enabled	**Receive Data** — SCI0 receive data input **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCI output. To deactivate the internal pull-up resistor, clear bit 1 in the GPIOE_PUR register.
TXD1 **(GPIOD6)**	40	Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Transmit Data** — SCI1 transmit data output **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCI output. To deactivate the internal pull-up resistor, clear bit 6 in the GPIOD_PUR register.

Table 2-2 Signal and Package Information for the 128-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
RXD1 **(GPIOD7)**	41	Input Input/ Output	Input, pull-up enabled	**Receive Data** — SCI1 receive data input **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCI input. To deactivate the internal pull-up resistor, clear bit 7 in the GPIOD_PUR register.
TCK	115	Schmitt Input	Input, pulled low internally	**Test Clock Input** — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pull-down resistor.
TMS	116	Schmitt Input	Input, pulled high internally	**Test Mode Select Input** — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. To deactivate the internal pull-up resistor, set the JTAG bit in the SIM_PUDR register. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
TDI	117	Schmitt Input	Input, pulled high internally	**Test Data Input** — This input pin provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. To deactivate the internal pull-up resistor, set the JTAG bit in the SIM_PUDR register.
TDO	118	Output	In reset, output is disabled, pull-up is enabled	**Test Data Output** — This tri-stateable output pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and changes on the falling edge of TCK.