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56F8347/56F8147

Data Sheet

Preliminary Technical Data

56F8300
16-bit Digital Signal Controllers

MC56F8347
Rev.11
01/2007

freescale.com

Document Revision History

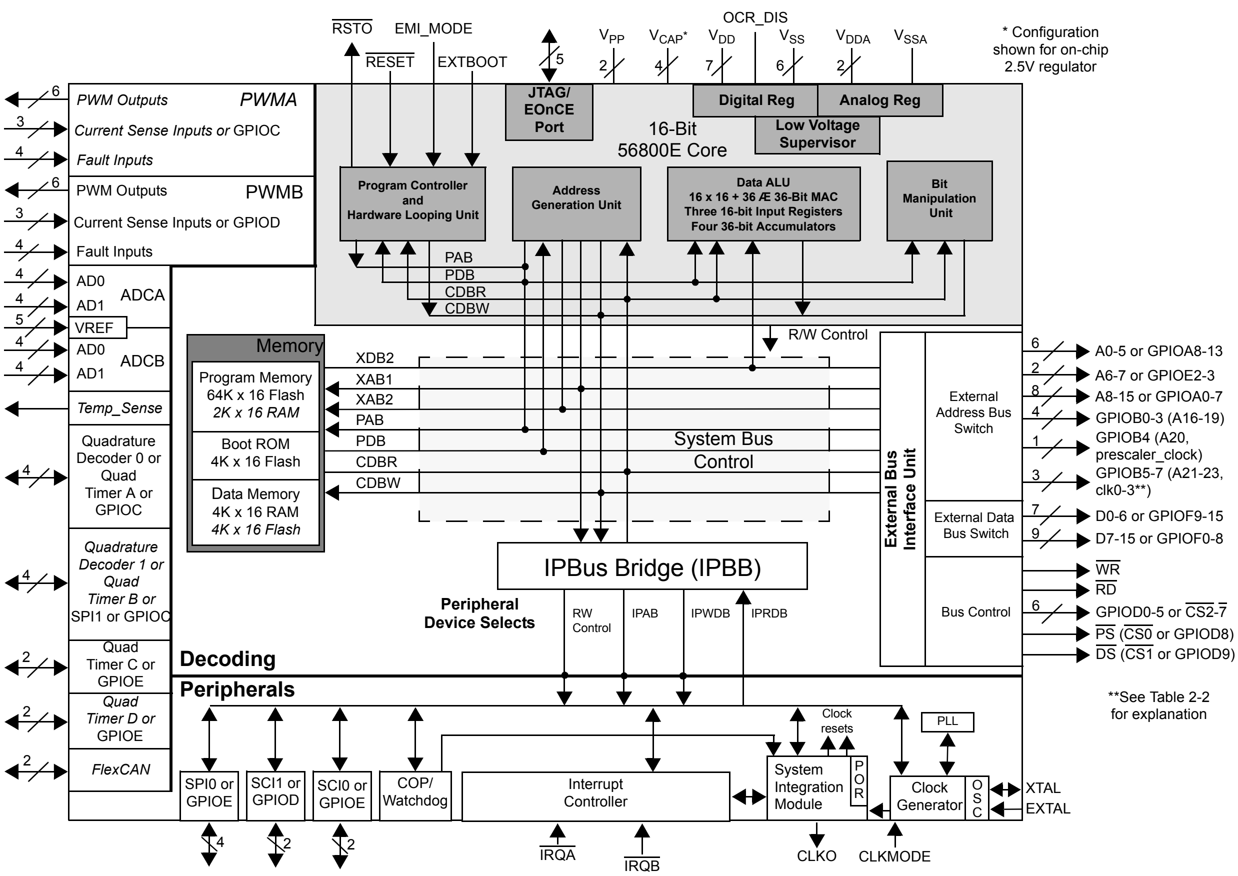
Version History	Description of Change
Rev 0	Initial release
Rev 1.0	Fixed typos in Section 1.1.3, Replace any reference to Flash Interface Unit with Flash Module, corrected pin number for D14 in **Table 2-2**, added note to Vcap pin in **Table 2-2**, corrected thermal numbers for 160 LQFP in **Table 10-4**,removed unneccessary notes in **Table 10-13**; corrected temperature range in **Table 10-14**; added ADC calibration information to **Table 10-24** and new graphs in **Figure 10-22**.
Rev 2.0	Clarification to **Table 10-23**, corrected Digital Input Current Low (pull-up enabled) numbers in **Table 10-5**. Removed text and Table 10-2; replaced with note to **Table 10-1**.
Rev 3.0	Added 56F8147 information; edited to indicate differences in 56F8347 and 56F8147. Reformatted for Freescale look and feel. Updated Temperature Sensor and ADC tables, then updaated balance of electrical tables for consistency throughout the family. Clarified I/O power description in **Table 2-2**, added note to **Table 10-7** and clarified **Section 12.3**.
Rev 4.0	Correcting **Figure 4-1** Boot Flash Start = $02_0000
Rev 5.0	Added output voltage maximum value and note to clarify in **Table 10-1**; also removed overall life expectancy note, since life expectancy is dependent on customer usage and must be determined by reliability engineering. Clarified value and unit measure for Maximum allowed P_D in **Table 10-3**. Corrected note about average value for Flash Data Retention in **Table 10-4**. Added new RoHS-compliant orderable part numbers in **Table 13-1**.
Rev 6.0	Added 160MAPBGA information, TA equation updated in **Table 10-4** and additional minor edits throughout data sheet
Rev 7.0	Updated **Table 10-24** to reflect new value for maximum Uncalibrated Gain Error
Rev 8.0	Deleted formula for Max Ambient Operating Temperature (Automotive) and Max Ambient Operating Temperature (Industrial) and corrected Flash Endurance to 10,000 in **Table 10-4**. Added RoHS-compliance and “pb-free” language to back cover.
Rev 9.0	Corrected **Section 6.4** title (from Operation Mode Register to Operating Mode Register). Updated JTAG ID in **Section 6.5.4**. Added information/corrected state during reset in **Table 2-2**. Clarified external reference crystal frequency for PLL in **Table 10-14** by increasing maximum value to 8.4MHz.
Rev 10.0	Replaced “Tri-stated” with an explanation in State During Reset column in **Table 2-2**.
Rev. 11	• Added the following note to the description of the TMS signal in **Table 2-2**: **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor. • Added the following note to the description of the $\overline{TRST}$ signal in **Table 2-2**: **Note:** For normal operation, connect $\overline{TRST}$ directly to V_{SS}. If the design is to be used in a debugging environment, $\overline{TRST}$ may be tied to V_{SS} through a 1K resistor.

Please see http://www.freescale.com for the most current data sheet revision.

56F8347/56F8147 General Description

Note: *Features in italics are NOT available in the 56F8147 device.*

- Up to 60 MIPS at 60MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- Access up to 4MB of off-chip program and 32MB of data memory
- Chip Select Logic for glueless interface to ROM and SRAM
- 128KB of Program Flash
- *4KB of Program RAM*
- *8KB of Data Flash*
- 8KB of Data RAM
- 8KB of Boot Flash
- Up to two 6-channel PWM modules
- Four 4-channel, 12-bit ADCs
- *Temperature Sensor*
- Up to two Quadrature Decoders
- *FlexCAN module*
- Two Serial Communication Interfaces (SCIs)
- Up to two Serial Peripheral Interfaces (SPIs)
- Up to four general-purpose Quad Timers
- Computer Operating Properly (COP) / Watchdog
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Up to 76 GPIO lines
- 160-pin LQFP Package and *160MAPBGA*



56F8347/56F8147 Block Diagram

Table of Contents

Part 1 Overview

1.1 56F8347/56F8147 Features

1.1.1 Core

- Efficient 16-bit 56800E family controller engine with dual Harvard architecture
- Up to 60 Million Instructions Per Second (MIPS) at 60 MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- Arithmetic and logic multi-bit shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses
- Four internal data buses
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/EOnCE debug programming interface

1.1.2 Differences Between Devices

Table 1-1 outlines the key differences between the 56F8347 and 56F8147 devices.

Table 1-1 Device Differences

Feature	56F8347	56F8147
Guaranteed Speed	60MHz/60 MIPS	40MHZ/40MIPS
Program RAM	4KB	Not Available
Data Flash	8KB	Not Available
PWM	2 x 6	1 x 6
CAN	1	Not Available
Quad Timer	4	2
Quadrature Decoder	2 x 4	1 x 4
Temperature Sensor	1	Not Available
Dedicated GPIO	—	7

1.1.3 Memory

Note: *Features in italics are NOT available in the 56F8147 device.*

- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Flash security protection feature
- On-chip memory, including a low-cost, high-volume Flash solution
  - 128KB of Program Flash
  - *4KB of Program RAM*
  - *8KB of Data Flash*
  - 8KB of Data RAM
  - 8KB of Boot Flash
- Off-chip memory expansion capabilities provide a simple method for interfacing additional external memory and/or peripheral devices
  - Access up to 4MB of external program memory or 32MB of external data memory
  - External accesses supported at up to 60MHz (zero wait states)
- *EEPROM emulation capability*

1.1.4 Peripheral Circuits

Note: *Features in italics are NOT available in the 56F8147 device.*

- Pulse Width Modulator:
  - In the 56F8347, two Pulse Width Modulator modules, each with six PWM outputs, three Current Sense inputs, and three Fault inputs; fault-tolerant design with dead time insertion; supports both center-aligned and edge-aligned modes
  - In the 56F8147, one Pulse Width Modulator module, with six PWM outputs, three Current Sense inputs, and three Fault inputs; fault-tolerant design with dead time insertion; supports both center-aligned and edge-aligned modes
- Four 12-bit, Analog-to-Digital Converters (ADCs), which support four simultaneous conversions with quad, 4-pin multiplexed inputs; ADC and PWM modules can be synchronized through Timer C, channels 2 and 3
- Quadrature Decoder:
  - In the 56F8347, two four-input Quadrature Decoders or two additional Quad Timers
  - In the 56F8147, one four-input Quadrature Decoder, which works in conjunction with Quad Timer A
- *Temperature Sensor diode can be connected, on the board, to any of the ADC inputs to monitor the on-chip temperature*
- Quad Timer:
  - In the 56F8347, four dedicated general-purpose Quad Timers totaling six dedicated pins: Timer C with two pins and Timer D with four pins
  - In the 56F8147, two general-purpose Quad Timers; Timer A works in conjunction with Quadrature Decoder 0 or GPIO and Timer C works in conjunction with GPIO
- *FlexCAN (CAN Version 2.0 B-compliant) module with 2-pin port for transmit and receive*

- Two Serial Communication Interfaces (SCIs), each with two pins (or four additional GPIO lines)
- Up to two Serial Peripheral Interfaces (SPIs), both with configurable 4-pin port (or eight additional GPIO lines)
  - — In the 56F8347, SPI1 can also be used as Quadrature Decoder 1 or Quad Timer B
  - — In the 56F8147, SPI1 can alternately be used only as GPIO
- Computer Operating Properly (COP) / Watchdog timer
- Two dedicated external interrupt pins
- Up to 76 General Purpose I/O (GPIO) pins
- External reset input pin for hardware reset
- External reset output pin for system reset
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, processor speed-independent, real-time debugging
- Software-programmable, Phase Lock Loop (PLL)-based frequency synthesizer for the core clock

1.1.5 Energy Information

- Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
- On-board 3.3V down to 2.6V voltage regulator for powering internal logic and memories; can be disabled
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available
- ADC smart power management
- Each peripheral can be individually disabled to save power

1.2 Device Description

The 56F8347 and 56F8147 are members of the 56800E core-based family of controllers. Each combines, on a single chip, the processing power of a Digital Signal Processor (DSP) and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56F8347 and 56F8147 are well-suited for many applications. The device includes many peripherals that are especially useful for motion control, smart appliances, steppers, encoders, tachometers, limit switches, power supply and control, *automotive* control (56F8347 only), engine management, noise suppression, remote utility metering, industrial control for power, lighting, and automation applications.

The 56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C/C++ Compilers to enable rapid development of optimized control applications.

The 56F8347 and 56F8147 support program execution from internal or external memories. Two data operands can be accessed from the on-chip data RAM per instruction cycle. These devices also provide two external dedicated interrupt lines and up to 76 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

1.2.1 56F8347 Features

The 56F8347 controller includes 128KB of Program Flash and 8KB of Data Flash (each programmable through the JTAG port) with 4KB of Program RAM and 8KB of Data RAM. It also supports program execution from external memory.

A total of 8KB of Boot Flash is incorporated for easy customer inclusion of field-programmable software routines that can be used to program the main Program and Data Flash memory areas. Both Program and Data Flash memories can be independently bulk erased or erased in pages. Program Flash page erase size is 1KB. Boot and Data Flash page erase size is 512 bytes. The Boot Flash memory can also be either bulk or page erased.

A key application-specific feature of the 56F8347 is the inclusion of two Pulse Width Modulator (PWM) modules. These modules each incorporate three complementary, individually programmable PWM signal output pairs (each module is also capable of supporting six independent PWM functions, for a total of 12 PWM outputs) to enhance motor control functionality. Complementary operation permits programmable dead time insertion, distortion correction via current sensing by software, and separate top and bottom output polarity control. The up-counter value is programmable to support a continuously variable PWM frequency. Edge-aligned and center-aligned synchronous pulse width control (0% to 100% modulation) is supported. The device is capable of controlling most motor types: ACIM (AC Induction Motors); both BDC and BLDC (Brush and Brushless DC motors); SRM and VRM (Switched and Variable Reluctance Motors); and stepper motors. The PWMs incorporate fault protection and cycle-by-cycle current limiting with sufficient output drive capability to directly drive standard optoisolators. A “smoke-inhibit”, write-once protection feature for key parameters is also included. A patented PWM waveform distortion correction circuit is also provided. Each PWM is double-buffered and includes interrupt controls to permit integral reload rates to be programmable from 1 to 16. The PWM modules provide reference outputs to synchronize the Analog-to-Digital Converters through two channels of Quad Timer C.

The 56F8347 incorporates two Quadrature Decoders capable of capturing all four transitions on the two-phase inputs, permitting generation of a number proportional to actual position. Speed computation capabilities accommodate both fast- and slow-moving shafts. An integrated watchdog timer in the Quadrature Decoder can be programmed with a time-out value to alert when no shaft motion is detected. Each input is filtered to ensure only true transitions are recorded.

This controller also provides a full set of standard programmable peripherals that include two Serial Communications Interfaces (SCIs); two Serial Peripheral Interfaces (SPIs); and four Quad Timers. Any of these interfaces can be used as General Purpose Input/Outputs (GPIOs) if that function is not required. A Flex Controller Area Network (FlexCAN) interface (CAN Version 2.0 B-compliant) and an internal interrupt controller are a part of the 56F8347.

1.2.2 56F8147 Features

The 56F8147 controller includes 128KB of Program Flash, programmable through the JTAG port, with 8KB of Data RAM. It also supports program execution from external memory.

A total of 8KB of Boot Flash is incorporated for easy customer inclusion of field-programmable software routines that can be used to program the main Program Flash memory area, which can be independently bulk erased or erased in pages. Program Flash page erase size is 1KB. Boot Flash page erase size is 512 bytes and the Boot Flash memory can also be either bulk or page erased.

A key application-specific feature of the 56F8147 is the inclusion of one Pulse Width Modulator (PWM) module. This module incorporates three complementary, individually programmable PWM signal output pairs and can also support six independent PWM functions to enhance motor control functionality. Complementary operation permits programmable dead time insertion, distortion correction via current sensing by software, and separate top and bottom output polarity control. The up-counter value is programmable to support a continuously variable PWM frequency. Edge-aligned and center-aligned synchronous pulse width control (0% to 100% modulation) is supported. The device is capable of controlling most motor types: ACIM (AC Induction Motors); both BDC and BLDC (Brush and Brushless DC motors); SRM and VRM (Switched and Variable Reluctance Motors); and stepper motors. The PWM incorporates fault protection and cycle-by-cycle current limiting with sufficient output drive capability to directly drive standard optoisolators. A “smoke-inhibit”, write-once protection feature for key parameters is also included. A patented PWM waveform distortion correction circuit is also provided. Each PWM is double-buffered and includes interrupt controls to permit integral reload rates to be programmable from 1 to 16. The PWM module provides reference outputs to synchronize the Analog-to-Digital Converters through two channels of Quad Timer C.

The 56F8147 incorporates a Quadrature Decoder capable of capturing all four transitions on the two-phase inputs, permitting generation of a number proportional to actual position. Speed computation capabilities accommodate both fast- and slow-moving shafts. An integrated watchdog timer in the Quadrature Decoder can be programmed with a time-out value to alert when no shaft motion is detected. Each input is filtered to ensure only true transitions are recorded.

This controller also provides a full set of standard programmable peripherals that include two Serial Communications Interfaces (SCIs); two Serial Peripheral Interfaces (SPIs); and two Quad Timers. Any of these interfaces can be used as General Purpose Input/Outputs (GPIOs) if that function is not required. An internal interrupt controller is also a part of the 56F8147.

1.3 Award-Winning Development Environment

Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, CodeWarrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Architecture Block Diagram

Note: *Features in italics are NOT available in the 56F8147 device and are shaded in the following figures.*

The 56F8347/56F8147 architecture is shown in **Figure 1-1** and **Figure 1-2**. **Figure 1-1** illustrates how the 56800E system buses communicate with internal memories, the external memory interface and the IPBus Bridge. **Table 1-2** lists the internal buses in the 56800E architecture and provides a brief description of their function. **Figure 1-2** shows the peripherals and control blocks connected to the IPBus Bridge. The figures do not show the on-board regulator and power and ground signals. They also do not show the multiplexing between peripherals or the dedicated GPIOs. Please see **Part 2, Signal/Connection Descriptions,** to see which signals are multiplexed with those of other peripherals.

Also shown in **Figure 1-2** are connections between the PWM, Timer C and ADC blocks. These connections allow the PWM and/or Timer C to control the timing of the start of ADC conversions. The Timer C channel indicated can generate periodic start (SYNC) signals to the ADC to start its conversions. In another operating mode, the PWM load interrupt (SYNC output) signal is routed internally to the Timer C input channel as indicated. The timer can then be used to introduce a controllable delay before generating its output signal. The timer output then triggers the ADC. To fully understand this interaction, please see the **56F8300 Peripheral User's Manual** for clarification on the operation of all three of these peripherals.

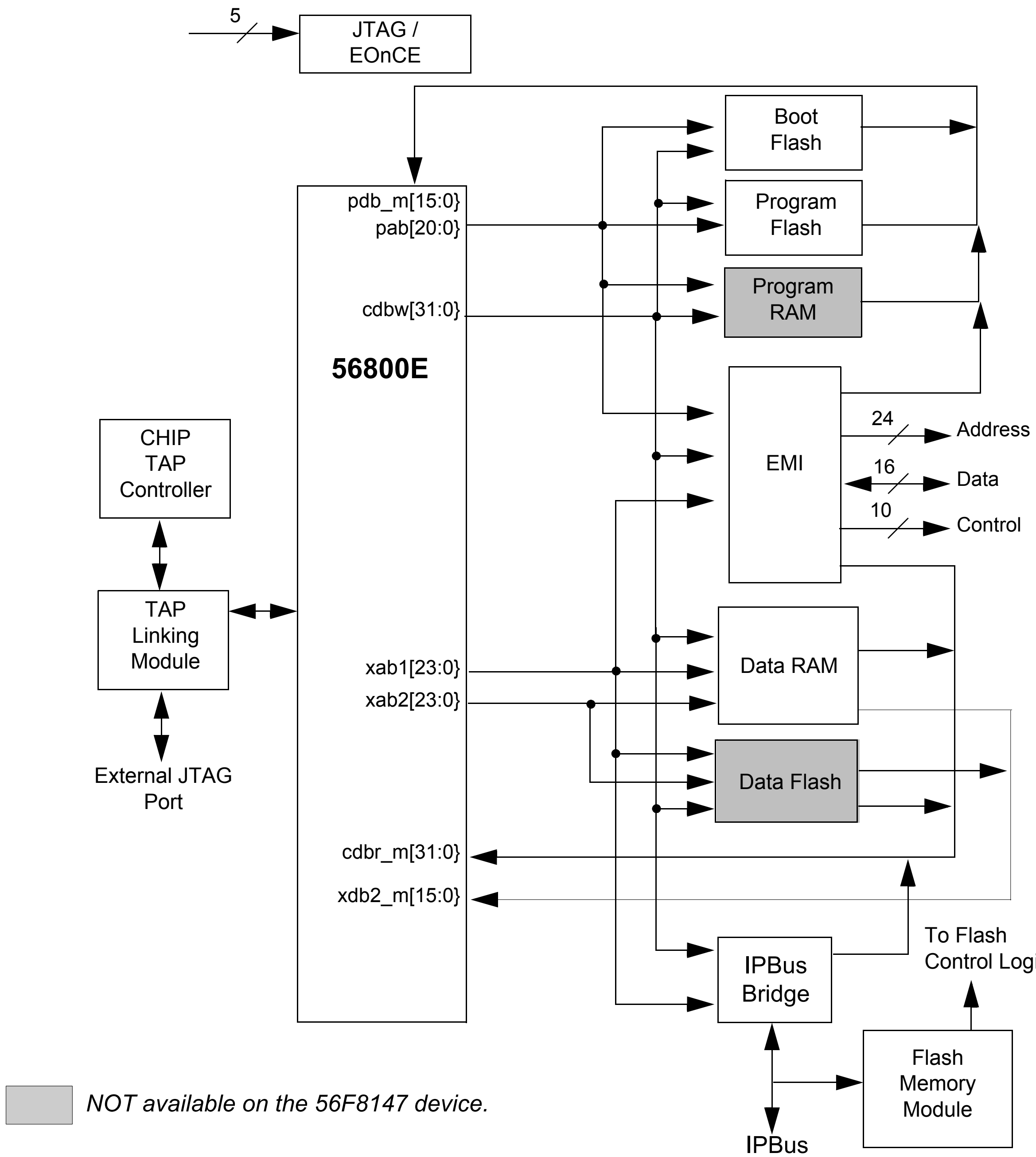


Figure 1-1 System Bus Interfaces

Note: Flash memories are encapsulated within the Flash Memory (FM) Module. Flash control is accomplished by the I/O to the FM over the peripheral bus, while reads and writes are completed between the core and the Flash memories.

Note: The primary data RAM port is 32 bits wide. Other data ports are 16 bits.

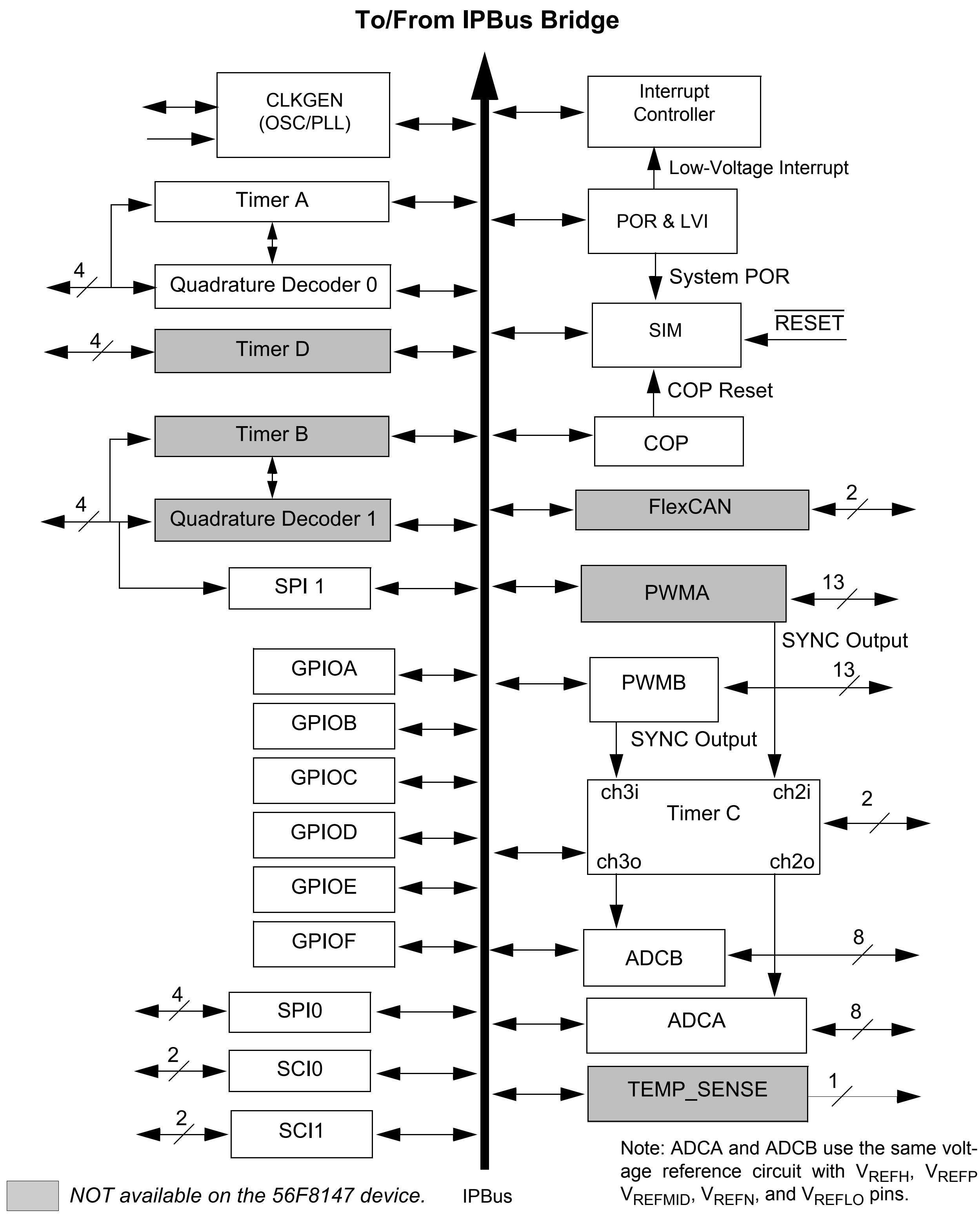


Figure 1-2 Peripheral Subsystem

Table 1-2 Bus Signal Names

Name	Function
Program Memory Interface	
pdb_m[15:0]	Program data bus for instruction word fetches or read operations.
cdbw[15:0]	Primary core data bus used for program memory writes. (Only these 16 bits of the cdbw[31:0] bus are used for writes to program memory.)
pab[20:0]	Program memory address bus. Data is returned on pdb_m bus.
Primary Data Memory Interface Bus	
cdbr_m[31:0]	Primary core data bus for memory reads. Addressed via xab1 bus.
cdbw[31:0]	Primary core data bus for memory writes. Addressed via xab1 bus.
xab1[23:0]	Primary data address bus. Capable of addressing bytes[1], words, and long data types. Data is written on cdbw and returned on cdbr_m. Also used to access memory-mapped I/O.
Secondary Data Memory Interface	
xdb2_m[15:0]	Secondary data bus used for secondary data address bus xab2 in the dual memory reads.
xab2[23:0]	Secondary data address bus used for the second of two simultaneous accesses. Capable of addressing only words. Data is returned on xdb2_m.
Peripheral Interface Bus	
IPBus [15:0]	Peripheral bus accesses all on-chip peripherals registers. This bus operates at the same clock rate as the Primary Data Memory and therefore generates no delays when accessing the processor. Write data is obtained from cdbw. Read data is provided to cdbr_m.

1. Byte accesses can only occur in the bottom half of the memory address space. The MSB of the address will be forced to 0.

1.5 Product Documentation

The documents in Table 1-3 are required for a complete description and proper design with the 56F8347 and 56F8147 devices. Documentation is available from local Freescale distributors, Freescale semiconductor sales offices, Freescale Literature Distribution Centers, or online at **http://www.freescale.com/dsp**.

Table 1-3 Chip Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, and 16-bit controller core processor and the instruction set	DSP56800ERM
56F8300 Peripheral User Manual	Detailed description of peripherals of the 56F8300 devices	MC56F8300UM
56F8300 SCI/CAN Bootloader User Manual	Detailed description of the SCI/CAN Bootloaders 56F8300 family of devices	MC56F83xxBLUM
56F8347/56F8147 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	MC56F8347
Errata	Details any chip issues that might be present	MC56F8347E MC56F8147E

1.6 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$ This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.

"asserted" A high true (active high) signal is high or a low true (active low) signal is low.

"deasserted" A high true (active high) signal is low or a low true (active low) signal is high.

Examples:

Signal/Symbol	Logic State	Signal State	Voltage[1]
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for VIL, VOL, VIH, and VOH are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the 56F8347 and 56F8147 are organized into functional groups, as detailed in Table 2-1 and as illustrated in Figure 2-2. In Table 2-2, each table row describes the signal or signals present on a pin.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins in Package	
	56F8347	56F8147
Power (V_{DD} or V_{DDA})	9	9
Power Option Control	1	1
Ground (V_{SS} or V_{SSA})	7	7
Supply Capacitors[1] & V_{PP}	6	6
PLL and Clock	4	4
Address Bus	24	24
Data Bus	16	16
Bus Control	10	10
Interrupt and Program Control	6	6
Pulse Width Modulator (PWM) Ports	26	13
Serial Peripheral Interface (SPI) Port 0	4	4
Serial Peripheral Interface (SPI) Port 1	—	4
Quadrature Decoder Port 0[2]	4	4
Quadrature Decoder Port 1[3]	4	—
Serial Communications Interface (SCI) Ports[2]	4	4
CAN Ports	2	—
Analog to Digital Converter (ADC) Ports	21	21
Timer Module Ports	6	2
JTAG/Enhanced On-Chip Emulation (EOnCE)	5	5
Temperature Sense	1	—
Dedicated GPIO	—	7

1. If the on-chip regulator is disabled, the V_{CAP} pins serve as 2.5V V_{DD_CORE} power inputs
2. Alternately, can function as Quad Timer pins
3. Pins in this section can function as Quad Timer, SPI #1, or GPIO

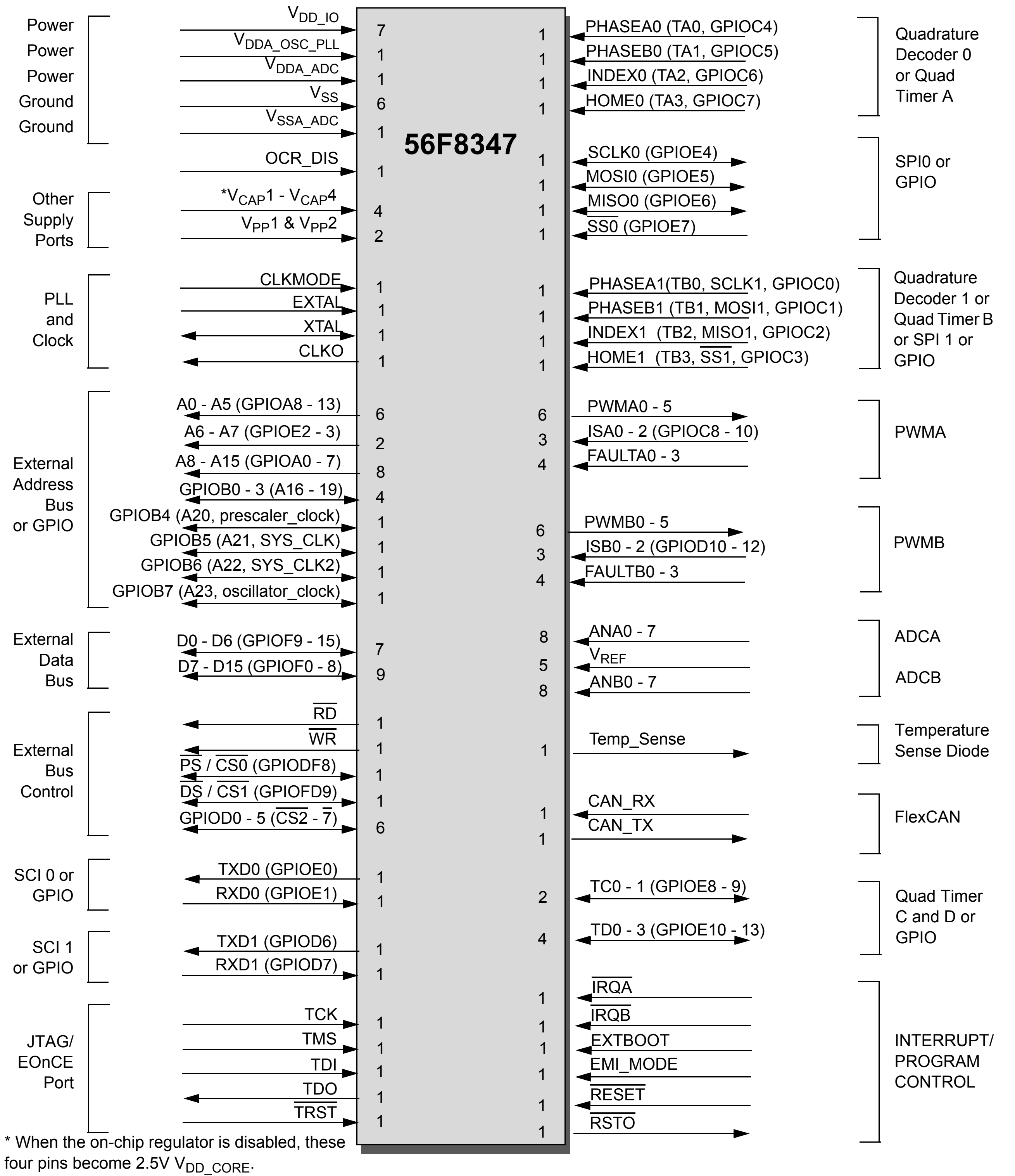
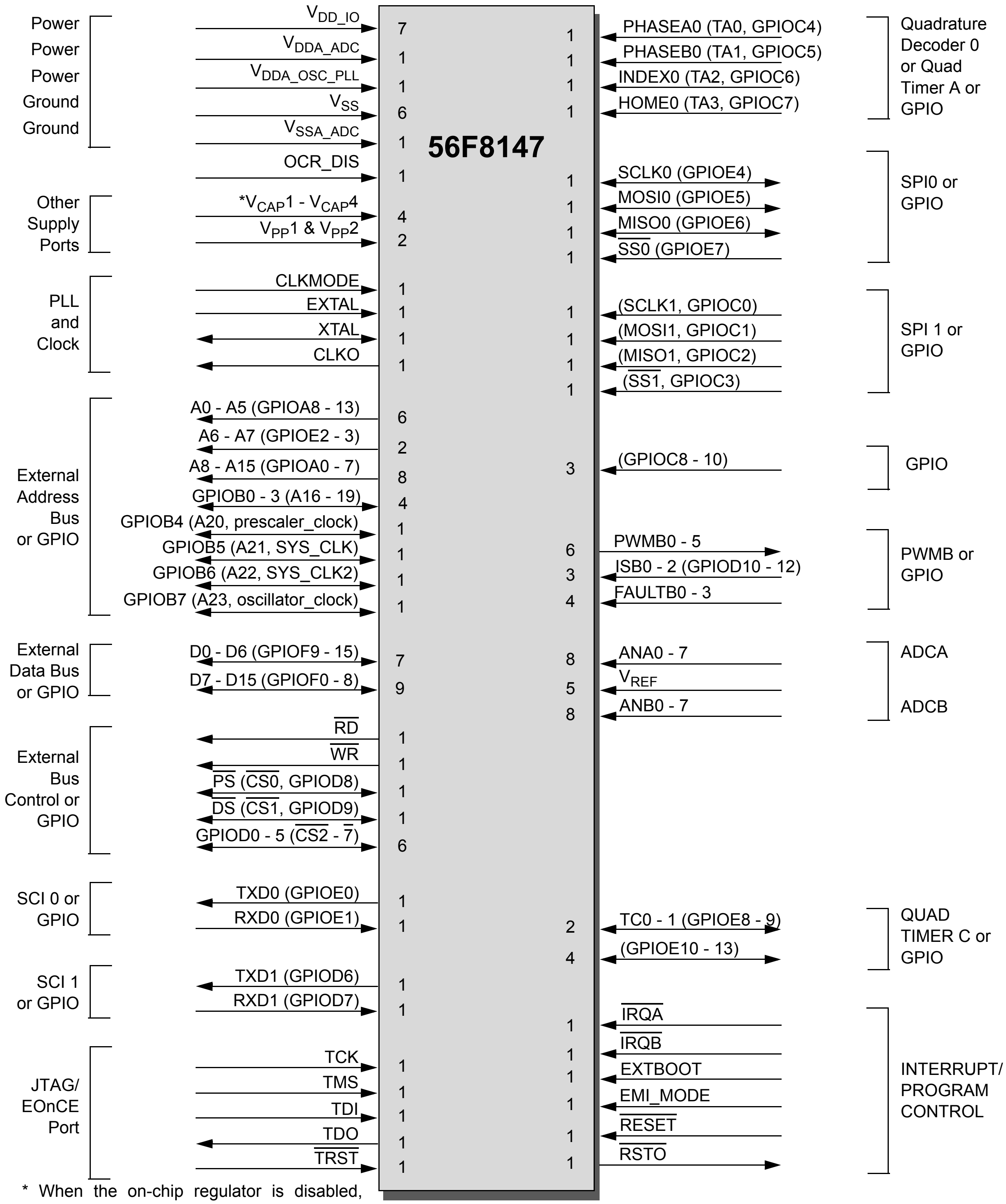


Figure 2-1 56F8347 Signals Identified by Functional Group[1] (160-pin LQFP)

1. Alternate pin functionality is shown in parenthesis; pin direction/type shown is the default functionality.



* When the on-chip regulator is disabled, these four pins become 2.5V V_{DD_CORE}.

Figure 2-2 56F8147 Signals Identified by Functional Group[1] (160-pin LQFP)

1. Alternate pin functionality is shown in parenthesis; pin direction/type shown is the default functionality.

2.2 Signal Pins

After reset, all pins are by default the primary function. Any alternate functionality must be programmed.

Note: *Signals in italics are NOT available in the 56F8147 device.*

If the "State During Reset" lists more than one state for a pin, the first state is the actual reset state. Other states show the reset condition of the alternate function, which you get if the alternate pin function is selected without changing the configuration of the alternate peripheral. For example, the A8/GPIOA0 pin shows that it is tri-stated during reset. If the GPIOA_PER is changed to select the GPIO function of the pin, it will become an input if no other registers are changed.

Note: LQFP Pin numbers and MBGA Ball numbers do not always correlate in **Table 2-2**. Please contact factory for exact correlation.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
V_{DD_IO}	1	F4	Supply		**I/O Power** — This pin supplies 3.3V power to the chip I/O interface and also the Processor core throught the on-chip voltage regulator, if it is enabled.
V_{DD_IO}	16	K5			
V_{DD_IO}	31	E5			
V_{DD_IO}	42	K7			
V_{DD_IO}	77	E9			
V_{DD_IO}	96	K10			
V_{DD_IO}	134	F11			
V_{DDA_ADC}	114	C14	Supply		**ADC Power** — This pin supplies 3.3V power to the ADC modules. It must be connected to a clean analog power supply.
$V_{DDA\_OSC\_PLL}$	92	K13	Supply		**Oscillator** and **PLL Power** — This pin supplies 3.3V power to the OSC and to the internal regulator that in turn supplies the Phase Locked Loop. It must be connected to a clean analog power supply.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
V_{SS}	27	J4	Supply		**V_{SS}** — These pins provide ground for chip logic and I/O drivers.
V_{SS}	41	K11			
V_{SS}	74	G11			
V_{SS}	80	E7			
V_{SS}	125	J11			
V_{SS}	160	E6			
V_{SSA_ADC}	115	D12	Supply		**ADC Analog Ground** — This pin supplies an analog ground to the ADC modules.
OCR_DIS	91	K14	Input	Input	**On-Chip Regulator Disable** — Tie this pin to V_{SS} to enable the on-chip regulator. Tie this pin to V_{DD} to disable the on-chip regulator. **This pin is intended to be a static DC signal from power-up to shut down. Do no try to toggle this pin for power savings during operation**.
V_{CAP}1*	62	K8	Supply	Supply	**V_{CAP}1 - 4** — When OCR_DIS is tied to V_{SS} (regulator enabled), connect each pin to a 2.2μF or greater bypass capacitor in order to bypass the core logic voltage regulator, required for proper chip operation. When OCR_DIS is tied to V_{DD} (regulator disabled), these pins become V_{DD_CORE} and should be connected to a regulated 2.5V power supply. **Note: This bypass is required even if the chip is powered with an external supply.**
V_{CAP}2*	144	E8			
V_{CAP}3*	95	H11			
V_{CAP}4*	15	G4			
* When the on-chip regulator is disabled, these four pins become 2.5V V_{DD_CORE}.					
V_{PP}1	141	A7	Input	Input	**V_{PP}1 - 2** — These pins should be left unconnected as an open circuit for normal functionality.
V_{PP}2	2	C2			
CLKMODE	99	H12	Input	Input	**Clock Input Mode Selection** — This input determines the function of the XTAL and EXTAL pins. 1 = External clock input on XTAL is used to directly drive the input clock of the chip. The EXTAL pin should be grounded. 0 = A crystal or ceramic resonator should be connected between XTAL and EXTAL.
EXTAL	94	J12	Input	Input	**External Crystal Oscillator Input** — This input can be connected to an 8MHz external crystal. Tie this pin low if XTAL is driven by an external clock source.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
XTAL	93	K12	Input/ Output	Chip-driven	**Crystal Oscillator Output** — This output connects the internal crystal oscillator output to an external crystal. If an external clock is used, XTAL must be used as the input and EXTAL connected to GND. The input clock can be selected to provide the clock directly to the core. This input clock can also be selected as the input clock for the on-chip PLL.
CLKO	3	D3	Output	In reset, output is disabled	**Clock Output** — This pin outputs a buffered clock signal. Using the SIM CLKO Select Register (SIM_CLKOSR), this pin can be programmed as any of the following: disabled, CLK_MSTR (system clock), IPBus clock, oscillator output, prescaler clock and postscaler clock. Other signals are also available for test purposes. See Part 6.5.7 for details.
A0 **(GPIOA8)**	154	C3	Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Address Bus** — A0 - A5 specify six of the address lines for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A0 - A5 and EMI control signals are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. **Port A GPIO** — These six GPIO pins can be individually programmed as input or output pins. After reset, the default state is Address Bus. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOA_PUR register. Example: GPIOA8, clear bit 8 in the GPIOA_PUR register.
A1 (GPIOA9)	10	E3			
A2 (GPIOA10)	11	E4			
A3 (GPIOA11)	12	F2			
A4 (GPIOA12)	13	F1			
A5 (GPIOA13)	14	F3			

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
A6 **(GPIOE2)**	17	G1	Output Schmitt Input/ Output	In reset, output is disabled, pull-up is enabled	**Address Bus** — A6 - A7 specify two of the address lines for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A6 - A7 and EMI control signals are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. **Port E GPIO** — These two GPIO pins can be individually programmed as input or output pins. After reset, the default state is Address Bus. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOE_PUR register. Example: GPIOE2, clear bit 2 in the GPIOE_PUR register.
A7 **(GPIOE3)**	18	G3			
A8 **(GPIOA0)**	19	G2	Output Schmitt Input/ Output	In reset, output is disabled, pull-up is enabled	**Address Bus**— A8 - A15 specify eight of the address lines for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A8 - A15 and EMI control signals are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. **Port A GPIO** — These eight GPIO pins can be individually programmed as input or output pins. After reset, the default state is Address Bus. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOA_PUR register. Example: GPIOA0, clear bit 0 in the GPIOA_PUR register.
A9 **(GPIOA1)**	20	H1			
A10 **(GPIOA2)**	21	H2			
A11 **(GPIOA3)**	22	H4			
A12 **(GPIOA4)**	23	H3			
A13 **(GPIOA5)**	24	J1			
A14 **(GPIOA6)**	25	J2			
A15 **(GPIOA7)**	26	J3			

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
GPIOB0	33	L1	Schmitt Input/ Output	Input, pull-up enabled	**Port B GPIO** — These four GPIO pins can be programmed as input or output pins.
(A16)			Output		**Address Bus** — A16 - A19 specify one of the address lines for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A16 - A19 and EMI control signals are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. After reset, the startup state of GPIOB0 - GPIOB3 (GPIO or address) is determined as a function of EXTBOOT, EMI_MODE and the Flash security setting. See Table 4-4 for further information on when this pin is configured as an address pin at reset. In all cases, this state may be changed by writing to GPIOB_PER. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOB_PUR register.
GPIOB1 (A17)	34	L3			
GPIOB2 (A18)	35	L2			
GPIOB3 (A19)	36	M1			
GPIOB4	37	M2	Schmitt Input/ Output	Input, pull-up enabled	**Port B GPIO** — These four GPIO pins can be programmed as input or output pins.
(A20)			Output		**Address Bus** — A20 - A23 specify one of the address lines for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A20–A23 and EMI control signals are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting.
(prescaler_ clock)			Output		**Clock Outputs** — can be used to monitor the prescaler_clock, SYS_CLK, SYS_CLK2 or oscillator-clock on GPIOB4 through GPIOB7, respectively. After reset, the default state is GPIO. These pins can also be used to extend the external address bus to its full length or to view any of several system clocks. In these cases, the GPIO_B_PER can be used to individually disable the GPIO. The CLKOSR register in the SIM (see Part 6.5.7) can then be used to choose between address and clock functions.
GPIOB5 (A21) (SYS_CLK)	46	N4			
GPIOB6 (A22) (SYS_CLK2)	47	P3			
GPIOB7 (A23) (oscillator_ Clock)	48	M4			

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
D0 **(GPIOF9)**	70	P10	Input/ Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Data Bus** — D0 - D6 specify part of the data for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), D0–D6 are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. **Port F GPIO** — These seven GPIO pins can be individually programmed as input or output pins. After reset, these pins default to the EMI Data bus function. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOF_PUR register. Example: GPIOF9, clear bit 9 in the GPIOF_PUR register.
D1 (GPIOF10)	71	N10			
D2 (GPIOF11)	83	P14			
D3 (GPIOF12)	86	L13			
D4 (GPIOF13)	88	L14			
D5 (GPIOF14)	89	L12			
D6 (GPIOF15)	90	L11			

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
D7 **(GPIOF0)**	28	K1	Input/ Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Data Bus** — D7 - D15 specify part of the data for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), D7 - D15 are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. **Port F GPIO** — These nine GPIO pins can be individually programmed as input or output pins. At reset, these pins default to data bus functionality. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOF_PUR register. Example: GPIOF0, clear bit 0 in the GPIOF_PUR register.
D8 **(GPIOF1)**	29	K3			
D9 **(GPIOF2)**	30	K2			
D10 **(GPIOF3)**	32	K4			
D11 **(GPIOF4)**	149	A5			
D12 **(GPIOF5)**	150	A4			
D13 **(GPIOF6)**	151	B5			
D14 **(GPIOF7)**	152	C4			
D15 **(GPIOF8)**	153	A3			
$\overline{RD}$	52	P5	Output	In reset, output is disabled, pull-up is enabled	**Read Enable** — $\overline{RD}$ is asserted during external memory read cycles. When $\overline{RD}$ is asserted low, pins D0 - D15 become inputs and an external device is enabled onto the data bus. When $\overline{RD}$ is deasserted high, the external data is latched inside the device. When $\overline{RD}$ is asserted, it qualifies the A0 - A16, $\overline{PS}$, and $\overline{DS}$ pins. $\overline{RD}$ can be connected directly to the $\overline{OE}$ pin of a static RAM or ROM. Depending upon the state of the DRV bit in the EMI bus control register (BCR), $\overline{RD}$ is tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. To deactivate the internal pull-up resistor, set the CTRL bit in the SIM_PUDR register.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
$\overline{WR}$	51	L4	Output	In reset, output is disabled, pull-up is enabled	**Write Enable** — $\overline{WR}$ is asserted during external memory write cycles. When $\overline{WR}$ is asserted low, pins D0 - D15 become outputs and the device puts data on the bus. When $\overline{WR}$ is deasserted high, the external data is latched inside the external device. When $\overline{WR}$ is asserted, it qualifies the A0 - A16, $\overline{PS}$, and $\overline{DS}$ pins. $\overline{WR}$ can be connected directly to the $\overline{WE}$ pin of a static RAM. Depending upon the state of the DRV bit in the EMI bus control register (BCR), $\overline{WR}$ is tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. To deactivate the internal pull-up resistor, set the CTRL bit in the SIM_PUDR register.
$\overline{PS}$ **($\overline{CS0}$)**	53	N6	Output	In reset, output is disabled, pull-up is enabled	**Program Memory Select** — This signal is actually $\overline{CS0}$ in the EMI, which is programmed at reset for compatibility with the 56F80x $\overline{PS}$ signal. $\overline{PS}$ is asserted low for external program memory access. Depending upon the state of the DRV bit in the EMI bus control register (BCR), $\overline{CS0}$ is tri-stated when the external bus is inactive. $\overline{CS0}$ resets to provide the $\overline{PS}$ function as defined on the 56F80x devices.
(GPIOD8)			Input/ Output		**Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. To deactivate the internal pull-up resistor, clear bit 8 in the GPIOD_PUR register.
$\overline{DS}$ **($\overline{CS1}$)**	54	L5	Output	In reset, output is disabled, pull-up is enabled	**Data Memory Select** — This signal is actually $\overline{CS1}$ in the EMI, which is programmed at reset for compatibility with the 56F80x $\overline{DS}$ signal. $\overline{DS}$ is asserted low for external data memory access. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A0 - A23 and EMI control signals are tri-stated when the external bus is inactive. $\overline{CS1}$ resets to provide the $\overline{DS}$ function as defined on the 56F80x devices.
(GPIOD9)			Input/ Output		**Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. To deactivate the internal pull-up resistor, clear bit 9 in the GPIOD_PUR register.