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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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MC56F847XX

MC56F847xx

Supports the 56F84789VLL, 56F84786VLK, 56F84769VLL, 56F84766VLK, 56F84763VLH

Features

- This family of digital signal controllers (DSCs) is based on the 32-bit 56800EX core. Each device combines, on a single chip, the processing power of a DSP and the functionality of an MCU with a flexible set of peripherals to support many target applications:
  - Industrial control
  - Home appliances
  - Smart sensors
  - Fire and security systems
  - Switched-mode power supply and power management
  - Uninterruptible Power Supply (UPS)
  - Solar and wind power generator
  - Power metering
  - Motor control (ACIM, BLDC, PMSM, SR, stepper)
  - Handheld power tools
  - Circuit breaker
  - Medical device/equipment
  - Instrumentation
  - Lighting

- DSC based on 32-bit 56800EX core
  - Up to 100 MIPS at 100 MHz core frequency
  - DSP and MCU functionality in a unified, C-efficient architecture

- On-chip memory
  - Up to 288 KB (256 KB + 32 KB) flash memory, including up to 32 KB FlexNVM
  - Up to 32 KB RAM
  - Up to 2 KB FlexRAM with EEE capability
  - 100 MHz program execution from both internal flash memory and RAM
  - On-chip flash memory and RAM can be mapped into both program and data memory spaces

- Analog
  - Two high-speed, 8-channel, 12-bit ADCs with dynamic x2, x4 programmable amplifier
  - One 20-channel, 16-bit ADC
  - Four analog comparators with integrated 6-bit DAC references
  - One 12-bit DAC

- PWMs and timers
  - Two eFlexPWM modules with up to 24 PWM outputs, one including 8 channels with high resolution NanoEdge placement
  - Two 16-bit quad timer (2 x 4 16-bit timers)
  - Two Periodic Interval Timers (PITs)
  - One Quadrature Decoder
  - Two Programmable Delay Blocks (PDBs)

- Communication interfaces
  - Three high-speed queued SCI (QSCI) modules with LIN slave functionality
  - Up to three queued SPI (QSPI) modules
  - Two SMBus-compatible I2C ports
  - One flexible controller area network (FlexCAN) module

- Security and integrity
  - Cyclic Redundancy Check (CRC) generator
  - Computer operating properly (COP) watchdog
  - External Watchdog Monitor (EWM)

- Clocks
  - Two on-chip relaxation oscillators: 8 MHz (400 kHz at standby mode) and 32 kHz
  - Crystal / resonator oscillator

- System
  - DMA controller
  - Integrated power-on reset (POR) and low-voltage interrupt (LVI) and brown-out reset module
  - Inter-module crossbar connection
  - JTAG/enhanced on-chip emulation (EOnCE) for unobtrusive, real-time debugging

- Operating characteristics
  - Single supply: 3.0 V to 3.6 V
  - 5 V–tolerant I/O (except RESETB pin)

- LQFP packages:
  - 64-pin
  - 80-pin
  - 100-pin

Table of Contents

1 Overview

1.1 MC56F844x/5x/7x Product Family

The following table highlights major features, including features that differ among members of the family. Features not listed are shared by all members of the family.

Table 1. 56F844x/5x/7x Family

Part Number	MC56F84																	
	789	**786**	**769**	**766**	**763**	**553**	**550**	**543**	**540**	**587**	**585**	**567**	**565**	**462**	**452**	**451**	**442**	**441**
Core freq. (MHz)	100	100	100	100	100	80	80	80	80	80	80	80	80	60	60	60	60	60
Flash memory (KB)	256	256	128	128	128	96	96	64	64	256	256	128	128	128	96	96	64	64
FlevNVM/ FlexRAM (KB)	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2
Total flash memory (KB)[1]	288	288	160	160	160	128	128	96	96	288	288	160	160	160	128	128	96	96
RAM (KB)	32	32	24	24	24	16	16	8	8	32	32	24	24	24	16	16	8	8
Memory resource protection	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
External Watchdog	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12-bit Cyclic ADC channels	2x8 (300 ns)	2x8 (300 ns)	2x8 (300 ns)	2x8 (300 ns)	2x8 (300 ns)	2x8 (300 ns)	2x5 (300 ns)	2x8 (300 ns)	2x5 (300 ns)	2x8 (600 ns)	2x8 (600 ns)	2x8 (600 ns)	2x8 (600 ns)	2x8 (600 ns)	2x8 (600 ns)	2x5 (600 ns)	2x8 (600 ns)	2x5 (600 ns)
16-bit SAR ADC (with Temp Sensor) channels	1x 16	1x 10	1x 16	1x 10	1x8	1x8	0	1x8	0	1x 16	1x 10	1x 16	1x 10	0	1x8	0	1x8	0
PWMA with input capture:																		
High-resolution channels	1x8	1x8	1x8	1x8	1x8	1x8	1x6	1x8	1x6	0	0	0	0	0	0	0	0	0
Standard channels	4	1	4	1	1	1	0	1	0	2x 12	1x 12, 1x9	2x 12	1x 12, 1x9	1x9	1x9	1x6	1x9	1x6

Table continues on the next page...

Table 1. 56F844x/5x/7x Family (continued)

Part Number	MC56F84																	
	789	786	769	766	763	553	550	543	540	587	585	567	565	462	452	451	442	441
PWMB with input capture: Standard channels	1x 12	1x7	1x 12	1x7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12-bit DAC	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0
Quad Decoder	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1
DMA	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
CMP	4	4	4	4	4	4	3	4	3	4	4	4	4	4	4	3	4	3
QSCI	3	3	3	3	2	2	2	2	2	3	3	3	3	2	2	2	2	2
QSPI	3	2	3	2	2	2	2	2	2	3	2	3	2	2	2	2	2	2
I2C/SMBus	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
FlexCAN	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
LQFP package pin count	100	80	100	80	64	64	48	64	48	100	80	100	80	64	64	48	64	48

1. This total includes FlexNVM and assumes no FlexNVM is used with FlexRAM for EEPROM.

1.2 56800EX 32-bit Digital Signal Controller Core

- Efficient 32-bit 56800EX Digital Signal Processor (DSP) engine with modified dual Harvard architecture
  - Three internal address buses
  - Four internal data buses: two 32-bit primary buses, one 16-bit secondary data bus, and one 16-bit instruction bus
  - 32-bit data accesses
  - Support for concurrent instruction fetches in the same cycle and dual data accesses in the same cycle
  - 20 addressing modes
- As many as 100 million instructions per second (MIPS) at 100 MHz core frequency
- 162 basic instructions
- Instruction set supports both fractional arithmetic and integer arithmetic
- 32-bit internal primary data buses supporting 8-bit, 16-bit, and 32-bit data movement, addition, subtraction, and logical operation
- Single-cycle 16 × 16-bit -> 32-bit and 32 x 32-bit -> 64-bit multiplier-accumulator (MAC) with dual parallel moves
- 32-bit arithmetic and logic multi-bit shifter
- Four 36-bit accumulators, including extension bits

- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Bit reverse address mode, effectively supporting DSP and Fast Fourier Transform algorithms
- Full shadowing of the register stack for zero-overhead context saves and restores: nine shadow registers corresponding to the R0, R1, R2, R3, R4, R5, N, N3, and M01 address registers
- Instruction set supporting both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Enhanced bit manipulation instruction set
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- Priority level setting for interrupt levels
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging that is independent of processor speed

1.3 Operation Parameters

- Up to 100 MHz operation at -40 °C to 105 °C ambient temperature
- Single 3.3 V power supply
- Supply range: V_{DD} - V_{SS} = 2.7 V to 3.6 V, V_{DDA} - V_{SSA} = 2.7 V to 3.6 V

1.4 On-Chip Memory and Memory Protection

- Modified dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Internal flash memory with security and protection to prevent unauthorized access
- Memory resource protection (MRP) unit to protect supervisor programs and resources from user programs
- Programming code can reside in flash memory during flash programming
- The dual-ported RAM controller supports concurrent instruction fetches and data accesses, or dual data accesses, by the DSC core.
  - Concurrent accesses provide increased performance.
  - The data and instruction arrive at the core in the same cycle, reducing latency.
- On-chip memory
  - Up to 144 KW program/data flash memory, including FlexNVM
  - Up to 16 KW dual port data/program RAM

- Up to 16 KW FlexNVM, which can be used as additional program or data flash memory
- Up to 1 KW FlexRAM, which can be configured as enhanced EEPROM (used in conjunction with FlexNVM) or used as additional RAM

1.5 Interrupt Controller

- Five interrupt priority levels
  - Three user programmable priority levels for each interrupt source: level 0, 1, 2
  - Unmaskable level 3 interrupts include: illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction
  - Maskable level 3 interrupts include: EOnCE step counter, EOnCE breakpoint unit, EOnCE trace buffer
  - Lowest-priority software interrupt: level LP
- Support for nested interrupt: higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Masking of interrupt priority level managed by the 56800EX core
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to System Integration Module (SIM) to restart clock when in wait and stop states
- Ability to relocate interrupt vector table

1.6 Peripheral highlights

1.6.1 Enhanced Flex Pulse Width Modulator (eFlexPWM)

- PWM module contains four identical submodules with up to three outputs per submodule
- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- PWMA with NanoEdge high resolution
  - Fractional delay for enhanced resolution of the PWM period and edge placement
  - Arbitrary PWM edge placement
  - 312 ps PWM frequency and duty-cycle resolution when NanoEdge functionality is enabled
- PWMB with supporting accumulative fractional clock calculation
  - Accumulative fractional clock calculation improves the resolution of the PWM period and edge placement
  - Arbitrary PWM edge placement
  - Equivalent to 312 ps PWM frequency and duty-cycle resolution on average

- PWM outputs can be configured as complementary output pairs or independent outputs
- Dedicated time-base counter with period and frequency control per submodule
- Independent top and bottom deadtime insertion for each complementary pair
- Independent control of both edges of each PWM output
- Enhanced input capture and output compare functionality on each input
  - Channels not used for PWM generation can be used for buffered output compare functions
  - Channels not used for PWM generation can be used for input capture functions
  - Enhanced dual edge capture functionality
- Synchronization of submodule to external hardware or other PWM supported
- Double buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half-cycle reload capability
- Multiple output trigger events can be generated per PWM cycle via hardware
- Support for double switching PWM outputs
- Up to eight fault inputs can be assigned to control multiple PWM outputs
  - Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Individual software control of each PWM output
- All outputs can be programmed to change simultaneously via a FORCE_OUT event
- PWMX pin can optionally output a third PWM signal from each submodule
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - Crossbar module outputs
  - External ADC input, taking into account values set in ADC high and low limit registers

1.6.2 12-bit Analog-to-Digital Converter (Cyclic type)

- Two independent 12-bit analog-to-digital converters (ADCs)
  - 2 x 8-channel external inputs
  - Built-in x1, x2, x4 programmable gain pre-amplifier
  - Maximum ADC clock frequency is up to 20 MHz with as low as 50 ns period
  - Single conversion time of 8.5 ADC clock cycles
  - Additional conversion time of 6 ADC clock cycles
- Support of analog inputs for single-ended and differential conversions
- Sequential, parallel, and independent scan mode
- First 8 samples have offset, limit and zero-crossing calculation supported
- ADC conversions can be synchronized by any module connected to internal crossbar module, such as PWM and timer modules and GPIO and comparators

- Support for simultaneous and software triggering conversions
- Support for multi-triggering mode with a programmable number of conversions on each trigger
- Each ADC has ability to scan and store up to 8 conversion results
- Current injection protection

1.6.3 Inter-Module Crossbar and AND-OR-INVERT logic

- Provides generalized connections between and among on-chip peripherals: ADCs, 12-bit DAC, Comparators, Quad Timers, eFlexPWMs, PDBs, EWM, Quadrature Decoder, and select I/O pins
- User-defined input/output pins for all modules connected to crossbar
- DMA request and interrupt generation from crossbar
- Write-once protection for all registers
- AND-OR-INVERT function that provides a universal Boolean function generator using a four-term sum-of-products expression, with each product term containing true or complement values of the four selected inputs (A, B, C, D).

1.6.4 Comparator

- Full rail-to-rail comparison range
- Support for high speed mode and low speed mode
- Selectable input source includes external pins and internal DACs
- Programmable output polarity
- 6-bit programmable DAC as voltage reference per comparator
- Three programmable hysteresis levels
- Selectable interrupt on rising edge, falling edge, or toggle of comparator output

1.6.5 12-bit Digital-to-Analog Converter

- 12-bit resolution
- Powerdown mode
- Automatic mode allows the DAC to automatically generate pre-programmed output waveforms including square, triangle, and sawtooth waveforms for applications such as slope compensation
- Programmable period, update rate, and range
- Output can be routed to an internal comparator, ADC, or optionally off chip

1.6.6 Quad Timer

- Four 16-bit up/down counters with programmable prescaler for each counter
- Operation modes: edge count, gated count, signed count, capture, compare, PWM, signal shot, single pulse, pulse string, cascaded, quadrature decode
- Programmable input filter
- Counting start can be synchronized across counters

1.6.7 Queued Serial Communications Interface (QSCI) Modules

- Operating clock up to two times CPU operating frequency
- Four-word-deep FIFOs available on both transmit and receive buffers
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit integer and 3-bit fractional baud rate selection
- Full-duplex or single-wire operation
- Programmable 8-bit or 9-bit data format
- Error detection capability
- Two receiver wakeup methods:
  - Idle line
  - Address mark
- 1/16 bit-time noise detection

1.6.8 Queued Serial Peripheral Interface (QSPI) Modules

- Maximum 25 Mbps baud rate
- Selectable baud rate clock sources for low baud rate communication
- Baud rate as low as Baudrate_Freq_in / 8192
- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four-word-deep FIFOs available on transmit and receive buffers
- Programmable length transmissions (2 bits to 16 bits)
- Programmable transmit and receive shift order (MSB as first bit transmitted)

1.6.9 Inter-Integrated Circuit (I2C)/System Management Bus (SMBus) Modules

- Compatible with I2C bus standard
- Support for System Management Bus (SMBus) specification, version 2
- Multi-master operation

- General call recognition
- 10-bit address extension
- Start/Repeat and Stop indication flags
- Support for dual slave addresses or configuration of a range of slave addresses
- Programmable glitch input filter

1.6.10 Flex Controller Area Network (FlexCAN) Module

- Clock source from PLL or XOSC/CLKIN
- Implementation of the CAN protocol Version 2.0 A/B
- Standard and extended data frames
- 0-to-8 bytes data length
- Programmable bit rate up to 1 Mbps
- Support for remote frames
- Sixteen Message Buffers, each configurable as receive or transmit, all supporting standard and extended messages
- Individual Rx Mask Registers per Message Buffer
- Internal timer for time-stamping of received and transmitted messages
- Listen-only mode capability
- Programmable loopback mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Global network time, synchronized by a specific message
- Low power modes, with programmable wakeup on bus activity

1.6.11 Computer Operating Properly (COP) Watchdog

- Programmable timeout period
- Support for operation in all power modes: run mode, wait mode, stop mode
- Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
- Selectable reference clock source in support of EN60730 and IEC61508
- Selectable clock sources:
  - External crystal oscillator/external clock source
  - On-chip low-power 32 kHz oscillator
  - System bus (IPBus up to 100 MHz)
  - 8 MHz / 400 kHz ROSC
- Support for interrupt triggered when the counter reaches the timeout value

1.6.12 Power Supervisor

- Power-on reset (POR) to reset CPU, peripherals, and JTAG/EOnCE controllers (VDD > 2.1 V)
- Brownout reset (VDD < 1.9 V)
- Critical warn low voltage interrupt (LVI2.0)
- Peripheral low voltage interrupt (LVI2.7)

1.6.13 Phase Locked Loop

- Wide programmable output frequency: 240 MHz to 400 MHz
- Input reference clock frequency: 8 MHz to 16 MHz
- Detection of loss of lock and loss of reference clock
- Ability to power down

1.6.14 Clock sources

1.6.14.1 On-Chip Oscillators

- Tunable 8 MHz relaxation oscillator with 400 kHz at standby mode (divide-by-two output)
- 32 kHz low frequency clock as secondary clock source for COP, EWM, PIT

1.6.14.2 Crystal Oscillator

- Support for both high ESR crystal oscillator (greater than 100-ohm ESR) and ceramic resonator
- 4 MHz to 16 MHz operating frequency

1.6.15 Cyclic Redundancy Check (CRC) Generator

- Hardware 16/32-bit CRC generator
- High-speed hardware CRC calculation
- Programmable initial seed value
- Programmable 16/32-bit polynomial
- Error detection for all single, double, odd, and most multi-bit errors

- Option to transpose input data or output data (CRC result) bitwise or bytewise,[1] which is required for certain CRC standards
- Option for inversion of final CRC result

1.6.16 General Purpose I/O (GPIO)

- 5 V tolerance
- Individual control of peripheral mode or GPIO mode for each pin
- Programmable push-pull or open drain output
- Configurable pullup or pulldown on all input pins
- All pins except JTAG and RESETB pins default to be GPIO inputs
- 2 mA / 9 mA source/sink capability
- Controllable output slew rate

1.7 Block Diagrams

The 56800EX core is based on a modified dual Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The device's basic architecture appears in Figure 1 and Figure 2. Figure 1 illustrates how the 56800EX system buses communicate with internal memories and the IPBus interface and the internal connections among each unit of the 56800EX core. Figure 2 shows the peripherals and control blocks connected to the IPBus bridge. See the specific device’s Reference Manual for details.

1. A bytewise transposition is not possible when accessing the CRC data register via 8-bit accesses. In this case, user software must perform the bytewise transposition.

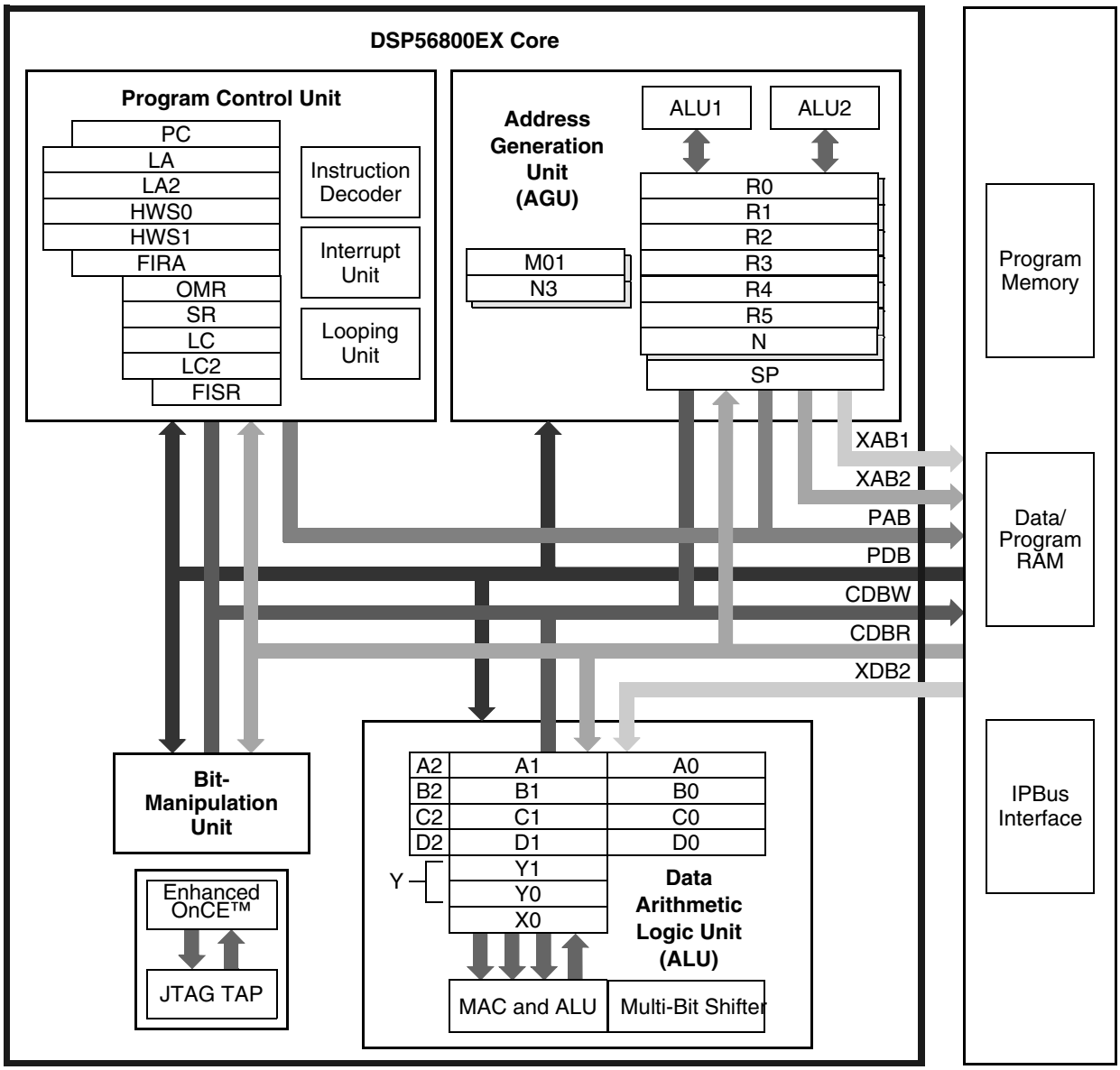


Figure 1. 56800EX Basic Block Diagram

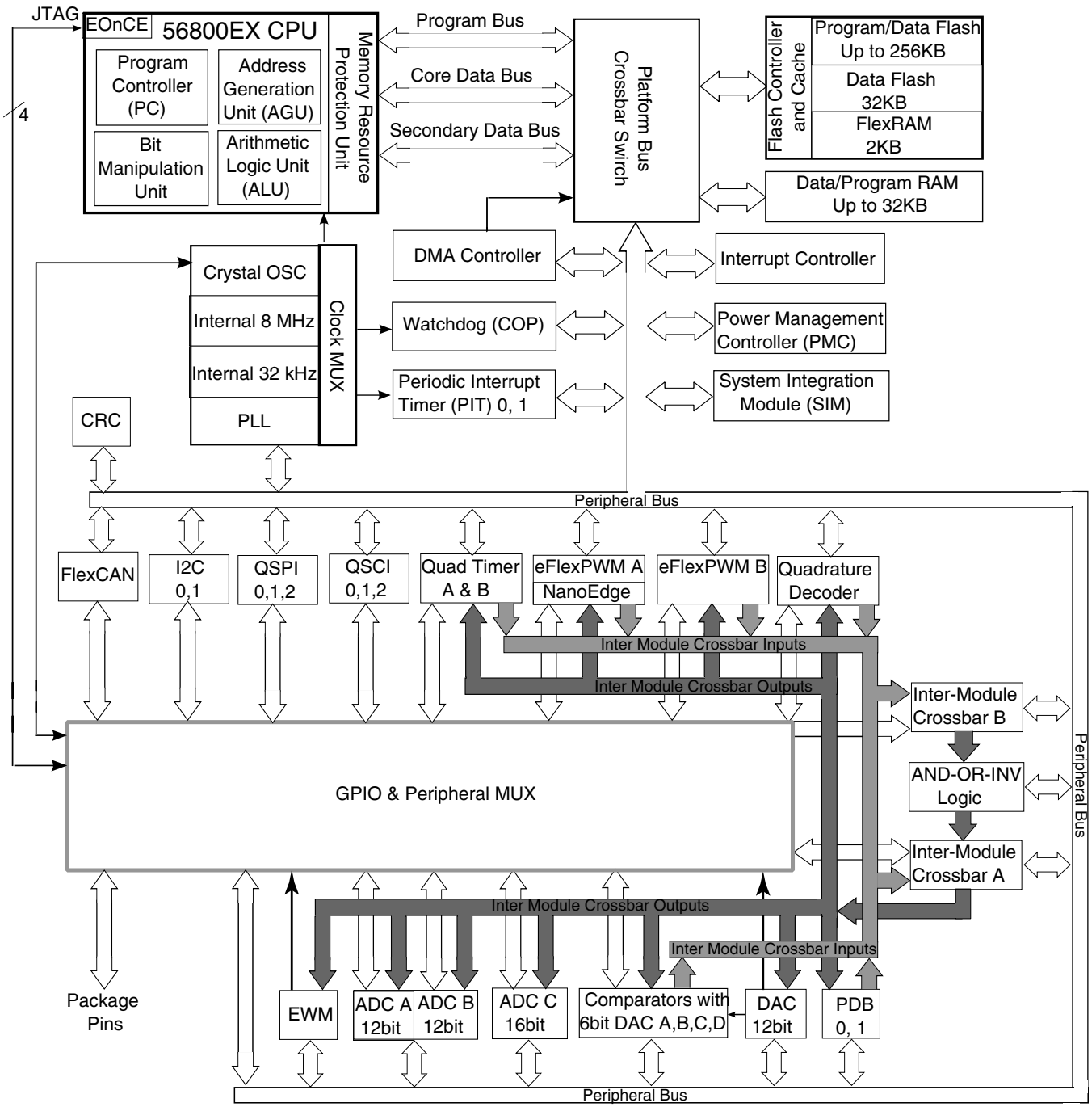


Figure 2. System Diagram

2 Signal groups

The input and output signals of the MC56F84xxx are organized into functional groups, as detailed in Table 2.

Table 2. Functional Group Pin Allocations

Functional Group	Number of Pins in 48LQFP	Number of Pins in 64LQFP	Number of Pins in 80LQFP	Number of Pins in 100LQFP
Power Inputs (V_{DD}, V_{DDA}, V_{CAP})	5	6	6	6
Ground (V_{SS}, V_{SSA})	4	4	4	4
Reset	1	1	1	1
eFlexPWM with NanoEdge ports, not including fault pins	6	8	8	8
eFlexPWM without NanoEdge ports, not including fault pins	0	1	7	16
Queued Serial Peripheral Interface (QSPI) ports	5	6	8	15
Queued Serial Communications Interface (QSCI) ports	6	9	13	15
Inter-Integrated Circuit (I^2C) interface ports	4	6	6	6
12-bit Analog-to-Digital Converter (Cyclic ADC) inputs	10	16	16	16
16-bit Analog-to-Digital Converter (SAR ADC) inputs	2	8	10	16
Analog Comparator inputs/outputs	10/4	13/6	13/6	16/6
12-bit Digital-to-Analog output	1	1	1	1
Quad Timer Module (TMR) ports	6	9	11	13
Controller Area Network (FlexCAN)	2	2	2	2
Inter-Module Crossbar inputs/outputs	12/2	16/6	19/17	25/19
Clock inputs/outputs	2/2	2/2	2/3	2/3
JTAG / Enhanced On-Chip Emulation (EOnCE)	4	4	4	4

3 Ordering parts

3.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the following device numbers: MC56F84

4 Part identification

4.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

4.2 Format

Part numbers for this device have the following format: Q 56F8 4 C F P T PP N

4.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• MC = Fully qualified, general market flow • PC = Prequalification
56F8	DSC family with flash memory and DSP56800/ DSP56800E/DSP56800EX core	• 56F8
4	DSC subfamily	• 4
C	Maximum CPU frequency (MHz)	• 4 = 60 MHz • 5 = 80 MHz • 7 = 100 MHz
F	Primary program flash memory size	• 4 = 64 KB • 5 = 96 KB • 6 = 128 KB • 8 = 256 KB
P	Pin count	• 0 and 1 = 48 • 2 and 3 = 64 • 4, 5, and 6 = 80 • 7, 8, and 9 = 100
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LF = 48LQFP • LH = 64LQFP • LK = 80LQFP • LL = 100LQFP
N	Packaging type	• R = Tape and reel • (Blank) = Trays

4.4 Example

This is an example part number: MC56F84789VLL

5 Terminology and guidelines

5.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

5.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

5.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

5.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

5.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

5.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

5.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

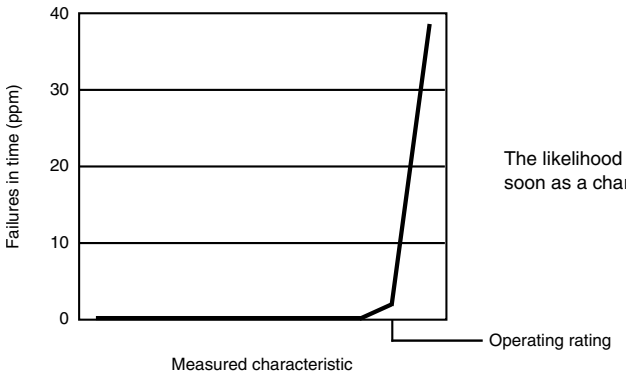
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

5.4.1 Example

This is an example of an operating rating:

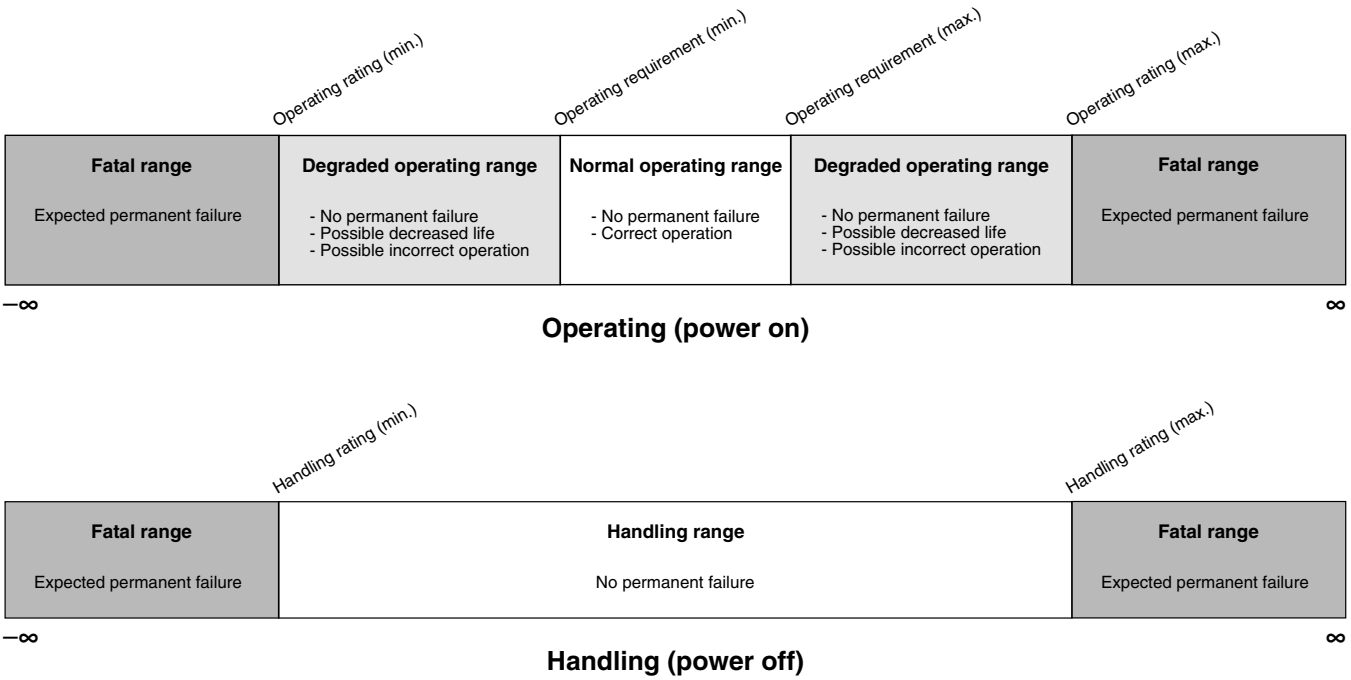
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

5.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

5.6 Relationship between ratings and operating requirements



5.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

5.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

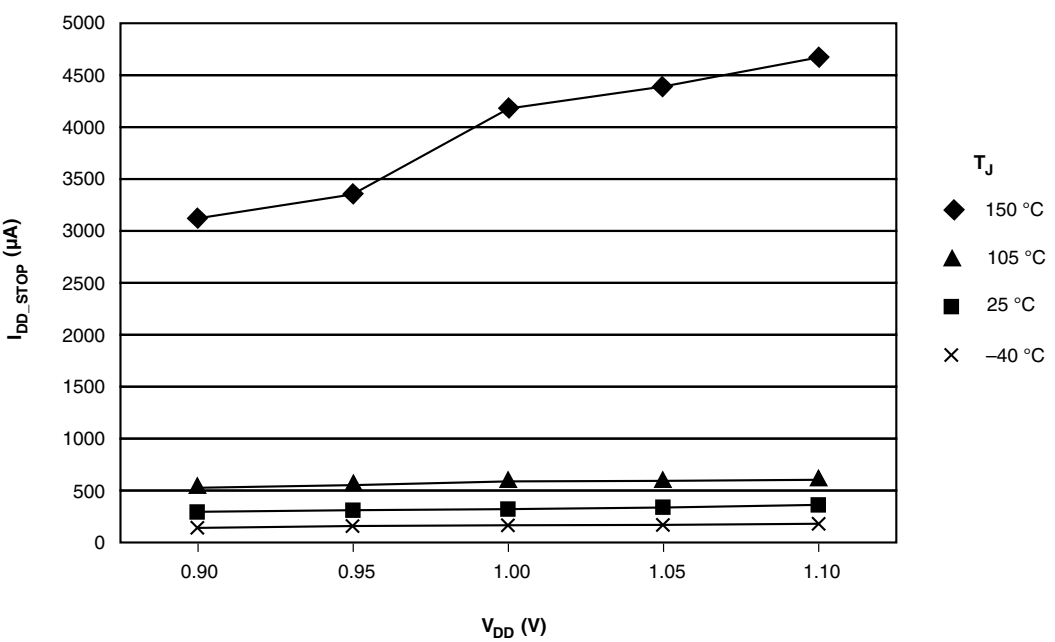
5.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

5.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



5.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

6 Ratings

6.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.3 ESD handling ratings

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM), and the charge device model (CDM).

All latch-up testing is in conformity with AEC-Q100 Stress Test Qualification.

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 3. ESD/Latch-up Protection

Characteristic[1]	Min	Max	Unit
ESD for Human Body Model (HBM)	–2000	+2000	V
ESD for Machine Model (MM)	–200	+200	V
ESD for Charge Device Model (CDM)	–500	+500	V
Latch-up current at TA= 85°C (I_{LAT})	–100	+100	mA

1. Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

6.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 4 may affect device reliability or cause permanent damage to the device.

Table 4. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes[1]	Min	Max	Unit
Supply Voltage Range	V_{DD}		-0.3	4.0	V
Analog Supply Voltage Range	V_{DDA}		-0.3	4.0	V
ADC High Voltage Reference	V_{REFHx}		-0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		-0.3	0.3	V

Table continues on the next page...

Table 4. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V) (continued)

Characteristic	Symbol	Notes[1]	Min	Max	Unit
Digital Input Voltage Range	V_{IN}	Pin Group 1	-0.3	5.5	V
$\overline{\text{RESET}}$ Input Voltage Range	V_{IN_RESET}	Pin Group 2	-0.3	4.0	V
Oscillator Input Voltage Range	V_{OSC}	Pin Group 4	-0.4	4.0	V
Analog Input Voltage Range	V_{INA}	Pin Group 3	-0.3	4.0	V
Input clamp current, per pin (V_{IN} < V_{SS} - 0.3 V)[2, 3]	V_{IC}		—	-5.0	mA
Output clamp current, per pin[4]	V_{OC}		—	±20.0	mA
Contiguous pin DC injection current—regional limit sum of 16 contiguous pins	I_{ICont}		-25	25	mA
Output Voltage Range (normal push-pull mode)	V_{OUT}	Pin Group 1, 2	-0.3	4.0	V
Output Voltage Range (open drain mode)	V_{OUTOD}	Pin Group 1	-0.3	5.5	V
$\overline{\text{RESET}}$ Output Voltage Range	V_{OUTOD_RESET}	Pin Group 2	-0.3	4.0	V
DAC Output Voltage Range	V_{OUT_DAC}	Pin Group 5	-0.3	4.0	V
Ambient Temperature Industrial	T_A		-40	105	°C
Storage Temperature Range (Extended Industrial)	T_{STG}		-55	150	°C

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output
2. Continuous clamp current
3. All 5 volt tolerant digital I/O pins are internally clamped to VSS through a ESD protection diode. There is no diode connection to VDD. If VIN greater than VDIO_MIN (=VSS-0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required.
4. I/O is configured as push-pull mode.

7 General

7.1 General Characteristics

The device is fabricated in high-density, low-power CMOS with 5 V–tolerant TTL-compatible digital inputs, except for the $\overline{\text{RESET}}$ pin which is 3.3 V only. The term “5 V–tolerant” refers to the capability of an I/O pin, built on a 3.3 V–compatible process technology, to withstand a voltage up to 5.5 V without damaging the device.

5 V–tolerant I/O is desirable because many systems have a mixture of devices designed for 3.3 V and 5 V power supplies. In such systems, a bus may carry both 3.3 V– and 5 V–compatible I/O voltage levels (a standard 3.3 V I/O is designed to receive a maximum

voltage of 3.3 V ± 10% during normal operation without causing damage). This 5 V–tolerant capability therefore offers the power savings of 3.3 V I/O levels combined with the ability to receive 5 V levels without damage.

Absolute maximum ratings in Table 4 are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this chapter apply over the temperature range of -40°C to 105°C ambient temperature over the following supply ranges: VSS = VSSA = 0 V, VDD = VDDA = 3.0 V to 3.6 V, CL ≤ 50 pF, f_{OP} = 100 MHz.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

7.2 AC Electrical Characteristics

Tests are conducted using the input levels specified in Table 7. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in Figure 3.

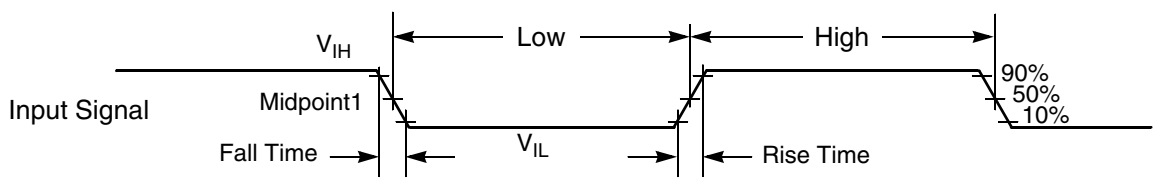


Figure 3. Input Signal Measurement References

Figure 4 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}