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MC68302

Integrated Multiprotocol Processor
User's Manual

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PREFACE

The complete documentation package for the MC68302 consists of the M68000PM/AD, *MC68000 Family Programmer's Reference Manual,* MC68302UM/AD, *MC68302 Integrated Multiprotocol Processor User's Manual,* and the MC68302/D, *MC68302 Integrated Multiprotocol Processor Product Brief*.

The *MC68302 Integrated Multiprotocol Processor User's Manual* describes the programming, capabilities, registers, and operation of the MC68302; the *MC68000 Family Programmer's Reference Manual* provides instruction details for the MC68302; and the *MC68302 Low Power Integrated Multiprotocol Processor Product Brief* provides a brief description of the MC68302 capabilities.

This user's manual is organized as follows:

Section 1	General Description
Section 2	MC68000/MC68008 Core
Section 3	System Integration Block (SIB)
Section 4	Communications Processor (CP)
Section 5	Signal Description
Section 6	Electrical Characteristics
Section 7	Mechanical Data And Ordering Information
Appendix B	Development Tools and Support
Appendix C	RISC Microcode from RAM
Appendix D	MC68302 Applications
Appendix E	SCC Programming Reference
Appendix F	Design Checklist

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Modem: Call 1-800-843-3451 (outside US or Canada 512-891-3650) on a modem that runs at 14,400 bps or slower. Set your software to N/8/1/F emulating a vt100.

Internet: This access is provided by telneting to pirs.aus.sps.mot.com [129.38.233.1] or through the World Wide Web at http://pirs.aus.sps.mot.com.

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SECTION 1
GENERAL DESCRIPTION

The MC68302 integrated multiprotocol processor (IMP) is a very large-scale integration (VLSI) device incorporating the main building blocks needed for the design of a wide variety of controllers. The device is especially suitable to applications in the communications industry. The IMP is the first device to offer the benefits of a closely coupled, industry-standard M68000 microprocessor core and a flexible communications architecture. The IMP may be configured to support a number of popular industry interfaces, including those for the Integrated Services Digital Network (ISDN) basic rate and terminal adaptor applications. Concurrent operation of different protocols is easily achieved through a combination of architectural and programmable features. Data concentrators, line cards, modems, bridges, and gateways are examples of suitable applications for this device.

The IMP is a high-density complementary metal-oxide semiconductor (HCMOS) device consisting of an M68000 microprocessor core, a system integration block (SIB), and a communications processor (CP).

1.1 BLOCK DIAGRAM

The block diagram is shown in Figure 1-1.

By integrating the microprocessor core with the serial ports (in the CP) and the system peripherals (in the SIB), the IMP is capable of handling complex tasks such as all ISDN basic rate (2B + D) access tasks. For example, the IMP architecture and the serial communications controller (SCC) ports can support the interface of an S/T transceiver chip and the lower part (bit handling) ISO/OSI layer-2 functions. Other layer-2 functions and the higher protocol layers would then be implemented by software executed by the M68000 core.

Using the flexible memory-based buffer structure of the IMP, terminal adaptor applications also can be supported by transforming and sharing data buffer information between the three SCC ports and the serial communications port (SCP). Each SCC channel is available for HDLC/SDLC[1], UART, BISYNC, DDCMP[2], V.110, or transparent operation. The IMP provides a number of choices for various rate adaptive techniques and can be used for functions such as a terminal controller, multiplexer, or concentrator.

1. SDLC is a trademark of International Business Machines.
2. DDCMP is a trademark of Digital Equipment Corporation.

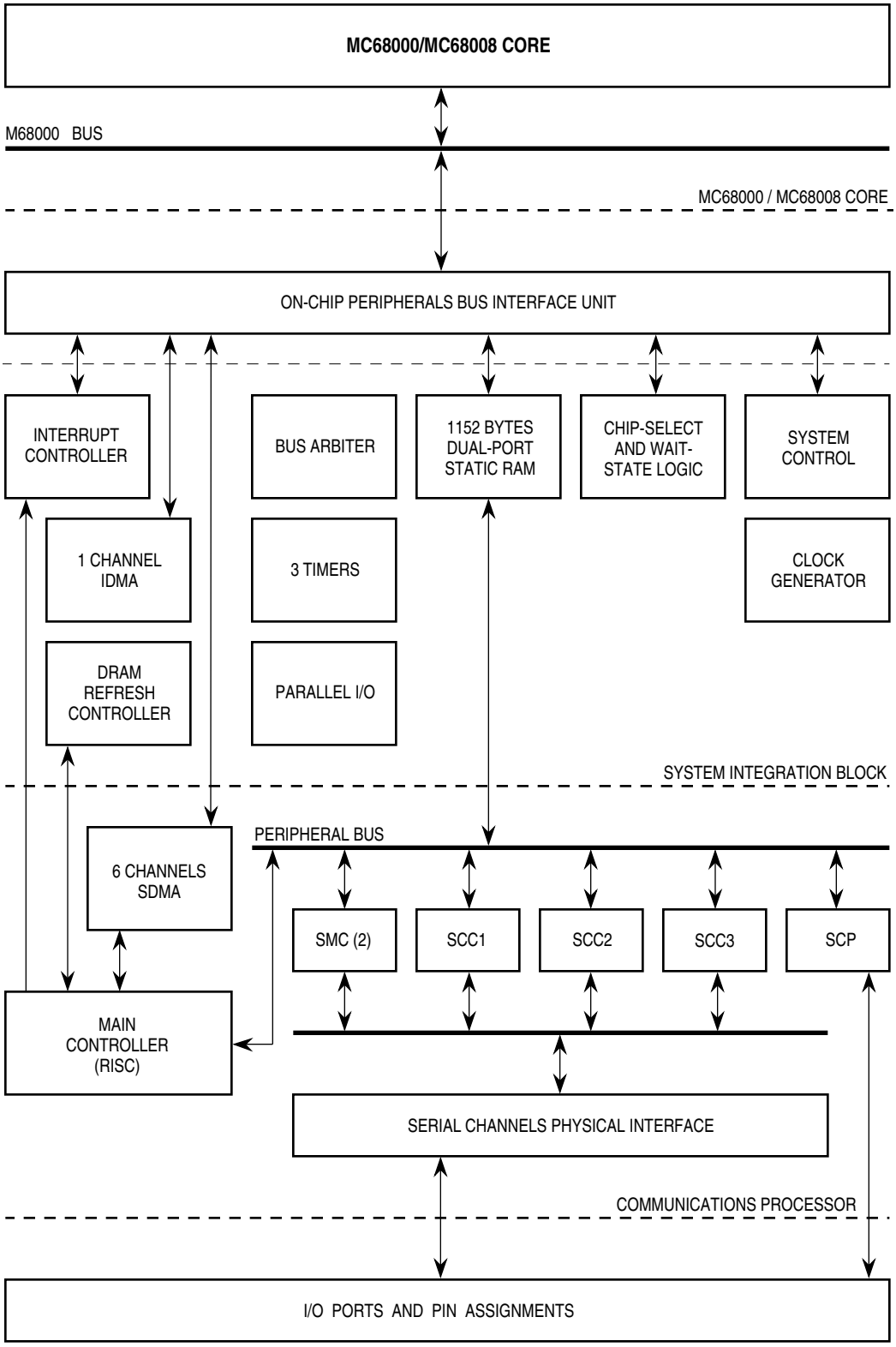

Figure 1-1. MC68302 Block Diagram

The MC68302 can also be used in applications such as board-level industrial controllers performing real-time control applications with a local control bus and an X.25 packet network connection. Such a system provides the real-time response to a demanding peripheral while permitting remote monitoring and communication through an X.25 packet network.

1.2 FEATURES

The features of the IMP are as follows:

- On-Chip HCMOS MC68000/MC68008 Core Supporting a 16- or 8-Bit M68000 Family-System
- IB Including:
  - —Independent Direct Memory Access (IDMA) Controller with Three Handshake Signals: $\overline{\text{DREQ}}$, $\overline{\text{DACK}}$, and $\overline{\text{DONE}}$.
  - —Interrupt Controller with Two Modes of Operation
  - —Parallel Input/Output (I/O) Ports, Some with Interrupt Capability
  - —On-Chip 1152-Byte Dual-Port RAM
  - —Three Timers Including a Watchdog Timer
  - —Four Programmable Chip-Select Lines with Wait-State Generator Logic
  - —Programmable Address Mapping of the Dual-Port RAM and IMP Registers
  - —On-Chip Clock Generator with Output Signal
  - —System Control:
    - Bus Arbitration Logic with Low-Interrupt Latency Support
    - System Status and Control Logic
    - Disable CPU Logic (M68000)
    - Hardware Watchdog
    - Low-Power (Standby) Modes
    - Freeze Control for Debugging
    - DRAM Refresh Controller
- CP Including:
  - —Main Controller (RISC Processor)
  - —Three Independent Full-Duplex Serial Communications Controllers (SCCs)
  - —Supporting Various Protocols:
    - High-Level/Synchronous Data Link Control (HDLC/SDLC)
    - Universal Asynchronous Receiver Transmitter (UART)
    - Binary Synchronous Communication (BISYNC)
    - Synchronous/Asynchronous Digital Data Communications Message Protocol (DDCMP)
    - Transparent Modes
    - V.110 Rate Adaption
  - —Six Serial DMA Channels for the Three SCCs
  - —Flexible Physical Interface Accessible by SCCs Including:
    - Motorola Interchip Digital Link (IDL)
    - General Circuit Interface (GCI, also known as IOM[3]-2)
    - Pulse Code Modulation (PCM) Highway Interface

[3] IOM is a trademark of Siemens AG