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# MC68332

## *Technical Summary* **32-Bit Modular Microcontroller**

### **1 Introduction**

The MC68332, a highly-integrated 32-bit microcontroller, combines high-performance data manipulation capabilities with powerful peripheral subsystems. The MCU is built up from standard modules that interface through a common intermodule bus (IMB). Standardization facilitates rapid development of devices tailored for specific applications.

The MCU incorporates a 32-bit CPU (CPU32), a system integration module (SIM), a time processor unit (TPU), a queued serial module (QSM), and a 2-Kbyte static RAM module with TPU emulation capability (TPURAM).

The MCU can either synthesize an internal clock signal from an external reference or use an external clock input directly. Operation with a 32.768-kHz reference frequency is standard. The maximum system clock speed is 20.97 MHz. System hardware and software allow changes in clock rate during operation. Because MCU operation is fully static, register and memory contents are not affected by clock rate changes.

High-density complementary metal-oxide semiconductor (HCMOS) architecture makes the basic power consumption of the MCU low. Power consumption can be minimized by stopping the system clock. The CPU32 instruction set includes a low-power stop (LPSTOP) command that efficiently implements this capability.



**Table 1 Ordering Information**

Package Type	TPU Type	Temperature	Frequency (MHz)	Package Order Quantity	Order Number
132-Pin PQFP	Motion Control	-40 to +85 °C	16 MHz	2 pc tray	SPAKMC332GCFC16
				36 pc tray	MC68332GCFC16
			20 MHz	2 pc tray	SPAKMC332GCFC20
				36 pc tray	MC68332GCFC20
		-40 to +105 °C	16 MHz	2 pc tray	SPAKMC332GVFC16
				36 pc tray	MC68332GVFC16
			20 MHz	2 pc tray	SPAKMC332GVFC20
				36 pc tray	MC68332GVFC20
		-40 to +125 °C	16 MHz	2 pc tray	SPAKMC332GMFC16
				36 pc tray	MC68332GMFC16
			20 MHz	2 pc tray	SPAKMC332GMFC20
				36 pc tray	MC68332GMFC20
	Standard	-40 to +85 °C	16 MHz	2 pc tray	SPAKMC332CFC16
				36 pc tray	MC68332CFC16
			20 MHz	2 pc tray	SPAKMC332CFC20
				36 pc tray	MC68332CFC20
		-40 to +105 °C	16 MHz	2 pc tray	SPAKMC332VFC16
				36 pc tray	MC68332VFC16
			20 MHz	2 pc tray	SPAKMC332VFC20
				36 pc tray	MC68332VFC20
		-40 to +125 °C	16 MHz	2 pc tray	SPAKMC332MFC16
				36 pc tray	MC68332MFC16
			20 MHz	2 pc tray	SPAKMC332MFC20
				36 pc tray	MC68332MFC20
	Std w/enhanced PPWA	-40 to +85 °C	16 MHz	2 pc tray	SPAKMC332ACFC16
				36 pc tray	MC68332ACFC16
			20 MHz	2 pc tray	SPAKMC332ACFC20
				36 pc tray	MC68332ACFC20
		-40 to +105 °C	16 MHz	2 pc tray	SPAKMC332AVFC16
				36 pc tray	MC68332AVFC16
			20 MHz	2 pc tray	SPAKMC332AVFC20
				36 pc tray	MC68332AVFC20
		-40 to +125 °C	16 MHz	2 pc tray	SPAKMC332AMFC16
				36 pc tray	MC68332AMFC16
			20 MHz	2 pc tray	SPAKMC332AMFC20
				36 pc tray	MC68332AMFC20

**Table 1 Ordering Information (Continued)**

Package Type	TPU Type	Temperature	Frequency (MHz)	Package Order Quantity	Order Number
144-Pin QFP	Motion Control	-40 to +85 °C	16 MHz	2 pc tray	SPAKMC332GCFV16
				44 pc tray	MC68332GCFV16
			20 MHz	2 pc tray	SPAKMC332GCFV20
				44 pc tray	MC68332GCFV20
		-40 to +105 °C	16 MHz	2 pc tray	SPAKMC332GVFV16
				44 pc tray	MC68332GVFV16
			20 MHz	2 pc tray	SPAKMC332GVFV20
				44 pc tray	MC68332GVFV20
		-40 to +125 °C	16 MHz	2 pc tray	SPAKMC332GMFV16
				44 pc tray	MC68332GMFV16
			20 MHz	2 pc tray	SPAKMC332GMFV20
				44 pc tray	MC68332GMFV20
	Standard	-40 to +85 °C	16 MHz	2 pc tray	SPAKMC332CFV16
				44 pc tray	MC68332CFV16
			20 MHz	2 pc tray	SPAKMC332CFV20
				44 pc tray	MC68332CFV20
		-40 to +105 °C	16 MHz	2 pc tray	SPAKMC332VfV16
				44 pc tray	MC68332VfV16
			20 MHz	2 pc tray	SPAKMC332VfV20
				44 pc tray	MC68332VfV20
		-40 to +125 °C	16 MHz	2 pc tray	SPAKMC332MFV16
				44 pc tray	MC68332MFV16
			20 MHz	2 pc tray	SPAKMC332MFV20
				44 pc tray	MC68332MFV20
	Std w/enhanced PPWA	-40 to +85 °C	16 MHz	2 pc tray	SPAKMC332ACFV16
				44 pc tray	MC68332ACFV16
			20 MHz	2 pc tray	SPAKMC332ACFV20
				44 pc tray	MC68332ACFV20
		-40 to +105 °C	16 MHz	2 pc tray	SPAKMC332AVfV16
				44 pc tray	MC68332AVfV16
			20 MHz	2 pc tray	SPAKMC332AVfC20
				44 pc tray	MC68332AVfV20
		-40 to +125 °C	16 MHz	2 pc tray	SPAKMC332AMFV16
				44 pc tray	MC68332AMFV16
			20 MHz	2 pc tray	SPAKMC332AMFV20
				44 pc tray	MC68332AMFV20



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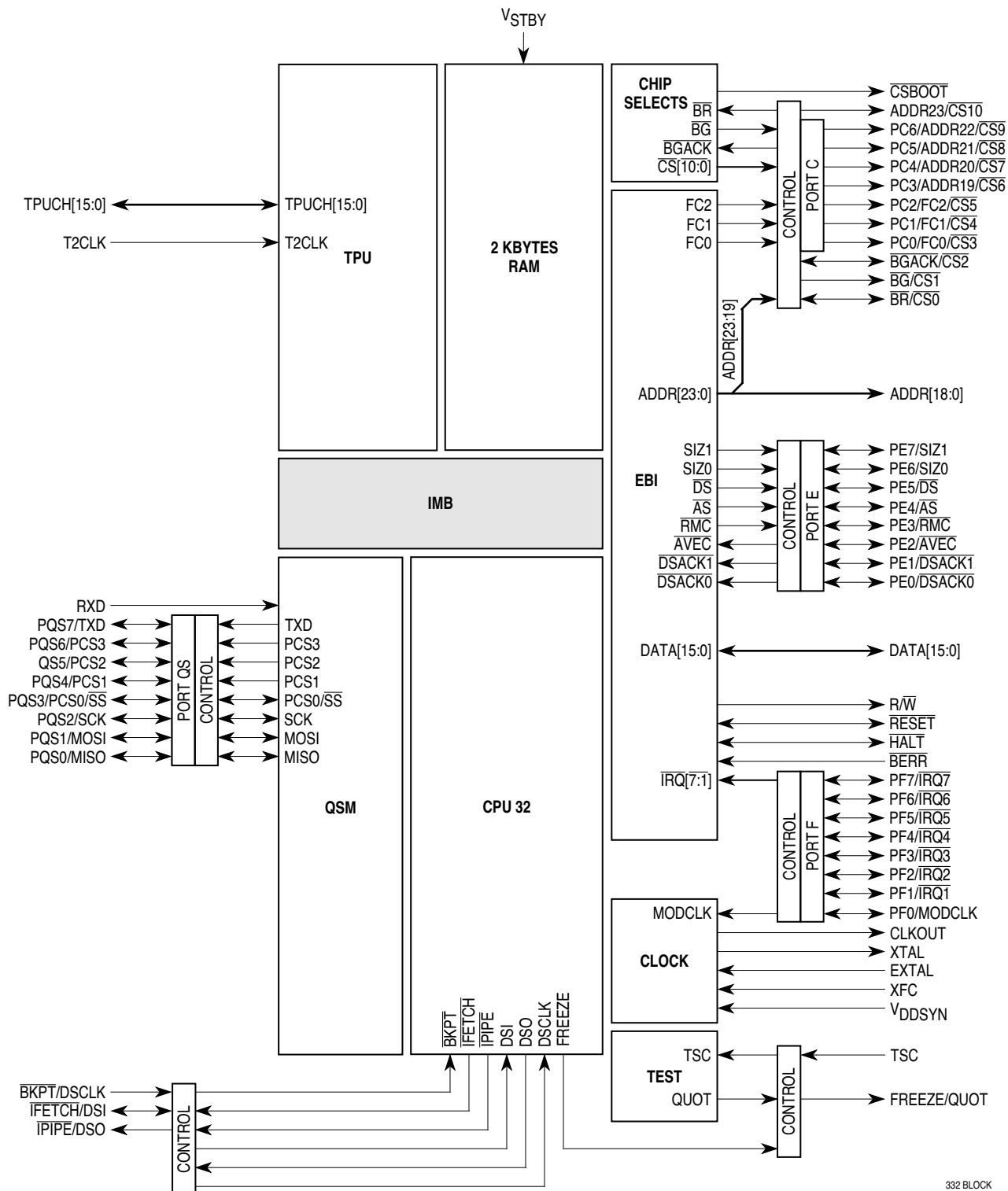
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## 1.1 Features

- Central Processing Unit (CPU32)
  - 32-Bit Architecture
  - Virtual Memory Implementation
  - Table Lookup and Interpolate Instruction
  - Improved Exception Handling for Controller Applications
  - High-Level Language Support
  - Background Debugging Mode
  - Fully Static Operation
- System Integration Module (SIM)
  - External Bus Support
  - Programmable Chip-Select Outputs
  - System Protection Logic
  - Watchdog Timer, Clock Monitor, and Bus Monitor
  - Two 8-Bit Dual Function Input/Output Ports
  - One 7-Bit Dual Function Output Port
  - Phase-Locked Loop (PLL) Clock System
- Time Processor Unit (TPU)
  - Dedicated Microengine Operating Independently of CPU32
  - 16 Independent, Programmable Channels and Pins
  - Any Channel can Perform any Time Function
  - Two Timer Count Registers with Programmable Prescalers
  - Selectable Channel Priority Levels
- Queued Serial Module (QSM)
  - Enhanced Serial Communication Interface
  - Queued Serial Peripheral Interface
  - One 8-Bit Dual Function Port
- Static RAM Module with TPU Emulation Capability (TPURAM)
  - 2-Kbytes of Static RAM
  - May be Used as Normal RAM or TPU Microcode Emulation RAM

## 1.2 Block Diagram

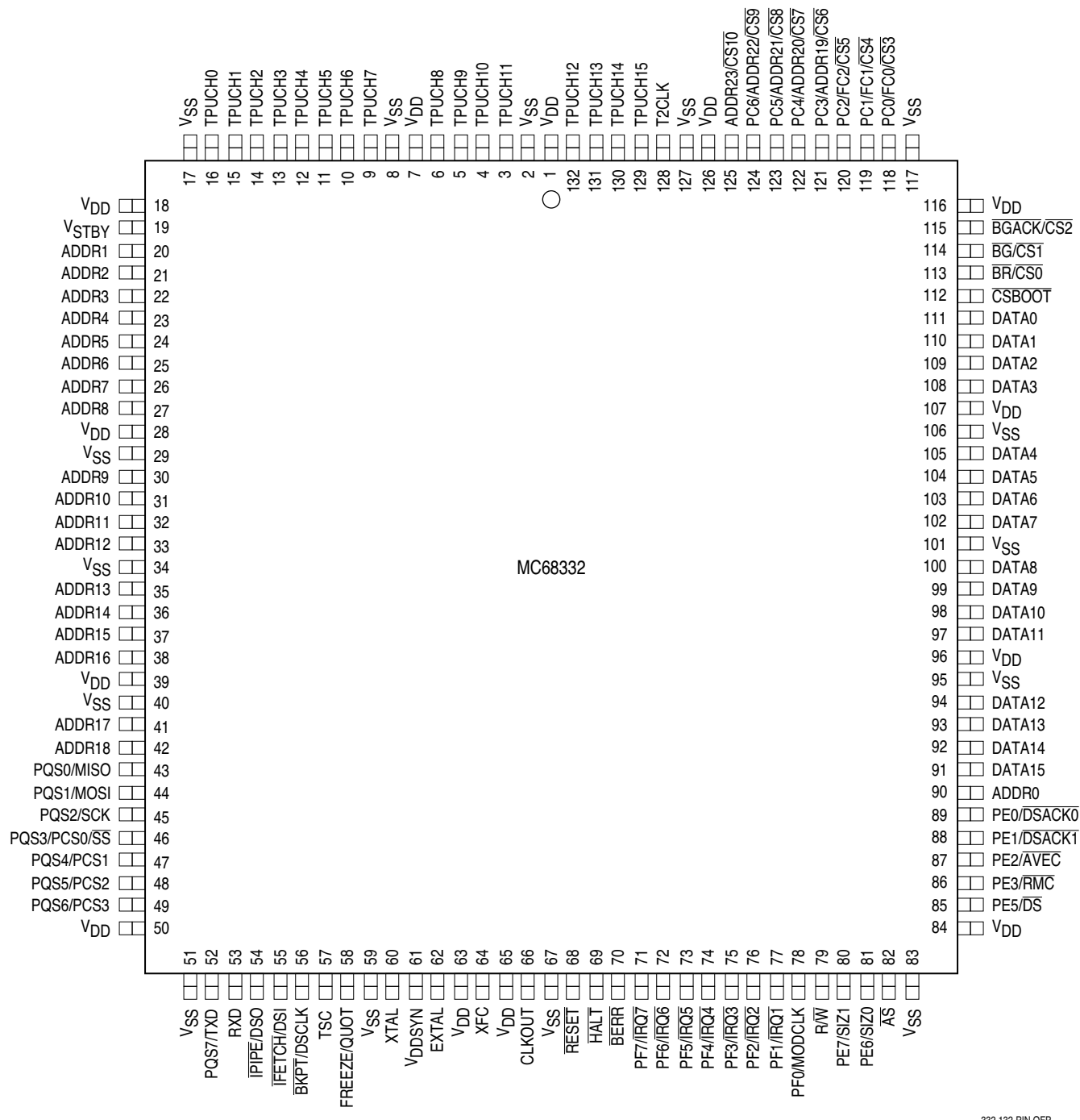


332 BLOCK

Figure 1 MCU Block Diagram



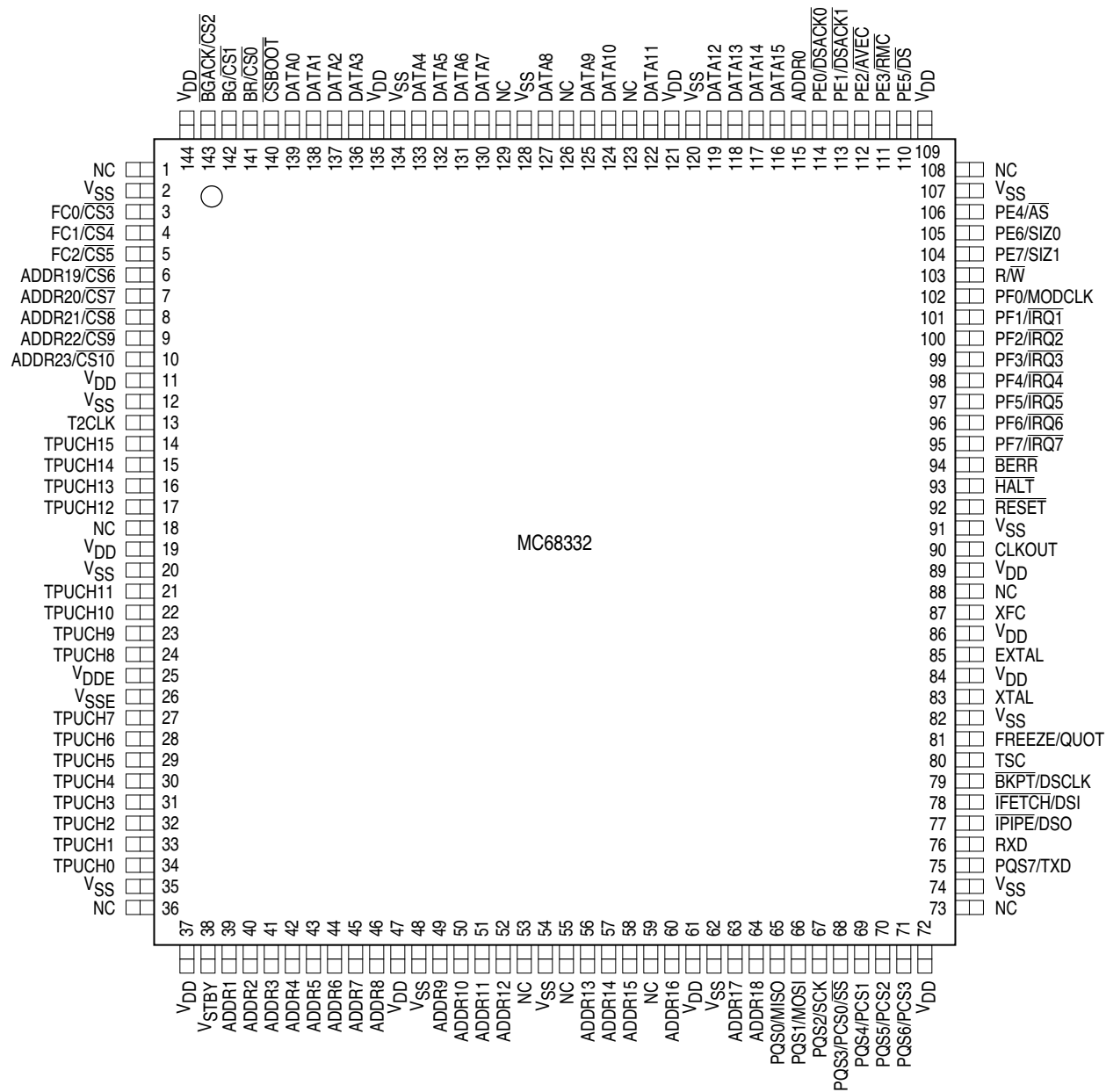
### 1.3 Pin Assignments



332 132-PIN QFP

Figure 2 MC68332 132-Pin QFP Pin Assignments



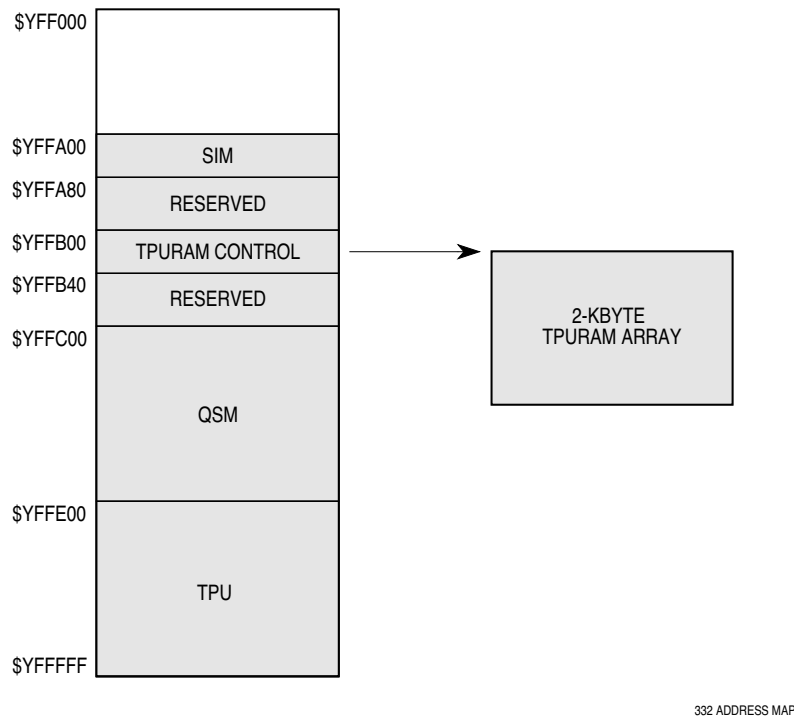


332 144-PIN QFP

Figure 3 MC68332 144-Pin QFP Pin Assignments

## 1.4 Address Map

The following figure is a map of the MCU internal addresses. The RAM array is positioned by the base address registers in the associated RAM control block. Unimplemented blocks are mapped externally.



**Figure 4 MCU Address Map**

## 1.5 Intermodule Bus

The intermodule bus (IMB) is a standardized bus developed to facilitate both design and operation of modular microcontrollers. It contains circuitry to support exception processing, address space partitioning, multiple interrupt levels, and vectored interrupts. The standardized modules in the MCU communicate with one another and with external components through the IMB. The IMB in the MCU uses 24 address and 16 data lines.

## 2 Signal Descriptions

### 2.1 Pin Characteristics

The following table shows MCU pins and their characteristics. All inputs detect CMOS logic levels. All inputs can be put in a high-impedance state, but the method of doing this differs depending upon pin function. Refer to the table, MCU Driver Types, for a description of output drivers. An entry in the discrete I/O column of the MCU Pin Characteristics table indicates that a pin has an alternate I/O function. The port designation is given when it applies. Refer to the MCU Block Diagram for information about port organization.

**Table 2 MCU Pin Characteristic**

Pin Mnemonic	Output Driver	Input Synchronized	Input Hysteresis	Discrete I/O	Port Designation
ADDR23/CS10/ECLK	A	Y	N	O	—
ADDR[22:19]/CS[9:6]	A	Y	N	O	PC[6:3]
ADDR[18:0]	A	Y	N	—	—
$\overline{AS}$	B	Y	N	I/O	PE5
$\overline{AVEC}$	B	Y	N	I/O	PE2
$\overline{BERR}$	B	Y	N	—	—
$\overline{BG/CS1}$	B	—	—	—	—
$\overline{BGACK/CS2}$	B	Y	N	—	—
$\overline{BKPT/DSCLK}$	—	Y	Y	—	—
$\overline{BR/CS0}$	B	Y	N	—	—
CLKOUT	A	—	—	—	—
$\overline{CSBOOT}$	B	—	—	—	—
DATA[15:0] <sup>1</sup>	Aw	Y	N	—	—
$\overline{DS}$	B	Y	N	I/O	PE4
$\overline{DSACK1}$	B	Y	N	I/O	PE1
$\overline{DSACK0}$	B	Y	N	I/O	PE0
DSI/IFETCH	A	Y	Y	—	—
DSO/IPIPE	A	—	—	—	—
EXTAL <sup>2</sup>	—	—	Special	—	—
FC[2:0]/CS[5:3]	A	Y	N	O	PC[2:0]
FREEZE/QUOT	A	—	—	—	—
$\overline{HALT}$	Bo	Y	N	—	—
$\overline{IRQ}[7:1]$	B	Y	Y	I/O	PF[7:1]
MISO	Bo	Y	Y	I/O	PQS0
MODCLK <sup>1</sup>	B	Y	N	I/O	PF0
MOSI	Bo	Y	Y	I/O	PQS1
PCS0/ $\overline{SS}$	Bo	Y	Y	I/O	PQS3
PCS[3:1]	Bo	Y	Y	I/O	PQS[6:4]
R/W	A	Y	N	—	—
$\overline{RESET}$	Bo	Y	Y	—	—
$\overline{RMC}$	B	Y	N	I/O	PE3
RXD	—	N	N	—	—
SCK	Bo	Y	Y	I/O	PQS2
SIZ[1:0]	B	Y	N	I/O	PE[7:6]

**Table 2 MCU Pin Characteristic (Continued)**

Pin Mnemonic	Output Driver	Input Synchronized	Input Hysteresis	Discrete I/O	Port Designation
T2CLK	—	Y	Y	—	—
TPUCH[15:0]	A	Y	Y	—	—
TSC	—	Y	Y	—	—
TXD	Bo	Y	Y	I/O	PQS7
XFC <sup>2</sup>	—	—	—	Special	—
XTAL <sup>2</sup>	—	—	—	Special	—

NOTES:

1. DATA[15:0] are synchronized during reset only. MODCLK is synchronized only when used as an input port pin.
2. EXTAL, XFC, and XTAL are clock reference connections.

## 2.2 MCU Power Connections

**Table 3 MCU Power Connections**

$V_{STBY}$	Standby RAM Power/Clock Synthesizer Power
$V_{DDSYN}$	Clock Synthesizer Power
$V_{SSE}/V_{DDE}$	External Periphery Power (Source and Drain)
$V_{SSI}/V_{DDI}$	Internal Module Power (Source and Drain)

## 2.3 MCU Driver Types

**Table 4 MCU Driver Types**

Type	I/O	Description
A	O	Output-only signals that are always driven; no external pull-up required
Aw	O	Type A output with weak P-channel pull-up during reset
B	O	Three-state output that includes circuitry to pull up output before high impedance is established, to ensure rapid rise time. An external holding resistor is required to maintain logic level while the pin is in the high-impedance state.
Bo	O	Type B output that can be operated in an open-drain mode

## 2.4 Signal Characteristics

**Table 5 MCU Signal Characteristics**

Signal Name	MCU Module	Signal Type	Active State
ADDR[23:0]	SIM	Bus	—
$\overline{AS}$	SIM	Output	0
$\overline{AVEC}$	SIM	Input	0
$\overline{BERR}$	SIM	Input	0
$\overline{BG}$	SIM	Output	0
$\overline{BGACK}$	SIM	Input	0
$\overline{BKPT}$	CPU32	Input	0
$\overline{BR}$	SIM	Input	0
CLKOUT	SIM	Output	—
$\overline{CS}$ [10:0]	SIM	Output	0
$\overline{CSBOOT}$	SIM	Output	0
DATA[15:0]	SIM	Bus	—
$\overline{DS}$	SIM	Output	0
$\overline{DSACK}$ [1:0]	SIM	Input	0
DSCLK	CPU32	Input	Serial Clock
DSI	CPU32	Input	(Serial Data)
DSO	CPU32	Output	(Serial Data)
EXTAL	SIM	Input	—
FC[2:0]	SIM	Output	—
FREEZE	SIM	Output	1
$\overline{HALT}$	SIM	Input/Output	0
$\overline{IFETCH}$	CPU32	Output	—
$\overline{IPIPE}$	CPU32	Output	—
$\overline{IRQ}$ [7:1]	SIM	Input	0
MISO	QSM	Input/Output	—
MODCLK	SIM	Input	—
MOSI	QSM	Input/Output	—
PC[6:0]	SIM	Output	(Port)
PCS[3:0]	QSM	Input/Output	—
PE[7:0]	SIM	Input/Output	(Port)
PF[7:0]	SIM	Input/Output	(Port)
PQS[7:0]	QSM	Input/Output	(Port)
QUOT	SIM	Output	—
$\overline{RESET}$	SIM	Input/Output	0
$\overline{RMC}$	SIM	Output	0
R/W	SIM	Output	1/0
RXD	QSM	Input	—
SCK	QSM	Input/Output	—
SIZ[1:0]	SIM	Output	—
$\overline{SS}$	QSM	Input	0
T2CLK	TPU	Input	—
TPUCH[15:0]	TPU	Input/Output	1

**Table 5 MCU Signal Characteristics (Continued)**

Signal Name	MCU Module	Signal Type	Active State
TSC	SIM	Input	—
TXD	QSM	Output	—
XFC	SIM	Input	—
XTAL	SIM	Output	—

## 2.5 Signal Function

**Table 6 MCU Signal Function**

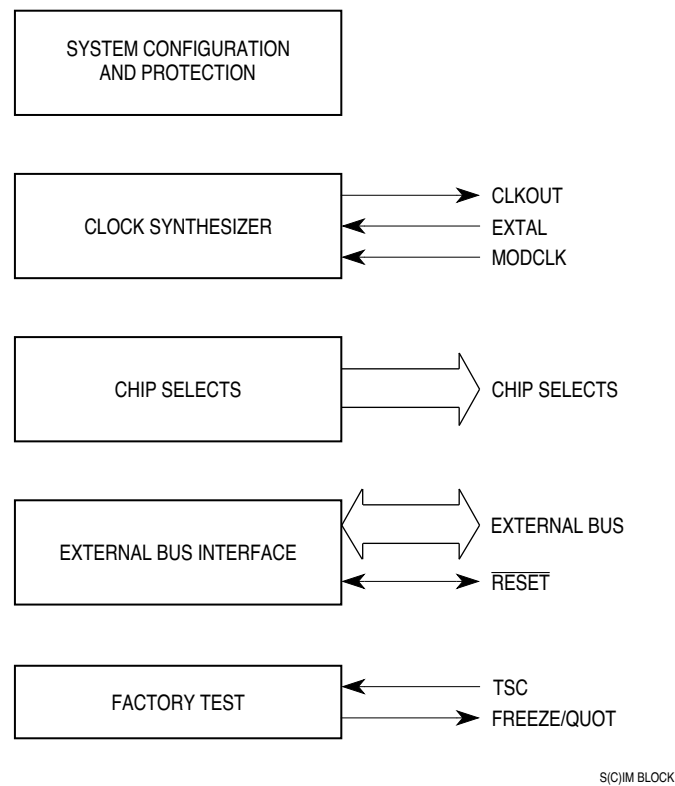
Signal Name	Mnemonic	Function
Address Bus	ADDR[23:0]	24-bit address bus
Address Strobe	$\overline{AS}$	Indicates that a valid address is on the address bus
Autovector	$\overline{AVEC}$	Requests an automatic vector during interrupt acknowledge
Bus Error	$\overline{BERR}$	Indicates that a bus error has occurred
Bus Grant	$\overline{BG}$	Indicates that the MCU has relinquished the bus
Bus Grant Acknowledge	$\overline{BGACK}$	Indicates that an external device has assumed bus mastership
Breakpoint	$\overline{BKPT}$	Signals a hardware breakpoint to the CPU
Bus Request	$\overline{BR}$	Indicates that an external device requires bus mastership
System Clockout	CLKOUT	System clock output
Chip Selects	$\overline{CS}[10:0]$	Select external devices at programmed addresses
Boot Chip Select	$\overline{CSBOOT}$	Chip select for external boot start-up ROM
Data Bus	DATA[15:0]	16-bit data bus
Data Strobe	$\overline{DS}$	During a read cycle, indicates when it is possible for an external device to place data on the data bus. During a write cycle, indicates that valid data is on the data bus.
Data and Size Acknowledge	$\overline{DSACK}[1:0]$	Provide asynchronous data transfers and dynamic bus sizing
Development Serial In, Out, Clock	DSI, DSO, DSCLK	Serial I/O and clock for background debugging mode
Crystal Oscillator	EXTAL, XTAL	Connections for clock synthesizer circuit reference; a crystal or an external oscillator can be used
Function Codes	FC[2:0]	Identify processor state and current address space
Freeze	FREEZE	Indicates that the CPU has entered background mode
Halt	$\overline{HALT}$	Suspend external bus activity
Instruction Pipeline	$\overline{IFETCH}$ $\overline{IPIPE}$	Indicate instruction pipeline activity
Interrupt Request Level	$\overline{IRQ}[7:1]$	Provides an interrupt priority level to the CPU
Master In Slave Out	MISO	Serial input to QSPI in master mode; serial output from QSPI in slave mode
Clock Mode Select	MODCLK	Selects the source and type of system clock
Master Out Slave In	MOSI	Serial output from QSPI in master mode; serial input to QSPI in slave mode
Port C	PC[6:0]	SIM digital output port signals
Peripheral Chip Select	PCS[3:0]	QSPI peripheral chip selects
Port E	PE[7:0]	SIM digital I/O port signals
Port F	PF[7:0]	SIM digital I/O port signals
Port QS	PQS[7:0]	QSM digital I/O port signals

**Table 6 MCU Signal Function (Continued)**

Signal Name	Mnemonic	Function
Quotient Out	QUOT	Provides the quotient bit of the polynomial divider
Reset	RESET	System reset
Read-Modify-Write Cycle	RMC	Indicates an indivisible read-modify-write instruction
Read/Write	R/W	Indicates the direction of data transfer on the bus
SCI Receive Data	RXD	Serial input to the SCI
QSPI Serial Clock	SCK	Clock output from QSPI in master mode; clock input to QSPI in slave mode
Size	SIZ[1:0]	Indicates the number of bytes to be transferred during a bus cycle
Slave Select	SS	Causes serial transmission when QSPI is in slave mode; causes mode fault in master mode
TCR2 Clock	T2CLK	External clock source for TCR2 counter
TPU Channel Pins	TPUCH[15:0]	Bidirectional pins associated with TPU channels
Three-State Control	TSC	Places all output drivers in a high-impedance state
SCI Transmit Data	TXD	Serial output from the SCI
External Filter Capacitor	XFC	Connection for external phase-locked loop filter capacitor

### 3 System Integration Module

The MCU system integration module (SIM) consists of five functional blocks that control system start-up, initialization, configuration, and external bus.



**Figure 5 SIM Block Diagram**

#### 3.1 Overview

The system configuration and protection block controls MCU configuration and operating mode. The block also provides bus and software watchdog monitors.

The system clock generates clock signals used by the SIM, other IMB modules, and external devices. In addition, a periodic interrupt generator supports execution of time-critical control routines.

The external bus interface handles the transfer of information between IMB modules and external address space.

The chip-select block provides eleven general-purpose chip-select signals and a boot ROM chip select signal. Both general-purpose and boot ROM chip-select signals have associated base address registers and option registers.

The system test block incorporates hardware necessary for testing the MCU. It is used to perform factory tests, and its use in normal applications is not supported.

The SIM control register address map occupies 128 bytes. Unused registers within the 128-byte address space return zeros when read. The “Access” column in the SIM address map below indicates which registers are accessible only at the supervisor privilege level and which can be assigned to either the supervisor or user privilege level, according to the value of the SUPV bit in the SIMCR.



**Table 7 SIM Address Map**

Access	Address	15	8	7	0
S	\$YFFA00	SIM CONFIGURATION (SIMCR)			
S	\$YFFA02	FACTORY TEST (SIMTR)			
S	\$YFFA04	CLOCK SYNTHESIZER CONTROL (SYNCR)			
S	\$YFFA06	NOT USED		RESET STATUS REGISTER (RSR)	
S	\$YFFA08	MODULE TEST E (SIMTRE)			
S	\$YFFA0A	NOT USED		NOT USED	
S	\$YFFA0C	NOT USED		NOT USED	
S	\$YFFA0E	NOT USED		NOT USED	
S/U	\$YFFA10	NOT USED		PORT E DATA (PORTE0)	
S/U	\$YFFA12	NOT USED		PORT E DATA (PORTE1)	
S/U	\$YFFA14	NOT USED		PORT E DATA DIRECTION (DDRE)	
S	\$YFFA16	NOT USED		PORT E PIN ASSIGNMENT (PEPAR)	
S/U	\$YFFA18	NOT USED		PORT F DATA (PORTF0)	
S/U	\$YFFA1A	NOT USED		PORT F DATA (PORTF1)	
S/U	\$YFFA1C	NOT USED		PORT F DATA DIRECTION (DDRF)	
S	\$YFFA1E	NOT USED		PORT F PIN ASSIGNMENT (PFPAR)	
S	\$YFFA20	NOT USED		SYSTEM PROTECTION CONTROL (SYPCR)	
S	\$YFFA22	PERIODIC INTERRUPT CONTROL (PICR)			
S	\$YFFA24	PERIODIC INTERRUPT TIMING (PITR)			
S	\$YFFA26	NOT USED		SOFTWARE SERVICE (SWSR)	
S	\$YFFA28	NOT USED		NOT USED	
S	\$YFFA2A	NOT USED		NOT USED	
S	\$YFFA2C	NOT USED		NOT USED	
S	\$YFFA2E	NOT USED		NOT USED	
S	\$YFFA30	TEST MODULE MASTER SHIFT A (TSTMSRA)			
S	\$YFFA32	TEST MODULE MASTER SHIFT B (TSTMSRB)			
S	\$YFFA34	TEST MODULE SHIFT COUNT (TSTSC)			
S	\$YFFA36	TEST MODULE REPETITION COUNTER (TSTRC)			
S	\$YFFA38	TEST MODULE CONTROL (CREG)			
S/U	\$YFFA3A	TEST MODULE DISTRIBUTED REGISTER (DREG)			
	\$YFFA3C	NOT USED		NOT USED	
	\$YFFA3E	NOT USED		NOT USED	
S/U	\$YFFA40	NOT USED		PORT C DATA (PORTC)	
	\$YFFA42	NOT USED		NOT USED	
S	\$YFFA44	CHIP-SELECT PIN ASSIGNMENT (CSPAR0)			
S	\$YFFA46	CHIP-SELECT PIN ASSIGNMENT (CSPAR1)			
S	\$YFFA48	CHIP-SELECT BASE BOOT (CSBARBT)			
S	\$YFFA4A	CHIP-SELECT OPTION BOOT (CSORBT)			
S	\$YFFA4C	CHIP-SELECT BASE 0 (CSBAR0)			
S	\$YFFA4E	CHIP-SELECT OPTION 0 (CSOR0)			
S	\$YFFA50	CHIP-SELECT BASE 1 (CSBAR1)			
S	\$YFFA52	CHIP-SELECT OPTION 1 (CSOR1)			
S	\$YFFA54	CHIP-SELECT BASE 2 (CSBAR2)			

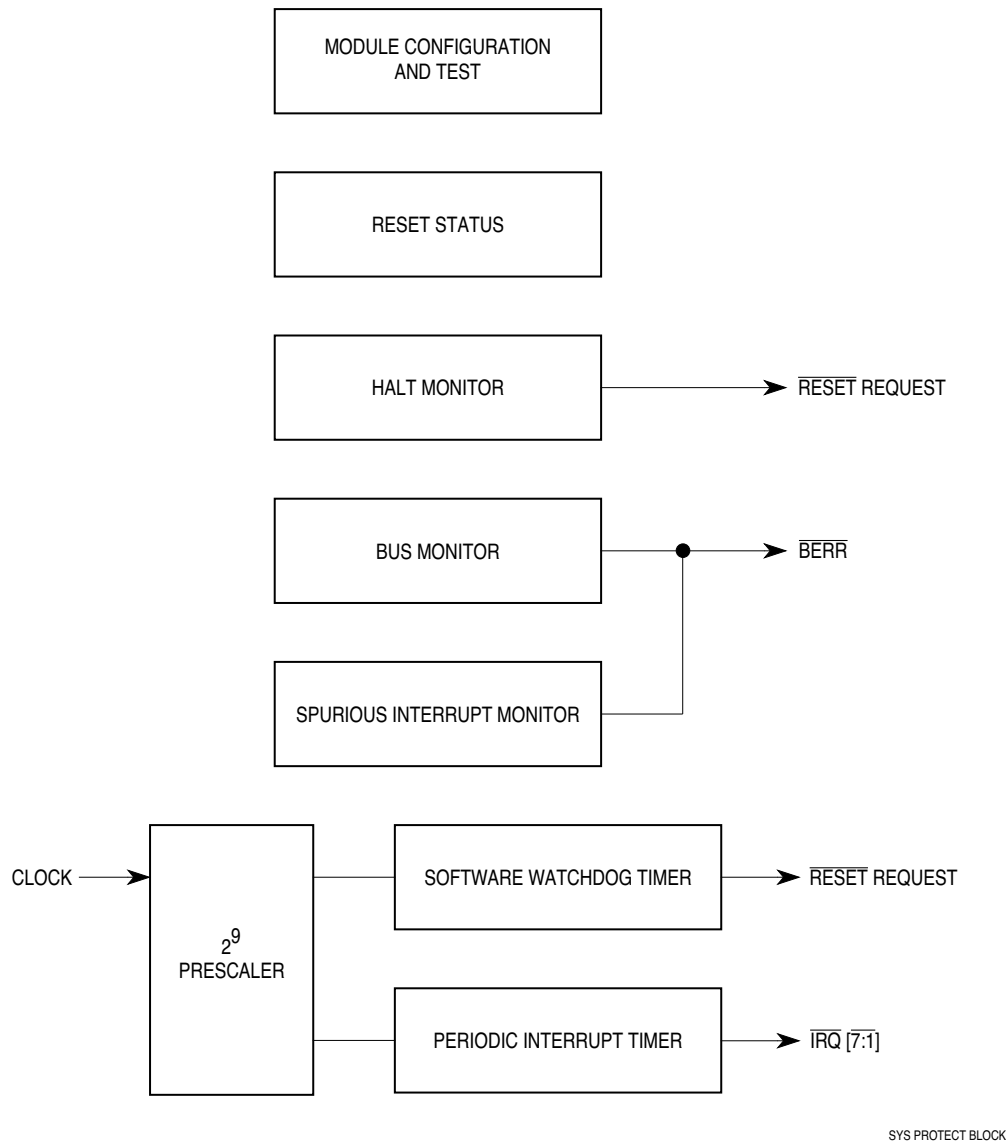
**Table 7 SIM Address Map (Continued)**

Access	Address	15	8	7	0
S	\$YFFA56	CHIP-SELECT OPTION 2 (CSOR2)			
S	\$YFFA58	CHIP-SELECT BASE 3 (CSBAR3)			
S	\$YFFA5A	CHIP-SELECT OPTION 3 (CSOR3)			
S	\$YFFA5C	CHIP-SELECT BASE 4 (CSBAR4)			
S	\$YFFA5E	CHIP-SELECT OPTION 4 (CSOR4)			
S	\$YFFA60	CHIP-SELECT BASE 5 (CSBAR5)			
S	\$YFFA62	CHIP-SELECT OPTION 5 (CSOR5)			
S	\$YFFA64	CHIP-SELECT BASE 6 (CSBAR6)			
S	\$YFFA66	CHIP-SELECT OPTION 6 (CSOR6)			
S	\$YFFA68	CHIP-SELECT BASE 7 (CSBAR7)			
S	\$YFFA6A	CHIP-SELECT OPTION 7 (CSOR7)			
S	\$YFFA6C	CHIP-SELECT BASE 8 (CSBAR8)			
S	\$YFFA6E	CHIP-SELECT OPTION 8 (CSOR8)			
S	\$YFFA70	CHIP-SELECT BASE 9 (CSBAR9)			
S	\$YFFA72	CHIP-SELECT OPTION 9 (CSOR9)			
S	\$YFFA74	CHIP-SELECT BASE 10 (CSBAR10)			
S	\$YFFA76	CHIP-SELECT OPTION 10 (CSOR10)			
	\$YFFA78	NOT USED			NOT USED
	\$YFFA7A	NOT USED			NOT USED
	\$YFFA7C	NOT USED			NOT USED
	\$YFFA7E	NOT USED			NOT USED

Y = M111, where M is the logic state of the module mapping (MM) bit in the SIMCR.

### 3.2 System Configuration and Protection

This functional block provides configuration control for the entire MCU. It also performs interrupt arbitration, bus monitoring, and system test functions. MCU system protection includes a bus monitor, a HALT monitor, a spurious interrupt monitor, and a software watchdog timer. These functions have been made integral to the microcontroller to reduce the number of external components in a complete control system.



**Figure 6 System Configuration and Protection Block**

### 3.2.1 System Configuration

The SIM controls MCU configuration during normal operation and during internal testing.

**SIMCR** —SIM Configuration Register

**\$YFFA00**

15	14	13	12	11	10	9	8	7	6	5	4	3	0
EXOFF	FRZSW	FRZBM	0	SLVEN	0	SHEN	SUPV	MM	0	0	IARB		

RESET:

0	0	0	0	DATA11	0	0	0	1	1	0	0	1	1	1	1
---	---	---	---	--------	---	---	---	---	---	---	---	---	---	---	---

The SIM configuration register controls system configuration. It can be read or written at any time, except for the module mapping (MM) bit, which can be written only once.

**EXOFF** — External Clock Off

- 0 = The CLKOUT pin is driven from an internal clock source.
- 1 = The CLKOUT pin is placed in a high-impedance state.

**FRZSW** — Freeze Software Enable

- 0 = When FREEZE is asserted, the software watchdog and periodic interrupt timer counters continue to run.
- 1 = When FREEZE is asserted, the software watchdog and periodic interrupt timer counters are disabled, preventing interrupts during software debug.

**FRZBM** — Freeze Bus Monitor Enable

- 0 = When FREEZE is asserted, the bus monitor continues to operate.
- 1 = When FREEZE is asserted, the bus monitor is disabled.

**SLVEN** — Factory Test Mode Enabled

- This bit is a read-only status bit that reflects the state of DATA11 during reset.
- 0 = IMB is not available to an external master.
  - 1 = An external bus master has direct access to the IMB.

**SHEN[1:0]** — Show Cycle Enable

This field determines what the EBI does with the external bus during internal transfer operations. A show cycle allows internal transfers to be externally monitored. The table below shows whether show cycle data is driven externally, and whether external bus arbitration can occur. To prevent bus conflict, external peripherals must not be enabled during show cycles.

SHEN	Action
00	Show cycles disabled, external arbitration enabled
01	Show cycles enabled, external arbitration disabled
10	Show cycles enabled, external arbitration enabled
11	Show cycles enabled, external arbitration enabled, internal activity is halted by a bus grant

**SUPV** — Supervisor/Unrestricted Data Space

- The SUPV bit places the SIM global registers in either supervisor or user data space.
- 0 = Registers with access controlled by the SUPV bit are accessible from either the user or supervisor privilege level.
  - 1 = Registers with access controlled by the SUPV bit are restricted to supervisor access only.

**MM** — Module Mapping

- 0 = Internal modules are addressed from \$7FF000 –\$7FFFFFF.
- 1 = Internal modules are addressed from \$FFF000 –\$FFFFFF.

**IARB[3:0]** — Interrupt Arbitration Field

Each module that can generate interrupt requests has an interrupt arbitration (IARB) field. Arbitration between interrupt requests of the same priority is performed by serial contention between IARB field bit values. Contention must take place whenever an interrupt request is acknowledged, even when there is only a single pending request. An IARB field must have a non-zero value for contention to take place. If an interrupt request from a module with an IARB field value of %0000 is recognized, the CPU processes a spurious interrupt exception. Because the SIM routes external interrupt requests to the CPU, the SIM IARB field value is used for arbitration between internal and external interrupts of the same priority. The reset value of IARB for the SIM is %1111, and the reset IARB value for all other modules is %0000, which prevents SIM interrupts from being discarded during initialization.

### 3.2.2 System Protection Control Register

The system protection control register controls system monitor functions, software watchdog clock prescaling, and bus monitor timing. This register can be written only once following power-on or reset, but can be read at any time.

#### SYPCR — System Protection Control Register

**\$YFFA21**

15	8	7	6	5	4	3	2	1	0
NOT USED		SWE	SWP	SWT		HME	BME	BMT	
RESET:									
		1	$\overline{\text{MODCLK}}$	0	0	0	0	0	0

**SWE** — Software Watchdog Enable  
 0 = Software watchdog disabled  
 1 = Software watchdog enabled

**SWP** — Software Watchdog Prescale  
 This bit controls the value of the software watchdog prescaler.  
 0 = Software watchdog clock not prescaled  
 1 = Software watchdog clock prescaled by 512

**SWT[1:0]** — Software Watchdog Timing  
 This field selects the divide ratio used to establish software watchdog time-out period. The following table gives the ratio for each combination of SWP and SWT bits.

SWP	SWT	Ratio
0	00	$2^9$
0	01	$2^{11}$
0	10	$2^{13}$
0	11	$2^{15}$
1	00	$2^{18}$
1	01	$2^{20}$
1	10	$2^{22}$
1	11	$2^{24}$

**HME** — Halt Monitor Enable  
 0 = Disable halt monitor function  
 1 = Enable halt monitor function

**BME** — Bus Monitor External Enable  
 0 = Disable bus monitor function for an internal to external bus cycle.  
 1 = Enable bus monitor function for an internal to external bus cycle.

**BMT[1:0]** — Bus Monitor Timing  
 This field selects a bus monitor time-out period as shown in the following table.

BMT	Bus Monitor Time-out Period
00	64 System Clocks
01	32 System Clocks
10	16 System Clocks
11	8 System Clocks

### 3.2.3 Bus Monitor

The internal bus monitor checks for excessively long  $\overline{DSACK}$  response times during normal bus cycles and for excessively long  $\overline{DSACK}$  or  $\overline{AVEC}$  response times during interrupt acknowledge cycles. The monitor asserts  $\overline{BERR}$  if response time is excessive.

$\overline{DSACK}$  and  $\overline{AVEC}$  response times are measured in clock cycles. The maximum allowable response time can be selected by setting the BMT field.

The monitor does not check  $\overline{DSACK}$  response on the external bus unless the CPU initiates the bus cycle. The BME bit in the SYPCR enables the internal bus monitor for internal to external bus cycles. If a system contains external bus masters, an external bus monitor must be implemented and the internal to external bus monitor option must be disabled.

### 3.2.4 Halt Monitor

The halt monitor responds to an assertion of  $\overline{HALT}$  on the internal bus. A flag in the reset status register (RSR) indicates that the last reset was caused by the halt monitor. The halt monitor reset can be inhibited by the HME bit in the SYPCR.

### 3.2.5 Spurious Interrupt Monitor

The spurious interrupt monitor issues  $\overline{BERR}$  if no interrupt arbitration occurs during an interrupt-acknowledge cycle.

### 3.2.6 Software Watchdog

The software watchdog is controlled by SWE in the SYPCR. Once enabled, the watchdog requires that a service sequence be written to SWSR on a periodic basis. If servicing does not take place, the watchdog times out and issues a reset. This register can be written at any time, but returns zeros when read.

#### SWSR —Software Service Register

**\$YFFA27**

15	8	7	6	5	4	3	2	1	0
NOT USED	0	0	0	0	0	0	0	0	0
RESET:	0	0	0	0	0	0	0	0	0

Register shown with read value

Perform a software watchdog service sequence as follows:

- a. Write \$55 to SWSR.
- b. Write \$AA to SWSR.

Both writes must occur before time-out in the order listed, but any number of instructions can be executed between the two writes.

The watchdog clock rate is affected by SWP and SWT in SYPCR. When SWT[1:0] are modified, a watchdog service sequence must be performed before the new time-out period takes effect.

The reset value of SWP is affected by the state of the MODCLK pin on the rising edge of reset, as shown in the following table.

MODCLK	SWP
0	1
1	0

### 3.2.7 Periodic Interrupt Timer

The periodic interrupt timer (PIT) generates interrupts of specified priorities at specified intervals. Timing for the PIT is provided by a programmable prescaler driven by the system clock.

#### PICR — Periodic Interrupt Control Register

**\$YFFA22**

15	14	13	12	11	10	8	7	0
0	0	0	0	0	PIRQL			PIV

RESET:

0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1

This register contains information concerning periodic interrupt priority and vectoring. Bits [10:0] can be read or written at any time. Bits [15:11] are unimplemented and always return zero.

#### PIRQL[2:0] — Periodic Interrupt Request Level

The following table shows what interrupt request level is asserted when a periodic interrupt is generated. If a PIT interrupt and an external  $\overline{IRQ}$  signal of the same priority occur simultaneously, the PIT interrupt is serviced first. The periodic timer continues to run when the interrupt is disabled.

PIRQL	Interrupt Request Level
000	Periodic Interrupt Disabled
001	Interrupt Request Level 1
010	Interrupt Request Level 2
011	Interrupt Request Level 3
100	Interrupt Request Level 4
101	Interrupt Request Level 5
110	Interrupt Request Level 6
111	Interrupt Request Level 7

#### PIV[7:0] — Periodic Interrupt Vector

The bits of this field contain the vector generated in response to an interrupt from the periodic timer. When the SIM responds, the periodic interrupt vector is placed on the bus.

#### PITR — Periodic Interrupt Timer Register

**\$YFFA24**

15	14	13	12	11	10	9	8	7	0
0	0	0	0	0	0	0	PTP		PITM

RESET:

0 0 0 0 0 0 0 MODCLK 0 0 0 0 0 0 0 0

The PITR contains the count value for the periodic timer. A zero value turns off the periodic timer. This register can be read or written at any time.

#### PTP — Periodic Timer Prescaler Control

- 0 = Periodic timer clock not prescaled
- 1 = Periodic timer clock prescaled by a value of 512

The reset state of PTP is the complement of the state of the MODCLK signal during reset.

#### PITM[7:0] — Periodic Interrupt Timing Modulus Field

This is an 8-bit timing modulus. The period of the timer can be calculated as follows:

$$\text{PIT Period} = [(PITM)(\text{Prescaler})(4)]/\text{EXTAL}$$

where

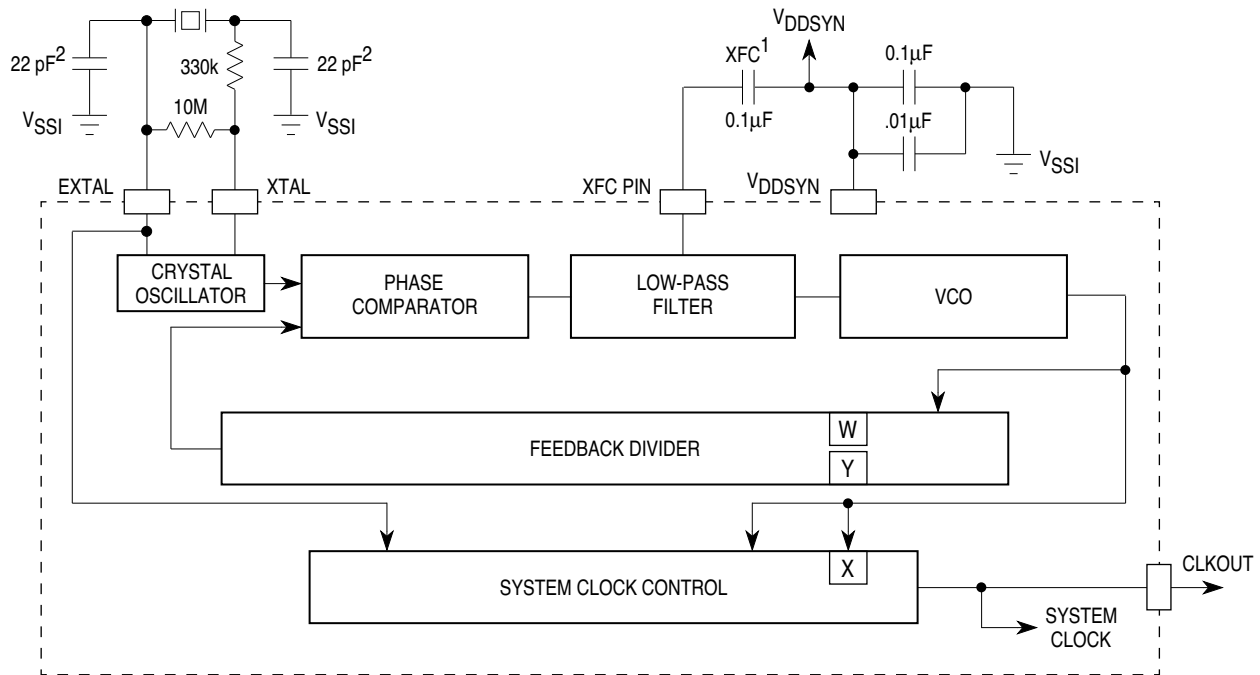
- PIT Period = Periodic interrupt timer period
- PITM = Periodic interrupt timer register modulus (PITR[7:0])
- EXTAL Frequency = Crystal frequency
- Prescale = 512 or 1 depending on the state of the PTP bit in the PITR

### 3.3 System Clock

The system clock in the SIM provides timing signals for the IMB modules and for an external peripheral bus. Because MCU operation is fully static, register and memory contents are not affected when the clock rate changes. System hardware and software support changes in the clock rate during operation.

The system clock signal can be generated in three ways. An internal phase-locked loop can synthesize the clock from an internal or external frequency source, or the clock signal can be input from an external source.

Following is a block diagram of the clock submodule.



1. MUST BE LOW-LEAKAGE CAPACITOR (INSULATION RESISTANCE 30,000 MΩ OR GREATER).
2. RESISTANCE AND CAPACITANCE BASED ON A TEST CIRCUIT CONSTRUCTED WITH A DAISHINKU DMX-38 32.768-kHz CRYSTAL. SPECIFIC COMPONENTS MUST BE BASED ON CRYSTAL TYPE. CONTACT CRYSTAL VENDOR FOR EXACT CIRCUIT.

SYS CLOCK  
BLOCK 32KHZ

**Figure 7 System Clock Block Diagram**

#### 3.3.1 Clock Sources

The state of the clock mode (MODCLK) pin during reset determines the clock source. When MODCLK is held high during reset, the clock synthesizer generates a clock signal from either a crystal oscillator or an external reference input. Clock synthesizer control register SYNCR determines operating frequency and various modes of operation. When MODCLK is held low during reset, the clock synthesizer is disabled, and an external system clock signal must be applied. When the synthesizer is disabled, SYNCR control bits have no effect.

A reference crystal must be connected between the EXTAL and XTAL pins to use the internal oscillator. Use of a 32.768-kHz crystal is recommended. These crystals are inexpensive and readily available. If an external reference signal or an external system clock signal is applied through the EXTAL pin, the XTAL pin must be left floating. External reference signal frequency must be less than or equal to maximum specified reference frequency. External system clock signal frequency must be less than or equal to maximum specified system clock frequency.



When an external system clock signal is applied (i.e., the PLL is not used), duty cycle of the input is critical, especially at near maximum operating frequencies. The relationship between clock signal duty cycle and clock signal period is expressed:

$$\text{Minimum external clock period} = \frac{\text{minimum external clock high/low time}}{50\% - \text{percentage variation of external clock input duty cycle}}$$

### 3.3.2 Clock Synthesizer Operation

A voltage controlled oscillator (VCO) generates the system clock signal. A portion of the clock signal is fed back to a divider/counter. The divider controls the frequency of one input to a phase comparator. The other phase comparator input is a reference signal, either from the internal oscillator or from an external source. The comparator generates a control signal proportional to the difference in phase between its two inputs. The signal is low-pass filtered and used to correct VCO output frequency.

The synthesizer locks when VCO frequency is identical to reference frequency. Lock time is affected by the filter time constant and by the amount of difference between the two comparator inputs. Whenever comparator input changes, the synthesizer must re-lock. Lock status is shown by the SLOCK bit in SYNCR.

The MCU does not come out of reset state until the synthesizer locks. Crystal type, characteristic frequency, and layout of external oscillator circuitry affect lock time.

The low-pass filter requires an external low-leakage capacitor, typically 0.1  $\mu\text{F}$ , connected between the XFC and  $V_{\text{DDSYN}}$  pins.

$V_{\text{DDSYN}}$  is used to power the clock circuits. A separate power source increases MCU noise immunity and can be used to run the clock when the MCU is powered down. Use a quiet power supply as the  $V_{\text{DDSYN}}$  source, since PLL stability depends on the VCO, which uses this supply. Place adequate external bypass capacitors as close as possible to the  $V_{\text{DDSYN}}$  pin to ensure stable operating frequency.

When the clock synthesizer is used, control register SYNCR determines operating frequency and various modes of operation. SYNCR can be read only when the processor is operating at the supervisor privilege level.

The SYNCR X bit controls a divide by two prescaler that is not in the synthesizer feedback loop. Setting X doubles clock speed without changing VCO speed. There is no VCO relock delay. The SYNCR W bit controls a 3-bit prescaler in the feedback divider. Setting W increases VCO speed by a factor of four. The SYNCR Y field determines the count modulus for a modulo 64 down counter, causing it to divide by a value of  $Y + 1$ . When either W or Y value changes, there is a VCO relock delay.

Clock frequency is determined by SYNCR bit settings as follows:

$$F_{\text{SYSTEM}} = F_{\text{REFERENCE}} [4(Y + 1)(2^{2W} + X)]$$

In order for the device to perform correctly, the clock frequency selected by the W, X, and Y bits must be within the limits specified for the MCU.

The VCO frequency is twice the system clock frequency if  $X = 1$  or four times the system clock frequency if  $X = 0$ .

The reset state of SYNCR ( $\$3\text{F}00$ ) produces a modulus-64 count.

### 3.3.3 Clock Control

The clock control circuits determine system clock frequency and clock operation under special circumstances, such as following loss of synthesizer reference or during low-power operation. Clock source is determined by the logic state of the MODCLK pin during reset.

#### SYNCR — Clock Synthesizer Control Register

**\$YFFA04**

15	14	13		8	7	6	5	4	3	2	1	0
W	X	Y			EDIV	0	0	SLIMP	SLOCK	RSTEN	STSIM	STEXT

RESET:

0 0 1 1 1 1 1 1 0 0 0 U U 0 0 0

When the on-chip clock synthesizer is used, system clock frequency is controlled by the bits in the upper byte of SYNCR. Bits in the lower byte show status of or control operation of internal and external clocks. The SYNCR can be read or written only when the CPU is operating at the supervisor privilege level.

#### W — Frequency Control (VCO)

This bit controls a prescaler tap in the synthesizer feedback loop. Setting the bit increases the VCO speed by a factor of four. VCO relock delay is required.

#### X — Frequency Control Bit (Prescale)

This bit controls a divide by two prescaler that is not in the synthesizer feedback loop. Setting the bit doubles clock speed without changing the VCO speed. There is no VCO relock delay.

#### Y[5:0] — Frequency Control (Counter)

The Y field controls the modulus down counter in the synthesizer feedback loop, causing it to divide by a value of Y + 1. Values range from 0 to 63. VCO relock delay is required.

#### EDIV — E Clock Divide Rate

0 = ECLK frequency is system clock divided by 8.

1 = ECLK frequency is system clock divided by 16.

ECLK is an external M6800 bus clock available on pin ADDR23. Refer to **3.5 Chip Selects** for more information.

#### SLIMP — Limp Mode Flag

0 = External crystal is VCO reference.

1 = Loss of crystal reference.

When the on-chip synthesizer is used, loss of reference frequency causes SLIMP to be set. The VCO continues to run using the base control voltage. Maximum limp frequency is maximum specified system clock frequency. X-bit state affects limp frequency.

#### SLOCK — Synthesizer Lock Flag

0 = VCO is enabled, but has not locked.

1 = VCO has locked on the desired frequency (or system clock is external).

The MCU maintains reset state until the synthesizer locks, but SLOCK does not indicate synthesizer lock status until after the user writes to SYNCR.

#### RSTEN — Reset Enable

0 = Loss of crystal causes the MCU to operate in limp mode.

1 = Loss of crystal causes system reset.

#### STSIM — Stop Mode SIM Clock

0 = When LPSTOP is executed, the SIM clock is driven from the crystal oscillator and the VCO is turned off to conserve power.

1 = When LPSTOP is executed, the SIM clock is driven from the VCO.

#### STEXT — Stop Mode External Clock

0 = When LPSTOP is executed, the CLKOUT signal is held negated to conserve power.

1 = When LPSTOP is executed, the CLKOUT signal is driven from the SIM clock, as determined by the state of the STSIM bit.