



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



MC68360

QUad Integrated Communications Controller User's Manual





PREFACE

The complete documentation package for the MC68360 consists of the MC68360UM/AD, *MC68360 QUad Integrated Communications Controller User's Manual*, M68000PM/AD, *MC68000 Family Programmer's Reference Manual*, and the MC68360/D, *MC68360 QUad Integrated Communications Controller Product Brief*.

The *MC68360 QUad Integrated Communications Controller User's Manual* describes the programming, capabilities, registers, and operation of the MC68360 and the MC68EN360; the *MC68000 Family Programmer's Reference Manual* provides instruction details for the MC68360; and the *MC68360 QUad Integrated Communications Controller Product Brief* provides a brief description of the MC68360 capabilities.

This user's manual is organized as follows:

- Section 1 Introduction
- Section 2 Signal Descriptions
- Section 3 Memory Map
- Section 4 Bus Operation
- Section 5 CPU32+
- Section 6 System Integration Module (SIM60)
- Section 7 Communication Processor Module (CPM)
- Section 8 IEEE 1149.1 Test Access Port
- Section 9 Applications
- Section 10 Electrical Characteristics
- Section 11 Ordering Information and Mechanical Data
- Appendix A Serial Performance
- Appendix B Development Tools and Support
- Appendix C RISC Microcode from RAM
- Appendix D MC68MH360 Product Brief

**Home Page:**

www.freescale.com

email:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
(800) 521-6274
480-768-2130

support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)

support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 2666 8080

support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
+800 2666 8080

support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
(800) 441-2447
303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Paragraph Number	Title	Page Number
Section 1		
Introduction		
1.1	QUICC Key Features	1-1
1.2	QUICC Architecture Overview.....	1-4
1.2.1	CPU32+ Core.....	1-5
1.2.2	System Integration Module (SIM60).....	1-5
1.2.3	Communications Processor Module (CPM)	1-6
1.3	Upgrading Designs from the MC68302.....	1-6
1.3.1	Architectural Approach.....	1-6
1.3.2	Hardware Compatibility Issues.....	1-7
1.3.3	Software Compatibility Issues	1-7
1.4	QUICC Glueless System Design.....	1-8
1.5	QUICC Serial Configurations	1-9
1.6	QUICC Serial Configuration Examples	1-16
1.7	QUICC System Bus Configurations	1-17
Section 2		
Signal Descriptions		
2.1	System Bus Signal Index	2-1
2.1.1	Address Bus.....	2-1
2.1.1.1	Address Bus (A27–A0).....	2-1
2.1.1.2	Address Bus (A31–A28).....	2-1
2.1.2	Function Codes (FC3–FC0)	2-5
2.1.3	Data Bus.....	2-5
2.1.3.1	Data Bus (D31–D16).....	2-5
2.1.3.2	Data Bus (D15–D0).....	2-6
2.1.4	Parity	2-6
2.1.4.1	Parity (PRTY0).....	2-6
2.1.4.2	Parity (PRTY1).....	2-6
2.1.4.3	Parity (PRTY2).....	2-6
2.1.4.4	Parity (PRTY3).....	2-6
2.1.5	Memory Controller.....	2-6
2.1.5.1	Chip Select/Row Address Select (CS6–CS0/RAS6–RAS0)	2-6
2.1.5.2	Chip Select/Row Address Select/Interrupt Acknowledge (CS7/RAS7/IACK7).	2-6
2.1.5.3	Column Address Select/Interrupt Acknowledge (CAS3–CAS0/IACK6, 3, 2, 1).	2-7
2.1.5.4	Address Multiplex (AMUX).....	2-7
2.1.6	Interrupt Request Level (IRQ7–IRQ1).....	2-7
2.1.7	Bus Control Signals.....	2-7
2.1.7.1	Data and Size Acknowledge (DSACK1–DSACK0).....	2-8
2.1.7.2	Autovector/Interrupt Acknowledge (AVEC/IACK5).....	2-8
2.1.7.3	Address Strobe (AS).....	2-8
2.1.7.4	Data Strobe (DS).....	2-8

Paragraph Number	Title	Page Number
2.1.7.5	Transfer Size (SIZ1, SIZ0).....	2-8
2.1.7.6	Read/Write (R/W).....	2-8
2.1.7.7	Output Enable/Address Multiplex (OE/AMUX).....	2-9
2.1.7.8	Byte Write Enable (WE3–WE0).	2-9
2.1.8	Bus Arbitration Signals.....	2-9
2.1.8.1	Bus Request (BR).	2-9
2.1.8.2	Bus Grant (BG).	2-9
2.1.8.3	Bus Grant Acknowledge (BGACK).	2-9
2.1.8.4	Read-Modify-Write Cycle/Initial Configuration (RMC/CONFIG0).....	2-9
2.1.8.5	Bus Clear Out/Initial Configuration/Row Address Select Double-Drive (BCL-RO/CONFIG1/RAS2DD).2-9	2-9
2.1.9	System Control Signals.....	2-10
2.1.9.1	Soft Reset (RESETS).	2-10
2.1.9.2	Hard Reset (RESETH).....	2-10
2.1.9.3	Halt (HALT).	2-10
2.1.9.4	Bus Error (BERR).	2-10
2.1.10	Clock Signals	2-10
2.1.10.1	System Clock Outputs (CLKO2–CLKO1).	2-10
2.1.10.2	Crystal Oscillator (EXTAL, XTAL).	2-11
2.1.10.3	External Filter Capacitor (XFC).....	2-11
2.1.10.4	Clock Mode Select (MODCK1–MODCK0).....	2-11
2.1.11	Instrumentation and Emulation Signals	2-11
2.1.11.1	Instruction Fetch/Development Serial Input (IFETCH/DSI).....	2-11
2.1.11.2	Instruction Pipe/Development Serial Output (IPIPE0/DSO).....	2-11
2.1.11.3	Instruction Pipe/Row Address Select Double-Drive (IPIPE1/RAS1DD).....	2-11
2.1.11.4	Breakpoint/Development Serial clock (BKPT/DSCLK).	2-11
2.1.11.5	Freeze/Initial Configuration (FREEZE/CONFIG2).	2-12
2.1.12	Test Signals	2-12
2.1.12.1	TRI-State Signal (TRIS).	2-12
2.1.12.2	Test Reset (TRST).....	2-12
2.1.12.3	Test Clock (TCK).	2-12
2.1.12.4	Test Mode Select (TMS).	2-12
2.1.12.5	Test Data In (TDI).	2-12
2.1.12.6	Test Data Out (TDO).....	2-12
2.1.13	Initial Configuration Pins (CONFIG).....	2-12
2.1.14	Power Signals	2-13
2.1.14.1	VCCSYN and GNDSYN.....	2-13
2.1.14.2	VCCCLK and GNDCLK.	2-13
2.1.14.3	GNDS1 and GNDS2.	2-13
2.1.14.4	VCC and GND.	2-13
2.1.14.5	NC4–NC1.....	2-13
2.2	System Bus Signal Index in Slave Mode	2-14
2.3	On-Chip Peripherals Signal Index.....	2-15

Section 3

Paragraph Number	Title	Page Number
QUICC Memory Map		
3.1	Dual-Port RAM Memory Map	3-2
3.2	CPM Sub-Module Base Addresses.....	3-3
3.3	Internal Registers Memory Map	3-4
3.3.1	SIM Registers Memory Map.....	3-4
3.3.2	CPM Registers Memory Map	3-6
Section 4		
Bus Operation		
4.1	Bus Transfer Signals.....	4-2
4.1.1	Bus Control Signals.....	4-3
4.1.2	Function Codes (FC3–FC0)	4-3
4.1.3	Address Bus (A31–A0).....	4-4
4.1.4	Address Strobe (AS)	4-4
4.1.5	Data Bus (D31–D0).....	4-4
4.1.6	Data Strobe (DS).....	4-4
4.1.7	Output Enable (OE).....	4-4
4.1.8	Byte Write Enable (WE0, WE1, WE2, WE3)	4-4
4.1.9	Bus Cycle Termination Signals	4-5
4.1.9.1	Data transfer and size acknowledge (DSACK1 and DSACK0).....	4-5
4.1.9.2	Bus Error (BERR).....	4-5
4.1.9.3	Autovector (AVEC).....	4-6
4.2	Data Transfer Mechanism	4-6
4.2.1	Dynamic Bus Sizing	4-6
4.2.2	Misaligned Operands	4-11
4.2.3	Effects of Dynamic Bus Sizing and Operand Misalignment	4-19
4.2.4	Bus Operation	4-20
4.2.5	Synchronous Operation with DSACKx.....	4-21
4.2.6	Fast Termination Cycles.....	4-21
4.3	Data Transfer Cycles.....	4-22
4.3.1	Read Cycle.....	4-23
4.3.2	Write Cycle	4-26
4.3.3	Read-Modify-Write Cycle	4-28
4.4	CPU Space Cycles.....	4-31
4.4.1	Breakpoint Acknowledge Cycle.....	4-31
4.4.2	LPSTOP Broadcast Cycle	4-35
4.4.3	Module Base Address Register (MBAR) Access	4-36
4.4.4	Interrupt Acknowledge Bus Cycles.....	4-36
4.4.4.1	Interrupt Acknowledge Cycle—Terminated Normally.....	4-36
4.4.4.2	Autovector Interrupt Acknowledge Cycle.	4-38
4.4.4.3	Spurious Interrupt Cycle.....	4-40
4.5	Bus Exception Control Cycles	4-41
4.5.1	Bus Errors	4-42
4.5.2	Retry Operation.....	4-44
4.5.3	Halt Operation	4-46
4.5.4	Double Bus Fault.....	4-48

Paragraph Number	Title	Page Number
4.6	Bus Arbitration	4-49
4.6.1	Bus Request	4-52
4.6.2	Bus Grant.....	4-53
4.6.3	Bus Grant Acknowledge	4-53
4.6.4	Bus Arbitration Control.....	4-54
4.6.5	Slave (Disable CPU32+) Mode Bus Arbitration	4-55
4.6.6	Slave (Disable CPU32+) Mode Bus Exceptions	4-59
4.6.6.1	HALT.....	4-59
4.6.6.2	RETRY.....	4-59
4.6.7	Internal Accesses.....	4-59
4.6.8	Show Cycles	4-62
4.7	Reset Operation.....	4-63

**Section 5
CPU32+**

5.1	Overview	5-1
5.1.1	Features.....	5-2
5.1.2	Loop Mode Instruction Execution.....	5-3
5.1.3	Vector Base Register	5-4
5.1.4	Exception Handling	5-4
5.1.5	Addressing Modes	5-5
5.2	Architecture Summary	5-5
5.2.1	Programming Model.....	5-6
5.2.2	Registers.....	5-7
5.3	Instruction Set.....	5-8
5.3.1	M68000 Family Compatibility	5-10
5.3.1.1	New Instructions.	5-10
5.3.1.2	Low-Power Stop (LPSTOP).	5-10
5.3.1.3	Table Lookup and Interpolate (TBL).	5-10
5.3.1.4	Unimplemented Instructions.	5-10
5.3.2	Instruction Format and Notation.....	5-10
5.3.3	Instruction Summary	5-13
5.3.3.1	Condition Code Register.....	5-17
5.3.3.2	Data Movement Instructions	5-19
5.3.3.3	Integer Arithmetic Operations	5-19
5.3.3.4	Logic Instructions.	5-21
5.3.3.5	Shift and Rotate Instructions.....	5-22
5.3.3.6	Bit Manipulation Instructions	5-23
5.3.3.7	Binary-Coded Decimal (BCD) Instructions.....	5-24
5.3.3.8	Program Control Instructions	5-24
5.3.3.9	System Control Instructions	5-25
5.3.3.10	Condition Tests.....	5-26
5.3.4	Using the TBL Instructions.....	5-27
5.3.4.1	Table Example 1: Standard Usage	5-28
5.3.4.2	Table Example 2: Compressed Table.....	5-29

Paragraph Number	Title	Page Number
5.3.4.3	Table Example 3: 8-Bit Independent Variable.....	5-30
5.3.4.4	Table Example 4: Maintaining Precision	5-32
5.3.4.5	Table Example 5: Surface Interpolations	5-33
5.3.5	Nested Subroutine Calls.....	5-33
5.3.6	Pipeline Synchronization with the NOP Instruction	5-34
5.4	Processing States	5-34
5.4.1	State Transitions	5-34
5.4.2	Privilege Levels	5-34
5.4.2.1	Supervisor Privilege Level.....	5-35
5.4.2.2	User Privilege Level	5-35
5.4.2.3	Changing Privilege Level.....	5-35
5.5	Exception Processing.....	5-36
5.5.1	Exception Vectors	5-36
5.5.1.1	Types of Exceptions	5-36
5.5.1.2	Exception Processing Sequence.....	5-38
5.5.1.3	Exception Stack Frame	5-38
5.5.1.4	Multiple Exceptions	5-39
5.5.2	Processing of Specific Exceptions	5-40
5.5.2.1	Reset	5-40
5.5.2.2	Bus Error	5-40
5.5.2.3	Address Error	5-42
5.5.2.4	Instruction Traps.....	5-42
5.5.2.5	Software Breakpoints	5-43
5.5.2.6	Hardware Breakpoints.....	5-43
5.5.2.7	Format Error	5-43
5.5.2.8	Illegal or Unimplemented Instructions	5-44
5.5.2.9	Privilege Violations.....	5-44
5.5.2.10	Tracing	5-45
5.5.2.11	Interrupts	5-46
5.5.2.12	Return from Exception.....	5-47
5.5.3	Fault Recovery	5-48
5.5.3.1	Types of Faults.....	5-51
5.5.3.1.1	Type I—Released Write Faults	5-51
5.5.3.1.2	Type II—Prefetch, Operand, RMW, and MOVEP Faults.....	5-51
5.5.3.1.3	Type III—Faults During MOVEM Operand Transfer	5-52
5.5.3.1.4	Type IV—Faults During Exception Processing	5-52
5.5.3.2	Correcting a Fault.....	5-53
5.5.3.2.1	Type I—Completing Released Writes via Software	5-53
5.5.3.2.2	Type I—Completing Released Writes via RTE	5-53
5.5.3.2.3	Type II—Correcting Faults via RTE.....	5-54
5.5.3.2.4	Type III—Correcting Faults via Software.....	5-54
5.5.3.2.5	Type III—Correcting Faults by Conversion and Restart.....	5-55
5.5.3.2.6	Type III—Correcting Faults via RTE.....	5-55
5.5.3.2.7	Type IV—Correcting Faults via Software	5-55
5.5.4	CPU32+ Stack Frames	5-56

Paragraph Number	Title	Page Number
5.5.4.1	Four-Word Stack Frame	5-56
5.5.4.2	Six-Word Stack Frame	5-56
5.5.4.3	Bus Error Stack Frame	5-56
5.6	Development Support	5-59
5.6.1	CPU32+ Integrated Development Support	5-59
5.6.1.1	Background Debug Mode (BDM) Overview	5-59
5.6.1.2	Deterministic Opcode Tracking Overview	5-60
5.6.1.3	On-Chip Hardware Breakpoint Overview	5-60
5.6.2	Background Debug Mode	5-60
5.6.2.1	Enabling BDM	5-60
5.6.2.2	BDM Sources	5-61
5.6.2.2.1	External BKPT Signal	5-62
5.6.2.2.2	BGND Instruction	5-62
5.6.2.2.3	Double Bus Fault	5-62
5.6.2.3	Entering BDM	5-62
5.6.2.4	Command Execution	5-62
5.6.2.5	BDM Registers	5-63
5.6.2.5.1	Fault Address Register (FAR)	5-63
5.6.2.5.2	Return Program Counter (RPC)	5-63
5.6.2.5.3	Current Instruction Program Counter (PCC)	5-63
5.6.2.6	Returning from BDM	5-63
5.6.2.7	Serial Interface	5-63
5.6.2.7.1	CPU Serial Logic	5-65
5.6.2.7.2	Development System Serial Logic	5-66
5.6.2.8	Command Set	5-68
5.6.2.8.1	Command Format	5-68
5.6.2.8.2	Command Sequence Diagram	5-69
5.6.2.8.3	Command Set Summary	5-69
5.6.2.8.4	Read A/D Register (RAREG/RDREG)	5-71
5.6.2.8.5	Write A/D Register (WAREG/WDREG)	5-71
5.6.2.8.6	Read System Register (RSREG)	5-71
5.6.2.8.7	Write System Register (WSREG)	5-72
5.6.2.8.8	Read Memory Location (READ)	5-73
5.6.2.8.9	Write Memory Location (WRITE)	5-74
5.6.2.8.10	Dump Memory Block (DUMP)	5-75
5.6.2.8.11	Fill Memory Block (FILL)	5-76
5.6.2.8.12	Resume Execution (GO)	5-77
5.6.2.8.13	Call User Code (CALL)	5-77
5.6.2.8.14	Reset Peripherals (RST)	5-79
5.6.2.8.15	No Operation (NOP)	5-79
5.6.2.8.16	Future Commands	5-80
5.6.3	Deterministic Opcode Tracking	5-80
5.6.3.1	Instruction Fetch (IFETCH)	5-80
5.6.3.2	Instruction Pipe (IPIPE1–IPIPE0)	5-80
5.6.3.3	Opcode Tracking during Loop Mode	5-82

Paragraph Number	Title	Page Number
5.7	Instruction Execution Timing	5-82
5.7.1	Resource Scheduling	5-83
5.7.1.1	Microsequencer.....	5-83
5.7.1.2	Instruction Pipeline.....	5-83
5.7.1.3	Bus Controller Resources	5-83
5.7.1.3.1	Prefetch Controller	5-84
5.7.1.3.2	Write-Pending Buffer	5-84
5.7.1.3.3	Microbus Controller	5-85
5.7.1.4	Instruction Execution Overlap	5-85
5.7.1.5	Effects of Wait States	5-86
5.7.1.6	Instruction Execution Time Calculation	5-86
5.7.1.7	Effects of Negative Tails.....	5-87
5.7.2	Instruction Timing Tables	5-88
5.7.2.1	Fetch Effective Address	5-90
5.7.2.2	Calculate Effective Address	5-91
5.7.2.3	MOVE Instruction	5-92
5.7.2.4	Special-Purpose MOVE Instruction.....	5-92
5.7.2.5	Arithmetic/Logic Instructions	5-93
5.7.2.6	Immediate Arithmetic/Logic Instructions.....	5-95
5.7.2.7	Binary-Coded Decimal and Extended Instructions.....	5-95
5.7.2.8	Single Operand Instructions	5-96
5.7.2.9	Shift/Rotate Instructions	5-96
5.7.2.10	Bit Manipulation Instructions	5-97
5.7.2.11	Conditional Branch Instructions.....	5-98
5.7.2.12	Control Instructions	5-99
5.7.2.13	Exception-Related Instructions and Operations.....	5-100
5.7.2.14	Save and Restore Operations	5-101

Section 6

System Integration Module (SIM60)

6.1	Module Overview.....	6-1
6.2	Module Base Address Register (MBAR)	6-3
6.3	System Configuration and Protection.....	6-3
6.3.1	System Configuration	6-5
6.3.1.1	SIM60 Interrupt Generation.....	6-6
6.3.1.2	Simultaneous SIM60 Interrupt Sources.....	6-8
6.3.1.2.1	Bus Monitor	6-8
6.3.1.2.2	Spurious Interrupt Monitor.....	6-8
6.3.1.2.3	Double Bus Fault Monitor.....	6-9
6.3.1.2.4	Software Watchdog Timer (SWT)	6-9
6.3.2	Periodic Interrupt Timer (PIT).....	6-10
6.3.2.1	PIT Period Calculation.....	6-10
6.3.2.2	Using the PIT as a Real-Time Clock	6-11
6.3.3	Freeze Support.....	6-11
6.3.4	Low-Power Stop Support	6-11
6.4	Low Power in Normal Operation	6-12

Paragraph Number	Title	Page Number
6.5	SIM60 System Clock Generation.....	6-12
6.5.1	Clock Generation Methods	6-12
6.5.2	Oscillator Prescaler (Divide by 128).....	6-13
6.5.3	Phase-Locked Loop (PLL)	6-14
6.5.3.1	Frequency Multiplication	6-14
6.5.3.2	Skew Elimination.....	6-15
6.5.4	Low-Power Divider.....	6-15
6.5.5	QUICC Internal Clock Signals.....	6-15
6.5.5.1	SPCLK	6-16
6.5.5.2	General System Clock	6-16
6.5.5.3	BRGCLK	6-17
6.5.5.4	SyncCLK.....	6-17
6.5.5.5	SIMCLK.....	6-18
6.5.5.6	CLKO1	6-18
6.5.5.7	CLKO2	6-18
6.5.6	PLL Power Pins	6-19
6.5.6.1	VCCSYN.....	6-19
6.5.6.2	GNDSYN.....	6-19
6.5.6.3	XFC.....	6-19
6.5.7	CLKO Power Pins	6-19
6.5.7.1	VCCCLK	6-19
6.5.7.2	GNDCLK.....	6-19
6.5.8	Configuration Pins (MODCK1–MODCK0)	6-19
6.6	Breakpoint Logic	6-20
6.7	External Bus Interface Control	6-21
6.7.1	Initial Configuration	6-22
6.7.2	Port D.....	6-22
6.7.3	Port E.....	6-23
6.8	Slave (Disable CPU32+) Mode.....	6-23
6.8.1	MBAR in a Multiple QUICC System.....	6-24
6.8.2	Global Chip Select (CS0) in Slave Mode	6-25
6.8.3	Bus Clear in Slave Mode	6-25
6.8.4	Interrupts in Slave Mode	6-26
6.8.5	Pin Differences in Slave Mode.....	6-26
6.8.6	Other Functionality in Slave Mode	6-27
6.9	Programmer's Model.....	6-27
6.9.1	Module Base Address Register (MBAR).....	6-27
6.9.2	Module Base Address Register Enable (MBARE).....	6-29
6.9.3	System Configuration and Protection Registers	6-29
6.9.3.1	Module Configuration Register (MCR).....	6-29
6.9.3.2	Autovector Register (AVR).....	6-34
6.9.3.3	Reset Status Register (RSR)	6-34
6.9.3.4	Software Watchdog Interrupt Vector Register (SWIV).....	6-35
6.9.3.5	System Protection Control Register (SYPCR)	6-35
6.9.3.6	Periodic Interrupt Control Register (PICR).....	6-37

Paragraph Number	Title	Page Number
6.9.3.7	Periodic Interrupt Timer Register (PITR).....	6-38
6.9.3.8	Software Service Register (SWSR).....	6-39
6.9.3.9	CLKO Control Register (CLKOCR).....	6-39
6.9.3.10	PLL Control Register (PLLCR).....	6-40
6.9.3.11	Clock Divider Control Register (CDVCR).....	6-42
6.9.3.12	Breakpoint Address Register (BKAR).....	6-44
6.9.3.13	Breakpoint Control Register (BKCR).....	6-44
6.9.4	Port E Pin Assignment Register (PEPAR).....	6-48
6.10	Memory Controller.....	6-50
6.10.1	Memory Controller Key Features.....	6-50
6.10.2	Memory Controller Overview.....	6-51
6.11	General-Purpose Chip-Select Overview (SRAM Banks).....	6-56
6.11.1	Associated Registers.....	6-56
6.11.2	8-, 16-, and 32-Bit Port Size Configuration.....	6-56
6.11.3	Write Protect Configuration.....	6-56
6.11.4	Programmable Wait State Configuration.....	6-56
6.11.5	Address and Address Space Checking.....	6-57
6.11.6	SRAM Bank Parity.....	6-57
6.11.7	External Master Support.....	6-57
6.11.8	Global (Boot) Chip-Select Operation.....	6-58
6.11.9	SRAM Bus Error.....	6-58
6.12	DRAM Controller Overview (DRAM Banks).....	6-58
6.12.1	DRAM Normal Access Support.....	6-60
6.12.2	DRAM Page Mode Support.....	6-60
6.12.3	DRAM Burst Access Support.....	6-61
6.12.4	DRAM Bank Parity.....	6-62
6.12.5	Refresh Operation.....	6-62
6.12.6	DRAM Bank External Master Support.....	6-63
6.12.7	Double-Drive RAS Lines.....	6-63
6.12.8	DRAM Bus Error.....	6-63
6.13	Programming Model.....	6-64
6.13.1	Global Memory Register (GMR).....	6-64
6.13.2	Memory Controller Status Register (MSTAT).....	6-69
6.13.3	Base Register (BR).....	6-70
6.13.4	Option Register (OR).....	6-74
6.13.5	DRAM-SRAM Performance Summary;.....	6-78

Section 7

Communication Processor Module (CPM)

	Introduction.....	7-1
7.1	RISC Controller.....	7-3
7.1.1	RISC Controller Configuration Register (RCCR).....	7-4
7.1.2	RISC Microcode Revision Number.....	7-5
7.2	Command Set.....	7-5
7.2.1	Command Register Examples.....	7-8
7.2.2	Command Execution Latency.....	7-8

Paragraph Number	Title	Page Number
7.3	Dual-Port RAM.....	7-8
7.3.1	Buffer Descriptors	7-10
7.3.2	Parameter RAM	7-10
7.4	RISC Timer Tables	7-11
7.4.1	RISC Timer Table Parameter RAM	7-12
7.4.2	RISC Timer Table Entries	7-14
7.4.3	RISC Timer Event Register (RTER)	7-14
7.4.4	RISC Timer Mask Register (RTMR)	7-14
7.4.5	SET TIMER Command	7-14
7.4.6	RISC Timer Initialization Sequence	7-14
7.4.7	RISC Timer Initialization Example	7-15
7.4.8	RISC Timer Interrupt Handling.....	7-16
7.4.9	RISC Timer Table Algorithm	7-16
7.4.10	RISC Timer Table Application: Track the RISC Loading	7-16
7.5	Timers	7-17
7.5.1	Timer Key Features	7-17
7.5.2	General-Purpose Timer Units	7-18
7.5.2.1	Cascaded Mode.....	7-19
7.5.2.2	Timer Global Configuration Register (TGCR)	7-20
7.5.2.3	Timer Mode Register (TMR1, TMR2, TMR3, TMR4).....	7-21
7.5.2.4	Timer Reference Registers (TRR1, TRR2, TRR3, TRR4)	7-22
7.5.2.5	Timer Capture Registers (TCR1, TCR2, TCR3, TCR4).....	7-22
7.5.2.6	Timer Counter (TCN1, TCN2, TCN3, TCN4)	7-22
7.5.2.7	Timer Event Registers (TER1, TER2, TER3, TER4)	7-22
7.5.3	Timer Examples	7-23
7.6	IDMA Channels.....	7-24
7.6.1	IDMA Key Features;.....	7-25
7.6.2	IDMA Registers.....	7-26
7.6.2.1	IDMA Channel Configuration Register (ICCR).....	7-26
7.6.2.2	Channel Mode Register (CMR).....	7-28
7.6.2.3	Source Address Pointer Register (SAPR)	7-30
7.6.2.4	Destination Address Pointer Register (DAPR).....	7-31
7.6.2.5	Function Code Register (FCR)	7-31
7.6.2.6	Byte Count Register (BCR).....	7-31
7.6.2.7	Channel Status Register (CSR)	7-32
7.6.2.8	Channel Mask Register (CMAR).....	7-33
7.6.2.9	Data Holding Register (DHR).....	7-33
7.6.3	Interface Signals	7-33
7.6.3.1	DREQ and DACK.....	7-33
7.6.3.2	DONEx.....	7-33
7.6.4	IDMA Operation	7-34
7.6.4.1	Single Buffer	7-34
7.6.4.2	Auto Buffer and Buffer Chaining	7-34
7.6.4.2.1	IDMA Parameter RAM	7-35
7.6.4.2.2	IDMA Buffer Descriptors (BDs).....	7-36

Paragraph Number	Title	Page Number
7.6.4.2.3	IDMA Commands (INIT_IDMA).....	7-38
7.6.4.3	Starting the IDMA.....	7-38
7.6.4.4	Requesting IDMA Transfers.....	7-39
7.6.4.4.1	Internal Maximum Rate.....	7-39
7.6.4.4.2	Internal Limited Rate.....	7-39
7.6.4.4.3	External Burst Mode.....	7-40
7.6.4.4.4	External Cycle Steal.....	7-42
7.6.4.5	IDMA Bus Arbitration.....	7-43
7.6.4.6	IDMA Operand Transfers.....	7-45
7.6.4.6.1	Dual Address Mode.....	7-45
7.6.4.6.2	Single Address Mode (Flyby Transfers).....	7-48
7.6.4.6.3	Fast-Termination Option.....	7-50
7.6.4.6.4	Externally Recognizing IDMA Operand Transfers.....	7-51
7.6.4.7	Bus Exceptions.....	7-51
7.6.4.7.1	Reset.....	7-51
7.6.4.7.2	Bus Error.....	7-51
7.6.4.7.3	Retry.....	7-51
7.6.4.8	Ending the IDMA Transfer.....	7-52
7.6.4.8.1	Single Buffer Mode Termination.....	7-52
7.6.4.8.2	Auto Buffer Mode Termination.....	7-53
7.6.4.8.3	Buffer Chaining Mode Termination.....	7-54
7.6.5	IDMA Examples.....	7-55
7.6.5.1	Single Buffer Examples.....	7-55
7.6.5.2	Buffer Chaining Example.....	7-55
7.6.5.3	Auto Buffer Example.....	7-56
7.7	SDMA Channels.....	7-57
7.7.1	SDMA Bus Arbitration and Bus Transfers.....	7-57
7.7.2	SDMA Registers.....	7-59
7.7.2.1	SDMA Configuration Register (SDCR).....	7-59
7.7.2.2	SDMA Status Register (SDSR).....	7-61
7.7.2.3	SDMA Address Register (SDAR).....	7-61
7.8	Serial Interface with Time Slot Assigner.....	7-62
7.8.1	SI Key Features.....	7-62
7.8.2	TSA Overview.....	7-64
7.8.3	Enabling Connections to the TSA.....	7-67
7.8.4	SI RAM.....	7-68
7.8.4.1	One Multiplexed Channel with Static Frames.....	7-69
7.8.4.2	One Multiplexed Channel with Dynamic Frames.....	7-69
7.8.4.3	Two Multiplexed Channels with Static Frames.....	7-70
7.8.4.4	Two Multiplexed Channels with Dynamic Frames.....	7-71
7.8.4.5	Programming SI RAM Entries.....	7-72
7.8.4.6	SI RAM Programming Example.....	7-75
7.8.4.7	SI RAM Dynamic Changes.....	7-75
7.8.5	SI Registers.....	7-77
7.8.5.1	SI Global Mode Register (SIGMR).....	7-77

Paragraph Number	Title	Page Number
7.8.5.2	SI Mode Register (SIMODE).....	7-78
7.8.5.3	SI Clock Route Register (SICR).....	7-86
7.8.5.4	SI Command Register (SICMR).....	7-87
7.8.5.5	SI Status Register (SISTR).....	7-87
7.8.5.6	SI RAM Pointers (SIRP).....	7-88
7.8.5.6.1	SIRP When RDM = 00 (One Static TDM).....	7-89
7.8.5.6.2	SIRP When RDM = 01 (One Dynamic TDM).....	7-89
7.8.5.6.3	SIRP When RDM = 10 (Two Static TDMs).....	7-90
7.8.5.6.4	SIRP When RDM = 11 (Two Dynamic TDMs).....	7-90
7.8.6	SI IDL Interface Support.....	7-90
7.8.6.1	IDL Interface Example.....	7-91
7.8.6.2	IDL Interface Programming.....	7-95
7.8.7	SI GCI Support.....	7-96
7.8.7.1	SI GCI Activation/Deactivation Procedure.....	7-98
7.8.7.2	SI GCI Programming.....	7-98
7.8.7.2.1	Normal Mode GCI Programming.....	7-98
7.8.7.2.2	SCIT Programming.....	7-98
7.8.8	Serial Interface Synchronization.....	7-100
7.8.9	NMSI Configuration.....	7-100
7.9	Baud Rate Generators (BRGs).....	7-103
7.9.1	Autobaud Support.....	7-105
7.9.2	BRG Configuration Register (BRGC).....	7-106
7.9.3	UART Baud Rate Examples.....	7-108
7.10	Serial Communication Controllers (SCCs).....	7-109
7.10.1	SCC Overview.....	7-110
7.10.2	General SCC Mode Register (GSMR).....	7-111
7.10.3	SCC Protocol-Specific Mode Register (PSMR).....	7-120
7.10.4	SCC Data Synchronization Register (DSR).....	7-121
7.10.5	SCC Transmit on Demand Register (TODR).....	7-121
7.10.6	SCC Buffer Descriptors.....	7-122
7.10.7	SCC Parameter RAM.....	7-124
7.10.7.1	BD Table Pointer (RBASE, TBASE).....	7-125
7.10.7.2	SCC Function Code Registers (RFCR, TFCR).....	7-125
7.10.7.3	Maximum Receive Buffer Length Register (MRBLR).....	7-127
7.10.7.4	Receiver BD Pointer (RBPTR).....	7-127
7.10.7.5	Transmitter BD Pointer (TBPTR).....	7-127
7.10.7.6	Other General Parameters.....	7-128
7.10.8	Interrupts from the SCCs.....	7-128
7.10.8.1	SCC Event Register (SCCE).....	7-128
7.10.8.2	SCC Mask Register (SCCM).....	7-129
7.10.8.3	SCC Status Register (SCCS).....	7-129
7.10.9	SCC Initialization.....	7-129
7.10.10	SCC Interrupt Handling.....	7-130
7.10.11	SCC Timing Control.....	7-130
7.10.11.1	Synchronous Protocols.....	7-130

Paragraph Number	Title	Page Number
7.10.11.2	Asynchronous Protocols.....	7-134
7.10.12	Digital Phase-Locked Loop (DPLL)	7-135
7.10.12.1	Data Encoding.....	7-135
7.10.12.2	DPLL Operation.....	7-136
7.10.13	Clock Glitch Detection	7-139
7.10.14	Disabling the SCCs on the Fly	7-139
7.10.14.1	SCC Transmitter Full Sequence.....	7-140
7.10.14.2	SCC Transmitter Shortcut SEQUENCE	7-140
7.10.14.3	SCC Receiver Full Sequence.....	7-140
7.10.14.4	SCC Receiver Shortcut Sequence	7-141
7.10.14.5	Switching Protocols.....	7-141
7.10.15	Saving Power	7-141
7.10.16	UART Controller	7-141
7.10.16.1	UART Key Features	7-143
7.10.16.2	Normal Asynchronous Mode	7-143
7.10.16.3	Synchronous Mode	7-144
7.10.16.4	UART Memory Map.....	7-145
7.10.16.5	UART Programming Model	7-147
7.10.16.6	UART Command Set.....	7-147
7.10.16.6.1	Transmit Commands.....	7-147
7.10.16.6.2	Receive Commands.....	7-148
7.10.16.7	UART Address Recognition (Receiver).....	7-149
7.10.16.8	UART Control Characters (Receiver).....	7-150
7.10.16.9	Wake-Up Timer (Receiver).....	7-151
7.10.16.10	Break Support (Receiver).....	7-151
7.10.16.11	Send Break (Transmitter)	7-153
7.10.16.12	Sending a Preamble (Transmitter)	7-153
7.10.16.13	Fractional Stop Bits (Transmitter).....	7-153
7.10.16.14	UART Error-Handling Procedure.....	7-154
7.10.16.14.1	Transmission Error	7-155
7.10.16.14.2	Reception Errors	7-155
7.10.16.15	UART Mode Register (PSMR)	7-156
7.10.16.16	UART Receive Buffer Descriptor (Rx BD).....	7-159
7.10.16.17	UART Transmit Buffer Descriptor (Tx BD).....	7-163
7.10.16.18	UART Event Register (SCCE).....	7-164
7.10.16.19	UART Mask Register (SCCM).....	7-167
7.10.16.20	SCC Status Register (SCCS).....	7-167
7.10.16.21	SCC UART Example	7-167
7.10.16.22	S-Records Programming Example	7-169
7.10.17	HDLC Controller	7-169
7.10.17.1	HDLC Controller Key Features.....	7-170
7.10.17.2	HDLC Channel Frame Transmission Processing.....	7-171
7.10.17.3	HDLC Channel Frame Reception Processing.....	7-172
7.10.17.4	HDLC Memory Map.....	7-172
7.10.17.5	HDLC Programming Model	7-174

Paragraph Number	Title	Page Number
7.10.17.6	HDLC Command Set	7-175
7.10.17.6.1	Transmit Commands.....	7-175
7.10.17.6.2	Receive Commands.....	7-176
7.10.17.7	HDLC Error-handling Procedure	7-176
7.10.17.7.1	Transmission Errors.....	7-176
7.10.17.7.2	Reception Errors	7-177
7.10.17.8	HDLC Mode Register (PSMR)	7-178
7.10.17.9	HDLC Receive Buffer Descriptor (Rx BD)	7-179
7.10.17.10	HDLC Transmit Buffer Descriptor (Tx BD)	7-183
7.10.17.11	HDLC Event Register (SCCE)	7-184
7.10.17.12	HDLC Mask Register (SCCM)	7-186
7.10.17.13	SCC Status Register (SCCS)	7-187
7.10.17.14	SCC HDLC Example #1	7-187
7.10.17.15	SCC HDLC Example #2.....	7-189
7.10.18	HDLC Bus Controller	7-189
7.10.18.1	HDLC Bus Key Features.....	7-192
7.10.18.2	HDLC Bus Operation	7-192
7.10.18.2.1	Accessing the HDLC Bus.....	7-192
7.10.18.2.2	More Performance	7-193
7.10.18.2.3	Delayed RTS Mode.....	7-194
7.10.18.2.4	Using the TSA.....	7-195
7.10.18.3	HDLC Bus Memory Map and Programming	7-196
7.10.18.3.1	GSMR Programming.....	7-196
7.10.18.3.2	PSMR Programming	7-196
7.10.18.3.3	HDLC Bus Controller Example	7-196
7.10.19	AppleTalk Controller	7-196
7.10.19.1	LocalTalk Bus Operation.....	7-197
7.10.19.2	Appletalk Controller Key Features	7-198
7.10.19.3	QUICC AppleTalk Hardware Connection.....	7-198
7.10.19.4	AppleTalk Memory Map and Programming Model.....	7-198
7.10.19.4.1	GSMR Programming.....	7-199
7.10.19.4.2	PSMR Programming	7-200
7.10.19.4.3	TODR Programming	7-200
7.10.19.4.4	AppleTalk Controller Example	7-200
7.10.20	BISYNC Controller	7-200
7.10.20.1	BISYNC Controller Features.....	7-201
7.10.20.2	BISYNC Channel Frame Transmission	7-201
7.10.20.3	BISYNC Channel Frame Reception.....	7-202
7.10.20.4	BISYNC Memory Map.....	7-203
7.10.20.5	BISYNC Command Set.....	7-204
7.10.20.5.1	Transmit Commands.....	7-204
7.10.20.5.2	Receive Commands.....	7-205
7.10.20.6	BISYNC Control Character Recognition	7-206
7.10.20.7	BSYNC-BISYNC SYNC Register.....	7-207
7.10.20.8	BDLE-BISYNC DLE Register.....	7-208

Paragraph Number	Title	Page Number
7.10.20.9	Transmitting and Receiving the Synchronization Sequence	7-208
7.10.20.10	BISYNC Error-Handling PROCEDURE.....	7-209
7.10.20.10.1	Transmission Errors	7-209
7.10.20.10.2	Reception Errors	7-209
7.10.20.11	BISYNC Mode Register (PSMR).....	7-209
7.10.20.12	BISYNC Receive Buffer Descriptor (Rx BD)	7-211
7.10.20.13	BISYNC Transmit Buffer Descriptor (Tx BD).....	7-213
7.10.20.14	BISYNC Event Register (SCCE)	7-216
7.10.20.15	BISYNC Mask Register (SCCM).....	7-217
7.10.20.16	SCC Status Register (SCCS).....	7-217
7.10.20.17	Programming the BISYNC Controller.....	7-217
7.10.20.18	SCC BISYNC Example	7-218
7.10.21	Transparent Controller	7-220
7.10.21.1	Transparent Controller Features	7-221
7.10.21.2	Transparent Channel Frame Transmission Processing	7-221
7.10.21.3	Transparent Channel Frame Reception Processing	7-222
7.10.21.4	Achieving Synchronization in Transparent Mode	7-223
7.10.21.4.1	In-Line Synchronization Pattern	7-223
7.10.21.4.2	Transparent Synchronization Example	7-224
7.10.21.5	Transparent Memory Map	7-225
7.10.21.6	Transparent Command Set.....	7-226
7.10.21.6.1	Transmit Commands.....	7-226
7.10.21.6.2	Receive Commands.....	7-227
7.10.21.7	Transparent Error-Handling Procedure	7-227
7.10.21.7.1	Transmission Errors	7-227
7.10.21.7.2	Reception Errors	7-228
7.10.21.8	Transparent Mode Register (PSMR).....	7-228
7.10.21.9	Transparent Receive Buffer Descriptor (Rx BD)	7-228
7.10.21.10	Transparent Transmit Buffer Descriptor (Tx BD).....	7-230
7.10.21.11	Transparent Event Register (SCCE)	7-232
7.10.21.12	Transparent Mask Register (SCCM)	7-233
7.10.21.13	SCC Status Register (SCCS).....	7-233
7.10.21.14	SCC Transparent Example	7-233
7.10.22	RAM Microcodes	7-235
7.10.23	Ethernet Controller	7-235
7.10.23.1	Ethernet On QUICC—MC68EN360	7-236
7.10.23.2	Ethernet Key Features	7-237
7.10.23.3	Learning Ethernet on the QUICC	7-238
7.10.23.4	Connecting QUICC to Ethernet.....	7-239
7.10.23.5	Ethernet Channel Frame Transmission.....	7-241
7.10.23.6	Ethernet Channel Frame Reception.....	7-242
7.10.23.7	CAM Interface	7-243
7.10.23.8	Ethernet Memory Map.....	7-246
7.10.23.9	Ethernet Programming Model	7-250
7.10.23.10	Ethernet Command Set.....	7-250

Paragraph Number	Title	Page Number
7.10.23.10.1	Transmit Commands.....	7-250
7.10.23.10.2	Receive Commands.....	7-251
7.10.23.10.3	SET GROUP ADDRESS Command.....	7-251
7.10.23.11	Ethernet Address Recognition	7-252
7.10.23.12	Hash Table Algorithm	7-253
7.10.23.13	Interpacket Gap Time	7-254
7.10.23.14	Collision Handling	7-254
7.10.23.15	Internal and External Loopback	7-255
7.10.23.16	Ethernet Error-handling Procedure	7-255
7.10.23.16.1	Transmission Errors.....	7-255
7.10.23.16.2	Reception Errors	7-256
7.10.23.17	Ethernet Mode Register (PSMR)	7-256
7.10.23.18	Ethernet Receive Buffer Descriptor (Rx BD).....	7-258
7.10.23.19	Ethernet Transmit Buffer Descriptor (Tx BD).....	7-261
7.10.23.20	Ethernet Event Register (SCCE)	7-264
7.10.23.21	Ethernet Mask Register (SCCM)	7-265
7.10.23.22	Ethernet Status Register (SCCS)	7-265
7.10.23.23	SCC Ethernet Example.....	7-266
7.11	Serial Management Controllers (SMCs)	7-268
7.11.1	SMC Overview	7-268
7.11.2	General SMC Mode Register (SMCMR).....	7-270
7.11.3	SMC Buffer Descriptors	7-270
7.11.4	SMC Parameter RAM	7-270
7.11.4.1	BD Table Pointer (RBASE, TBASE)	7-271
7.11.4.2	SMC Function Code Registers (RFCR, TFCR)	7-272
7.11.4.3	Maximum Receive Buffer Length Register (MRBLR)	7-273
7.11.4.4	Receiver Buffer Descriptor Pointer (RBPTR).....	7-273
7.11.4.5	Transmitter Buffer Descriptor Pointer (TBPTR)	7-274
7.11.4.6	Other General Parameters.....	7-274
7.11.5	Disabling the SMCs on the Fly.....	7-274
7.11.5.1	SMC Transmitter Full Sequence.....	7-275
7.11.5.2	SMC Transmitter Shortcut Sequence	7-275
7.11.5.3	SMC Receiver Full Sequence.....	7-275
7.11.5.4	SMC Receiver Shortcut Sequence	7-276
7.11.5.5	Switching Protocols.....	7-276
7.11.6	Saving Power.....	7-276
7.11.7	SMC as a UART	7-276
7.11.7.1	SMC UART Key Features.....	7-276
7.11.7.2	SMC UART Comparison.....	7-276
7.11.7.3	SMC UART Memory Map	7-277
7.11.7.4	SMC UART Transmission Processing.....	7-278
7.11.7.5	SMC UART Reception Processing	7-279
7.11.7.6	SMC UART Programming Model.....	7-279
7.11.7.7	SMC UART Command Set	7-279
7.11.7.7.1	Transmit Commands.....	7-279

Paragraph Number	Title	Page Number
7.11.7.7.2	Receive Commands	7-280
7.11.7.8	Send Break (Transmitter)	7-280
7.11.7.9	Sending a Preamble (Transmitter)	7-280
7.11.7.10	SMC UART Error-Handling Procedure.....	7-281
7.11.7.10.1	Overrun Error	7-281
7.11.7.10.2	Parity Error	7-281
7.11.7.10.3	Idle Sequence Receive	7-281
7.11.7.10.4	Framing Error	7-281
7.11.7.10.5	Break Sequence.....	7-281
7.11.7.11	SMC UART Mode Register (SMCMR)	7-281
7.11.7.12	SMC UART Receive Buffer Descriptor (Rx BD).....	7-283
7.11.7.13	SMC UART Transmit Buffer Descriptor (Tx BD)	7-286
7.11.7.14	SMC UART Event Register (SMCE)	7-288
7.11.7.15	SMC UART Mask Register (SMCM)	7-290
7.11.8	SMC UART Example.....	7-290
7.11.9	SMC Interrupt Handling.....	7-291
7.11.10	SMC as a Transparent Controller.....	7-291
7.11.10.1	SMC Transparent Controller KEY Features	7-291
7.11.10.2	SMC Transparent Comparison.....	7-292
7.11.10.3	SMC Transparent Memory Map	7-292
7.11.10.4	SMC Transparent Transmission Processing.....	7-292
7.11.10.5	SMC Transparent Reception Processing	7-293
7.11.10.6	Using the SMSYNx Pin for Synchronization.....	7-293
7.11.10.7	Using the TSA for Synchronization	7-295
7.11.10.8	SMC Transparent Command Set.....	7-297
7.11.10.8.1	Transmit Commands.....	7-297
7.11.10.8.2	Receive Commands.....	7-297
7.11.10.9	SMC Transparent Error-Handling Procedure	7-298
7.11.10.9.1	Transmission Error (Underrun).....	7-298
7.11.10.9.2	Reception Error (Overrun).....	7-298
7.11.10.10	SMC Transparent Mode Register (SMCMR).....	7-298
7.11.10.11	SMC Transparent Receive Buffer Descriptor (Rx BD)	7-299
7.11.10.12	SMC Transparent Transmit Buffer Descriptor (Tx BD).....	7-300
7.11.10.13	SMC Transparent Event Register (SMCE).....	7-302
7.11.10.14	SMC Transparent Mask Register (SMCM).....	7-303
7.11.11	SMC Transparent NMSI Example	7-303
7.11.12	SMC Transparent TSA Example	7-304
7.11.13	SMC Interrupt Handling.....	7-305
7.11.14	SMC as a GCI Controller.....	7-305
7.11.14.1	SMC GCI Memory Map	7-306
7.11.14.1.1	SMC Monitor Channel Transmission.....	7-306
7.11.14.1.2	SMC Monitor Channel Reception.....	7-307
7.11.14.2	SMC C/I Channel Handling	7-307
7.11.14.2.1	SMC C/I Channel Transmission	7-307
7.11.14.2.2	SMC C/I Channel Reception	7-307

Paragraph Number	Title	Page Number
7.11.14.3	SMC Commands in GCI Mode	7-307
7.11.14.4	SMC GCI Mode Register (SMCMR)	7-308
7.11.14.5	SMC Monitor Channel Rx BD	7-309
7.11.14.6	SMC Monitor Channel Tx BD.....	7-310
7.11.14.7	SMC C/I Channel Receive Buffer Descriptor (Rx BD)	7-310
7.11.14.8	SMC C/I Channel Transmit Buffer Descriptor (Tx BD).....	7-311
7.11.14.9	SMC Event Register (SMCE).....	7-311
7.11.14.10	SMC Mask Register (SMCM).....	7-312
7.12	Serial Peripheral Interface (SPI)	7-312
7.12.1	Overview	7-312
7.12.2	SPI Key Features.....	7-313
7.12.3	SPI Clocking and Pin Functions.....	7-314
7.12.4	SPI Transmit/Receive Process	7-315
7.12.4.1	SPI Master Mode	7-315
7.12.4.2	SPI Slave Mode	7-316
7.12.4.3	SPI Multi-Master Operation.....	7-316
7.12.5	SPI Programming Model.....	7-317
7.12.5.1	SPI Mode Register (SPMODE).....	7-317
7.12.5.2	SPI Command Register (SPCOM).....	7-319
7.12.5.3	SPI Parameter RAM Memory Map	7-320
7.12.5.3.1	BD Table Pointer (RBASE, TBASE)	7-320
7.12.5.3.2	SPI Function Code Registers (RFCR, TFCR).....	7-321
7.12.5.3.3	Maximum Receive Buffer Length Register (MRBLR)	7-322
7.12.5.3.4	Receiver Buffer Descriptor Pointer (RBPTR).....	7-322
7.12.5.3.5	Transmitter Buffer Descriptor Pointer (TBPTR)	7-323
7.12.5.3.6	Other General Parameters.....	7-323
7.12.5.4	SPI Commands.....	7-323
7.12.5.4.1	INIT TX PARAMETERS Command	7-323
7.12.5.4.2	CLOSE Rx BD Command.....	7-323
7.12.5.4.3	INIT RX PARAMETERS Command.....	7-323
7.12.5.5	SPI Buffer Descriptor Ring.....	7-324
7.12.5.5.1	SPI Receive Buffer Descriptor (Rx BD)	7-324
7.12.5.5.2	SPI Transmit Buffer Descriptor (Tx BD).....	7-326
7.12.5.6	SPI Event Register (SPIE)	7-328
7.12.5.7	SPI Mask Register (SPIM).....	7-329
7.12.6	SPI Master Example	7-329
7.12.7	SPI Slave Example	7-330
7.12.8	SPI Interrupt Handling.....	7-331
7.13	Parallel Interface Port (PIP)	7-331
7.13.1	PIP Key Features.....	7-331
7.13.2	PIP Overview	7-332
7.13.3	General-Purpose I/O Pins (Port B)	7-333
7.13.4	Interlocked Data Transfers.....	7-333
7.13.5	Pulsed Data Transfers	7-334
7.13.5.1	Busy Signal.....	7-335

Paragraph Number	Title	Page Number
7.13.5.2	Pulsed Handshake Timing	7-336
7.13.6	Transparent Data Transfers	7-338
7.13.7	Programming Model	7-338
7.13.7.1	Parameter RAM.....	7-338
7.13.7.2	PIP Configuration Register (PIPC)	7-339
7.13.7.3	PIP Timing Parameters Register (PTPR).....	7-341
7.13.7.4	PIP Buffer Descriptors.....	7-341
7.13.7.5	PIP Event Register (PIPE)	7-341
7.13.7.6	PIP Mask Register (PIPM)	7-342
7.13.8	Centronics Controller Overview.....	7-342
7.13.8.1	Centronics Controller Key Features	7-344
7.13.8.2	Centronics Channel Transmission	7-345
7.13.8.3	Centronics Transmitter Memory Map.....	7-345
7.13.8.4	Buffer Descriptor Table Pointer (TBASE).....	7-346
7.13.8.5	Status Mask Register (SMASK)	7-346
7.13.8.6	Centronics Function Code Register (CFCR).....	7-346
7.13.8.7	Transmitter Buffer Descriptor Pointer (TBPTR).....	7-347
7.13.8.8	Centronics Transmitter Programming Model.....	7-347
7.13.8.9	Centronics Transmitter Command Set.....	7-347
7.13.8.9.1	<i>STOP TRANSMIT</i> Command.....	7-347
7.13.8.9.2	<i>RESTART TRANSMIT</i> Command.....	7-347
7.13.8.9.3	<i>INIT TX PARAMETERS</i> Command.....	7-348
7.13.8.10	Transmission Errors	7-348
7.13.8.10.1	Buffer Descriptor Not Ready	7-348
7.13.8.10.2	Printer Off-Line Error	7-348
7.13.8.10.3	Printer Fault.....	7-348
7.13.8.10.4	Paper Error.....	7-348
7.13.8.10.5	Centronics Transmitter Buffer Descriptor	7-348
7.13.8.11	Centronics Transmitter Event Register (PIPE).....	7-349
7.13.8.12	Centronics Channel Reception.....	7-350
7.13.8.13	Centronics Receiver Memory Map	7-350
7.13.8.14	Buffer Descriptor Table Pointer (RBASE)	7-351
7.13.8.15	Centronics Function Code Register (CFCR).....	7-351
7.13.8.16	Receiver Buffer Descriptor Pointer (RBPTR)	7-352
7.13.8.17	Centronics Receiver Programming Model.....	7-352
7.13.8.18	Centronics Control Characters	7-352
7.13.8.19	Centronics Silence Period	7-354
7.13.8.20	Centronics Receiver Command Set.....	7-354
7.13.8.20.1	<i>INIT RX PARAMETERS</i> Command	7-354
7.13.8.20.2	<i>CLOSE RX BD</i> Command.....	7-354
7.13.8.21	Receiver Errors	7-354
7.13.8.21.1	Buffer Descriptor Busy	7-354
7.13.8.22	Centronics Receive Buffer Descriptor	7-354
7.13.8.23	Centronics Receiver Event Register (PIPE).....	7-355
7.13.9	Port B Registers	7-356

Paragraph Number	Title	Page Number
7.13.9.1	Port B Assignment Registers (PBPARG)	7-356
7.13.9.2	Data Direction Register (PBDIR)	7-356
7.13.9.3	Data Register (PBDAT).....	7-356
7.13.9.4	Open-Drain Register (PBODR).....	7-356
7.14	Parallel I/O Ports.....	7-356
7.14.1	Parallel I/O Key Features.....	7-357
7.14.2	Parallel I/O Overview	7-357
7.14.3	Port A Pin Functions	7-357
7.14.4	Port A Registers.....	7-359
7.14.4.1	Port A Open-Drain Register (PAODR).....	7-359
7.14.4.2	Port A Data Register (PADAT).....	7-359
7.14.4.3	Port A Data Direction Register (PADIR)	7-359
7.14.4.4	Port A Pin Assignment Register (PAPAR).....	7-359
7.14.5	Port A Examples	7-360
7.14.6	Port B Pin Functions	7-362
7.14.7	Port B Registers.....	7-363
7.14.7.1	Port B Open-Drain Register (PBODR).....	7-363
7.14.7.2	Port B Data Register (PBDAT).....	7-364
7.14.7.3	Port B Data Direction Register (PBDIR)	7-364
7.14.7.4	Port B Pin Assignment Register (PBPARG).....	7-364
7.14.8	Port B Example	7-365
7.14.9	Port C Pin Functions	7-365
7.14.10	Port C Registers.....	7-367
7.14.10.1	Port C Data Register (PCDAT)	7-368
7.14.10.2	Port C Data Direction Register (PCDIR)	7-368
7.14.10.3	Port C Pin Assignment Register (PCPAR).....	7-368
7.14.10.4	Port C Special Options (PCSO)	7-368
7.14.10.5	Port C Interrupt Control Register (PCINT)	7-369
7.15	CPM Interrupt Controller (CPIC).....	7-369
7.15.1	Overview	7-370
7.15.2	CPM Interrupt Source Priorities	7-372
7.15.2.1	SCC Relative Priority	7-372
7.15.2.2	Highest Priority Interrupt	7-372
7.15.2.3	Nested Interrupts	7-373
7.15.3	Masking Interrupt Sources in the CPM	7-374
7.15.4	Interrupt Vector Generation and Calculation.....	7-375
7.15.5	CPIC Programming Model	7-377
7.15.5.1	CPM Interrupt Configuration Register (CICR).....	7-377
7.15.5.2	CPM Interrupt Pending Register (CIPR)	7-379
7.15.5.3	CPM Interrupt Mask Register (CIMR).....	7-380
7.15.5.4	CPM Interrupt In-Service Register (CISR)	7-380
7.15.6	Interrupt Handler Examples	7-381
7.15.6.1	Example 1—PC6 Interrupt Handler	7-381
7.15.6.2	Example 2—SCC1 Interrupt Handler.....	7-381

Paragraph Number	Title	Page Number
Section 8		
Scan Chain Test Access Port		
8.1	Overview	8-1
8.2	TAP Controller.....	8-2
8.3	Boundary Scan Register	8-3
8.4	Instruction Register	8-10
8.4.1	EXTEST	8-10
8.4.2	SAMPLE/PRELOAD.....	8-10
8.4.3	BYPASS.....	8-11
8.4.4	CLAMP	8-11
8.4.5	HI-Z	8-11
8.5	QUICC Restrictions.....	8-11
8.6	Non-Scan Chain Operation	8-12
Section 9		
Applications		
9.1	Minimum System Configuration	9-1
9.1.1	QUICC Hardware Configuration.....	9-1
9.1.1.1	QUICC Basic Accesses.....	9-1
9.1.1.2	Clocking Strategy.	9-3
9.1.1.3	Resetting the QUICC.....	9-3
9.1.1.4	Interrupts.	9-3
9.1.1.5	Bus Arbitration.....	9-3
9.1.1.6	Breakpoint Generation.	9-3
9.1.1.7	Bus Monitor Function.	9-3
9.1.1.8	Spurious Interrupt Monitor.....	9-3
9.1.1.9	Software Watchdog.....	9-3
9.1.1.10	Double Bus Fault.....	9-4
9.1.1.11	JTAG and Three-State.	9-4
9.1.1.12	QUICC Serial Ports.	9-4
9.1.2	Memory Interfaces.....	9-4
9.1.2.1	QUICC Memory Interface Pins.....	9-4
9.1.2.2	Regular EPROM.....	9-5
9.1.2.3	Flash EPROM.	9-5
9.1.2.4	SRAM.....	9-6
9.1.2.5	EEPROM.....	9-7
9.1.2.6	DRAM SIMM.	9-8
9.1.2.7	DRAM Devices.	9-9
9.1.3	Software Configuration.....	9-10
9.1.3.1	Basic Initialization.....	9-10
9.1.3.2	Configuring the Memory Controller.	9-11
9.1.3.3	Using the QUICC in 16-Bit Data Bus Mode.....	9-12
9.2	How to take A QUICC Software Test-Drive.....	9-13
	Step 1: Decide on Reset Stack Pointer and Initial Program Counter	9-13
	Step 2: Stay in Supervisor Mode.....	9-13
	Step 3: Write the VBR	9-14