



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





MC68336/376

USER'S MANUAL

TouCAN is a trademark of Motorola, Inc.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. MOTOROLA and ! are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

© MOTOROLA, INC. 1996



TABLE OF CONTENTS

Paragraph	Title	Page
-----------	-------	------

SECTION 1 INTRODUCTION

SECTION 2 NOMENCLATURE

2.1	Symbols and Operators	2-1
2.2	CPU32 Registers	2-2
2.3	Pin and Signal Mnemonics	2-2
2.4	Register Mnemonics	2-4
2.5	Conventions	2-8

SECTION 3 OVERVIEW

3.1	MCU Features	3-1
3.1.1	Central Processing Unit (CPU32)	3-1
3.1.2	System Integration Module (SIM)	3-1
3.1.3	Standby RAM Module (SRAM)	3-1
3.1.4	Masked ROM Module (MRM)	3-1
3.1.5	10-Bit Queued Analog-to-Digital Converter (QADC)	3-2
3.1.6	Queued Serial Module (QSM)	3-2
3.1.7	Configurable Timer Module Version 4 (CTM4)	3-2
3.1.8	Time Processor Unit (TPU)	3-2
3.1.9	Static RAM Module with TPU Emulation Capability (TPURAM)	3-2
3.1.10	CAN 2.0B Controller Module (TouCAN)	3-3
3.2	Intermodule Bus	3-3
3.3	System Block Diagram and Pin Assignment Diagrams	3-3
3.4	Pin Descriptions	3-6
3.5	Signal Descriptions	3-9
3.6	Internal Register Map	3-13
3.7	Address Space Maps	3-14

SECTION 4 CENTRAL PROCESSOR UNIT

4.1	General	4-1
4.2	CPU32 Registers	4-2
4.2.1	Data Registers	4-4
4.2.2	Address Registers	4-5
4.2.3	Program Counter	4-6
4.2.4	Control Registers	4-6
4.2.4.1	Status Register	4-6
4.2.4.2	Alternate Function Code Registers	4-7
4.2.5	Vector Base Register (VBR)	4-7
4.3	Memory Organization	4-7



TABLE OF CONTENTS (Continued)

Paragraph	Title	Page
4.4	Virtual Memory	4-9
4.5	Addressing Modes	4-9
4.6	Processing States	4-9
4.7	Privilege Levels	4-10
4.8	Instructions	4-10
4.8.1	M68000 Family Compatibility	4-14
4.8.2	Special Control Instructions	4-14
4.8.2.1	Low-Power Stop (LPSTOP)	4-14
4.8.2.2	Table Lookup and Interpolate (TBL)	4-14
4.8.2.3	Loop Mode Instruction Execution	4-15
4.9	Exception Processing	4-15
4.9.1	Exception Vectors	4-15
4.9.2	Types of Exceptions	4-17
4.9.3	Exception Processing Sequence	4-17
4.10	Development Support	4-17
4.10.1	M68000 Family Development Support	4-18
4.10.2	Background Debug Mode	4-18
4.10.3	Enabling BDM	4-19
4.10.4	BDM Sources	4-19
4.10.4.1	External BKPT Signal	4-20
4.10.4.2	BGND Instruction	4-20
4.10.4.3	Double Bus Fault	4-20
4.10.4.4	Peripheral Breakpoints	4-20
4.10.5	Entering BDM	4-20
4.10.6	BDM Commands	4-21
4.10.7	Background Mode Registers	4-22
4.10.7.1	Fault Address Register (FAR)	4-22
4.10.7.2	Return Program Counter (RPC)	4-22
4.10.7.3	Current Instruction Program Counter (PCC)	4-23
4.10.8	Returning from BDM	4-23
4.10.9	Serial Interface	4-23
4.10.10	Recommended BDM Connection	4-25
4.10.11	Deterministic Opcode Tracking	4-26
4.10.12	On-Chip Breakpoint Hardware	4-26

SECTION 5 SYSTEM INTEGRATION MODULE

5.1	General	5-1
5.2	System Configuration	5-2
5.2.1	Module Mapping	5-2
5.2.2	Interrupt Arbitration	5-2
5.2.3	Show Internal Cycles	5-3



TABLE OF CONTENTS (Continued)

Paragraph	Title	Page
5.2.4	Register Access	5-3
5.2.5	Freeze Operation	5-3
5.3	System Clock	5-4
5.3.1	Clock Sources	5-4
5.3.2	Clock Synthesizer Operation	5-5
5.3.3	External Bus Clock	5-12
5.3.4	Low-Power Operation	5-12
5.4	System Protection	5-14
5.4.1	Reset Status	5-14
5.4.2	Bus Monitor	5-14
5.4.3	Halt Monitor	5-15
5.4.4	Spurious Interrupt Monitor	5-15
5.4.5	Software Watchdog	5-15
5.4.6	Periodic Interrupt Timer	5-17
5.4.7	Interrupt Priority and Vectoring	5-18
5.4.8	Low-Power STOP Mode Operation	5-19
5.5	External Bus Interface	5-19
5.5.1	Bus Control Signals	5-21
5.5.1.1	Address Bus	5-21
5.5.1.2	Address Strobe	5-21
5.5.1.3	Data Bus	5-21
5.5.1.4	Data Strobe	5-22
5.5.1.5	Read/Write Signal	5-22
5.5.1.6	Size Signals	5-22
5.5.1.7	Function Codes	5-22
5.5.1.8	Data and Size Acknowledge Signals	5-23
5.5.1.9	Bus Error Signal	5-23
5.5.1.10	Halt Signal	5-23
5.5.1.11	Autovector Signal	5-24
5.5.2	Dynamic Bus Sizing	5-24
5.5.3	Operand Alignment	5-25
5.5.4	Misaligned Operands	5-25
5.5.5	Operand Transfer Cases	5-26
5.6	Bus Operation	5-26
5.6.1	Synchronization to CLKOUT	5-26
5.6.2	Regular Bus Cycles	5-27
5.6.2.1	Read Cycle	5-28
5.6.2.2	Write Cycle	5-29
5.6.3	Fast Termination Cycles	5-30
5.6.4	CPU Space Cycles	5-30
5.6.4.1	Breakpoint Acknowledge Cycle	5-31



TABLE OF CONTENTS (Continued)

Paragraph	Title	Page
5.6.4.2	LPSTOP Broadcast Cycle	5-34
5.6.5	Bus Exception Control Cycles	5-34
5.6.5.1	Bus Errors	5-36
5.6.5.2	Double Bus Faults	5-36
5.6.5.3	Retry Operation	5-37
5.6.5.4	Halt Operation	5-37
5.6.6	External Bus Arbitration	5-38
5.6.6.1	Show Cycles	5-39
5.7	Reset	5-40
5.7.1	Reset Exception Processing	5-40
5.7.2	Reset Control Logic	5-40
5.7.3	Reset Mode Selection	5-41
5.7.3.1	Data Bus Mode Selection	5-42
5.7.3.2	Clock Mode Selection	5-44
5.7.3.3	Breakpoint Mode Selection	5-45
5.7.4	MCU Module Pin Function During Reset	5-45
5.7.5	Pin States During Reset	5-46
5.7.5.1	Reset States of SIM Pins	5-46
5.7.5.2	Reset States of Pins Assigned to Other MCU Modules	5-47
5.7.6	Reset Timing	5-47
5.7.7	Power-On Reset	5-48
5.7.8	Use of the Three-State Control Pin	5-49
5.7.9	Reset Processing Summary	5-50
5.7.10	Reset Status Register	5-50
5.8	Interrupts	5-50
5.8.1	Interrupt Exception Processing	5-50
5.8.2	Interrupt Priority and Recognition	5-51
5.8.3	Interrupt Acknowledge and Arbitration	5-52
5.8.4	Interrupt Processing Summary	5-53
5.8.5	Interrupt Acknowledge Bus Cycles	5-54
5.9	Chip-Selects	5-54
5.9.1	Chip-Select Registers	5-57
5.9.1.1	Chip-Select Pin Assignment Registers	5-57
5.9.1.2	Chip-Select Base Address Registers	5-58
5.9.1.3	Chip-Select Option Registers	5-59
5.9.1.4	Port C Data Register	5-60
5.9.2	Chip-Select Operation	5-60
5.9.3	Using Chip-Select Signals for Interrupt Acknowledge	5-61
5.9.4	Chip-Select Reset Operation	5-62
5.10	Parallel Input/Output Ports	5-64
5.10.1	Pin Assignment Registers	5-64



TABLE OF CONTENTS (Continued)

Paragraph	Title	Page
5.10.2	Data Direction Registers	5-64
5.10.3	Data Registers	5-64
5.11	Factory Test	5-64

SECTION 6 STANDBY RAM MODULE

6.1	SRAM Register Block	6-1
6.2	SRAM Array Address Mapping	6-1
6.3	SRAM Array Address Space Type	6-1
6.4	Normal Access	6-2
6.5	Standby and Low-Power Stop Operation	6-2
6.6	Reset	6-3

SECTION 7 MASKED ROM MODULE

7.1	MRM Register Block	7-1
7.2	MRM Array Address Mapping	7-1
7.3	MRM Array Address Space Type	7-2
7.4	Normal Access	7-2
7.5	Low-Power Stop Mode Operation	7-3
7.6	ROM Signature	7-3
7.7	Reset	7-3

SECTION 8 QUEUED ANALOG-TO-DIGITAL CONVERTER MODULE

8.1	General	8-1
8.2	QADC Address Map	8-2
8.3	QADC Registers	8-2
8.4	QADC Pin Functions	8-2
8.4.1	Port A Pin Functions	8-3
8.4.1.1	Port A Analog Input Pins	8-4
8.4.1.2	Port A Digital Input/Output Pins	8-4
8.4.2	Port B Pin Functions	8-4
8.4.2.1	Port B Analog Input Pins	8-4
8.4.2.2	Port B Digital Input Pins	8-4
8.4.3	External Trigger Input Pins	8-5
8.4.4	Multiplexed Address Output Pins	8-5
8.4.5	Multiplexed Analog Input Pins	8-5
8.4.6	Voltage Reference Pins	8-5
8.4.7	Dedicated Analog Supply Pins	8-6
8.4.8	External Digital Supply Pin	8-6
8.4.9	Digital Supply Pins	8-6



TABLE OF CONTENTS (Continued)

Paragraph	Title	Page
8.5	QADC Bus Interface	8-6
8.6	Module Configuration	8-6
8.6.1	Low-Power Stop Mode	8-6
8.6.2	Freeze Mode	8-7
8.6.3	Supervisor/Unrestricted Address Space	8-7
8.6.4	Interrupt Arbitration Priority	8-8
8.7	Test Register	8-8
8.8	General-Purpose I/O Port Operation	8-8
8.8.1	Port Data Register	8-9
8.8.2	Port Data Direction Register	8-9
8.9	External Multiplexing Operation	8-10
8.10	Analog Input Channels	8-12
8.11	Analog Subsystem	8-12
8.11.1	Conversion Cycle Times	8-13
8.11.1.1	Amplifier Bypass Mode Conversion Timing	8-14
8.11.2	Front-End Analog Multiplexer	8-15
8.11.3	Digital to Analog Converter Array	8-15
8.11.4	Comparator	8-16
8.11.5	Successive Approximation Register	8-16
8.12	Digital Control Subsystem	8-16
8.12.1	Queue Priority	8-16
8.12.2	Queue Boundary Conditions	8-19
8.12.3	Scan Modes	8-20
8.12.3.1	Disabled Mode and Reserved Mode	8-20
8.12.3.2	Single-Scan Modes	8-20
8.12.3.3	Continuous-Scan Modes	8-22
8.12.4	QADC Clock (QCLK) Generation	8-24
8.12.5	Periodic/Interval Timer	8-27
8.12.6	Control and Status Registers	8-28
8.12.6.1	Control Register 0 (QACR0)	8-28
8.12.6.2	Control Register 1 (QACR1)	8-28
8.12.6.3	Control Register 2 (QACR2)	8-28
8.12.6.4	Status Register (QASR)	8-28
8.12.7	Conversion Command Word Table	8-28
8.12.8	Result Word Table	8-31
8.13	Interrupts	8-32
8.13.1	Interrupt Sources	8-32
8.13.2	Interrupt Register	8-32
8.13.3	Interrupt Vectors	8-33
8.13.4	Initializing the QADC for Interrupt Driven Operation	8-34

SECTION 9 QUEUED SERIAL MODULE



TABLE OF CONTENTS (Continued)

Paragraph	Title	Page
9.1	General	9-1
9.2	QSM Registers and Address Map	9-2
9.2.1	QSM Global Registers	9-2
9.2.1.1	Low-Power Stop Operation	9-2
9.2.1.2	Freeze Operation	9-3
9.2.1.3	QSM Interrupts	9-3
9.2.2	QSM Pin Control Registers	9-4
9.3	Queued Serial Peripheral Interface	9-5
9.3.1	QSPI Registers	9-6
9.3.1.1	Control Registers	9-6
9.3.1.2	Status Register	9-7
9.3.2	QSPI RAM	9-7
9.3.2.1	Receive RAM	9-7
9.3.2.2	Transmit RAM	9-7
9.3.2.3	Command RAM	9-8
9.3.3	QSPI Pins	9-8
9.3.4	QSPI Operation	9-8
9.3.5	QSPI Operating Modes	9-9
9.3.5.1	Master Mode	9-16
9.3.5.2	Master Wrap-Around Mode	9-19
9.3.5.3	Slave Mode	9-19
9.3.5.4	Slave Wrap-Around Mode	9-20
9.3.6	Peripheral Chip Selects	9-20
9.4	Serial Communication Interface	9-21
9.4.1	SCI Registers	9-21
9.4.1.1	Control Registers	9-21
9.4.1.2	Status Register	9-24
9.4.1.3	Data Register	9-24
9.4.2	SCI Pins	9-24
9.4.3	SCI Operation	9-24
9.4.3.1	Definition of Terms	9-25
9.4.3.2	Serial Formats	9-25
9.4.3.3	Baud Clock	9-25
9.4.3.4	Parity Checking	9-26
9.4.3.5	Transmitter Operation	9-26
9.4.3.6	Receiver Operation	9-28
9.4.3.7	Idle-Line Detection	9-28
9.4.3.8	Receiver Wake-Up	9-29
9.4.3.9	Internal Loop	9-30
9.5	QSM Initialization	9-30

SECTION 10 CONFIGURABLE TIMER MODULE 4



TABLE OF CONTENTS (Continued)

Paragraph	Title	Page
10.1	General	10-1
10.2	Address Map	10-2
10.3	Time Base Bus System	10-2
10.4	Bus Interface Unit Submodule (BIUSM)	10-3
10.4.1	STOP Effect On the BIUSM	10-3
10.4.2	Freeze Effect On the BIUSM	10-3
10.4.3	LPSTOP Effect on the BIUSM	10-4
10.4.4	BIUSM Registers	10-4
10.5	Counter Prescaler Submodule (CPSM)	10-4
10.5.1	CPSM Registers	10-5
10.6	Free-Running Counter Submodule (FCSM)	10-5
10.6.1	FCSM Counter	10-6
10.6.2	FCSM Clock Sources	10-6
10.6.3	FCSM External Event Counting	10-6
10.6.4	FCSM Time Base Bus Driver	10-6
10.6.5	FCSM Interrupts	10-6
10.6.6	FCSM Registers	10-7
10.7	Modulus Counter Submodule (MCSM)	10-7
10.7.1	MCSM Modulus Latch	10-8
10.7.2	MCSM Counter	10-8
10.7.2.1	Loading the MCSM Counter Register	10-8
10.7.2.2	Using the MCSM as a Free-Running Counter	10-9
10.7.3	MCSM Clock Sources	10-9
10.7.4	MCSM External Event Counting	10-9
10.7.5	MCSM Time Base Bus Driver	10-9
10.7.6	MCSM Interrupts	10-9
10.7.7	MCSM Registers	10-10
10.8	Double-Action Submodule (DASM)	10-10
10.8.1	DASM Interrupts	10-12
10.8.2	DASM Registers	10-12
10.9	Pulse-Width Modulation Submodule (PWMSM)	10-12
10.9.1	Output Flip-Flop and Pin	10-13
10.9.2	Clock Selection	10-13
10.9.3	PWMSM Counter	10-14
10.9.4	PWMSM Period Registers and Comparator	10-14
10.9.5	PWMSM Pulse-Width Registers and Comparator	10-15
10.9.6	PWMSM Coherency	10-15
10.9.7	PWMSM Interrupts	10-15
10.9.8	PWM Frequency	10-16
10.9.9	PWM Pulse Width	10-17
10.9.10	PWM Period and Pulse Width Register Values	10-17



TABLE OF CONTENTS (Continued)

Paragraph	Title	Page
10.9.10.1	PWM Duty Cycle Boundary Cases	10-17
10.9.11	PWMSM Registers	10-17
10.10	CTM4 Interrupts	10-18

SECTION 11 TIME PROCESSOR UNIT

11.1	General	11-1
11.2	TPU Components	11-2
11.2.1	Time Bases	11-2
11.2.2	Timer Channels	11-2
11.2.3	Scheduler	11-3
11.2.4	Microengine	11-3
11.2.5	Host Interface	11-3
11.2.6	Parameter RAM	11-3
11.3	TPU Operation	11-3
11.3.1	Event Timing	11-4
11.3.2	Channel Orthogonality	11-4
11.3.3	Interchannel Communication	11-4
11.3.4	Programmable Channel Service Priority	11-4
11.3.5	Coherency	11-4
11.3.6	Emulation Support	11-5
11.3.7	TPU Interrupts	11-5
11.4	A Mask Set Time Functions	11-6
11.4.1	Discrete Input/Output (DIO)	11-6
11.4.2	Input Capture/Input Transition Counter (ITC)	11-6
11.4.3	Output Compare (OC)	11-7
11.4.4	Pulse-Width Modulation (PWM)	11-7
11.4.5	Synchronized Pulse-Width Modulation (SPWM)	11-7
11.4.6	Period Measurement with Additional Transition Detect (PMA)	11-8
11.4.7	Period Measurement with Missing Transition Detect (PMM)	11-8
11.4.8	Position-Synchronized Pulse Generator (PSP)	11-8
11.4.9	Stepper Motor (SM)	11-9
11.4.10	Period/Pulse-Width Accumulator (PPWA)	11-9
11.4.11	Quadrature Decode (QDEC)	11-10
11.5	G Mask Set Time Functions	11-10
11.5.1	Table Stepper Motor (TSM)	11-10
11.5.2	New Input Capture/Transition Counter (NITC)	11-11
11.5.3	Queued Output Match (QOM)	11-11
11.5.4	Programmable Time Accumulator (PTA)	11-11
11.5.5	Multichannel Pulse-Width Modulation (MCPWM)	11-11
11.5.6	Fast Quadrature Decode (FQD)	11-12
11.5.7	Universal Asynchronous Receiver/Transmitter (UART)	11-12



TABLE OF CONTENTS (Continued)

Paragraph	Title	Page
11.5.8	Brushless Motor Commutation (COMM)	11-12
11.5.9	Frequency Measurement (FQM)	11-13
11.5.10	Hall Effect Decode (HALLD)	11-13
11.6	Host Interface Registers	11-13
11.6.1	System Configuration Registers	11-13
11.6.1.1	Prescaler Control for TCR1	11-13
11.6.1.2	Prescaler Control for TCR2	11-14
11.6.1.3	Emulation Control	11-15
11.6.1.4	Low-Power Stop Control	11-15
11.6.2	Channel Control Registers	11-15
11.6.2.1	Channel Interrupt Enable and Status Registers	11-15
11.6.2.2	Channel Function Select Registers	11-16
11.6.2.3	Host Sequence Registers	11-16
11.6.2.4	Host Service Registers	11-17
11.6.2.5	Channel Priority Registers	11-17
11.6.3	Development Support and Test Registers	11-17

SECTION 12 STANDBY RAM WITH TPU EMULATION

12.1	General	12-1
12.2	TPURAM Register Block	12-1
12.3	TPURAM Array Address Mapping	12-1
12.4	TPURAM Privilege Level	12-2
12.5	Normal Operation	12-2
12.6	Standby Operation	12-2
12.7	Low-Power Stop Operation	12-3
12.8	Reset	12-3
12.9	TPU Microcode Emulation	12-3

SECTION 13 CAN 2.0B CONTROLLER MODULE (TouCAN)

13.1	General	13-1
13.2	External Pins	13-2
13.3	Programmer's Model	13-2
13.4	TouCAN Architecture	13-3
13.4.1	TX/RX Message Buffer Structure	13-3
13.4.1.1	Common Fields for Extended and Standard Format Frames	13-4
13.4.1.2	Fields for Extended Format Frames	13-5
13.4.1.3	Fields for Standard Format Frames	13-5
13.4.1.4	Serial Message Buffers	13-6
13.4.1.5	Message Buffer Activation/Deactivation Mechanism	13-6
13.4.1.6	Message Buffer Lock/Release/Busy Mechanism	13-6



TABLE OF CONTENTS (Continued)

Paragraph	Title	Page
13.4.2	Receive Mask Registers	13-7
13.4.3	Bit Timing	13-8
13.4.3.1	Configuring the TouCAN Bit Timing	13-9
13.4.4	Error Counters	13-9
13.4.5	Time Stamp	13-10
13.5	TouCAN Operation	13-11
13.5.1	TouCAN Reset	13-11
13.5.2	TouCAN Initialization	13-11
13.5.3	Transmit Process	13-12
13.5.3.1	Transmit Message Buffer Deactivation	13-13
13.5.3.2	Reception of Transmitted Frames	13-13
13.5.4	Receive Process	13-13
13.5.4.1	Receive Message Buffer Deactivation	13-14
13.5.4.2	Locking and Releasing Message Buffers	13-15
13.5.5	Remote Frames	13-15
13.5.6	Overload Frames	13-16
13.6	Special Operating Modes	13-16
13.6.1	Debug Mode	13-16
13.6.2	Low-Power Stop Mode	13-17
13.6.3	Auto Power Save Mode	13-18
13.7	Interrupts	13-19

APPENDIX A ELECTRICAL CHARACTERISTICS

APPENDIX B MECHANICAL DATA AND ORDERING INFORMATION

B.1	Obtaining Updated MC68336/376 Mechanical Information	B-4
B.2	Ordering Information	B-4

APPENDIX C DEVELOPMENT SUPPORT

C.1	M68MMDS1632 Modular Development System	C-1
C.2	M68MEVB1632 Modular Evaluation Board	C-1

APPENDIX D REGISTER SUMMARY

D.1	Central Processor Unit	D-1
D.1.1	CPU32 Register Model	D-2
D.1.2	Status Register	D-3
D.2	System Integration Module	D-5
D.2.1	SIM Configuration Register	D-6
D.2.2	System Integration Test Register	D-7



TABLE OF CONTENTS (Continued)

Paragraph	Title	Page
D.2.3	Clock Synthesizer Control Register	D-8
D.2.4	Reset Status Register	D-9
D.2.5	System Integration Test Register (ECLK)	D-9
D.2.6	Port E Data Register	D-10
D.2.7	Port E Data Direction Register	D-10
D.2.8	Port E Pin Assignment Register	D-10
D.2.9	Port F Data Register	D-11
D.2.10	Port F Data Direction Register	D-11
D.2.11	Port F Pin Assignment Register	D-11
D.2.12	System Protection Control Register	D-12
D.2.13	Periodic Interrupt Control Register	D-13
D.2.14	Periodic Interrupt Timer Register	D-14
D.2.15	Software Watchdog Service Register	D-14
D.2.16	Port C Data Register	D-15
D.2.17	Chip-Select Pin Assignment Registers	D-15
D.2.18	Chip-Select Base Address Register Boot ROM	D-17
D.2.19	Chip-Select Base Address Registers	D-17
D.2.20	Chip-Select Option Register Boot ROM	D-18
D.2.21	Chip-Select Option Registers	D-18
D.2.22	Master Shift Registers	D-21
D.2.23	Test Module Shift Count Register	D-21
D.2.24	Test Module Repetition Count Register	D-21
D.2.25	Test Submodule Control Register	D-21
D.2.26	Distributed Register	D-21
D.3	Standby RAM Module	D-22
D.3.1	RAM Module Configuration Register	D-22
D.3.2	RAM Test Register	D-23
D.3.3	Array Base Address Register High	D-23
D.3.4	Array Base Address Register Low	D-23
D.4	Masked ROM Module	D-24
D.4.1	Masked ROM Module Configuration Register	D-24
D.4.2	ROM Array Base Address Register High	D-26
D.4.3	ROM Array Base Address Register Low	D-26
D.4.4	ROM Signature High Register	D-26
D.4.5	ROM Signature Low Register	D-26
D.4.6	ROM Bootstrap Words	D-27
D.5	QADC Module	D-28
D.5.1	QADC Module Configuration Register	D-28
D.5.2	QADC Test Register	D-29
D.5.3	QADC Interrupt Register	D-29
D.5.4	Port A/B Data Register	D-30



TABLE OF CONTENTS (Continued)

Paragraph	Title	Page
D.5.5	Port Data Direction Register	D-30
D.5.6	QADC Control Registers	D-31
D.5.7	QADC Status Register	D-35
D.5.8	Conversion Command Word Table	D-37
D.5.9	Result Word Table	D-39
D.6	Queued Serial Module	D-40
D.6.1	QSM Configuration Register	D-40
D.6.2	QSM Test Register	D-41
D.6.3	QSM Interrupt Level Register	D-41
D.6.4	QSM Interrupt Vector Register	D-42
D.6.5	SCI Control Register	D-42
D.6.7	SCI Status Register	D-45
D.6.8	SCI Data Register	D-46
D.6.9	Port QS Data Register	D-46
D.6.10	Port QS Pin Assignment Register/Data Direction Register	D-47
D.6.11	QSPI Control Register 0	D-48
D.6.12	QSPI Control Register 1	D-50
D.6.13	QSPI Control Register 2	D-51
D.6.14	QSPI Control Register 3	D-52
D.6.15	QSPI Status Register	D-53
D.6.16	Receive Data RAM	D-53
D.6.17	Transmit Data RAM	D-54
D.6.18	Command RAM	D-54
D.7	Configurable Timer Module 4	D-56
D.7.1	BIU Module Configuration Register	D-57
D.7.2	BIUSM Test Configuration Register	D-58
D.7.3	BIUSM Time Base Register	D-58
D.7.4	CPSM Control Register	D-58
D.7.5	CPSM Test Register	D-59
D.7.6	FCSM Status/Interrupt/Control Register	D-59
D.7.7	FCSM Counter Register	D-61
D.7.8	MCSM Status/Interrupt/Control Registers	D-61
D.7.9	MCSM Counter Registers	D-63
D.7.10	MCSM Modulus Latch Registers	D-63
D.7.11	DASM Status/Interrupt/Control Registers	D-63
D.7.12	DASM Data Register A	D-66
D.7.13	DASM Data Register B	D-67
D.7.14	PWM Status/Interrupt/Control Register	D-68
D.7.15	PWM Period Register	D-71
D.7.16	PWM Pulse Width Register	D-71
D.7.17	PWM Counter Register	D-72



TABLE OF CONTENTS (Continued)

Paragraph	Title	Page
D.8	Time Processor Unit (TPU)	D-73
D.8.1	TPU Module Configuration Register	D-73
D.8.2	Test Configuration Register	D-75
D.8.3	Development Support Control Register	D-75
D.8.4	Development Support Status Register	D-76
D.8.5	TPU Interrupt Configuration Register	D-77
D.8.6	Channel Interrupt Enable Register	D-77
D.8.7	Channel Function Select Registers	D-78
D.8.8	Host Sequence Registers	D-78
D.8.9	Host Service Request Registers	D-79
D.8.10	Channel Priority Registers	D-79
D.8.11	Channel Interrupt Status Register	D-80
D.8.12	Link Register	D-80
D.8.13	Service Grant Latch Register	D-80
D.8.14	Decoded Channel Number Register	D-80
D.8.15	TPU Parameter RAM	D-80
D.9	Standby RAM Module with TPU Emulation Capability (TPURAM)	D-82
D.9.1	TPURAM Module Configuration Register	D-82
D.9.2	TPURAM Test Register	D-82
D.9.3	TPURAM Module Configuration Register	D-82
D.10	TouCAN Module	D-84
D.10.1	TouCAN Module Configuration Register	D-85
D.10.2	TouCAN Test Configuration Register	D-88
D.10.3	TouCAN Interrupt Configuration Register	D-88
D.10.4	Control Register 0	D-88
D.10.5	Control Register 1	D-90
D.10.6	Prescaler Divide Register	D-91
D.10.7	Control Register 2	D-91
D.10.8	Free Running Timer	D-92
D.10.9	Receive Global Mask Registers	D-93
D.10.10	Receive Buffer 14 Mask Registers	D-93
D.10.11	Receive Buffer 15 Mask Registers	D-93
D.10.12	Error and Status Register	D-94
D.10.13	Interrupt Mask Register	D-96
D.10.14	Interrupt Flag Register	D-96
D.10.15	Error Counters	D-97



LIST OF ILLUSTRATIONS

Figure	Title	Page
3-1	MC68336/376 Block Diagram	3-4
3-2	MC68336 Pin Assignments for 160-Pin Package	3-5
3-3	MC68376 Pin Assignments for 160-Pin Package	3-6
3-4	MC68336/376 Address Map	3-13
3-5	Overall Memory Map	3-15
3-6	Separate Supervisor and User Space Map	3-16
3-7	Supervisor Space (Separate Program/Data Space) Map	3-17
3-8	User Space (Separate Program/Data Space) Map	3-18
4-1	CPU32 Block Diagram	4-2
4-2	User Programming Model	4-3
4-3	Supervisor Programming Model Supplement	4-4
4-4	Data Organization in Data Registers	4-5
4-5	Address Organization in Address Registers	4-6
4-6	Memory Operand Addressing	4-8
4-7	Loop Mode Instruction Sequence	4-15
4-8	Common In-Circuit Emulator Diagram	4-19
4-9	Bus State Analyzer Configuration	4-19
4-10	Debug Serial I/O Block Diagram	4-24
4-11	BDM Serial Data Word	4-25
4-12	BDM Connector Pinout	4-25
5-1	System Integration Module Block Diagram	5-2
5-2	System Clock Block Diagram	5-4
5-3	System Clock Oscillator Circuit	5-5
5-4	System Clock Filter Networks	5-6
5-5	LPSTOP Flowchart	5-13
5-6	System Protection Block	5-14
5-7	Periodic Interrupt Timer and Software Watchdog Timer	5-17
5-8	MCU Basic System	5-20
5-9	Operand Byte Order	5-25
5-10	Word Read Cycle Flowchart	5-28
5-11	Write Cycle Flowchart	5-29
5-12	CPU Space Address Encoding	5-31
5-13	Breakpoint Operation Flowchart	5-33
5-14	LPSTOP Interrupt Mask Level	5-34
5-15	Bus Arbitration Flowchart for Single Request	5-39
5-16	Preferred Circuit for Data Bus Mode Select Conditioning	5-43
5-17	Alternate Circuit for Data Bus Mode Select Conditioning	5-44
5-18	Power-On Reset	5-49
5-19	Basic MCU System	5-55
5-20	Chip-Select Circuit Block Diagram	5-56
5-21	CPU Space Encoding for Interrupt Acknowledge	5-61



LIST OF ILLUSTRATIONS (Continued)

Figure	Title	Page
8-1	QADC Block Diagram	8-1
8-2	QADC Input and Output Signals	8-3
8-3	Example of External Multiplexing	8-11
8-4	QADC Module Block Diagram	8-13
8-5	Conversion Timing	8-14
8-6	Bypass Mode Conversion Timing	8-15
8-7	QADC Queue Operation with Pause	8-18
8-8	QADC Clock Subsystem Functions	8-24
8-9	QADC Clock Programmability Examples	8-26
8-10	QADC Conversion Queue Operation	8-29
8-11	QADC Interrupt Vector Format	8-33
9-1	QSM Block Diagram	9-1
9-2	QSPI Block Diagram	9-5
9-3	QSPI RAM	9-7
9-4	Flowchart of QSPI Initialization Operation	9-10
9-5	Flowchart of QSPI Master Operation (Part 1)	9-11
9-6	Flowchart of QSPI Master Operation (Part 2)	9-12
9-7	Flowchart of QSPI Master Operation (Part 3)	9-13
9-8	Flowchart of QSPI Slave Operation (Part 1)	9-14
9-9	Flowchart of QSPI Slave Operation (Part 2)	9-15
9-10	SCI Transmitter Block Diagram	9-22
9-11	SCI Receiver Block Diagram	9-23
10-1	CTM4 Block Diagram	10-1
10-2	CPSM Block Diagram	10-4
10-3	FCSM Block Diagram	10-5
10-4	MCSM Block Diagram	10-8
10-5	DASM Block Diagram	10-11
10-6	Pulse-Width Modulation Submodule Block Diagram	10-13
11-1	TPU Block Diagram	11-1
11-2	TCR1 Prescaler Control	11-14
11-3	TCR2 Prescaler Control	11-14
13-1	TouCAN Block Diagram	13-1
13-2	Typical CAN Network	13-2
13-3	Extended ID Message Buffer Structure	13-3
13-4	Standard ID Message Buffer Structure	13-4
13-5	TouCAN Interrupt Vector Generation	13-19
A-1	CLKOUT Output Timing Diagram	A-10
A-2	External Clock Input Timing Diagram	A-10
A-3	ECLK Output Timing Diagram	A-10
A-4	Read Cycle Timing Diagram	A-11
A-5	Write Cycle Timing Diagram	A-12



LIST OF ILLUSTRATIONS (Continued)

Figure	Title	Page
A-6	Fast Termination Read Cycle Timing Diagram	A-13
A-7	Fast Termination Write Cycle Timing Diagram	A-14
A-8	Bus Arbitration Timing Diagram — Active Bus Case	A-15
A-9	Bus Arbitration Timing Diagram — Idle Bus Case	A-16
A-10	Show Cycle Timing Diagram	A-17
A-11	Chip-Select Timing Diagram	A-18
A-12	Reset and Mode Select Timing Diagram	A-18
A-13	Background Debugging Mode Timing — Serial Communication	A-20
A-14	Background Debugging Mode Timing — Freeze Assertion	A-20
A-15	ECLK Timing Diagram	A-22
A-16	QSPI Timing — Master, CPHA = 0	A-24
A-17	QSPI Timing — Master, CPHA = 1	A-24
A-18	QSPI Timing — Slave, CPHA = 0	A-25
A-19	QSPI Timing — Slave, CPHA = 1	A-25
A-20	TPU Timing Diagram	A-26
B-1	MC68336 Pin Assignments for 160-Pin Package	B-1
B-2	MC68376 Pin Assignments for 160-Pin Package	B-2
B-3	160-Pin Package Dimensions	B-3
D-1	User Programming Model	D-2
D-2	Supervisor Programming Model Supplement	D-3
D-3	TouCAN Message Buffer Address Map	D-85



LIST OF ILLUSTRATIONS
(Continued)
Title

Figure

Page



LIST OF TABLES

Table	Title	Page
3-1	MC68336/376 Pin Characteristics	3-7
3-2	MC68336/376 Output Driver Types.....	3-8
3-3	MC68336/376 Power Connections.....	3-8
3-4	MC68336/376 Signal Characteristics	3-9
3-5	MC68336/376 Signal Functions	3-11
4-1	Unimplemented MC68020 Instructions	4-10
4-2	Instruction Set Summary	4-11
4-3	Exception Vector Assignments.....	4-16
4-4	BDM Source Summary.....	4-20
4-5	Polling the BDM Entry Source.....	4-21
4-6	Background Mode Command Summary	4-22
4-7	CPU Generated Message Encoding	4-25
5-1	Show Cycle Enable Bits	5-3
5-2	Clock Control Multipliers.....	5-8
5-3	System Frequencies from 4.194 MHz Reference	5-10
5-4	Bus Monitor Period.....	5-15
5-5	MODCLK Pin and SWP Bit During Reset	5-16
5-6	Software Watchdog Ratio.....	5-16
5-7	MODCLK Pin and PTP Bit at Reset	5-17
5-8	Periodic Interrupt Priority.....	5-18
5-9	Size Signal Encoding	5-22
5-10	Address Space Encoding	5-23
5-11	Effect of DSACK Signals	5-24
5-12	Operand Alignment	5-26
5-13	DSACK, BERR, and HALT Assertion Results.....	5-35
5-14	Reset Source Summary	5-41
5-15	Reset Mode Selection	5-42
5-16	Module Pin Functions During Reset.....	5-46
5-17	SIM Pin Reset States	5-47
5-18	Chip-Select Pin Functions	5-57
5-19	Pin Assignment Field Encoding.....	5-58
5-20	Block Size Encoding.....	5-59
5-21	Chip-Select Base and Option Register Reset Values	5-63
5-22	CSBOOT Base and Option Register Reset Values.....	5-63
6-1	SRAM Array Address Space Type	6-2
7-1	ROM Array Space Type	7-2
7-2	Wait States Field	7-2
8-1	Multiplexed Analog Input Channels.....	8-5
8-2	Analog Input Channels	8-12
8-3	Queue 1 Priority Assertion	8-17
8-4	QADC Clock Programmability	8-27



LIST OF TABLES (Continued)

Table	Title	Page
8-5	QADC Status Flags and Interrupt Sources	8-32
9-1	Effect of DDRQS on QSM Pin Function	9-4
9-2	QSPI Pins	9-8
9-3	Bits Per Transfer	9-17
9-4	SCI Pins	9-24
9-5	Serial Frame Formats.....	9-25
9-6	Effect of Parity Checking on Data Size	9-26
10-1	CTM4 Time Base Bus Allocation.....	10-3
10-2	DASM Modes of Operation	10-10
10-3	Channel B Data Register Access	10-11
10-4	PWMSM Divide By Options.....	10-14
10-5	PWM Pulse and Frequency Ranges (in Hz) Using ÷ 2 Option (20.97 MHz)	10-16
10-6	PWM Pulse and Frequency Ranges (in Hz) Using ÷ 3 Option (20.97 MHz)	10-16
10-7	CTM4 Interrupt Priority and Vector/Pin Allocation	10-18
11-1	TCR1 Prescaler Control	11-14
11-2	TCR2 Prescaler Control	11-15
11-3	TPU Function Encodings.....	11-16
11-4	Channel Priority Encodings	11-17
13-1	Common Extended/Standard Format Frames	13-4
13-2	Message Buffer Codes for Receive Buffers	13-4
13-3	Message Buffer Codes for Transmit Buffers	13-5
13-4	Extended Format Frames.....	13-5
13-5	Standard Format Frames	13-6
13-6	Receive Mask Register Bit Values	13-7
13-7	Mask Examples for Normal/Extended Messages.....	13-8
13-8	Example System Clock, CAN Bit Rate and S-Clock Frequencies.....	13-9
13-9	Interrupt Sources and Vector Addresses	13-20
A-1	Maximum Ratings.....	A-1
A-2	Typical Ratings.....	A-2
A-3	Thermal Characteristics	A-2
A-4	Clock Control Timing	A-3
A-5	DC Characteristics	A-4
A-6	AC Timing.....	A-7
A-7	Background Debug Mode Timing.....	A-19
A-8	ECLK Bus Timing	A-21
A-9	QSPI Timing	A-23
A-10	Time Processor Unit Timing	A-26
A-11	QADC Maximum Ratings	A-27
A-12	QADC DC Electrical Characteristics (Operating)	A-28
A-13	QADC AC Electrical Characteristics (Operating)	A-29
A-14	QADC Conversion Characteristics (Operating).....	A-30



LIST OF TABLES (Continued)

Table	Title	Page
A-15	FCSM Timing Characteristics.....	A-31
A-16	MCSM Timing Characteristics.....	A-31
A-17	SASM Timing Characteristics.....	A-32
A-18	DASM Timing Characteristics.....	A-33
A-19	PWMSM Timing Characteristics.....	A-34
B-1	MC68336 Ordering Information.....	B-4
B-2	MC68376 Ordering Information.....	B-5
D-1	Module Address Map.....	D-1
D-2	T[1:0] Encoding.....	D-3
D-3	SIM Address Map.....	D-5
D-4	Show Cycle Enable Bits.....	D-7
D-5	Port E Pin Assignments.....	D-11
D-6	Port F Pin Assignments.....	D-12
D-7	Software Watchdog Timing Field.....	D-13
D-8	Bus Monitor Time-Out Period.....	D-13
D-9	Pin Assignment Field Encoding.....	D-15
D-10	CSPAR0 Pin Assignments.....	D-16
D-11	CSPAR1 Pin Assignments.....	D-16
D-12	Reset Pin Function of CS[10:6].....	D-17
D-13	Block Size Field Bit Encoding.....	D-18
D-14	BYTE Field Bit Encoding.....	D-19
D-15	Read/Write Field Bit Encoding.....	D-19
D-16	DSACK Field Encoding.....	D-20
D-17	Address Space Bit Encodings.....	D-20
D-18	Interrupt Priority Level Field Encoding.....	D-20
D-19	SRAM Address Map.....	D-22
D-20	RASP Encoding.....	D-22
D-21	MRM Address Map.....	D-24
D-22	ROM Array Space Field.....	D-25
D-23	Wait States Field.....	D-25
D-24	QADC Address Map.....	D-28
D-25	Queue 1 Operating Modes.....	D-32
D-26	Queue 2 Operating Modes.....	D-34
D-27	Queue Status.....	D-36
D-28	Input Sample Times.....	D-37
D-29	Non-multiplexed Channel Assignments and Pin Designations.....	D-38
D-30	Multiplexed Channel Assignments and Pin Designations.....	D-38
D-31	QSM Address Map.....	D-40
D-32	PQSPAR Pin Assignments.....	D-47
D-33	Effect of DDRQS on QSM Pin Function.....	D-48
D-34	Bits Per Transfer.....	D-49



LIST OF TABLES (Continued)

Table	Title	Page
D-35	CTM4 Address Map	D-56
D-36	Interrupt Vector Base Number Bit Field.....	D-57
D-37	Time Base Register Bus Select Bits.....	D-58
D-38	Prescaler Division Ratio Select Field	D-59
D-39	Drive Time Base Bus Field.....	D-60
D-40	Counter Clock Select Field.....	D-60
D-41	Drive Time Base Bus Field.....	D-62
D-42	Modulus Load Edge Sensitivity Bits	D-62
D-43	Counter Clock Select Field.....	D-62
D-44	DASM Mode Flag Status Bit States	D-64
D-45	Edge Polarity.....	D-65
D-46	DASM Mode Select Field	D-66
D-47	DASMA Operations	D-67
D-48	DASMB Operations	D-68
D-49	PWMSM Output Pin Polarity Selection	D-70
D-50	PWMSM Divide By Options.....	D-71
D-51	TPU Register Map.....	D-73
D-52	TCR1 Prescaler Control Bits	D-74
D-53	TCR2 Prescaler Control Bits	D-74
D-54	FRZ[1:0] Encoding	D-76
D-55	Breakpoint Enable Bits.....	D-76
D-56	Channel Priorities	D-80
D-57	Parameter RAM Address Map	D-81
D-58	TPURAM Address Map.....	D-82
D-59	TouCAN Address Map	D-84
D-60	RX MODE[1:0] Configuration	D-89
D-61	Transmit Pin Configuration.....	D-89
D-62	Transmit Bit Error Status	D-94
D-63	Fault Confinement State Encoding.....	D-95



SECTION 1 INTRODUCTION

The MC68336 and the MC68376 are highly-integrated 32-bit microcontrollers, combining high-performance data manipulation capabilities with powerful peripheral subsystems.

MC68300 microcontrollers are built up from standard modules that interface through a common intermodule bus (IMB). Standardization facilitates rapid development of devices tailored for specific applications.

The MC68336 incorporates a 32-bit CPU (CPU32), a system integration module (SIM), a time processor unit (TPU), a configurable timer module (CTM4), a queued serial module (QSM), a 10-bit queued analog-to-digital converter module (QADC), a 3.5-Kbyte TPU emulation RAM module (TPURAM), and a 4-Kbyte standby RAM module (SRAM).

The MC68376 includes all of the aforementioned modules, plus a CAN 2.0B protocol controller module (TouCAN™) and an 8-Kbyte masked ROM (MRM).

The MC68336/376 can either synthesize the system clock signal from a fast reference or use an external clock input directly. Operation with a 4.194 MHz reference frequency is standard. The maximum system clock speed is 20.97 MHz. System hardware and software allow changes in clock rate during operation. Because MCU operation is fully static, register and memory contents are not affected by clock rate changes.

High-density complementary metal-oxide semiconductor (HCMOS) architecture makes the basic power consumption of the MCU low. Power consumption can be minimized by stopping the system clock. The CPU32 instruction set includes a low-power stop (LPSTOP) instruction that efficiently implements this capability.

Documentation for the Modular Microcontroller Family follows the modular construction of the devices in the product line. Each microcontroller has a comprehensive user's manual that provides sufficient information for normal operation of the device. The user's manual is supplemented by module reference manuals that provide detailed information about module operation and applications. Refer to Motorola publication *Advanced Microcontroller Unit (AMCU) Literature* (BR1116/D) for a complete listing of documentation.