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# M68HC11E Family

Data Sheet

**HC11  
Microcontrollers**

M68HC11E  
Rev. 5.1  
07/2005

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# MC68HC11E Family

## Data Sheet

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

## Revision History

Date	Revision Level	Description	Page Number(s)
May, 2001	3.1	2.3.3.1 System Configuration Register — Addition to NOCOP bit description	44
		Added 10.21 EPROM Characteristics	175
June, 2001	3.2	10.21 EPROM Characteristics — For clarity, addition to note 2 following the table	175
December, 2001	3.3	7.7.2 Serial Communications Control Register 1 — SCCR1 bit 4 (M) description corrected	110
July, 2002	4	10.7 MC68L11E9/E20 DC Electrical Characteristics — Title changed to include the MC68L11E20	153
		10.8 MC68L11E9/E20 Supply Currents and Power Dissipation — Title changed to include the MC68L11E20	154
		10.10 MC68L11E9/E20 Control Timing — Title changed to include the MC68L11E20	157
		10.12 MC68L11E9/E20 Peripheral Port Timing — Title changed to include the MC68L11E20	163
		10.14 MC68L11E9/E20 Analog-to-Digital Converter Characteristics — Title changed to include the MC68L11E20	167
		10.16 MC68L11E9/E20 Expansion Bus Timing Characteristics — Title changed to include the MC68L11E20	169
		10.18 MC68L11E9/E20 Serial Peripheral Interface Characteristics — Title changed to include the MC68L11E20	172
		— Title changed to include the MC68L11E20	175
11.4 Extended Voltage Device Ordering Information (3.0 Vdc to 5.5 Vdc) — Updated table to include MC68L1120	181		
June, 2003	5	Format updated to current publications standards	Throughout
		1.4.6 Non-Maskable Interrupt (XIRQ/VPPE) — Added Caution note pertaining to EPROM programming of the MC68HC711E9 device only.	23
		6.4 Port C — Clarified description of DDR[C:0] bits	100
		10.21 EPROM Characteristics — Added note pertaining to EPROM programming of the MC68HC711E9 device only.	175
July, 2005	5.1	Updated to meet Freescale identity guidelines.	Throughout

## List of Chapters

Chapter 1 General Description . . . . .	13
Chapter 2 Operating Modes and On-Chip Memory . . . . .	29
Chapter 3 Analog-to-Digital (A/D) Converter . . . . .	57
Chapter 4 Central Processor Unit (CPU) . . . . .	65
Chapter 5 Resets and Interrupts . . . . .	79
Chapter 6 Parallel Input/Output (I/O) Ports . . . . .	97
Chapter 7 Serial Communications Interface (SCI) . . . . .	105
Chapter 8 Serial Peripheral Interface (SPI) . . . . .	119
Chapter 9 Timing Systems . . . . .	127
Chapter 10 Electrical Characteristics . . . . .	149
Chapter 11 Ordering Information and Mechanical Specifications . . . . .	177
Appendix A Development Support . . . . .	187
Appendix B EVBU Schematic . . . . .	191
AN1060 — M68HC11 Bootstrap Mode . . . . .	193
EB184 — Enabling the Security Feature on the MC68HC711E9 Devices with PCbug11 on the M68HC711E9PGMR . . . . .	229
EB188 — Enabling the Security Feature on M68HC811E2 Devices with PCbug11 on the M68HC711E9PGMR . . . . .	233
EB296 — Programming MC68HC711E9 Devices with PCbug11 and the M68HC11EVBU . . . . .	237



**List of Chapters**

# Table of Contents

## Chapter 1 General Description

1.1	Introduction	13
1.2	Features	13
1.3	Structure	14
1.4	Pin Descriptions	14
1.4.1	$V_{DD}$ and $V_{SS}$	21
1.4.2	RESET	22
1.4.3	Crystal Driver and External Clock Input (XTAL and EXTAL)	22
1.4.4	E-Clock Output (E)	23
1.4.5	Interrupt Request ( $\overline{IRQ}$ )	23
1.4.6	Non-Maskable Interrupt ( $\overline{XIRQ}/V_{PPE}$ )	23
1.4.7	MODA and MODB ( $MODA/\overline{LIR}$ and $MODB/V_{STBY}$ )	24
1.4.7.1	$V_{RL}$ and $V_{RH}$	24
1.4.8	STRA/AS	25
1.4.9	STRB/ $\overline{RW}$	25
1.4.10	Port Signals	25
1.4.10.1	Port A	25
1.4.10.2	Port B	27
1.4.10.3	Port C	27
1.4.10.4	Port D	28
1.4.10.5	Port E	28

## Chapter 2 Operating Modes and On-Chip Memory

2.1	Introduction	29
2.2	Operating Modes	29
2.2.1	Single-Chip Mode	29
2.2.2	Expanded Mode	29
2.2.3	Test Mode	30
2.2.4	Bootstrap Mode	30
2.3	Memory Map	31
2.3.1	RAM and Input/Output Mapping	39
2.3.2	Mode Selection	40
2.3.3	System Initialization	42
2.3.3.1	System Configuration Register	43
2.3.3.2	RAM and I/O Mapping Register	45
2.3.3.3	System Configuration Options Register	46
2.4	EPROM/OTPROM	47
2.4.1	Programming an Individual EPROM Address	48
2.4.2	Programming the EPROM with Downloaded Data	48



## Table of Contents

2.4.3	EPROM and EEPROM Programming Control Register . . . . .	49
2.5	EEPROM . . . . .	51
2.5.1	EEPROM and CONFIG Programming and Erasure . . . . .	51
2.5.1.1	Block Protect Register . . . . .	51
2.5.1.2	EPROM and EEPROM Programming Control Register . . . . .	53
2.5.1.3	EEPROM Bulk Erase . . . . .	54
2.5.1.4	EEPROM Row Erase . . . . .	54
2.5.1.5	EEPROM Byte Erase . . . . .	55
2.5.1.6	CONFIG Register Programming . . . . .	55
2.5.2	EEPROM Security . . . . .	55

## Chapter 3 Analog-to-Digital (A/D) Converter

3.1	Introduction . . . . .	57
3.2	Overview . . . . .	57
3.2.1	Multiplexer . . . . .	57
3.2.2	Analog Converter . . . . .	57
3.2.3	Digital Control . . . . .	59
3.2.4	Result Registers . . . . .	59
3.2.5	A/D Converter Clocks . . . . .	59
3.2.6	Conversion Sequence . . . . .	59
3.3	A/D Converter Power-Up and Clock Select . . . . .	60
3.4	Conversion Process . . . . .	61
3.5	Channel Assignments . . . . .	61
3.6	Single-Channel Operation . . . . .	61
3.7	Multiple-Channel Operation . . . . .	62
3.8	Operation in Stop and Wait Modes . . . . .	62
3.9	A/D Control/Status Register . . . . .	62
3.10	A/D Converter Result Registers . . . . .	64

## Chapter 4 Central Processor Unit (CPU)

4.1	Introduction . . . . .	65
4.2	CPU Registers . . . . .	65
4.2.1	Accumulators A, B, and D . . . . .	66
4.2.2	Index Register X (IX) . . . . .	66
4.2.3	Index Register Y (IY) . . . . .	66
4.2.4	Stack Pointer (SP) . . . . .	66
4.2.5	Program Counter (PC) . . . . .	68
4.2.6	Condition Code Register (CCR) . . . . .	68
4.2.6.1	Carry/Borrow (C) . . . . .	68
4.2.6.2	Overflow (V) . . . . .	68
4.2.6.3	Zero (Z) . . . . .	68
4.2.6.4	Negative (N) . . . . .	68
4.2.6.5	Interrupt Mask (I) . . . . .	69
4.2.6.6	Half Carry (H) . . . . .	69
4.2.6.7	X Interrupt Mask (X) . . . . .	69
4.2.6.8	STOP Disable (S) . . . . .	69

4.3	Data Types . . . . .	69
4.4	Opcodes and Operands . . . . .	70
4.5	Addressing Modes . . . . .	70
4.5.1	Immediate . . . . .	70
4.5.2	Direct . . . . .	70
4.5.3	Extended . . . . .	71
4.5.4	Indexed . . . . .	71
4.5.5	Inherent . . . . .	71
4.5.6	Relative . . . . .	71
4.6	Instruction Set . . . . .	71

## Chapter 5 Resets and Interrupts

5.1	Introduction . . . . .	79
5.2	Resets . . . . .	79
5.2.1	Power-On Reset (POR) . . . . .	79
5.2.2	External Reset (RESET) . . . . .	80
5.2.3	Computer Operating Properly (COP) Reset . . . . .	80
5.2.4	Clock Monitor Reset . . . . .	81
5.2.5	System Configuration Options Register . . . . .	82
5.2.6	Configuration Control Register . . . . .	83
5.3	Effects of Reset . . . . .	83
5.3.1	Central Processor Unit (CPU) . . . . .	83
5.3.2	Memory Map . . . . .	84
5.3.3	Timer . . . . .	84
5.3.4	Real-Time Interrupt (RTI) . . . . .	84
5.3.5	Pulse Accumulator . . . . .	84
5.3.6	Computer Operating Properly (COP) . . . . .	84
5.3.7	Serial Communications Interface (SCI) . . . . .	84
5.3.8	Serial Peripheral Interface (SPI) . . . . .	84
5.3.9	Analog-to-Digital (A/D) Converter . . . . .	85
5.3.10	System . . . . .	85
5.4	Reset and Interrupt Priority . . . . .	85
5.4.1	Highest Priority Interrupt and Miscellaneous Register . . . . .	86
5.5	Interrupts . . . . .	87
5.5.1	Interrupt Recognition and Register Stacking . . . . .	88
5.5.2	Non-Maskable Interrupt Request (XIRQ) . . . . .	89
5.5.3	Illegal Opcode Trap . . . . .	89
5.5.4	Software Interrupt (SWI) . . . . .	90
5.5.5	Maskable Interrupts . . . . .	90
5.5.6	Reset and Interrupt Processing . . . . .	90
5.6	Low-Power Operation . . . . .	90
5.6.1	Wait Mode . . . . .	90
5.6.2	Stop Mode . . . . .	95

**Chapter 6**  
**Parallel Input/Output (I/O) Ports**

6.1	Introduction .....	97
6.2	Port A .....	98
6.3	Port B .....	99
6.4	Port C .....	99
6.5	Port D .....	100
6.6	Port E .....	101
6.7	Handshake Protocol .....	101
6.8	Parallel I/O Control Register .....	102

**Chapter 7**  
**Serial Communications Interface (SCI)**

7.1	Introduction .....	105
7.2	Data Format .....	105
7.3	Transmit Operation .....	105
7.4	Receive Operation .....	107
7.5	Wakeup Feature .....	107
7.5.1	Idle-Line Wakeup .....	107
7.5.2	Address-Mark Wakeup .....	109
7.6	SCI Error Detection .....	109
7.7	SCI Registers .....	109
7.7.1	Serial Communications Data Register .....	110
7.7.2	Serial Communications Control Register 1 .....	110
7.7.3	Serial Communications Control Register 2 .....	111
7.7.4	Serial Communication Status Register .....	112
7.7.5	Baud Rate Register .....	113
7.8	Status Flags and Interrupts .....	116
7.9	Receiver Flags .....	117

**Chapter 8**  
**Serial Peripheral Interface (SPI)**

8.1	Introduction .....	119
8.2	Functional Description .....	119
8.3	SPI Transfer Formats .....	119
8.4	Clock Phase and Polarity Controls .....	120
8.5	SPI Signals .....	121
8.5.1	Master In/Slave Out .....	121
8.5.2	Master Out/Slave In .....	121
8.5.3	Serial Clock .....	122
8.5.4	Slave Select .....	122
8.6	SPI System Errors .....	122
8.7	SPI Registers .....	123
8.7.1	Serial Peripheral Control Register .....	123
8.7.2	Serial Peripheral Status Register .....	124
8.7.3	Serial Peripheral Data I/O Register .....	125

## Chapter 9 Timing Systems

9.1	Introduction . . . . .	127
9.2	Timer Structure . . . . .	129
9.3	Input Capture . . . . .	129
9.3.1	Timer Control Register 2 . . . . .	131
9.3.2	Timer Input Capture Registers . . . . .	131
9.3.3	Timer Input Capture 4/Output Compare 5 Register . . . . .	133
9.4	Output Compare . . . . .	133
9.4.1	Timer Output Compare Registers . . . . .	134
9.4.2	Timer Compare Force Register . . . . .	135
9.4.3	Output Compare Mask Register . . . . .	136
9.4.4	Output Compare Data Register . . . . .	136
9.4.5	Timer Counter Register . . . . .	137
9.4.6	Timer Control Register 1 . . . . .	137
9.4.7	Timer Interrupt Mask 1 Register . . . . .	138
9.4.8	Timer Interrupt Flag 1 Register . . . . .	138
9.4.9	Timer Interrupt Mask 2 Register . . . . .	139
9.4.10	Timer Interrupt Flag Register 2 . . . . .	140
9.5	Real-Time Interrupt (RTI) . . . . .	140
9.5.1	Timer Interrupt Mask Register 2 . . . . .	141
9.5.2	Timer Interrupt Flag Register 2 . . . . .	142
9.5.3	Pulse Accumulator Control Register . . . . .	142
9.6	Computer Operating Properly (COP) Watchdog Function . . . . .	143
9.7	Pulse Accumulator . . . . .	143
9.7.1	Pulse Accumulator Control Register . . . . .	145
9.7.2	Pulse Accumulator Count Register . . . . .	146
9.7.3	Pulse Accumulator Status and Interrupt Bits . . . . .	146

## Chapter 10 Electrical Characteristics

10.1	Introduction . . . . .	149
10.2	Maximum Ratings for Standard and Extended Voltage Devices . . . . .	149
10.3	Functional Operating Range . . . . .	150
10.4	Thermal Characteristics . . . . .	150
10.5	DC Electrical Characteristics . . . . .	151
10.6	Supply Currents and Power Dissipation . . . . .	152
10.7	MC68L11E9/E20 DC Electrical Characteristics . . . . .	153
10.8	MC68L11E9/E20 Supply Currents and Power Dissipation . . . . .	154
10.9	Control Timing . . . . .	156
10.10	MC68L11E9/E20 Control Timing . . . . .	157
10.11	Peripheral Port Timing . . . . .	162
10.12	MC68L11E9/E20 Peripheral Port Timing . . . . .	163
10.13	Analog-to-Digital Converter Characteristics . . . . .	166
10.14	MC68L11E9/E20 Analog-to-Digital Converter Characteristics . . . . .	167

## Table of Contents

10.15	Expansion Bus Timing Characteristics	168
10.16	MC68L11E9/E20 Expansion Bus Timing Characteristics	169
10.17	Serial Peripheral Interface Timing Characteristics	171
10.18	MC68L11E9/E20 Serial Peripheral Interface Characteristics	172
10.19	EEPROM Characteristics	175
10.20	MC68L11E9/E20 EEPROM Characteristics	175
10.21	EPROM Characteristics	175

## Chapter 11

### Ordering Information and Mechanical Specifications

11.1	Introduction	177
11.2	Standard Device Ordering Information	177
11.3	Custom ROM Device Ordering Information	179
11.4	Extended Voltage Device Ordering Information (3.0 Vdc to 5.5 Vdc)	181
11.5	52-Pin Plastic-Leaded Chip Carrier (Case 778)	182
11.6	52-Pin Windowed Ceramic-Leaded Chip Carrier (Case 778B)	183
11.7	64-Pin Quad Flat Pack (Case 840C)	184
11.8	52-Pin Thin Quad Flat Pack (Case 848D)	185
11.9	56-Pin Dual in-Line Package (Case 859)	186
11.10	48-Pin Plastic DIP (Case 767)	186

## Appendix A

### Development Support

A.1	Introduction	187
A.2	M68HC11 E-Series Development Tools	187
A.3	EVS — Evaluation System	187
A.4	Modular Development System (MMDS11)	188
A.5	SPGMR11 — Serial Programmer for M68HC11 MCUs	189

## Appendix B

### EVBU Schematic

AN1060	— M68HC11 Bootstrap Mode	193
EB184	— Enabling the Security Feature on the MC68HC711E9 Devices with PCbug11 on the M68HC711E9PGMR	229
EB188	— Enabling the Security Feature on M68HC811E2 Devices with PCbug11 on the M68HC711E9PGMR	233
EB296	— Programming MC68HC711E9 Devices with PCbug11 and the M68HC11EVBU	237

# Chapter 1

## General Description

### 1.1 Introduction

This document contains a detailed description of the M68HC11 E series of 8-bit microcontroller units (MCUs). These MCUs all combine the M68HC11 central processor unit (CPU) with high-performance, on-chip peripherals.

The E series is comprised of many devices with various configurations of:

- Random-access memory (RAM)
- Read-only memory (ROM)
- Erasable programmable read-only memory (EPROM)
- Electrically erasable programmable read-only memory (EEPROM)
- Several low-voltage devices are also available.

With the exception of a few minor differences, the operation of all E-series MCUs is identical. A fully static design and high-density complementary metal-oxide semiconductor (HCMOS) fabrication process allow the E-series devices to operate at frequencies from 3 MHz to dc with very low power consumption.

### 1.2 Features

Features of the E-series devices include:

- M68HC11 CPU
- Power-saving stop and wait modes
- Low-voltage devices available (3.0–5.5 Vdc)
- 0, 256, 512, or 768 bytes of on-chip RAM, data retained during standby
- 0, 12, or 20 Kbytes of on-chip ROM or EPROM
- 0, 512, or 2048 bytes of on-chip EEPROM with block protect for security
- 2048 bytes of EEPROM with selectable base address in the MC68HC811E2
- Asynchronous non-return-to-zero (NRZ) serial communications interface (SCI)
- Additional baud rates available on MC68HC(7)11E20
- Synchronous serial peripheral interface (SPI)
- 8-channel, 8-bit analog-to-digital (A/D) converter
- 16-bit timer system:
  - Three input capture (IC) channels
  - Four output compare (OC) channels
  - One additional channel, selectable as fourth IC or fifth OC
- 8-bit pulse accumulator
- Real-time interrupt circuit

## General Description

- Computer operating properly (COP) watchdog system
- 38 general-purpose input/output (I/O) pins:
  - 16 bidirectional I/O pins
  - 11 input-only pins
  - 11 output-only pins
- Several packaging options:
  - 52-pin plastic-leaded chip carrier (PLCC)
  - 52-pin windowed ceramic leaded chip carrier (CLCC)
  - 52-pin plastic thin quad flat pack, 10 mm x 10 mm (TQFP)
  - 64-pin quad flat pack (QFP)
  - 48-pin plastic dual in-line package (DIP), MC68HC811E2 only
  - 56-pin plastic shrink dual in-line package, .070-inch lead spacing (SDIP)

## 1.3 Structure

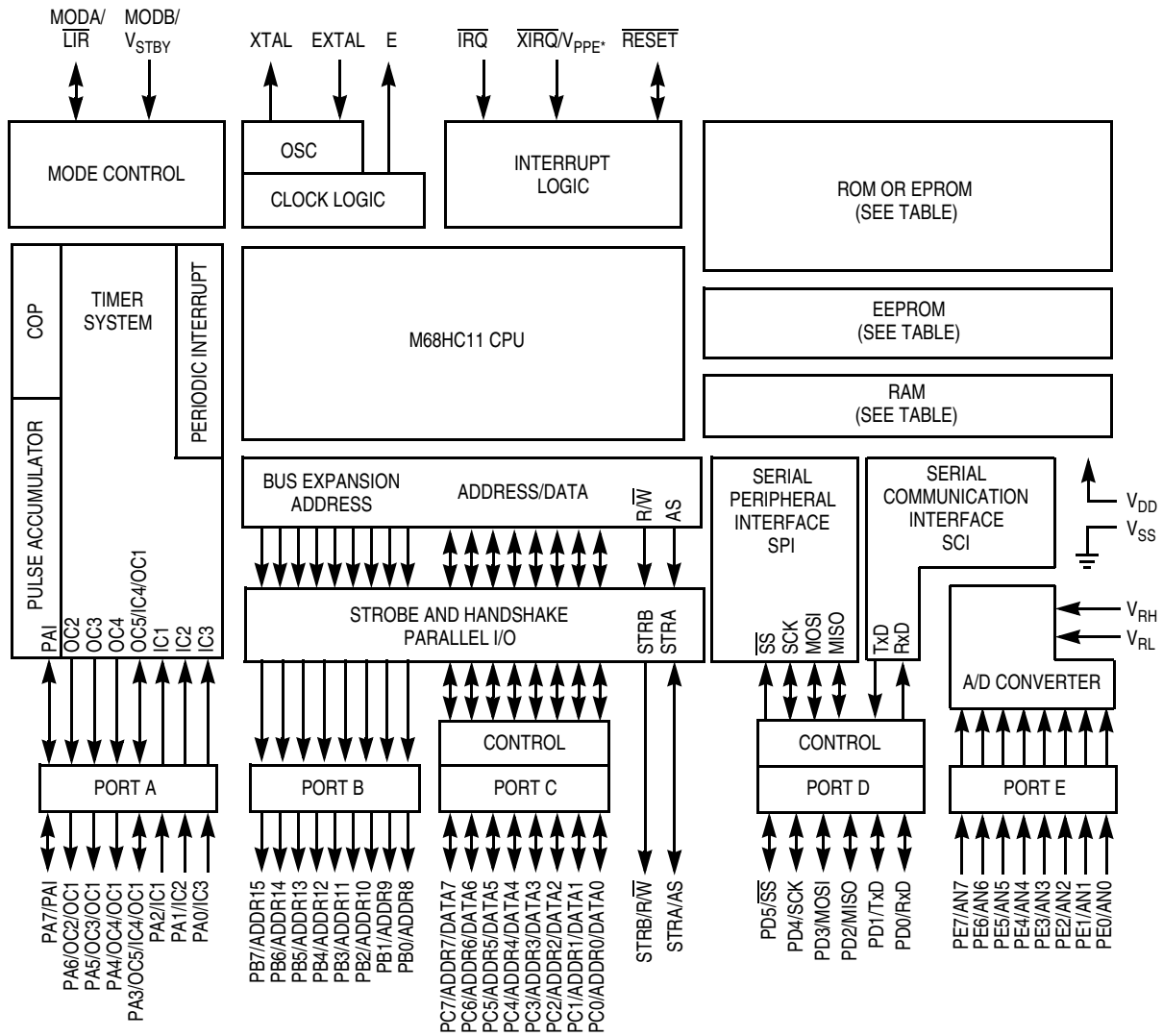
See [Figure 1-1](#) for a functional diagram of the E-series MCUs. Differences among devices are noted in the table accompanying [Figure 1-1](#).

## 1.4 Pin Descriptions

M68HC11 E-series MCUs are available packaged in:

- 52-pin plastic-leaded chip carrier (PLCC)
- 52-pin windowed ceramic leaded chip carrier (CLCC)
- 52-pin plastic thin quad flat pack, 10 mm x 10 mm (TQFP)
- 64-pin quad flat pack (QFP)
- 48-pin plastic dual in-line package (DIP), MC68HC811E2 only
- 56-pin plastic shrink dual in-line package, .070-inch lead spacing (SDIP)

Most pins on these MCUs serve two or more functions, as described in the following paragraphs. Refer to [Figure 1-2](#), [Figure 1-3](#), [Figure 1-4](#), [Figure 1-5](#), and [Figure 1-6](#) which show the M68HC11 E-series pin assignments for the PLCC/CLCC, QFP, TQFP, SDIP, and DIP packages.

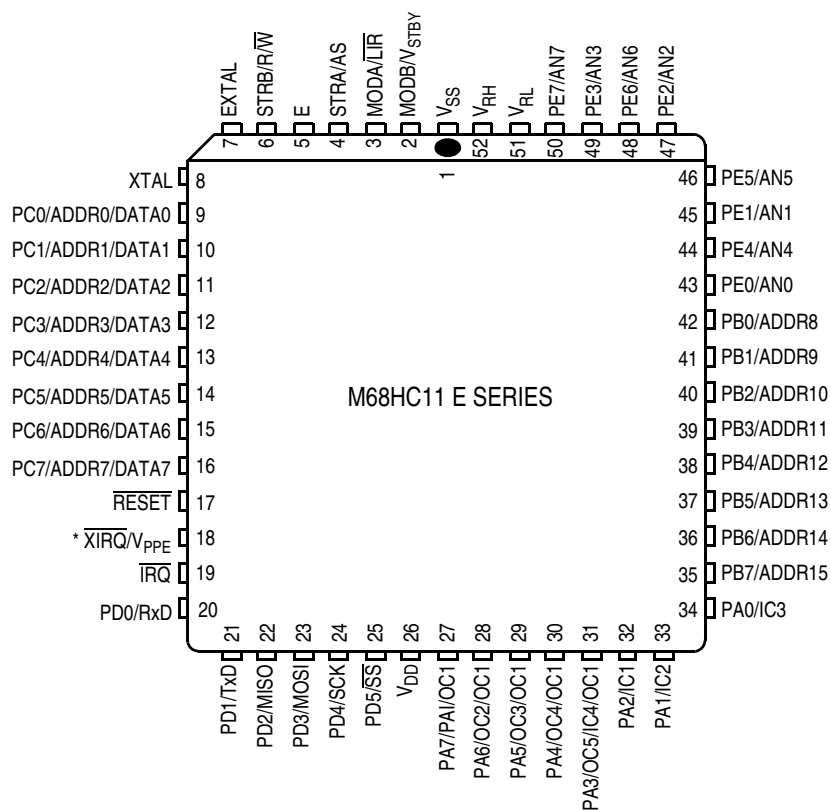


DEVICE	RAM	ROM	EPROM	EEPROM
MC68HC11E0	512	—	—	—
MC68HC11E1	512	—	—	512
MC68HC11E9	512	12 K	—	512
MC68HC711E9	512	—	12 K	512
MC68HC11E20	768	20 K	—	512
MC68HC711E20	768	—	20 K	512
MC68HC811E2	256	—	—	2048

\* V<sub>PPE</sub> applies only to devices with EPROM/OTPROM.

Figure 1-1. M68HC11 E-Series Block Diagram

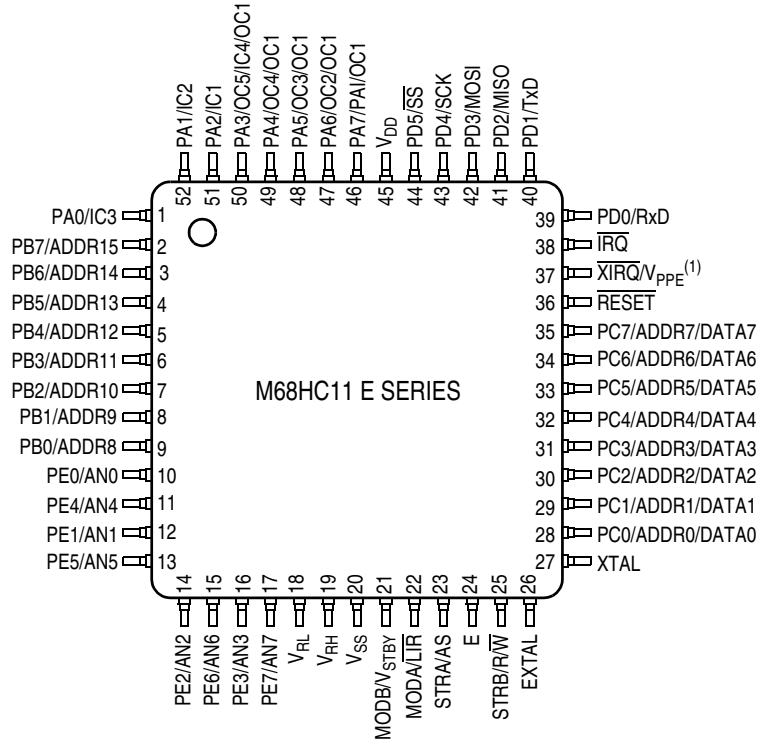




\* V<sub>PPE</sub> applies only to devices with EPROM/OTPROM.

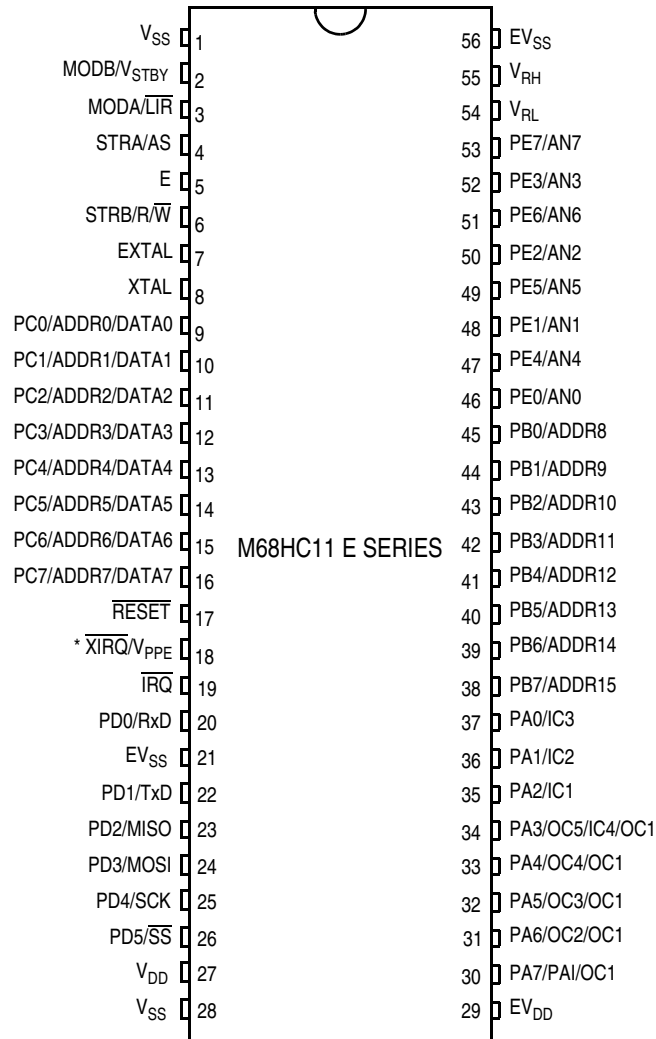
**Figure 1-2. Pin Assignments for 52-Pin PLCC and CLCC**





1. V<sub>PPE</sub> applies only to devices with EPROM/OTPROM.

**Figure 1-4. Pin Assignments for 52-Pin TQFP**



\*  $V_{PPE}$  applies only to devices with EPROM/OTPROM.

**Figure 1-5. Pin Assignments for 56-Pin SDIP**

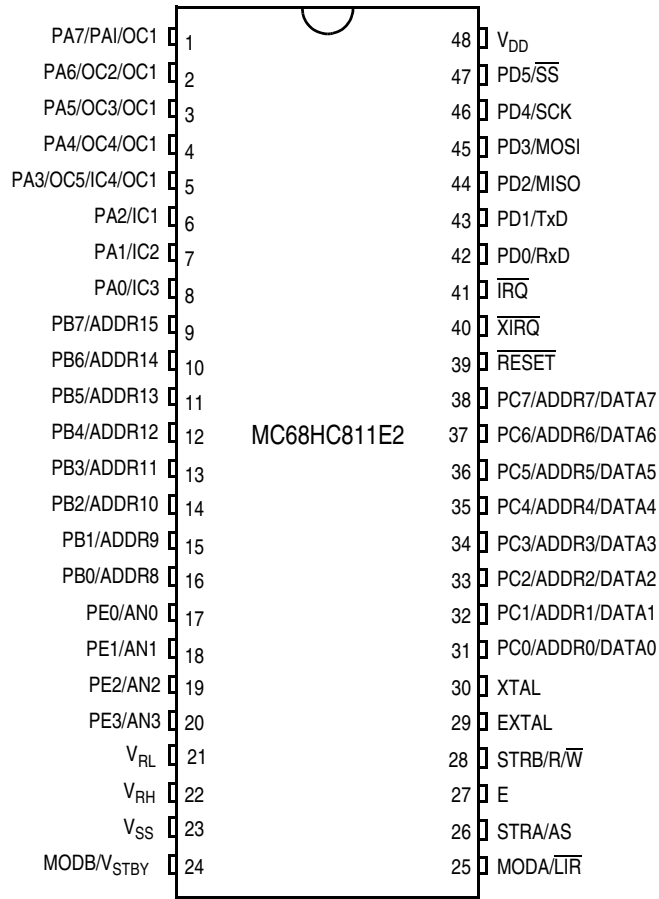


Figure 1-6. Pin Assignments for 48-Pin DIP (MC68HC811E2)

### 1.4.1 $V_{DD}$ and $V_{SS}$

Power is supplied to the MCU through  $V_{DD}$  and  $V_{SS}$ .  $V_{DD}$  is the power supply,  $V_{SS}$  is ground. The MCU operates from a single 5-volt (nominal) power supply. Low-voltage devices in the E series operate at 3.0–5.5 volts.

Very fast signal transitions occur on the MCU pins. The short rise and fall times place high, short duration current demands on the power supply. To prevent noise problems, provide good power supply bypassing at the MCU. Also, use bypass capacitors that have good

high-frequency characteristics and situate them as close to the MCU as possible. Bypass requirements vary, depending on how heavily the MCU pins are loaded.

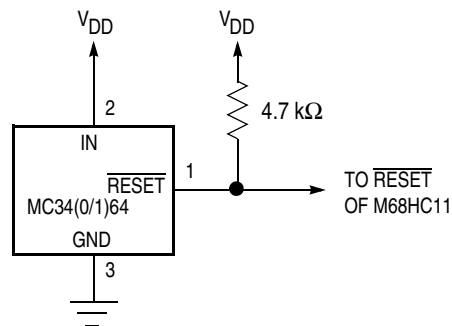


Figure 1-7. External Reset Circuit

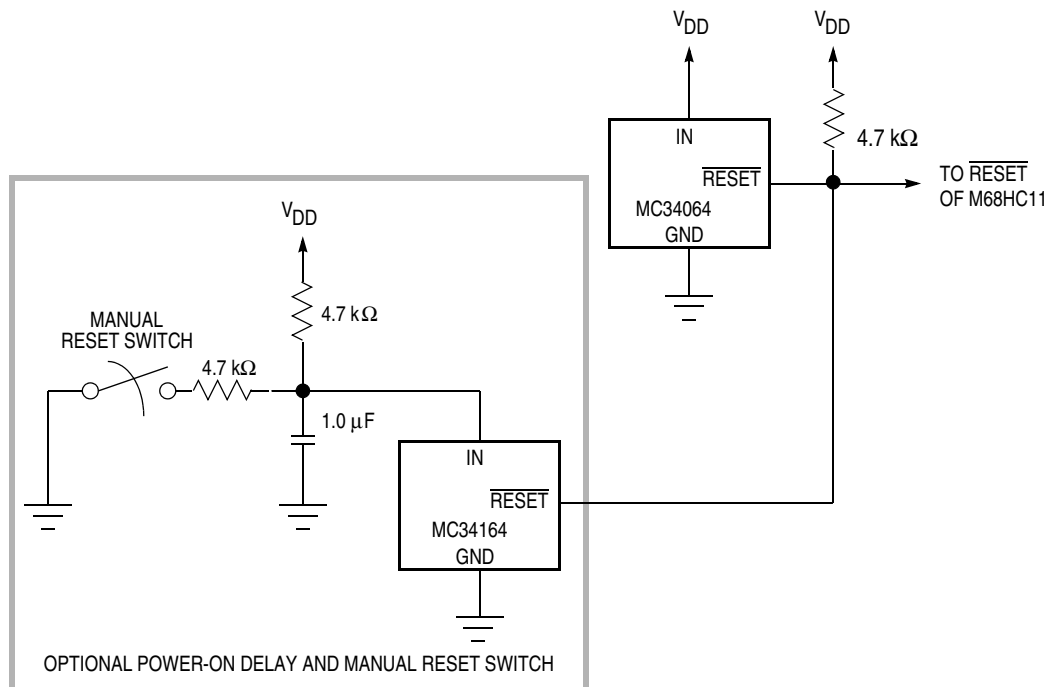


Figure 1-8. External Reset Circuit with Delay

## 1.4.2 $\overline{\text{RESET}}$

A bidirectional control signal,  $\overline{\text{RESET}}$ , acts as an input to initialize the MCU to a known startup state. It also acts as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or computer operating properly (COP) watchdog circuit. The CPU distinguishes between internal and external reset conditions by sensing whether the reset pin rises to a logic 1 in less than two E-clock cycles after a reset has occurred. See [Figure 1-7](#) and [Figure 1-8](#).

### CAUTION

*Do not connect an external resistor capacitor (RC) power-up delay circuit to the reset pin of M68HC11 devices because the circuit charge time constant can cause the device to misinterpret the type of reset that occurred.*

Because the CPU is not able to fetch and execute instructions properly when  $V_{DD}$  falls below the minimum operating voltage level, reset must be controlled. A low-voltage inhibit (LVI) circuit is required primarily for protection of EEPROM contents. However, since the configuration register (CONFIG) value is read from the EEPROM, protection is required even if the EEPROM array is not being used.

Presently, there are several economical ways to solve this problem. For example, two good external components for LVI reset are:

1. The Seiko S0854HN (or other S805 series devices):
  - a. Extremely low power (2  $\mu\text{A}$ )
  - a. TO-92 package
  - a. Limited temperature range,  $-20^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$
  - a. Available in various trip-point voltage ranges
2. The Freescale MC34064:
  - a. TO-92 or SO-8 package
  - a. Draws about 300  $\mu\text{A}$
  - a. Temperature range  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
  - a. Well controlled trip point
  - a. Inexpensive

Refer to [Chapter 5 Resets and Interrupts](#) for further information.

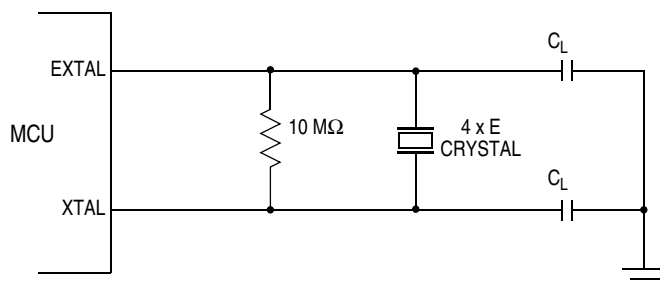
## 1.4.3 Crystal Driver and External Clock Input (XTAL and EXTAL)

These two pins provide the interface for either a crystal or a CMOS-compatible clock to control the internal clock generator circuitry. The frequency applied to these pins is four times higher than the desired E-clock rate.

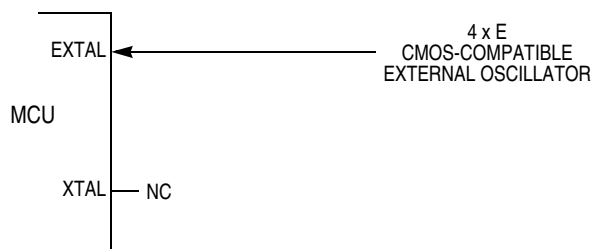
The XTAL pin must be left unterminated when an external CMOS-compatible clock input is connected to the EXTAL pin. The XTAL output is normally intended to drive only a crystal. Refer to [Figure 1-9](#) and [Figure 1-10](#).

### CAUTION

*In all cases, use caution around the oscillator pins. Load capacitances shown in the oscillator circuit are specified by the crystal manufacturer and should include all stray layout capacitances.*



**Figure 1-9. Common Parallel Resonant Crystal Connections**



**Figure 1-10. External Oscillator Connections**

#### 1.4.4 E-Clock Output (E)

E is the output connection for the internally generated E clock. The signal from E is used as a timing reference. The frequency of the E-clock output is one fourth that of the input frequency at the XTAL and EXTAL pins. When E-clock output is low, an internal process is taking place. When it is high, data is being accessed.

All clocks, including the E clock, are halted when the MCU is in stop mode. To reduce RFI emissions, the E-clock output of most E-series devices can be disabled while operating in single-chip modes.

The E-clock signal is always enabled on the MC68HC811E2.

#### 1.4.5 Interrupt Request ( $\overline{\text{IRQ}}$ )

The  $\overline{\text{IRQ}}$  input provides a means of applying asynchronous interrupt requests to the MCU. Either negative edge-sensitive triggering or level-sensitive triggering is program selectable (OPTION register).  $\overline{\text{IRQ}}$  is always configured to level-sensitive triggering at reset. When using  $\overline{\text{IRQ}}$  in a level-sensitive wired-OR configuration, connect an external pullup resistor, typically 4.7 k $\Omega$ , to  $V_{DD}$ .

#### 1.4.6 Non-Maskable Interrupt ( $\overline{\text{XIRQ}}/V_{PPE}$ )

The  $\overline{\text{XIRQ}}$  input provides a means of requesting a non-maskable interrupt after reset initialization. During reset, the X bit in the condition code register (CCR) is set and any interrupt is masked until MCU software enables it. Because the  $\overline{\text{XIRQ}}$  input is level-sensitive, it can be connected to a multiple-source wired-OR network with an external pullup resistor to  $V_{DD}$ .  $\overline{\text{XIRQ}}$  is often used as a power loss detect interrupt.

Whenever  $\overline{\text{XIRQ}}$  or  $\overline{\text{IRQ}}$  is used with multiple interrupt sources each source must drive the interrupt input with an open-drain type of driver to avoid contention between outputs.



**NOTE**

$\overline{IRQ}$  must be configured for level-sensitive operation if there is more than one source of  $\overline{IRQ}$  interrupt.

There should be a single pullup resistor near the MCU interrupt input pin (typically 4.7 k $\Omega$ ). There must also be an interlock mechanism at each interrupt source so that the source holds the interrupt line low until the MCU recognizes and acknowledges the interrupt request. If one or more interrupt sources are still pending after the MCU services a request, the interrupt line will still be held low and the MCU will be interrupted again as soon as the interrupt mask bit in the MCU is cleared (normally upon return from an interrupt). Refer to [Chapter 5 Resets and Interrupts](#).

$V_{PPE}$  is the input for the 12-volt nominal programming voltage required for EPROM/OTPROM programming. On devices without EPROM/OTPROM, this pin is only an  $\overline{XIRQ}$  input.

**CAUTION**

*During EPROM programming of the MC68HC711E9 device, the  $V_{PPE}$  pin circuitry may latch-up and be damaged if the input current is not limited to 10 mA. For more information please refer to MC68HC711E9 8-Bit Microcontroller Unit Mask Set Errata 3 (Freescale document order number 68HC711E9MSE3).*

### 1.4.7 MODA and MODB (MODA/ $\overline{LIR}$ and MODB/ $V_{STBY}$ )

During reset, MODA and MODB select one of the four operating modes:

- Single-chip mode
- Expanded mode
- Test mode
- Bootstrap mode

Refer to [Chapter 2 Operating Modes and On-Chip Memory](#).

After the operating mode has been selected, the load instruction register ( $\overline{LIR}$ ) pin provides an open-drain output to indicate that execution of an instruction has begun. A series of E-clock cycles occurs during execution of each instruction. The  $\overline{LIR}$  signal goes low during the first E-clock cycle of each instruction (opcode fetch). This output is provided for assistance in program debugging.

The  $V_{STBY}$  pin is used to input random-access memory (RAM) standby power. When the voltage on this pin is more than one MOS threshold (about 0.7 volts) above the  $V_{DD}$  voltage, the internal RAM and part of the reset logic are powered from this signal rather than the  $V_{DD}$  input. This allows RAM contents to be retained without  $V_{DD}$  power applied to the MCU. Reset must be driven low before  $V_{DD}$  is removed and must remain low until  $V_{DD}$  has been restored to a valid level.

### 1.4.8 $V_{RL}$ and $V_{RH}$

These two inputs provide the reference voltages for the analog-to-digital (A/D) converter circuitry:

- $V_{RL}$  is the low reference, typically 0 Vdc.
- $V_{RH}$  is the high reference.

For proper A/D converter operation:

- $V_{RH}$  should be at least 3 Vdc greater than  $V_{RL}$ .
- $V_{RL}$  and  $V_{RH}$  should be between  $V_{SS}$  and  $V_{DD}$ .

### 1.4.9 STRA/AS

The strobe A (STRA) and address strobe (AS) pin performs either of two separate functions, depending on the operating mode:

- In single-chip mode, STRA performs an input handshake (strobe input) function.
- In the expanded multiplexed mode, AS provides an address strobe function.

AS can be used to demultiplex the address and data signals at port C. Refer to [Chapter 2 Operating Modes and On-Chip Memory](#).

### 1.4.10 STRB/R $\overline{W}$

The strobe B (STRB) and read/write (R $\overline{W}$ ) pin act as either an output strobe or as a data bus direction indicator, depending on the operating mode.

In single-chip operating mode, STRB acts as a programmable strobe for handshake with other parallel devices. Refer to [Chapter 6 Parallel Input/Output \(I/O\) Ports](#) for further information.

In expanded multiplexed operating mode, R $\overline{W}$  is used to indicate the direction of transfers on the external data bus. A low on the R $\overline{W}$  pin indicates data is being written to the external data bus. A high on this pin indicates that a read cycle is in progress. R $\overline{W}$  stays low during consecutive data bus write cycles, such as a double-byte store. It is possible for data to be driven out of port C, if internal read visibility (IRV) is enabled and an internal address is read, even though R $\overline{W}$  is in a high-impedance state. Refer to [Chapter 2 Operating Modes and On-Chip Memory](#) for more information about IRVNE (internal read visibility not E).

### 1.4.11 Port Signals

Port pins have different functions in different operating modes. Pin functions for port A, port D, and port E are independent of operating modes. Port B and port C, however, are affected by operating mode. Port B provides eight general-purpose output signals in single-chip operating modes. When the microcontroller is in expanded multiplexed operating mode, port B pins are the eight high-order address lines.

Port C provides eight general-purpose input/output signals when the MCU is in the single-chip operating mode. When the microcontroller is in the expanded multiplexed operating mode, port C pins are a multiplexed address/data bus.

Refer to [Table 1-1](#) for a functional description of the 40 port signals within different operating modes. Terminate unused inputs and input/output (I/O) pins configured as inputs high or low.

### 1.4.12 Port A

In all operating modes, port A can be configured for three timer input capture (IC) functions and four timer output compare (OC) functions. An additional pin can be configured as either the fourth IC or the fifth OC. Any port A pin that is not currently being used for a timer function can be used as either a general-purpose input or output line. Only port A pins PA7 and PA3 have an associated data direction control bit that allows the pin to be selectively configured as input or output. Bits DDRA7 and DDRA3 located in PACTL register control data direction for PA7 and PA3, respectively. All other port A pins are fixed as either input or output.

PA7 can function as general-purpose I/O or as timer output compare for OC1. PA7 is also the input to the pulse accumulator, even while functioning as a general-purpose I/O or an OC1 output.