



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# MC68HC908GZ16

# MC68HC908GZ8

Data Sheet

***M68HC08***  
***Microcontrollers***

MC68HC908GZ16  
Rev. 4.0  
10/2006

[freescale.com](http://freescale.com)



# MC68HC908GZ16

# MC68HC908GZ8

## Data Sheet

---

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.  
This product incorporates SuperFlash® technology licensed from SST.

© Freescale Semiconductor, Inc., 2005, 2006. All rights reserved.

## Revision History

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

## Revision History

Date	Revision Level	Description	Page Number(s)
February, 2003	N/A	Initial release	N/A
October, 2004	1.0	Reorganized to meet latest publication standards for M68HC08 Family documentation	N/A
		Added Table 1-1. Summary of Device Variations	19
		Figure 5-2. Configuration Register 1 (CONFIG1) — Changed bit 0 from SCIBDSRC to ESCIBDSRC.	80
		Chapter 15 Enhanced Serial Communications Interface (ESCI) Module — Updated with additional data	181–212
		Chapter 17 Serial Peripheral Interface (SPI) Module — Removed all references to DMAS	N/A
		Added DC injection current values to: 21.5 5-Vdc Electrical Characteristics 21.6 3.3-Vdc Electrical Characteristics	289 291
		21.15 Memory Characteristics — Updated table entries	302
		Corrected ICG references to CGM throughout document.	N/A
		Chapter 22 Ordering Information and Mechanical Specifications — Corrected device ordering information	303
		Added the following: Appendix A MC68HC908GZ8	311–314
June, 2005	2.0	205 — Corrected Functionality entries	205
		15.9.1 ESCI Arbiter Control Register — Corrected bit ACLK bit description	209
		15.9.3 Bit Time Measurement — Corrected definition for ACLK bit	210
March, 2006	3.0	10.5 Clock Generator Module (CGM) — Updated description to remove erroneous information.	110
October, 2006	4.0	<a href="#">1.6 Unused Pin Termination</a> — Added new section.	<a href="#">26</a>
		<a href="#">12.2 Features</a> — Corrected timer link connection from TIM2 channel 0 to TIM1 channel 0.	<a href="#">121</a>
		<a href="#">12.9 Timer Link</a> — Corrected timer link connection from TIM2 channel 0 to TIM1 channel 0.	<a href="#">133</a>
		<a href="#">13.1 Introduction</a> — Replaced note with unused pin termination text.	<a href="#">155</a>
		<a href="#">21.5 5-Vdc Electrical Characteristics</a> and <a href="#">21.6 3.3-Vdc Electrical Characteristics</a> — Updated DC injection current specification.	<a href="#">289</a> <a href="#">291</a>

# List of Chapters

Chapter 1 General Description . . . . .	19
Chapter 2 Memory . . . . .	27
Chapter 3 Analog-to-Digital Converter (ADC) . . . . .	47
Chapter 4 Clock Generator Module (CGM) . . . . .	59
Chapter 5 Configuration Register (CONFIG) . . . . .	79
Chapter 6 Computer Operating Properly (COP) Module . . . . .	83
Chapter 7 Central Processor Unit (CPU) . . . . .	87
Chapter 8 External Interrupt (IRQ) . . . . .	99
Chapter 9 Keyboard Interrupt Module (KBI) . . . . .	103
Chapter 10 Low-Power Modes . . . . .	109
Chapter 11 Low-Voltage Inhibit (LVI) . . . . .	117
Chapter 12 MSCAN08 Controller (MSCAN08) . . . . .	121
Chapter 13 Input/Output (I/O) Ports . . . . .	155
Chapter 14 Resets and Interrupts . . . . .	169
Chapter 15 Enhanced Serial Communications Interface (ESCI) Module . . . . .	181
Chapter 16 System Integration Module (SIM) . . . . .	213
Chapter 17 Serial Peripheral Interface (SPI) Module . . . . .	231
Chapter 18 Timebase Module (TBM) . . . . .	251
Chapter 19 Timer Interface Module (TIM) . . . . .	255
Chapter 20 Development Support . . . . .	271
Chapter 21 Electrical Specifications . . . . .	287
Chapter 22 Ordering Information and Mechanical Specifications . . . . .	303
Appendix A MC68HC908GZ8 . . . . .	311



# Table of Contents

## Chapter 1 General Description

1.1	Introduction	19
1.2	Features	19
1.2.1	Standard Features	19
1.2.2	Features of the CPU08	21
1.3	MCU Block Diagram	21
1.4	Pin Assignments	21
1.5	Pin Functions	24
1.5.1	Power Supply Pins ( $V_{DD}$ and $V_{SS}$ )	24
1.5.2	Oscillator Pins (OSC1 and OSC2)	24
1.5.3	External Reset Pin ( $\overline{RST}$ )	24
1.5.4	External Interrupt Pin ( $\overline{IRQ}$ )	24
1.5.5	CGM Power Supply Pins ( $V_{DDA}$ and $V_{SSA}$ )	25
1.5.6	External Filter Capacitor Pin ( $V_{CGMXFC}$ )	25
1.5.7	ADC Power Supply/Reference Pins ( $V_{DDAD}/V_{REFH}$ and $V_{SSAD}/V_{REFL}$ )	25
1.5.8	Port A Input/Output (I/O) Pins (PTA7/KBD7–PTA0/KBD0)	25
1.5.9	Port B I/O Pins (PTB7/AD7–PTB0/AD0)	25
1.5.10	Port C I/O Pins (PTC6–PTC0/CANTX)	25
1.5.11	Port D I/O Pins (PTD7/T2CH1–PTD0/ $\overline{SS}$ )	25
1.5.12	Port E I/O Pins (PTE5–PTE2, PTE1/RxD, and PTE0/TxD)	26
1.6	Unused Pin Termination	26

## Chapter 2 Memory

2.1	Introduction	27
2.2	Unimplemented Memory Locations	27
2.3	Reserved Memory Locations	27
2.4	Input/Output (I/O) Section	27
2.5	Random-Access Memory (RAM)	38
2.6	FLASH Memory (FLASH)	38
2.6.1	Functional Description	38
2.6.2	FLASH Control Register	39
2.6.3	FLASH Page Erase Operation	40
2.6.4	FLASH Mass Erase Operation	41
2.6.5	FLASH Program/Read Operation	41
2.6.6	FLASH Block Protection	44
2.6.7	FLASH Block Protect Register	44
2.6.8	Wait Mode	45
2.6.9	Stop Mode	45



## Chapter 3 Analog-to-Digital Converter (ADC)

3.1	Introduction . . . . .	47
3.2	Features . . . . .	47
3.3	Functional Description . . . . .	47
3.3.1	ADC Port I/O Pins . . . . .	47
3.3.2	Voltage Conversion . . . . .	49
3.3.3	Conversion Time . . . . .	50
3.3.4	Conversion . . . . .	50
3.3.5	Accuracy and Precision . . . . .	50
3.3.6	Result Justification . . . . .	50
3.4	Monotonicity . . . . .	51
3.5	Interrupts . . . . .	51
3.6	Low-Power Modes . . . . .	51
3.6.1	Wait Mode . . . . .	52
3.6.2	Stop Mode . . . . .	52
3.7	I/O Signals . . . . .	52
3.7.1	ADC Analog Power Pin ( $V_{DDAD}$ ) . . . . .	52
3.7.2	ADC Analog Ground Pin ( $V_{SSAD}$ ) . . . . .	52
3.7.3	ADC Voltage Reference High Pin ( $V_{REFH}$ ) . . . . .	52
3.7.4	ADC Voltage Reference Low Pin ( $V_{REFL}$ ) . . . . .	53
3.7.5	ADC Voltage In ( $V_{ADIN}$ ) . . . . .	53
3.8	I/O Registers . . . . .	53
3.8.1	ADC Status and Control Register . . . . .	53
3.8.2	ADC Data Register High and Data Register Low . . . . .	55
3.8.2.1	Left Justified Mode . . . . .	55
3.8.2.2	Right Justified Mode . . . . .	55
3.8.2.3	Left Justified Signed Data Mode . . . . .	56
3.8.2.4	Eight Bit Truncation Mode . . . . .	56
3.8.3	ADC Clock Register . . . . .	57

## Chapter 4 Clock Generator Module (CGM)

4.1	Introduction . . . . .	59
4.2	Features . . . . .	59
4.3	Functional Description . . . . .	59
4.3.1	Crystal Oscillator Circuit . . . . .	61
4.3.2	Phase-Locked Loop Circuit (PLL) . . . . .	61
4.3.3	PLL Circuits . . . . .	61
4.3.4	Acquisition and Tracking Modes . . . . .	62
4.3.5	Manual and Automatic PLL Bandwidth Modes . . . . .	62
4.3.6	Programming the PLL . . . . .	63
4.3.7	Special Programming Exceptions . . . . .	65
4.3.8	Base Clock Selector Circuit . . . . .	65
4.3.9	CGM External Connections . . . . .	66

4.4	I/O Signals	67
4.4.1	Crystal Amplifier Input Pin (OSC1)	67
4.4.2	Crystal Amplifier Output Pin (OSC2)	67
4.4.3	External Filter Capacitor Pin (CGMXFC)	67
4.4.4	PLL Analog Power Pin ( $V_{DDA}$ )	67
4.4.5	PLL Analog Ground Pin ( $V_{SSA}$ )	67
4.4.6	Oscillator Enable Signal (SIMOSCEN)	67
4.4.7	Oscillator Stop Mode Enable Bit (OSCSTOPENB)	67
4.4.8	Crystal Output Frequency Signal (CGMXCLK)	68
4.4.9	CGM Base Clock Output (CGMOUT)	68
4.4.10	CGM CPU Interrupt (CGMINT)	68
4.5	CGM Registers	68
4.5.1	PLL Control Register	69
4.5.2	PLL Bandwidth Control Register	71
4.5.3	PLL Multiplier Select Register High	72
4.5.4	PLL Multiplier Select Register Low	73
4.5.5	PLL VCO Range Select Register	73
4.6	Interrupts	74
4.7	Special Modes	75
4.7.1	Wait Mode	75
4.7.2	Stop Mode	75
4.7.3	CGM During Break Interrupts	75
4.8	Acquisition/Lock Time Specifications	75
4.8.1	Acquisition/Lock Time Definitions	75
4.8.2	Parametric Influences on Reaction Time	76
4.8.3	Choosing a Filter	76

## Chapter 5 Configuration Register (CONFIG)

5.1	Introduction	79
5.2	Functional Description	79

## Chapter 6 Computer Operating Properly (COP) Module

6.1	Introduction	83
6.2	Functional Description	83
6.3	I/O Signals	84
6.3.1	CGMXCLK	84
6.3.2	STOP Instruction	84
6.3.3	COPCTL Write	84
6.3.4	Power-On Reset	84
6.3.5	Internal Reset	84
6.3.6	Reset Vector Fetch	85
6.3.7	COPD (COP Disable)	85
6.3.8	COPRS (COP Rate Select)	85
6.4	COP Control Register	85
6.5	Interrupts	85
6.6	Monitor Mode	85

## Table of Contents

6.7	Low-Power Modes . . . . .	85
6.7.1	Wait Mode . . . . .	85
6.7.2	Stop Mode . . . . .	86
6.8	COP Module During Break Mode . . . . .	86

## Chapter 7 Central Processor Unit (CPU)

7.1	Introduction . . . . .	87
7.2	Features . . . . .	87
7.3	CPU Registers . . . . .	87
7.3.1	Accumulator . . . . .	88
7.3.2	Index Register . . . . .	88
7.3.3	Stack Pointer . . . . .	89
7.3.4	Program Counter . . . . .	89
7.3.5	Condition Code Register . . . . .	90
7.4	Arithmetic/Logic Unit (ALU) . . . . .	91
7.5	Low-Power Modes . . . . .	91
7.5.1	Wait Mode . . . . .	91
7.5.2	Stop Mode . . . . .	91
7.6	CPU During Break Interrupts . . . . .	91
7.7	Instruction Set Summary . . . . .	92
7.8	Opcode Map . . . . .	97

## Chapter 8 External Interrupt (IRQ)

8.1	Introduction . . . . .	99
8.2	Features . . . . .	99
8.3	Functional Description . . . . .	99
8.4	$\overline{\text{IRQ}}$ Pin . . . . .	101
8.5	IRQ Module During Break Interrupts . . . . .	101
8.6	IRQ Status and Control Register . . . . .	102

## Chapter 9 Keyboard Interrupt Module (KBI)

9.1	Introduction . . . . .	103
9.2	Features . . . . .	103
9.3	Functional Description . . . . .	103
9.4	Keyboard Initialization . . . . .	106
9.5	Low-Power Modes . . . . .	106
9.5.1	Wait Mode . . . . .	106
9.5.2	Stop Mode . . . . .	107
9.6	Keyboard Module During Break Interrupts . . . . .	107
9.7	I/O Registers . . . . .	107
9.7.1	Keyboard Status and Control Register . . . . .	107
9.7.2	Keyboard Interrupt Enable Register . . . . .	108

## Chapter 10 Low-Power Modes

10.1	Introduction	109
10.1.1	Wait Mode	109
10.1.2	Stop Mode	109
10.2	Analog-to-Digital Converter (ADC)	109
10.2.1	Wait Mode	109
10.2.2	Stop Mode	109
10.3	Break Module (BRK)	110
10.3.1	Wait Mode	110
10.3.2	Stop Mode	110
10.4	Central Processor Unit (CPU)	110
10.4.1	Wait Mode	110
10.4.2	Stop Mode	110
10.5	Clock Generator Module (CGM)	110
10.5.1	Wait Mode	110
10.5.2	Stop Mode	110
10.6	Computer Operating Properly Module (COP)	111
10.6.1	Wait Mode	111
10.6.2	Stop Mode	111
10.7	External Interrupt Module (IRQ)	111
10.7.1	Wait Mode	111
10.7.2	Stop Mode	111
10.8	Keyboard Interrupt Module (KBI)	111
10.8.1	Wait Mode	111
10.8.2	Stop Mode	111
10.9	Low-Voltage Inhibit Module (LVI)	112
10.9.1	Wait Mode	112
10.9.2	Stop Mode	112
10.10	Enhanced Serial Communications Interface Module (ESCI)	112
10.10.1	Wait Mode	112
10.10.2	Stop Mode	112
10.11	Serial Peripheral Interface Module (SPI)	112
10.11.1	Wait Mode	112
10.11.2	Stop Mode	112
10.12	Timer Interface Module (TIM1 and TIM2)	113
10.12.1	Wait Mode	113
10.12.2	Stop Mode	113
10.13	Timebase Module (TBM)	113
10.13.1	Wait Mode	113
10.13.2	Stop Mode	113
10.14	MSCAN	113
10.14.1	Wait Mode	113
10.14.2	Stop Mode	113
10.15	Exiting Wait Mode	114
10.16	Exiting Stop Mode	115

## Chapter 11 Low-Voltage Inhibit (LVI)

11.1	Introduction .....	117
11.2	Features .....	117
11.3	Functional Description .....	117
11.3.1	Polled LVI Operation .....	118
11.3.2	Forced Reset Operation .....	118
11.3.3	Voltage Hysteresis Protection .....	119
11.3.4	LVI Trip Selection .....	119
11.4	LVI Status Register .....	119
11.5	LVI Interrupts .....	119
11.6	Low-Power Modes .....	120
11.6.1	Wait Mode .....	120
11.6.2	Stop Mode .....	120

## Chapter 12 MSCAN08 Controller (MSCAN08)

12.1	Introduction .....	121
12.2	Features .....	121
12.3	External Pins .....	122
12.4	Message Storage .....	123
12.4.1	Background .....	123
12.4.2	Receive Structures .....	124
12.4.3	Transmit Structures .....	125
12.5	Identifier Acceptance Filter .....	126
12.6	Interrupts .....	129
12.6.1	Interrupt Acknowledge .....	129
12.6.2	Interrupt Vectors .....	129
12.7	Protocol Violation Protection .....	130
12.8	Low-Power Modes .....	130
12.8.1	MSCAN08 Sleep Mode .....	131
12.8.2	MSCAN08 Soft Reset Mode .....	132
12.8.3	MSCAN08 Power-Down Mode .....	132
12.8.4	CPU Wait Mode .....	133
12.8.5	Programmable Wakeup Function .....	133
12.9	Timer Link .....	133
12.10	Clock System .....	133
12.11	Memory Map .....	136
12.12	Programmer's Model of Message Storage .....	137
12.12.1	Message Buffer Outline .....	137
12.12.2	Identifier Registers .....	139
12.12.3	Data Length Register (DLR) .....	140
12.12.4	Data Segment Registers (DSRn) .....	140
12.12.5	Transmit Buffer Priority Registers .....	140
12.13	Programmer's Model of Control Registers .....	141
12.13.1	MSCAN08 Module Control Register 0 .....	142
12.13.2	MSCAN08 Module Control Register 1 .....	143

12.13.3	MSCAN08 Bus Timing Register 0	144
12.13.4	MSCAN08 Bus Timing Register 1	145
12.13.5	MSCAN08 Receiver Flag Register (CRFLG)	146
12.13.6	MSCAN08 Receiver Interrupt Enable Register	148
12.13.7	MSCAN08 Transmitter Flag Register	149
12.13.8	MSCAN08 Transmitter Control Register	150
12.13.9	MSCAN08 Identifier Acceptance Control Register	150
12.13.10	MSCAN08 Receive Error Counter	151
12.13.11	MSCAN08 Transmit Error Counter	152
12.13.12	MSCAN08 Identifier Acceptance Registers	152
12.13.13	MSCAN08 Identifier Mask Registers (CIDMR0–CIDMR3)	153

## Chapter 13 Input/Output (I/O) Ports

13.1	Introduction	155
13.2	Unused Pin Termination	155
13.3	Port A	158
13.3.1	Port A Data Register	158
13.3.2	Data Direction Register A	158
13.3.3	Port A Input Pullup Enable Register	159
13.4	Port B	160
13.4.1	Port B Data Register	160
13.4.2	Data Direction Register B	160
13.5	Port C	162
13.5.1	Port C Data Register	162
13.5.2	Data Direction Register C	162
13.5.3	Port C Input Pullup Enable Register	164
13.6	Port D	164
13.6.1	Port D Data Register	164
13.6.2	Data Direction Register D	165
13.6.3	Port D Input Pullup Enable Register	166
13.7	Port E	167
13.7.1	Port E Data Register	167
13.7.2	Data Direction Register E	167

## Chapter 14 Resets and Interrupts

14.1	Introduction	169
14.2	Resets	169
14.2.1	Effects	169
14.2.2	External Reset	169
14.2.3	Internal Reset	169
14.2.3.1	Power-On Reset (POR)	170
14.2.3.2	Computer Operating Properly (COP) Reset	170
14.2.3.3	Low-Voltage Inhibit (LVI) Reset	170
14.2.3.4	Illegal Opcode Reset	171
14.2.3.5	Illegal Address Reset	171
14.2.4	System Integration Module (SIM) Reset Status Register	171

## Table of Contents

14.3	Interrupts	172
14.3.1	Effects	172
14.3.2	Sources	173
14.3.2.1	Software Interrupt (SWI) Instruction	173
14.3.2.2	Break Interrupt	173
14.3.2.3	$\overline{\text{IRQ}}$ Pin	176
14.3.2.4	Clock Generator (CGM)	176
14.3.2.5	Timer Interface Module 1 (TIM1)	176
14.3.2.6	Timer Interface Module 2 (TIM2)	176
14.3.2.7	Serial Peripheral Interface (SPI)	176
14.3.2.8	Serial Communications Interface (SCI)	177
14.3.2.9	$\overline{\text{KBD0}}\text{--}\overline{\text{KBD7}}$ Pins	177
14.3.2.10	Analog-to-Digital Converter (ADC)	177
14.3.2.11	Timebase Module (TBM)	178
14.3.2.12	MSCAN	178
14.3.3	Interrupt Status Registers	179
14.3.3.1	Interrupt Status Register 1	180
14.3.3.2	Interrupt Status Register 2	180
14.3.3.3	Interrupt Status Register 3	180

## Chapter 15

### Enhanced Serial Communications Interface (ESCI) Module

15.1	Introduction	181
15.2	Features	181
15.3	Pin Name Conventions	183
15.4	Functional Description	183
15.4.1	Data Format	186
15.4.2	Transmitter	186
15.4.2.1	Character Length	187
15.4.2.2	Character Transmission	187
15.4.2.3	Break Characters	187
15.4.2.4	Idle Characters	188
15.4.2.5	Inversion of Transmitted Output	188
15.4.2.6	Transmitter Interrupts	188
15.4.3	Receiver	189
15.4.3.1	Character Length	190
15.4.3.2	Character Reception	190
15.4.3.3	Data Sampling	190
15.4.3.4	Framing Errors	192
15.4.3.5	Baud Rate Tolerance	192
15.4.3.6	Receiver Wakeup	193
15.4.3.7	Receiver Interrupts	194
15.4.3.8	Error Interrupts	194
15.5	Low-Power Modes	195
15.5.1	Wait Mode	195
15.5.2	Stop Mode	195
15.6	ESCI During Break Module Interrupts	195

15.7	I/O Signals	195
15.7.1	PTE0/TxD (Transmit Data)	195
15.7.2	PTE1/RxD (Receive Data)	195
15.8	I/O Registers	196
15.8.1	ESCI Control Register 1	196
15.8.2	ESCI Control Register 2	198
15.8.3	ESCI Control Register 3	200
15.8.4	ESCI Status Register 1	201
15.8.5	ESCI Status Register 2	203
15.8.6	ESCI Data Register	204
15.8.7	ESCI Baud Rate Register	204
15.8.8	ESCI Prescaler Register	206
15.9	ESCI Arbiter	209
15.9.1	ESCI Arbiter Control Register	209
15.9.2	ESCI Arbiter Data Register	210
15.9.3	Bit Time Measurement	210
15.9.4	Arbitration Mode	212

## Chapter 16 System Integration Module (SIM)

16.1	Introduction	213
16.2	SIM Bus Clock Control and Generation	215
16.2.1	Bus Timing	215
16.2.2	Clock Startup from POR or LVI Reset	215
16.2.3	Clocks in Stop Mode and Wait Mode	215
16.3	Reset and System Initialization	216
16.3.1	External Pin Reset	216
16.3.2	Active Resets from Internal Sources	217
16.3.2.1	Power-On Reset	217
16.3.2.2	Computer Operating Properly (COP) Reset	218
16.3.2.3	Illegal Opcode Reset	218
16.3.2.4	Illegal Address Reset	218
16.3.2.5	Low-Voltage Inhibit (LVI) Reset	218
16.3.2.6	Monitor Mode Entry Module Reset (MODRST)	219
16.4	SIM Counter	219
16.4.1	SIM Counter During Power-On Reset	219
16.4.2	SIM Counter During Stop Mode Recovery	219
16.4.3	SIM Counter and Reset States	219
16.5	Exception Control	219
16.5.1	Interrupts	219
16.5.1.1	Hardware Interrupts	222
16.5.1.2	SWI Instruction	223
16.5.1.3	Interrupt Status Registers	223
16.5.2	Reset	225
16.5.3	Break Interrupts	225
16.5.4	Status Flag Protection in Break Mode	225



## Table of Contents

16.6	Low-Power Modes . . . . .	225
16.6.1	Wait Mode . . . . .	225
16.6.2	Stop Mode . . . . .	226
16.7	SIM Registers . . . . .	227
16.7.1	Break Status Register . . . . .	228
16.7.2	SIM Reset Status Register . . . . .	228
16.7.3	Break Flag Control Register . . . . .	229

## Chapter 17 Serial Peripheral Interface (SPI) Module

17.1	Introduction . . . . .	231
17.2	Features . . . . .	231
17.3	Pin Name Conventions . . . . .	231
17.4	Functional Description . . . . .	233
17.4.1	Master Mode . . . . .	233
17.4.2	Slave Mode . . . . .	235
17.5	Transmission Formats . . . . .	235
17.5.1	Clock Phase and Polarity Controls . . . . .	235
17.5.2	Transmission Format When CPHA = 0 . . . . .	236
17.5.3	Transmission Format When CPHA = 1 . . . . .	237
17.5.4	Transmission Initiation Latency . . . . .	237
17.6	Queuing Transmission Data . . . . .	239
17.7	Error Conditions . . . . .	240
17.7.1	Overflow Error . . . . .	240
17.7.2	Mode Fault Error . . . . .	241
17.8	Interrupts . . . . .	243
17.9	Resetting the SPI . . . . .	244
17.10	Low-Power Modes . . . . .	244
17.10.1	Wait Mode . . . . .	244
17.10.2	Stop Mode . . . . .	244
17.11	SPI During Break Interrupts . . . . .	245
17.12	I/O Signals . . . . .	245
17.12.1	MISO (Master In/Slave Out) . . . . .	245
17.12.2	MOSI (Master Out/Slave In) . . . . .	246
17.12.3	SPSCK (Serial Clock) . . . . .	246
17.12.4	$\overline{SS}$ (Slave Select) . . . . .	246
17.12.5	CGND (Clock Ground) . . . . .	247
17.13	I/O Registers . . . . .	247
17.13.1	SPI Control Register . . . . .	247
17.13.2	SPI Status and Control Register . . . . .	248
17.13.3	SPI Data Register . . . . .	250

## Chapter 18 Timebase Module (TBM)

18.1	Introduction . . . . .	251
18.2	Features . . . . .	251
18.3	Functional Description . . . . .	251

18.4	Interrupts	251
18.5	TBM Interrupt Rate	252
18.6	Low-Power Modes	253
18.6.1	Wait Mode	253
18.6.2	Stop Mode	253
18.7	Timebase Control Register	254

## Chapter 19 Timer Interface Module (TIM)

19.1	Introduction	255
19.2	Features	257
19.3	Pin Name Conventions	257
19.4	Functional Description	257
19.4.1	TIM Counter Prescaler	259
19.4.2	Input Capture	259
19.4.3	Output Compare	260
19.4.3.1	Unbuffered Output Compare	260
19.4.3.2	Buffered Output Compare	260
19.4.4	Pulse Width Modulation (PWM)	261
19.4.4.1	Unbuffered PWM Signal Generation	261
19.4.4.2	Buffered PWM Signal Generation	262
19.4.4.3	PWM Initialization	262
19.5	Interrupts	263
19.6	Low-Power Modes	263
19.6.1	Wait Mode	263
19.6.2	Stop Mode	264
19.7	TIM During Break Interrupts	264
19.8	I/O Signals	264
19.9	I/O Registers	264
19.9.1	TIM Status and Control Register	265
19.9.2	TIM Counter Registers	266
19.9.3	TIM Counter Modulo Registers	267
19.9.4	TIM Channel Status and Control Registers	267
19.9.5	TIM Channel Registers	270

## Chapter 20 Development Support

20.1	Introduction	271
20.2	Break Module (BRK)	271
20.2.1	Functional Description	271
20.2.1.1	Flag Protection During Break Interrupts	273
20.2.1.2	TIM During Break Interrupts	273
20.2.1.3	COP During Break Interrupts	273
20.2.2	Break Module Registers	273
20.2.2.1	Break Status and Control Register	274
20.2.2.2	Break Address Registers	274
20.2.2.3	Break Status Register	275
20.2.2.4	Break Flag Control Register	275

## Table of Contents

20.2.3	Low-Power Modes . . . . .	275
20.3	Monitor ROM (MON) . . . . .	275
20.3.1	Functional Description . . . . .	276
20.3.1.1	Normal Monitor Mode . . . . .	280
20.3.1.2	Forced Monitor Mode . . . . .	280
20.3.1.3	Monitor Vectors . . . . .	280
20.3.1.4	Data Format . . . . .	281
20.3.1.5	Break Signal . . . . .	281
20.3.1.6	Baud Rate . . . . .	281
20.3.1.7	Commands . . . . .	281
20.3.2	Security . . . . .	285

## Chapter 21 Electrical Specifications

21.1	Introduction . . . . .	287
21.2	Absolute Maximum Ratings . . . . .	287
21.3	Functional Operating Range . . . . .	288
21.4	Thermal Characteristics . . . . .	288
21.5	5-Vdc Electrical Characteristics . . . . .	289
21.6	3.3-Vdc Electrical Characteristics . . . . .	291
21.7	5.0-Volt Control Timing . . . . .	293
21.8	3.3-Volt Control Timing . . . . .	293
21.9	Clock Generation Module Characteristics . . . . .	294
21.9.1	CGM Component Specifications . . . . .	294
21.9.2	CGM Electrical Specifications . . . . .	294
21.10	5.0-Volt ADC Characteristics . . . . .	295
21.11	3.3-Volt ADC Characteristics . . . . .	296
21.12	5.0-Volt SPI Characteristics . . . . .	297
21.13	3.3-Volt SPI Characteristics . . . . .	298
21.14	Timer Interface Module Characteristics . . . . .	301
21.15	Memory Characteristics . . . . .	302

## Chapter 22 Ordering Information and Mechanical Specifications

22.1	Introduction . . . . .	303
22.2	MC Order Numbers . . . . .	303
22.3	Package Dimensions . . . . .	303

## Appendix A MC68HC908GZ8

A.1	Introduction . . . . .	311
A.2	Block Diagram . . . . .	311
A.3	Memory . . . . .	311
A.4	Ordering Information . . . . .	314

# Chapter 1

## General Description

### 1.1 Introduction

The MC68HC908GZ16 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

**Table 1-1. Summary of Device Variations**

Device	Memory Size
MC68HC908QZ16	16 Kbytes user FLASH
MC68HC908GZ8	8 Kbytes user FLASH

The information contained in this document pertains to both the MC68HC908GZ16 and the MC68HC908GZ8 with the exceptions shown [Appendix A MC68HC908GZ8](#)

### 1.2 Features

For convenience, features have been organized to reflect:

- Standard features
- Features of the CPU08

#### 1.2.1 Standard Features

Features include:

- High-performance M68HC08 architecture optimized for C-compilers
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- 8-MHz internal bus frequency
- Clock generation module supporting 1-MHz to 8-MHz crystals
- MSCAN08 (implementing 2.0b protocol as defined in BOSCH specification dated September 1991)
- FLASH program memory security<sup>(1)</sup>
- On-chip programming firmware for use with host personal computer which does not require high voltage for entry
- In-system programming (ISP)

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

## General Description

- System protection features:
  - Optional computer operating properly (COP) reset
  - Low-voltage detection with optional reset and selectable trip points for 3.3-V and 5.0-V operation
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- Low-power design; fully static with stop and wait modes
- Standard low-power modes of operation:
  - Wait mode
  - Stop mode
- Master reset pin and power-on reset (POR)
- On-chip FLASH memory:
  - MC68HC908GZ16 — 16 Kbytes
  - MC68HC908GZ8 — 8 Kbytes
- 1 Kbyte of on-chip random-access memory (RAM)
- 406 bytes of FLASH programming routines read-only memory (ROM)
- Serial peripheral interface (SPI) module
- Enhanced serial communications interface (ESCI) module
- Fine adjust baud rate prescalers for precise control of baud rate
- Arbiter module:
  - Measurement of received bit timings for baud rate recovery without use of external timer
  - Bitwise arbitration for arbitrated UART communications
- LIN specific enhanced features:
  - Generation of LIN 1.2 break symbols without extra software steps on each message
  - Break detection filtering to prevent false interrupts
- Two 16-bit, 2-channel timer interface modules (TIM1 and TIM2) with selectable input capture, output compare, and pulse-width modulation (PWM) capability on each channel. One 2-channel timer and one 1-channel timer on the 32-pin package.
- Up to 8-channel, 10-bit successive approximation analog-to-digital converter (ADC) depending on package choice
- BREAK (BRK) module to allow single breakpoint setting during in-circuit debugging
- Internal pullups on  $\overline{IRQ}$  and  $\overline{RST}$  to reduce customer system cost
- Up to 37 general-purpose input/output (I/O) pins, including:
  - 28 shared-function I/O pins
  - Up to nine dedicated I/O pins, depending on package choice
- Selectable pullups on inputs only on ports A, C, and D. Selection is on an individual port bit basis. During output mode, pullups are disengaged.
- High current 10-mA sink/source capability on all port pins
- Higher current 20-mA sink/source capability on PTC0–PTC4
- Timebase module (TBM) with clock prescaler circuitry for eight user selectable periodic real-time interrupts with optional active clock source during stop mode for periodic wakeup from stop using an external crystal
- User selection of having the oscillator enabled or disabled during stop mode
- Up to 8-bit keyboard wakeup port depending on package choice
- 2 mA maximum current injection on all port pins to maintain input protection
- Available packages:
  - 32-pin quad flat pack (LQFP)
  - 48-pin quad flat pack (LQFP)

- Specific features of the MC68HC908GZ16 in 32-pin LQFP are:
  - Port A is only 4 bits: PTA0–PTA3; 4-pin keyboard interrupt (KBI) module
  - Port B is only 6 bits: PTB0–PTB5; 6-channel ADC module
  - Port C is only 2 bits: PTC0–PTC1; shared with MSCAN08 module
  - Port D is only 7 bits: PTD0–PTD6; shared with SPI, TIM1, and TIM2 modules
  - Port E is only 2 bits: PTE0–PTE1; shared with ESCI module
- Specific features of the MC68HC908GZ16 in 48-pin LQFP are:
  - Port A is 8 bits: PTA0–PTA7; 8-pin KBI module
  - Port B is 8 bits: PTB0–PTB7; 8-channel ADC module
  - Port C is only 7 bits: PTC0–PTC6; shared with MSCAN08 module
  - Port D is 8 bits: PTD0–PTD7; shared with SPI, TIM1, and TIM2 modules
  - Port E is only 6 bits: PTE0–PTE5; shared with ESCI module

### 1.2.2 Features of the CPU08

Features of the CPU08 include:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast  $8 \times 8$  multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Efficient C language support

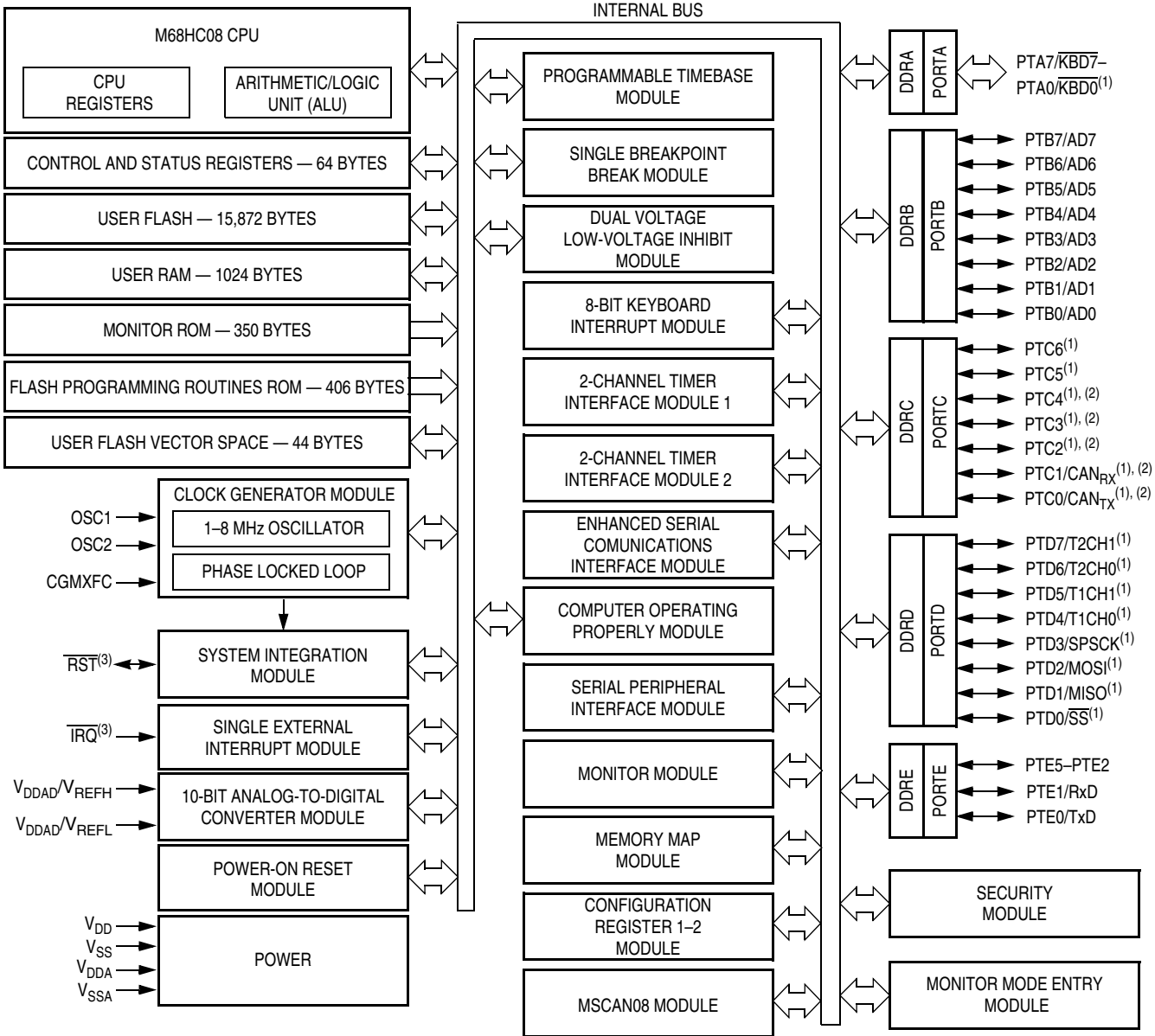
## 1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908GZ16.

## 1.4 Pin Assignments

Figure 1-2 and Figure 1-3 illustrate the pin assignments for the 32-pin LQFP and 48-pin LQFP respectively.

General Description



- 1. Ports are software configurable with pullup device if input port.
- 2. Higher current drive port pins
- 3. Pin contains integrated pullup device

Figure 1-1. MCU Block Diagram

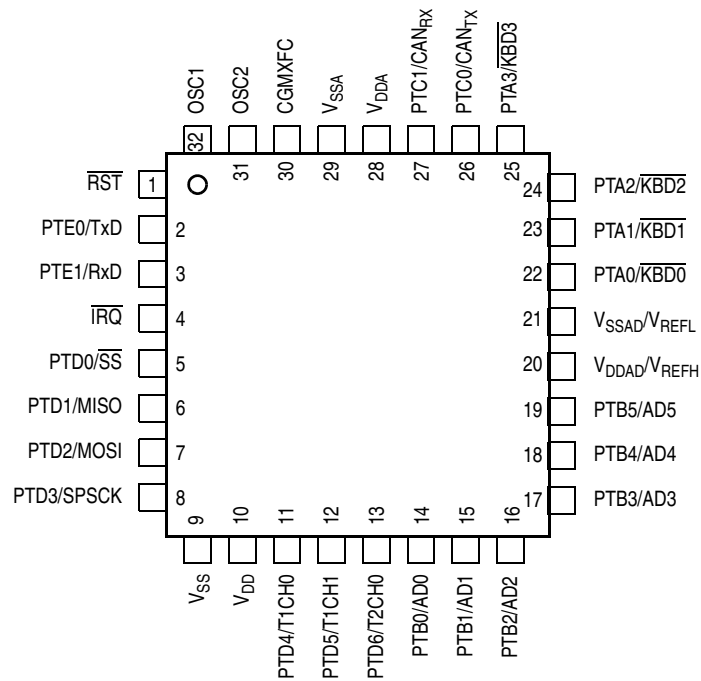


Figure 1-2. 32-Pin LQFP Pin Assignments

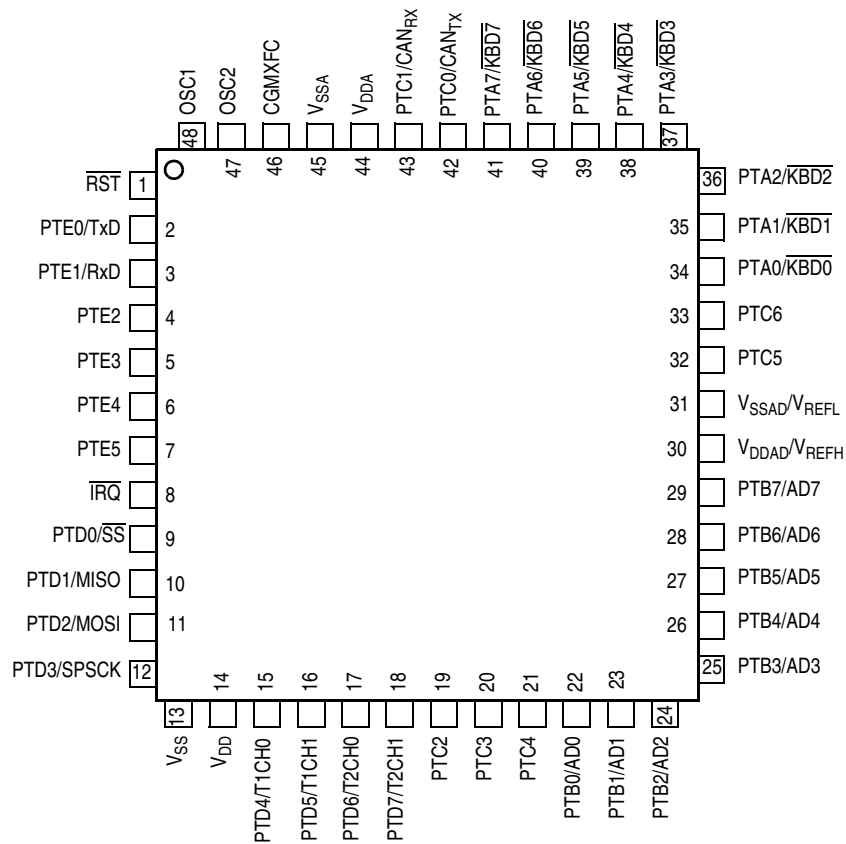


Figure 1-3. 48-Pin LQFP Pin Assignments



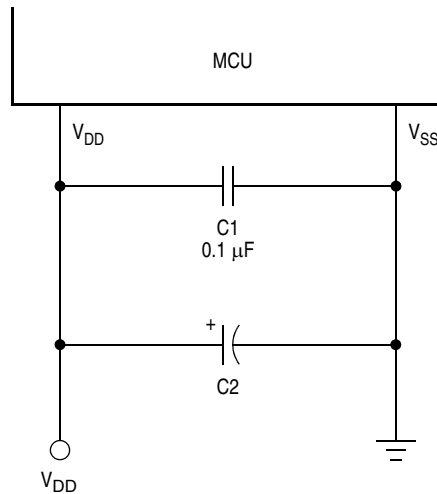
## 1.5 Pin Functions

Descriptions of the pin functions are provided here.

### 1.5.1 Power Supply Pins ( $V_{DD}$ and $V_{SS}$ )

$V_{DD}$  and  $V_{SS}$  are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU as [Figure 1-4](#) shows. Place the C1 bypass capacitor as close to the MCU as possible. Use a high-frequency-response ceramic capacitor for C1. C2 is an optional bulk current bypass capacitor for use in applications that require the port pins to source high current levels.



Note: Component values shown represent typical applications.

**Figure 1-4. Power Supply Bypassing**

### 1.5.2 Oscillator Pins (OSC1 and OSC2)

OSC1 and OSC2 are the connections for an external crystal, resonator, or clock circuit. See [Chapter 4 Clock Generator Module \(CGM\)](#).

### 1.5.3 External Reset Pin ( $\overline{RST}$ )

A logic 0 on the  $\overline{RST}$  pin forces the MCU to a known startup state.  $\overline{RST}$  is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted. This pin contains an internal pullup resistor. See [Chapter 16 System Integration Module \(SIM\)](#).

### 1.5.4 External Interrupt Pin ( $\overline{IRQ}$ )

$\overline{IRQ}$  is an asynchronous external interrupt pin. This pin contains an internal pullup resistor. See [Chapter 8 External Interrupt \(IRQ\)](#).

### 1.5.5 CGM Power Supply Pins ( $V_{DDA}$ and $V_{SSA}$ )

$V_{DDA}$  and  $V_{SSA}$  are the power supply pins for the analog portion of the clock generator module (CGM). Decoupling of these pins should be as per the digital supply. See [Chapter 4 Clock Generator Module \(CGM\)](#).

### 1.5.6 External Filter Capacitor Pin ( $V_{CGMXFC}$ )

$V_{CGMXFC}$  is an external filter capacitor connection for the CGM. See [Chapter 4 Clock Generator Module \(CGM\)](#).

### 1.5.7 ADC Power Supply/Reference Pins ( $V_{DDAD}/V_{REFH}$ and $V_{SSAD}/V_{REFL}$ )

$V_{DDAD}$  and  $V_{SSAD}$  are the power supply pins to the analog-to-digital converter (ADC).  $V_{REFH}$  and  $V_{REFL}$  are the reference voltage pins for the ADC.  $V_{REFH}$  is the high reference supply for the ADC, and by default the  $V_{DDAD}/V_{REFH}$  pin should be externally filtered and connected to the same voltage potential as  $V_{DD}$ .  $V_{REFL}$  is the low reference supply for the ADC, and by default the  $V_{SSAD}/V_{REFL}$  pin should be connected to the same voltage potential as  $V_{SS}$ . See [Chapter 3 Analog-to-Digital Converter \(ADC\)](#).

### 1.5.8 Port A Input/Output (I/O) Pins ( $PTA7/\overline{KBD7}$ – $PTA0/\overline{KBD0}$ )

$PTA7$ – $PTA0$  are general-purpose, bidirectional I/O port pins. Any or all of the port A pins can be programmed to serve as keyboard interrupt pins.  $PTA7$ – $PTA4$  are only available on the 48-pin LQFP package. See [Chapter 13 Input/Output \(I/O\) Ports](#) and [Chapter 9 Keyboard Interrupt Module \(KBI\)](#).

These port pins also have selectable pullups when configured for input mode. The pullups are disengaged when configured for output mode. The pullups are selectable on an individual port bit basis.

### 1.5.9 Port B I/O Pins ( $PTB7/AD7$ – $PTB0/AD0$ )

$PTB7$ – $PTB0$  are general-purpose, bidirectional I/O port pins that can also be used for analog-to-digital converter (ADC) inputs.  $PTB7$ – $PTB4$  are only available on the 48-pin LQFP package. See [Chapter 13 Input/Output \(I/O\) Ports](#) and [Chapter 3 Analog-to-Digital Converter \(ADC\)](#).

### 1.5.10 Port C I/O Pins ( $PTC6$ – $PTC0/CAN_{TX}$ )

$PTC6$  and  $PTC5$  are general-purpose, bidirectional I/O port pins.  $PTC4$ – $PTC0$  are general-purpose, bidirectional I/O port pins that contain higher current sink/source capability.  $PTC6$ – $PTC2$  are only available on the 48-pin LQFP package. See [Chapter 13 Input/Output \(I/O\) Ports](#) and [Chapter 12 MSCAN08 Controller \(MSCAN08\)](#).

$PTC1$  and  $PTC0$  can be programmed to be MSCAN08 pins.

These port pins also have selectable pullups when configured for input mode. The pullups are disengaged when configured for output mode. The pullups are selectable on an individual port bit basis.

### 1.5.11 Port D I/O Pins ( $PTD7/T2CH1$ – $PTD0/\overline{SS}$ )

$PTD7$ – $PTD0$  are special-function, bidirectional I/O port pins.  $PTD3$ – $PTD0$  can be programmed to be serial peripheral interface (SPI) pins, while  $PTD7$ – $PTD4$  can be individually programmed to be timer interface module (TIM1 and TIM2) pins.  $PTD7$  is only available on the 48-pin LQFP package. See [Chapter 19 Timer Interface Module \(TIM\)](#), [Chapter 17 Serial Peripheral Interface \(SPI\) Module](#), and [Chapter 13 Input/Output \(I/O\) Ports](#).