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MC68HC908GZ16
MC68HC908GZ8

Data Sheet

M68HC08
Microcontrollers

MC68HC908GZ16
Rev. 4.0
10/2006

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MC68HC908GZ16
MC68HC908GZ8
Data Sheet

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
February, 2003	N/A	Initial release	N/A
October, 2004	1.0	Reorganized to meet latest publication standards for M68HC08 Family documentation	N/A
		Added Table 1-1. Summary of Device Variations	19
		Figure 5-2. Configuration Register 1 (CONFIG1) — Changed bit 0 from SCIBDSRC to ESCIBDSRC.	80
		Chapter 15 Enhanced Serial Communications Interface (ESCI) Module — Updated with additional data	181–212
		Chapter 17 Serial Peripheral Interface (SPI) Module — Removed all references to DMAS	N/A
		Added DC injection current values to: 21.5 5-Vdc Electrical Characteristics 21.6 3.3-Vdc Electrical Characteristics	 289 291
		21.15 Memory Characteristics — Updated table entries	302
		Corrected ICG references to CGM throughout document.	N/A
		Chapter 22 Ordering Information and Mechanical Specifications — Corrected device ordering information	303
		Added the following: Appendix A MC68HC908GZ8	 311–314
June, 2005	2.0	205 — Corrected Functionality entries	205
		15.9.1 ESCI Arbiter Control Register — Corrected bit ACLK bit description	209
		15.9.3 Bit Time Measurement — Corrected definition for ACLK bit	210
March, 2006	3.0	10.5 Clock Generator Module (CGM) — Updated description to remove erroneous information.	110
October, 2006	4.0	1.6 Unused Pin Termination — Added new section.	26
		12.2 Features — Corrected timer link connection from TIM2 channel 0 to TIM1 channel 0.	121
		12.9 Timer Link — Corrected timer link connection from TIM2 channel 0 to TIM1 channel 0.	133
		13.1 Introduction — Replaced note with unused pin termination text.	155
		21.5 5-Vdc Electrical Characteristics and 21.6 3.3-Vdc Electrical Characteristics — Updated DC injection current specification.	289 291

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Appendix A
MC68HC908GZ8

Chapter 1
General Description

1.1 Introduction

The MC68HC908GZ16 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

Table 1-1. Summary of Device Variations

Device	Memory Size
MC68HC908QZ16	16 Kbytes user FLASH
MC68HC908GZ8	8 Kbytes user FLASH

The information contained in this document pertains to both the MC68HC908GZ16 and the MC68HC908GZ8 with the exceptions shown Appendix A MC68HC908GZ8

1.2 Features

For convenience, features have been organized to reflect:

- Standard features
- Features of the CPU08

1.2.1 Standard Features

Features include:

- High-performance M68HC08 architecture optimized for C-compilers
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- 8-MHz internal bus frequency
- Clock generation module supporting 1-MHz to 8-MHz crystals
- MSCAN08 (implementing 2.0b protocol as defined in BOSCH specification dated September 1991)
- FLASH program memory security[1]
- On-chip programming firmware for use with host personal computer which does not require high voltage for entry
- In-system programming (ISP)

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

- System protection features:
  - Optional computer operating properly (COP) reset
  - Low-voltage detection with optional reset and selectable trip points for 3.3-V and 5.0-V operation
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- Low-power design; fully static with stop and wait modes
- Standard low-power modes of operation:
  - Wait mode
  - Stop mode
- Master reset pin and power-on reset (POR)
- On-chip FLASH memory:
  - MC68HC908GZ16 — 16 Kbytes
  - MC68HC908GZ8 — 8 Kbytes
- 1 Kbyte of on-chip random-access memory (RAM)
- 406 bytes of FLASH programming routines read-only memory (ROM)
- Serial peripheral interface (SPI) module
- Enhanced serial communications interface (ESCI) module
- Fine adjust baud rate prescalers for precise control of baud rate
- Arbiter module:
  - Measurement of received bit timings for baud rate recovery without use of external timer
  - Bitwise arbitration for arbitrated UART communications
- LIN specific enhanced features:
  - Generation of LIN 1.2 break symbols without extra software steps on each message
  - Break detection filtering to prevent false interrupts
- Two 16-bit, 2-channel timer interface modules (TIM1 and TIM2) with selectable input capture, output compare, and pulse-width modulation (PWM) capability on each channel. One 2-channel timer and one 1-channel timer on the 32-pin package.
- Up to 8-channel, 10-bit successive approximation analog-to-digital converter (ADC) depending on package choice
- BREAK (BRK) module to allow single breakpoint setting during in-circuit debugging
- Internal pullups on $\overline{\text{IRQ}}$ and $\overline{\text{RST}}$ to reduce customer system cost
- Up to 37 general-purpose input/output (I/O) pins, including:
  - 28 shared-function I/O pins
  - Up to nine dedicated I/O pins, depending on package choice
- Selectable pullups on inputs only on ports A, C, and D. Selection is on an individual port bit basis. During output mode, pullups are disengaged.
- High current 10-mA sink/source capability on all port pins
- Higher current 20-mA sink/source capability on PTC0–PTC4
- Timebase module (TBM) with clock prescaler circuitry for eight user selectable periodic real-time interrupts with optional active clock source during stop mode for periodic wakeup from stop using an external crystal
- User selection of having the oscillator enabled or disabled during stop mode
- Up to 8-bit keyboard wakeup port depending on package choice
- 2 mA maximum current injection on all port pins to maintain input protection
- Available packages:
  - 32-pin quad flat pack (LQFP)
  - 48-pin quad flat pack (LQFP)

- Specific features of the MC68HC908GZ16 in 32-pin LQFP are:
  - Port A is only 4 bits: PTA0–PTA3; 4-pin keyboard interrupt (KBI) module
  - Port B is only 6 bits: PTB0–PTB5; 6-channel ADC module
  - Port C is only 2 bits: PTC0–PTC1; shared with MSCAN08 module
  - Port D is only 7 bits: PTD0–PTD6; shared with SPI, TIM1, and TIM2 modules
  - Port E is only 2 bits: PTE0–PTE1; shared with ESCI module
- Specific features of the MC68HC908GZ16 in 48-pin LQFP are:
  - Port A is 8 bits: PTA0–PTA7; 8-pin KBI module
  - Port B is 8 bits: PTB0–PTB7; 8-channel ADC module
  - Port C is only 7 bits: PTC0–PTC6; shared with MSCAN08 module
  - Port D is 8 bits: PTD0–PTD7; shared with SPI, TIM1, and TIM2 modules
  - Port E is only 6 bits: PTE0–PTE5; shared with ESCI module

1.2.2 Features of the CPU08

Features of the CPU08 include:

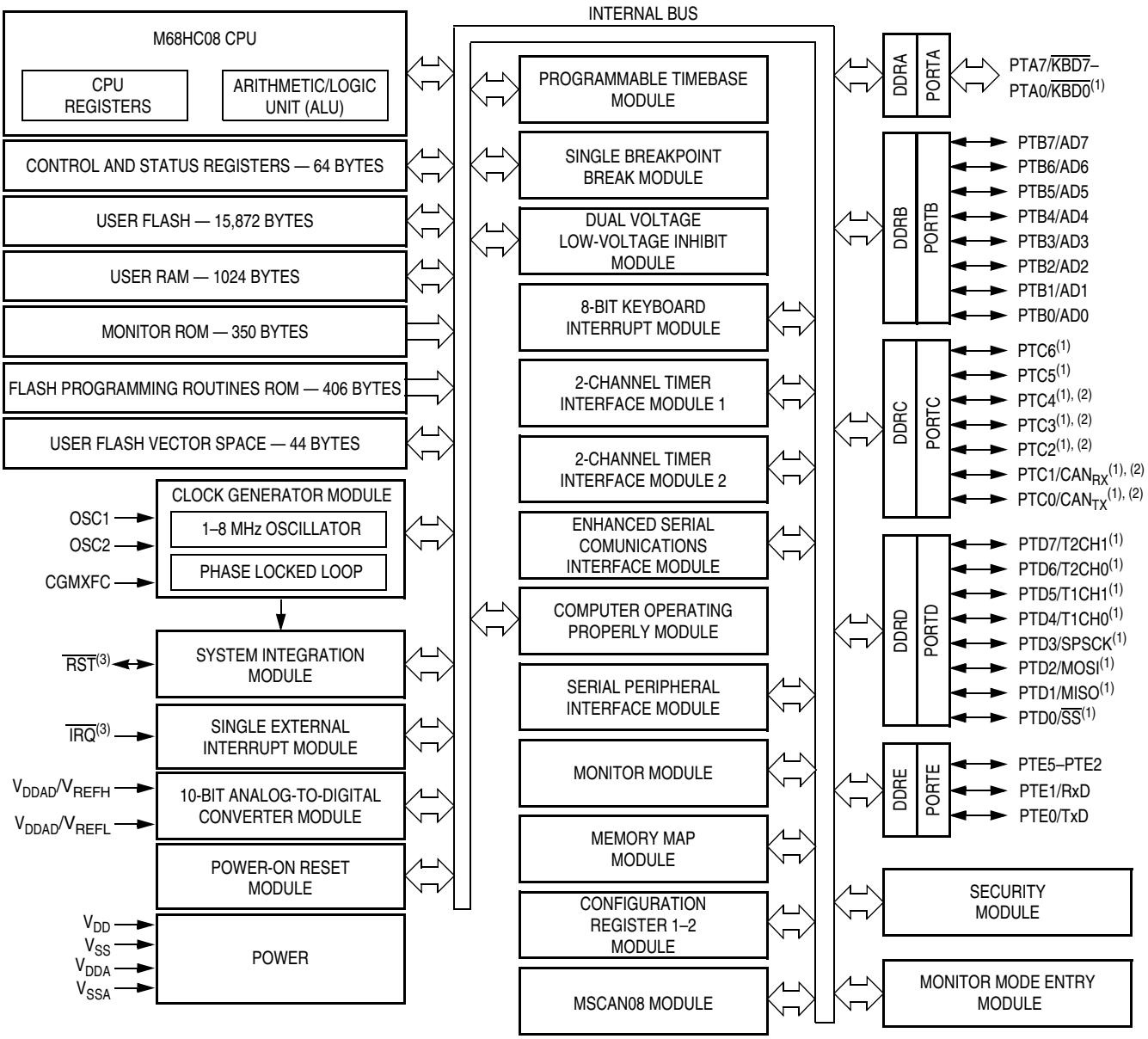
- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8 × 8 multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Efficient C language support

1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908GZ16.

1.4 Pin Assignments

Figure 1-2 and Figure 1-3 illustrate the pin assignments for the 32-pin LQFP and 48-pin LQFP respectively.



1. Ports are software configurable with pullup device if input port.
2. Higher current drive port pins
3. Pin contains integrated pullup device

Figure 1-1. MCU Block Diagram

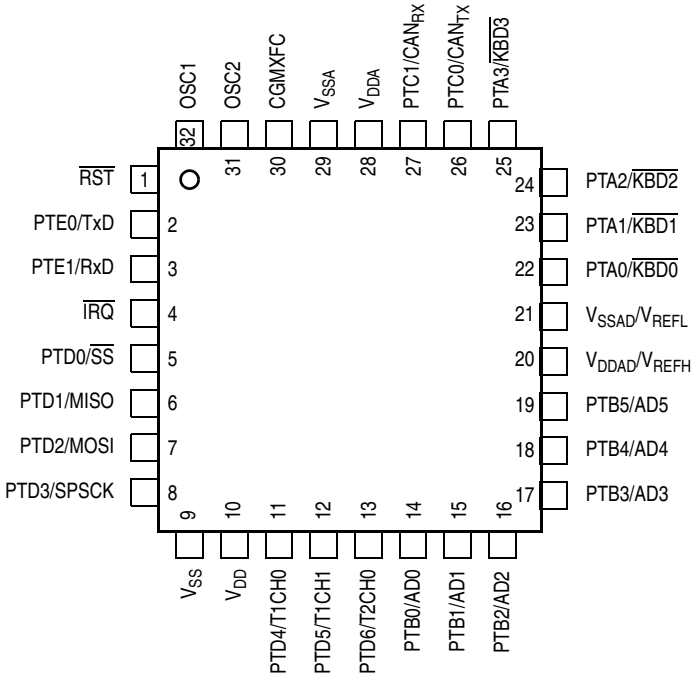


Figure 1-2. 32-Pin LQFP Pin Assignments

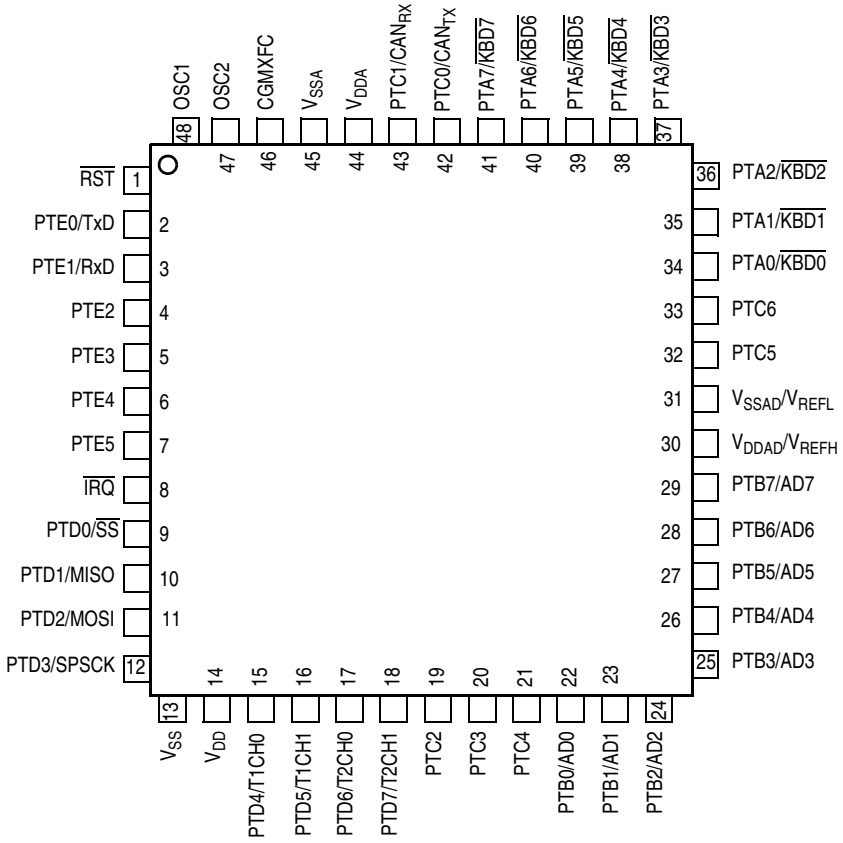


Figure 1-3. 48-Pin LQFP Pin Assignments

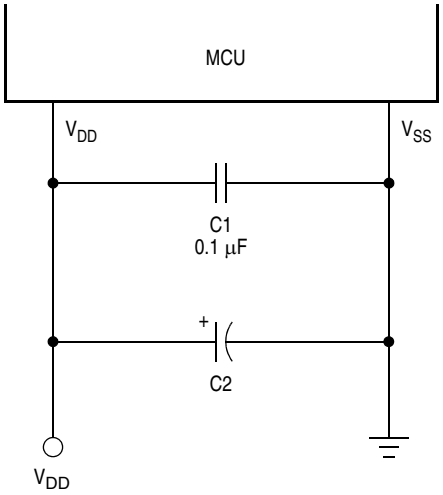
1.5 Pin Functions

Descriptions of the pin functions are provided here.

1.5.1 Power Supply Pins (V_{DD} and V_{SS})

V_{DD} and V_{SS} are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU as Figure 1-4 shows. Place the C1 bypass capacitor as close to the MCU as possible. Use a high-frequency-response ceramic capacitor for C1. C2 is an optional bulk current bypass capacitor for use in applications that require the port pins to source high current levels.



Note: Component values shown represent typical applications.

Figure 1-4. Power Supply Bypassing

1.5.2 Oscillator Pins (OSC1 and OSC2)

OSC1 and OSC2 are the connections for an external crystal, resonator, or clock circuit. See Chapter 4 Clock Generator Module (CGM).

1.5.3 External Reset Pin ($\overline{RST}$)

A logic 0 on the $\overline{RST}$ pin forces the MCU to a known startup state. $\overline{RST}$ is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted. This pin contains an internal pullup resistor. See Chapter 16 System Integration Module (SIM).

1.5.4 External Interrupt Pin ($\overline{IRQ}$)

$\overline{IRQ}$ is an asynchronous external interrupt pin. This pin contains an internal pullup resistor. See Chapter 8 External Interrupt (IRQ).

1.5.5 CGM Power Supply Pins (V_{DDA} and V_{SSA})

V_{DDA} and V_{SSA} are the power supply pins for the analog portion of the clock generator module (CGM). Decoupling of these pins should be as per the digital supply. See Chapter 4 Clock Generator Module (CGM).

1.5.6 External Filter Capacitor Pin (V_{CGMXFC})

CGMXFC is an external filter capacitor connection for the CGM. See Chapter 4 Clock Generator Module (CGM).

1.5.7 ADC Power Supply/Reference Pins (V_{DDAD}/V_{REFH} and V_{SSAD}/V_{REFL})

V_{DDAD} and V_{SSAD} are the power supply pins to the analog-to-digital converter (ADC). V_{REFH} and V_{REFL} are the reference voltage pins for the ADC. V_{REFH} is the high reference supply for the ADC, and by default the V_{DDAD}/V_{REFH} pin should be externally filtered and connected to the same voltage potential as V_{DD}. V_{REFL} is the low reference supply for the ADC, and by default the V_{SSAD}/V_{REFL} pin should be connected to the same voltage potential as V_{SS}. See Chapter 3 Analog-to-Digital Converter (ADC).

1.5.8 Port A Input/Output (I/O) Pins (PTA7/$\overline{\text{KBD7}}$–PTA0/$\overline{\text{KBD0}}$)

PTA7–PTA0 are general-purpose, bidirectional I/O port pins. Any or all of the port A pins can be programmed to serve as keyboard interrupt pins. PTA7–PTA4 are only available on the 48-pin LQFP package. See Chapter 13 Input/Output (I/O) Ports and Chapter 9 Keyboard Interrupt Module (KBI).

These port pins also have selectable pullups when configured for input mode. The pullups are disengaged when configured for output mode. The pullups are selectable on an individual port bit basis.

1.5.9 Port B I/O Pins (PTB7/AD7–PTB0/AD0)

PTB7–PTB0 are general-purpose, bidirectional I/O port pins that can also be used for analog-to-digital converter (ADC) inputs. PTB7–PTB4 are only available on the 48-pin LQFP package. See Chapter 13 Input/Output (I/O) Ports and Chapter 3 Analog-to-Digital Converter (ADC).

1.5.10 Port C I/O Pins (PTC6–PTC0/CAN_{TX})

PTC6 and PTC5 are general-purpose, bidirectional I/O port pins. PTC4–PTC0 are general-purpose, bidirectional I/O port pins that contain higher current sink/source capability. PTC6–PTC2 are only available on the 48-pin LQFP package. See Chapter 13 Input/Output (I/O) Ports and Chapter 12 MSCAN08 Controller (MSCAN08).

PTC1 and PTC0 can be programmed to be MSCAN08 pins.

These port pins also have selectable pullups when configured for input mode. The pullups are disengaged when configured for output mode. The pullups are selectable on an individual port bit basis.

1.5.11 Port D I/O Pins (PTD7/T2CH1–PTD0/$\overline{\text{SS}}$)

PTD7–PTD0 are special-function, bidirectional I/O port pins. PTD3–PTD0 can be programmed to be serial peripheral interface (SPI) pins, while PTD7–PTD4 can be individually programmed to be timer interface module (TIM1 and TIM2) pins. PTD7 is only available on the 48-pin LQFP package. See Chapter 19 Timer Interface Module (TIM), Chapter 17 Serial Peripheral Interface (SPI) Module, and Chapter 13 Input/Output (I/O) Ports.