Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MC68HC705C9A

Advance Information Data Sheet

M68HC05
Microcontrollers

MC68HC705C9A
Rev. 4.1
9/2005

freescale.com

freescale™
semiconductor

MC68HC705C9A

Advance Information Data Sheet

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://www.freescale.com/

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
October, 2001	3.0	Format update to current publication standards	N/A
		Figure 12-10. SPI Slave Timing Diagram — Corrected labels for MISO and MOSI and subtitle for part b.	145
February, 2002	4.0	Figure 8-3. Timer Status Register (TSR) — Corrected address designator from $0012 to $0013.	78
September, 2005	4.1	Updated to meet Freescale identity guidelines.	Throughout

List of Chapters

Table of Contents

Chapter 1
General Description

Chapter 2
Memory

Chapter 3
Central Processor Unit (CPU)

Chapter 4
Interrupts

Chapter 5
Resets

Chapter 6
Low-Power Modes

Chapter 7
Input/Output (I/O) Ports

Chapter 8
Capture/Compare Timer

Chapter 9
Serial Communications Interface (SCI)

Chapter 10
Serial Peripheral Interface (SPI)

Chapter 11
Instruction Set

Chapter 12
Electrical Specifications

Chapter 13
Mechanical Specifications

Chapter 14
Ordering Information

Appendix A
EPROM Programming

Appendix B
M68HC05Cx Family Feature Comparisons

Chapter 1
General Description

1.1 Introduction

The MC68HC705C9A HCMOS microcomputer is a member of the M68HC05 Family. The MC68HC705C9A is the EPROM version of the MC68HC05C9A and also can be configured as the EPROM version of the MC68HC05C12A. The MC68HC705C9A memory map consists of 12,092 bytes of user EPROM and 176 bytes of RAM when it is configured as an MC68HC05C12A and 15,932 bytes of user EPROM and 352 bytes of RAM when configured as an MC68HC05C9A. The MC68HC705C9A includes a serial communications interface, a serial peripheral interface, and a 16-bit capture/compare timer.

1.2 Features

Features include:

- Programmable mask option register (MOR) for C9A/C12A configuration
- Programmable MOR for port B pullups and interrupts
- Popular M68HC05 central processor unit (CPU)
- 15,932 bytes of EPROM (12,092 bytes for C12A configuration)
- 352 bytes of RAM (176 for C12A configuration)
- Memory mapped input/output (I/O)
- 31 bidirectional I/O lines (24 I/O + 6 input only for C12A configuration) with high current sink and source on PC7
- Asynchronous serial communications interface (SCI)
- Synchronous serial peripheral interface (SPI)
- 16-bit capture/compare timer
- Computer operating properly (COP) watchdog timer and clock monitor
- Power-saving wait and stop modes
- On-chip crystal oscillator connections
- Single 3.0 volts to 5.5 volts power supply requirement
- EPROM contents security[1] feature

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the EPROM difficult for unauthorized users.

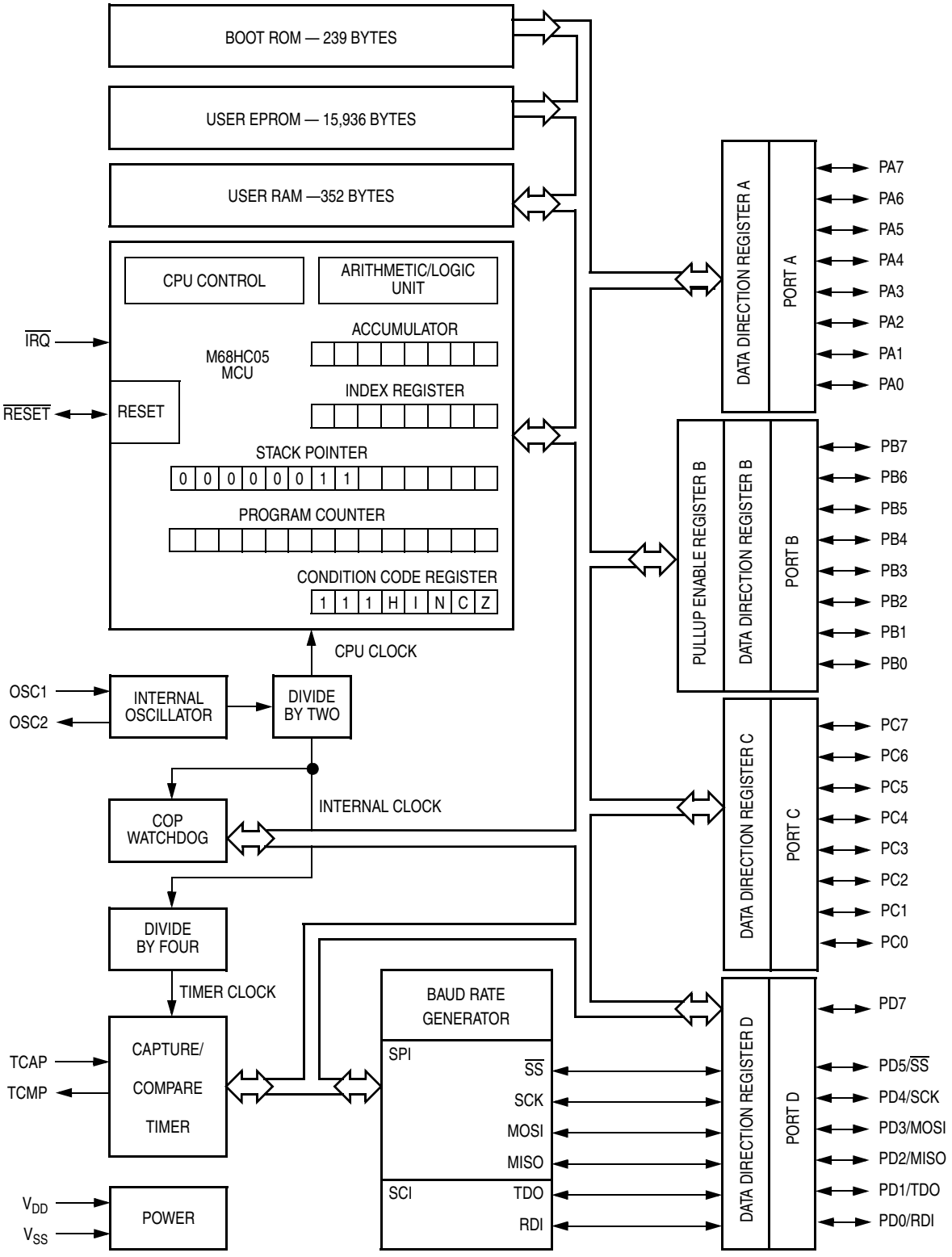

Figure 1-1. Block Diagram

1.3 Configuration Options

The options and functions of the MC68HC705C9A can be configured to emulate either the MC68HC05C9A or the MC68HC05C12A.

The ROM device MC68HC05C9A has eight ROM mask options to select external interrupt/internal pullup capability on each of the eight port B bits. Other optional features are controlled by software addressable registers during operation of the microcontroller. These features are IRQ sensitivity and memory map configuration.

On the ROM device MC68HC05C12A, all optional features are controlled by ROM mask options. These features are the eight port B interrupt/pullup options, IRQ sensitivity, STOP instruction disable, and COP enable.

On the MC68HC705C9A the ROM mask options of the MC68HC05C9A and the MC68HC05C12A are controlled by mask option registers (MORs). The MORs are EPROM registers which must be programmed appropriately prior to operation of the microcontroller. The software options of the MC68HC05C9A are implemented by identical software registers in the MC68HC705C9A.

When configured as an MC68HC05C9A:

- The entire 16K memory map of the C9A is enabled, including dual-mapped RAM and EPROM at locations $0020–$004F and $0100–$017F.
- C12A options in the C12MOR ($3FF1) are disabled.
- The C9A option register ($3FDF) is enabled, allowing software control over the IRQ sensitivity and the memory map configuration.
- The C9A COP reset register ($001D) and the C9A COP control register ($001E) are enabled, allowing software control over the C9A COP and clock monitor.
- The C12 COP clear register ($3FF0) is disabled.
- The port D data direction register ($0007) is enabled, allowing output capability on the seven port D pins.
- SPI output signals (MOSI, MISO, and SCK) require the corresponding bits in the port D data direction register to be set for output.
- The port D wire-OR mode control bit (bit 5 of SPCR $000A) is enabled, allowing open-drain configuration of port D.
- The $\overline{\text{RESET}}$ pin becomes bidirectional; this pin is driven low by a C9A COP or clock monitor timeout or during power-on reset.

When configured as an MC68HC05C12A:

- Memory locations $0100–$0FFF are disabled, creating a memory map identical to the MC68HC05C12A.
- C12A options in the C12MOR ($3FF1) are enabled; these bits control IRQ sensitivity, STOP instruction disable and C12 COP enable.
- The C9A option register ($3FDF) is disabled, preventing software control over the IRQ sensitivity and the memory map configuration.
- The C9A COP reset register ($001D) and the C9A COP control register ($001E) are disabled, preventing software control over the C9A COP and clock monitor.
- The C12 COP clear register ($3FF0) is enabled; this write-only register is used to clear the C12 COP.

- The port D data direction register ($0007) is disabled and the seven port D pins become input only.
- SPI output signals (MOSI, MISO, and SCK) do not require the data direction register control for output capability.
- The port D wire-OR mode control bit (bit 5 of SPCR $000A) is disabled, preventing open-drain configuration of port D.
- The $\overline{\text{RESET}}$ pin becomes input only.

1.4 Mask Options

The following two mask option registers are used to select features controlled by mask changes on the MC68HC05C9A and the MC68HC05C12A:

- Port B mask option register (PBMOR)
- C12 mask option register (C12MOR)

The mask option registers are EPROM locations which must be programmed prior to operation of the microcontroller.

1.4.1 Port B Mask Option Register (PBMOR)

The PBMOR register, shown in Figure 1-2, contains eight programmable bits which determine whether each port B bit (when in input mode) has the pullup and interrupt enabled. The port B interrupts share the vector and edge/edge-level sensitivity with the $\overline{\text{IRQ}}$ pin. For more details, (see 4.3 External Interrupt (IRQ or Port B)).

$3FF0	Bit 7	6	5	4	3	2	1	Bit 0
	PBPU7	PBPU6	PBPU5	PBPU4	PBPU3	PBPU2	PBPU1	PBPU0

Figure 1-2. Port B Mask Option Register

PBPU7–PBPU0 — Port B Pullup/Interrupt Enable Bits
1 = Pullup and CPU interrupt enabled
0 = Pullup and CPU interrupt disabled

NOTE

The current capability of the port B pullup devices is equivalent to the MC68HC05C9A, which is less than the MC68HC05C12A.

1.4.2 C12 Mask Option Register (C12MOR)

The C12MOR register, shown in Figure 1-3, controls the following options:

- Select between MC68HC05C9A/C12A configuration
- Enable/disable stop mode (C12A mode only)
- Enable/disable COP (C12A mode only)
- Edge-triggered only or edge- and level-triggered external interrupt pin (IRQ pin) (C12A mode only).

$3FF1	Bit 7	6	5	4	3	2	1	Bit 0
Read:	SEC				C12COPE	STOPDIS	C12IRQ	C12A
Write:								

= Unimplemented

Figure 1-3. Mask Option Register 2

C12A — C12A/C9A Mode Select Bit

This read/write bit selects between C12A configuration and C9A configuration.

1 = Configured to emulate MC68HC05C12A
0 = Configured to emulate MC68HC05C9A

C12IRQ — C12A Interrupt Request Bit

This read/write bit selects between an edge-triggered only or edge- and level-triggered external interrupt pin. If configured in C9A mode, this bit has no effect and will be forced to 0 regardless of the programmed state.

1 = Edge and level interrupt option selected
0 = Edge-only interrupt option selected

NOTE

Any Port B pin configured for interrupt capability will follow the same edge or edge/level trigger as the $\overline{IRQ}$ pin.

STOPDIS — STOP Instruction Disable Bit

This read-only bit allows emulation of the “STOP disable” mask option on the MC68HC05C12A. (See 5.9 COP During Stop Mode.) If configured in MC68HC05C9A mode, this bit has no effect and will be forced to 0 regardless of the programmed state.

1 = If the MCU enters stop mode, the clock monitor is enabled to force a system reset
0 = STOP instruction executed as normal

C12COPE — C12A COP Enable Bit

This read-only bit enables the COP function when configured in MC68HC05C12A mode. If configured in MC68HC05C9A mode, this bit has no effect and will be forced to 0 regardless of the programmed state.

1 = When in C12A mode, this enables the C12ACOP watchdog timer.
0 = When in C12A mode, this disables the C12ACOP watchdog timer.

SEC — Security Enable Bit

This read-only bit enables the EPROM security feature. Once programmed, this bit helps to prevent external access to the programmed EPROM data. The EPROM data cannot be verified or modified.

1 = Security enabled
0 = Security disabled

NOTE

During power-on reset, the device always will be configured as MC68HC05C9A regardless of the state of the C12A bit.

1.5 Software-Programmable Options (MC68HC05C9A Mode Only)

The C9A option register (OR), shown in Figure 1-4, is enabled only if configured in C9A mode. This register contains the programmable bits for the following options:

- Map two different areas of memory between RAM and EPROM, one of 48 bytes and one of 128 bytes
- Edge-triggered only or edge- and level-triggered external interrupt ($\overline{\text{IRQ}}$ pin and any port B pin configured for interrupt)

This register must be written to by user software during operation of the microcontroller.

$3FDF	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	RAM0	RAM1					IRQ	
Reset:	0	0	0	0	0	0	1	0

= Unimplemented

Figure 1-4. C9A Option Register

RAM0 — Random Access Memory Control Bit 0

This read/write bit selects between RAM or EPROM in location $0020 to $004F. This bit can be read or written at any time.

1 = RAM selected
0 = EPROM selected

RAM1— Random Access Memory Control Bit 1

This read/write bit selects between RAM or EPROM in location $0100 to $017F. This bit can be read or written at any time.

1 = RAM selected
0 = EPROM selected

IRQ — Interrupt Request Bit

This bit selects between an edge-triggered only or edge- and level- triggered external interrupt pin. This bit is set by reset, but can be cleared by software. This bit can be written only once.

1 = Edge and level interrupt option selected
0 = Edge-only interrupt option selected

1.6 Functional Pin Descriptions

Figure 1-5, Figure 1-6, Figure 1-7, and Figure 1-8 show the pin assignments for the available packages. A functional description of the pins follows.

NOTE

A line over a signal name indicates an active low signal. For example, RESET is active high and $\overline{RESET}$ is active low.

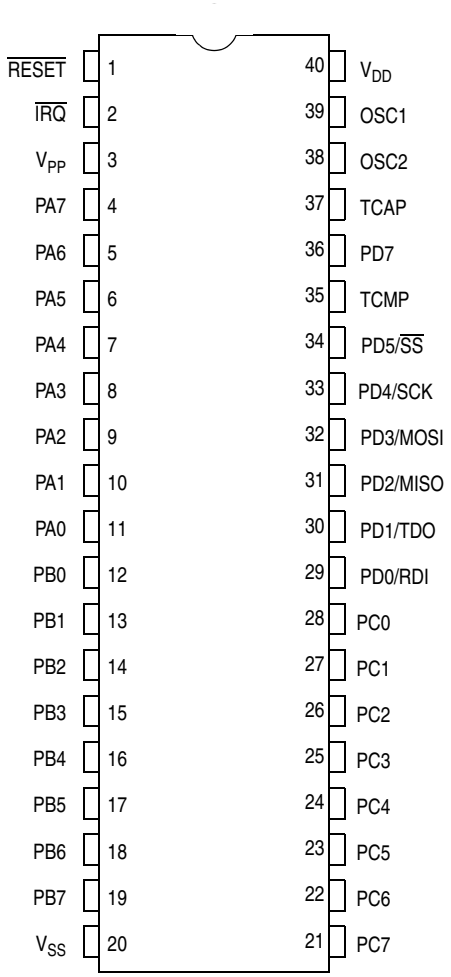

Figure 1-5. 40-Pin PDIP Pin Assignments

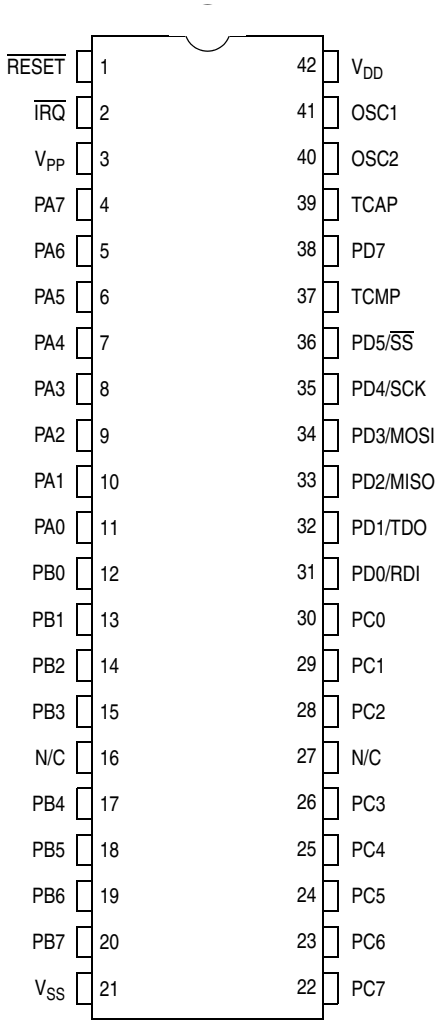

Figure 1-6. 42-Pin SDIP Pin Assignments

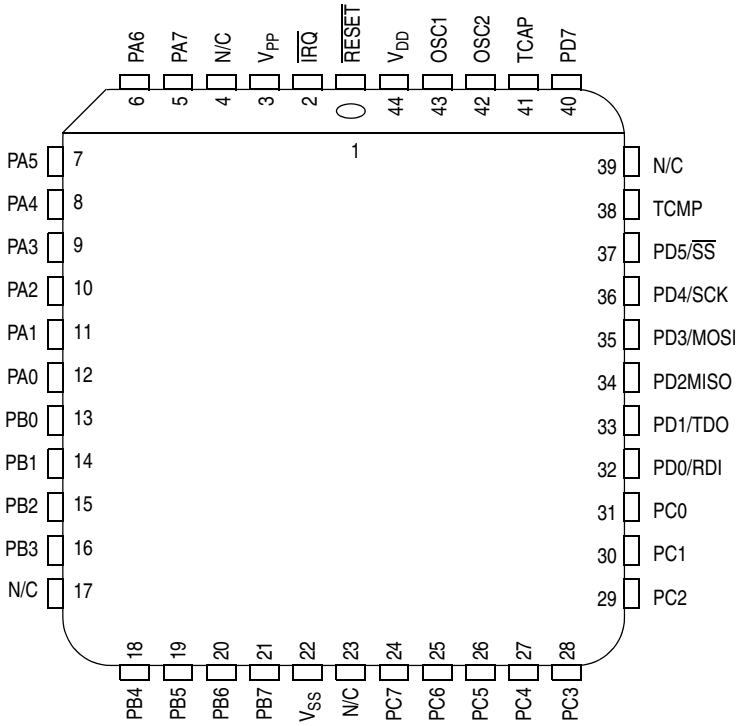

Figure 1-7. 44-Lead PLCC Pin Assignments

NOTE

The above 44-pin PLCC pin assignment diagram is for compatibility with MC68HC05C9A. To allow compatibility with the 44-pin PLCC MC68HC05C12A, pin17 and pin18 must be tied together and pin 39 and pin 40 also must be tied together.

To allow compatibility with MC68HC705C8A, pin 3 and pin 4 also should be tied together.

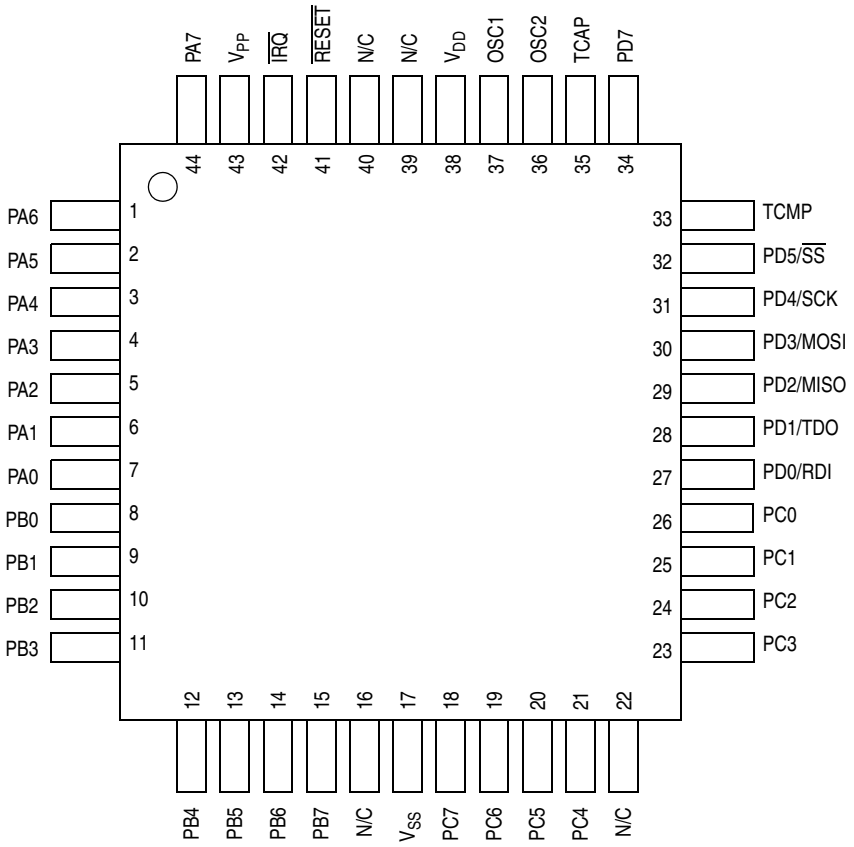

Figure 1-8. 44-Pin QFP Pin Assignments

1.6.1 V_{DD} and V_{SS}

Power is supplied to the MCU using these two pins. V_{DD} is the positive supply and V_{SS} is ground.

1.6.2 V_{PP}

This pin provides the programming voltage to the EPROM array. For normal operation, V_{PP} should be tied to V_{DD}.

1.6.3 $\overline{IRQ}$

This interrupt pin has an option that provides two different choices of interrupt triggering sensitivity. The $\overline{IRQ}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. Refer to Chapter 4 Interrupts for more detail.

1.6.4 OSC1 andOSC2

These pins provide control input for an on-chip clock oscillator circuit. A crystal connected to these pins provides a system clock. The internal frequency is one-half the crystal frequency.

1.6.5 $\overline{\text{RESET}}$

As an input pin, this active low $\overline{\text{RESET}}$ pin is used to reset the MCU to a known startup state by pulling $\overline{\text{RESET}}$ low. As an output pin, when in MC68HC05C9A mode only, the $\overline{\text{RESET}}$ pin indicates that an internal MCU reset has occurred. The $\overline{\text{RESET}}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. Refer to
Chapter 5 Resets for more detail.

1.6.6 TCAP

This pin controls the input capture feature for the on-chip programmable timer. The TCAP pin contains an internal Schmitt trigger as part of its input to improve noise immunity. Refer to Chapter 8 Capture/Compare Timer for more detail.

1.6.7 TCMP

The TCMP pin provides an output for the output compare feature of the on-chip programmable timer. Refer to Chapter 8 Capture/Compare Timer for more detail.

1.6.8 PA0–PA7

These eight I/O lines comprise port A. The state of each pin is software programmable and all port A pins are configured as inputs during reset. Refer to Chapter 7 Input/Output (I/O) Ports for more detail.

1.6.9 PB0–PB7

These eight I/O lines comprise port B. The state of each pin is software programmable and all port B pins are configured as inputs during reset. Port B has mask option register enabled pullup devices and interrupt capability selectable for any pin. Refer to Chapter 7 Input/Output (I/O) Ports for more detail.

1.6.10 PC0–PC7

These eight I/O lines comprise port C. The state of each pin is software programmable and all port C pins are configured as inputs during reset. PC7 has high current sink and source capability. Refer to Chapter 7 Input/Output (I/O) Ports for more detail.

1.6.11 PD0–PD5 and PD7

These seven I/O lines comprise port D. When configured as a C9A the state of each pin is software programmable and all port D pins are configured as inputs during reset. When configured as a C12A, the port D pins are input only. Refer to Chapter 7 Input/Output (I/O) Ports for more detail.

Chapter 2
Memory

2.1 Introduction

The MCU has a 16-Kbyte memory map when configured as either an MC68HC05C9A or an MC68HC05C12A. The memory map consists of registers (I/O, control, and status), user RAM, user EPROM, bootloader ROM, and reset and interrupt vectors as shown in Figure 2-1 and Figure 2-2.

When configured as an MC68HC05C9A, two control bits in the option register ($3FDF) allow the user to switch between RAM and EPROM at any time in two special areas of the memory map, $0020-$004F (48 bytes) and $0100-$017F (128 bytes). When configured as an MC68HC05C12A, the section of the memory map from $0020 to $004F is fixed as EPROM and the section from $0100 to $0FFF becomes unused.

2.2 RAM

The main user RAM consists of 176 bytes at $0050–$00FF. This RAM area is always present in the memory map and includes a 64-byte stack area. The stack pointer can access 64 bytes of RAM in the range $00FF down to $00C0.

NOTE

Using the stack area for data storage or temporary work locations requires care to prevent it from being overwritten due to stacking from an interrupt or subroutine call.

In MC68HC05C9A configuration, two additional RAM areas are available at $0020–$004F (48 bytes) and $0100–$017F (128 bytes) (see Figure 2-1 and Figure 2-2.) These may be accessed at any time by setting the RAM0 and RAM1 bits, respectively, in the C9A option register. Refer to 1.5 Software-Programmable Options (MC68HC05C9A Mode Only) for additional information.

2.3 EPROM

When configured as a C12A the main user EPROM consists of 48 bytes of page zero EPROM from $0020 to $004F, 12,032 bytes of EPROM from $1000 to $3EFF, and 14 bytes of user vectors from $3FF4 to $3FFF. When configured as a C9A, an additional 3,840 bytes of user EPROM from $0100 to $0FFF are enabled.

Locations $3FF0 and $3FF1 are the mask option registers (MOR) (see 1.4 Mask Options).

For detailed information on programming the EPROM see Appendix A EPROM Programming.