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MC68HC05SR3
MC68HC705SR3

Technical Data

M68HC05
Microcontrollers

MC68HC05SR3D/H
Rev. 2.1
08/2005

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A MC68HC705SR3

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High-density Complementary Metal Oxide Semiconductor (HCMOS) Microcontroller Units

Conventions

Register and bit mnemonics are defined in the paragraphs describing them.

An overbar is used to designate an active-low signal, eg: $\overline{\text{RESET}}$.

Unless otherwise stated, blank cells in a register diagram indicate that the bit is either unused or reserved; shaded cells indicate that the bit is not described in the following paragraphs; ‘u’ is used to indicate an undefined state (on reset).

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1
GENERAL DESCRIPTION

The MC68HC05SR3 HCMOS microcontroller is a member of the M68HC05 family of low-cost single-chip microcontrollers. This 8-bit microcontroller unit (MCU) contains on-chip oscillator, CPU, RAM, ROM, I/O, Timer, and Analog-to-Digital Converter. The MC68HC05SR3 is pin compatible with the MC6805R3 and is provided as a low power upgrade path for MC6805R3 applications. The low power advantage of CMOS is combined with the addition of I/O and port modifications which help eliminate external components in cost sensitive applications.

The MC68HC705SR3 is an EPROM version of the MC68HC05SR3; it is available in windowed and OTP packages. All references to the MC68HC05SR3 apply equally to the MC68HC705SR3, unless otherwise stated. *References specific to the MC68HC705SR3 are italicized in the text and also, for quick reference, they are summarized in Appendix A.*

1.1 Features

- Fully static chip design featuring the industry standard 8-bit M68HC05 core
- Pin compatible with the MC6805R3
- Power saving STOP, WAIT, and SLOW modes
- 3840 bytes of user ROM with security feature in MC68HC05SR3
  3840 bytes of EPROM with security bit in MC68HC705SR3
- 192 bytes of RAM (64 bytes for stack)
- 32 bidirectional I/O lines
- Keyboard interrupts
- 8-bit count-down timer with programmable 7-bit prescaler
- On-chip crystal oscillator, with built-in capacitor for RC option
- Second software programmable external interrupt line ($\overline{\text{IRQ2}}$)
- Direct LED drive capability on all ports
- Programmable 20KΩ pull-up resistors integrated into I/O ports

- Internal 100KΩ pull-up resistors on $\overline{\text{IRQ}}$ and $\overline{\text{RESET}}$ pins
- Four channel 8-bit Analog to Digital Converter
- Low Voltage Reset
- Available in 40-pin PDIP, 42-pin SDIP and 44-pin QFP packages

1.2 Mask Options

The following mask options are available:

- RC or Crystal Oscillator (see Section 2.2). The default is crystal option.
- Power-On Reset delay — Table 1-1 shows available options. The default value is 4096 cycles.

Table 1-1 Power-On Reset Delay Mask Option

Power-On Reset Delay (cycles)
256
512
1024
2048
4096
8192
16384
32768

- Power-On Reset Slow mode. If enabled, the device goes into Slow mode directly upon power-on reset. The bus frequency is 16 times slower than the normal mode. Thus, the power-on reset delay will also be 16 times longer. The default setting is “Slow mode” disabled.

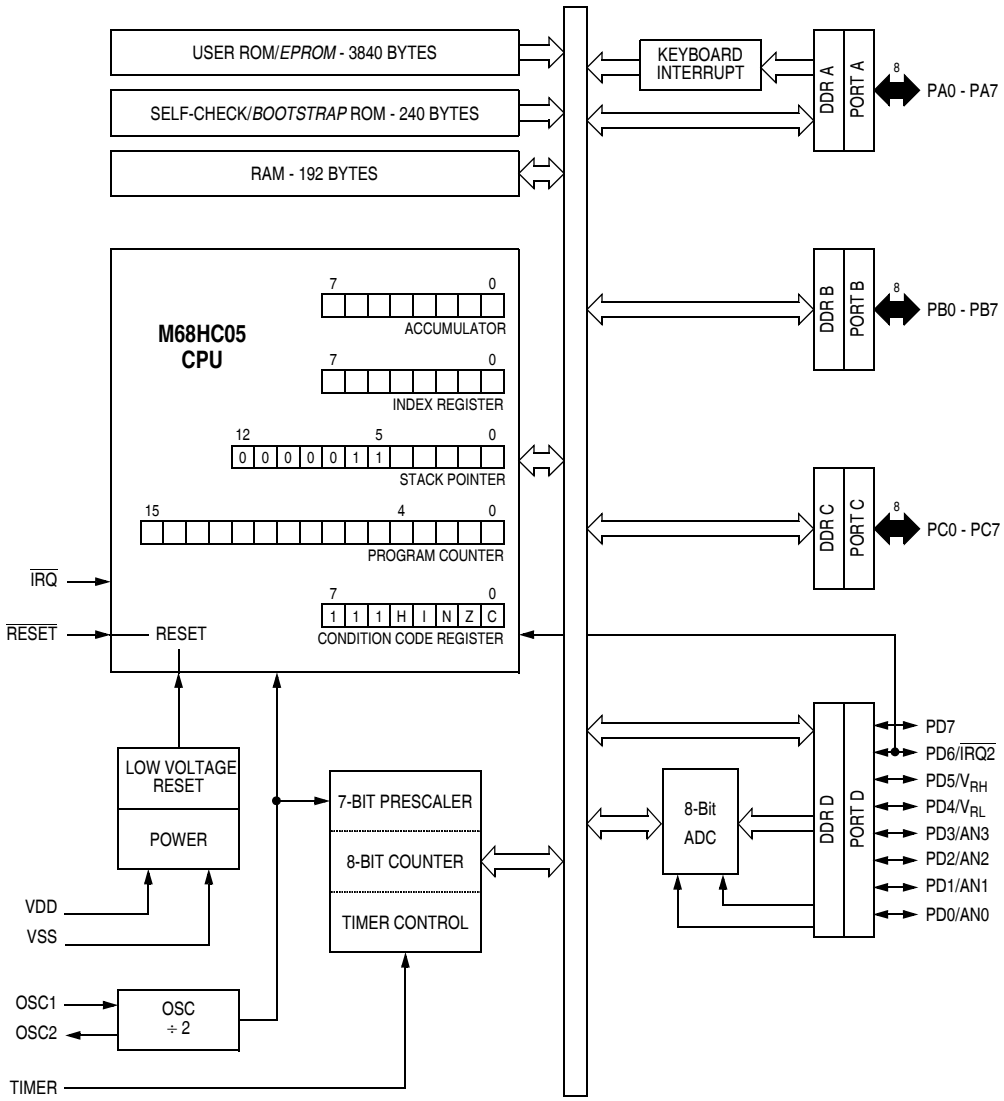

Figure 1-1 MC68HC05SR3/*MC68HC705SR3* Block Diagram

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2
PIN DESCRIPTIONS

This section provides a description of the functional pins of the MC68HC05SR3 microcontroller.

2.1 Functional Pin Descriptions

PIN NAME	40-pin PDIP PIN No.	42-pin SDIP PIN No.	44-pin QFP PIN No.	DESCRIPTION
VDD VSS VSS(INT) VSS(EXT)	4 1 — —	5 — 1 2	10, 33 32 6 7	Power is supplied to the MCU using these pins. VDD should be connected to the positive supply. VSS, VSS(INT), and VSS(EXT) should be connected to supply ground.
VPP	*7*	*8*	*13*	*This is the EPROM programming voltage input pin on the MC68HC705SR3. On the MC68HC05SR3 part, this pin should be connected to VDD or VSS.*
$\overline{\text{IRQ}}$	3	4	9	$\overline{\text{IRQ}}$ is software programmable to provide two choices of interrupt triggering sensitivity. These options are: 1) negative-edge-sensitive triggering only, or 2) both negative-edge-sensitive and level-sensitive triggering. This pin has an integrated pull-up resistor to VDD but should be tied to VDD if not needed to improve noise immunity. The $\overline{\text{IRQ}}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. The voltage on this pin may affect the mode of operation as described in Section 10.
$\overline{\text{RESET}}$	2	3	8	This pin can be used as an input to reset the MCU to a known start-up state by pulling it to the low state. The $\overline{\text{RESET}}$ pin contains an internal Schmitt trigger to improve its noise immunity as an input. It also has an internal pull-down device that pulls the $\overline{\text{RESET}}$ pin low during the power-on reset cycles and an integrated pull-up resistor to VDD.
TIMER	8	9	14	The TIMER pin provides an optional gating input to the timer. Refer to Section 6 for additional information.
OSC1, OSC2	5, 6	6, 7	11, 12	The OSC1 and OSC2 pins are the connections for the on-chip oscillator. See Section 2.2 for detail.

PIN NAME	40-pin PDIP PIN No.	42-pin SDIP PIN No.	44-pin QFP PIN No.	DESCRIPTION
PA0-PA7	33-40	34-41	42-44, 1-5	These eight I/O lines comprise port A. The state of any pin is software programmable. All port A lines are configured as input during power-on or external reset. PA0-PA7 are also associated with the Keyboard Interrupt function. Each pin is equipped with a programmable integrated 20KΩ pull-up resistor connected to VDD when configured as input. When programmed as output, each pin can provide a current drive of 10mA. See Section 3 for details on the I/O ports.
PB0-PB7	25-32	26-33	31, 35-41	These eight I/O lines comprise port B. The state of any pin is software programmable. All port B lines are configured as input during power-on or external reset. Each pin is equipped with a programmable integrated 20KΩ pull-up resistor connected to VDD when configured as input. When programmed as output, each pin can provide a current drive of 10mA. PB5-PB7 can also be programmed to provide a lower current drive of 2mA. See Section 3 for details on the I/O ports.
PC0-PC7	9-16	10-17	15-22	These eight I/O lines comprise port C. The state of any pin is software programmable. All port C lines are configured as input during power-on or external reset. Each pin is equipped with a programmable integrated 20KΩ pull-up resistor connected to VDD when configured as input. When programmed as output, each pin can provide a current drive of 10mA. See Section 3 for details on the I/O ports.
PD0-PD7 AN0-AN3 $\overline{IRQ2}$ VRH VRL	24-21, 20-17 24-21 18 19 20	25-22, 21-18 25-22 19 20 21	30-23 30-27 24 25 26	These eight I/O lines comprise port D. The state of any pin is software programmable. All port D lines are configured as input during power-on or external reset. Each pin is equipped with a programmable integrated 20KΩ pull-up resistor connected to VDD when configured as input. When programmed as output, each pin can provide a current drive of 10mA. PD0-PD3 become analog inputs AN0-AN3 when the ADON bit is set in the ADC Status and Control Register ($0E). PD4 and PD5 becomes VRL and VRH respectively for the ADC reference voltage inputs. PD6 is configured as $\overline{IRQ2}$ by setting IRQ2E in the Miscellaneous Control Register ($0C). See Section 3 for details on the I/O ports.

2.2 OSC1 and OSC2 Connections

The OSC1 and OSC2 pins are the connections for the on-chip oscillator — the following configurations are available:

1) A crystal or ceramic resonator as shown in Figure 2-1(a).
2) An external clock signal as shown in Figure 2-1(b).
3) RC options as shown in Figure 2-1(c) and Figure 2-1(d).

The external oscillator clock frequency, f_{OSC}, is divided by two to produce the internal operating frequency, f_{OP}.

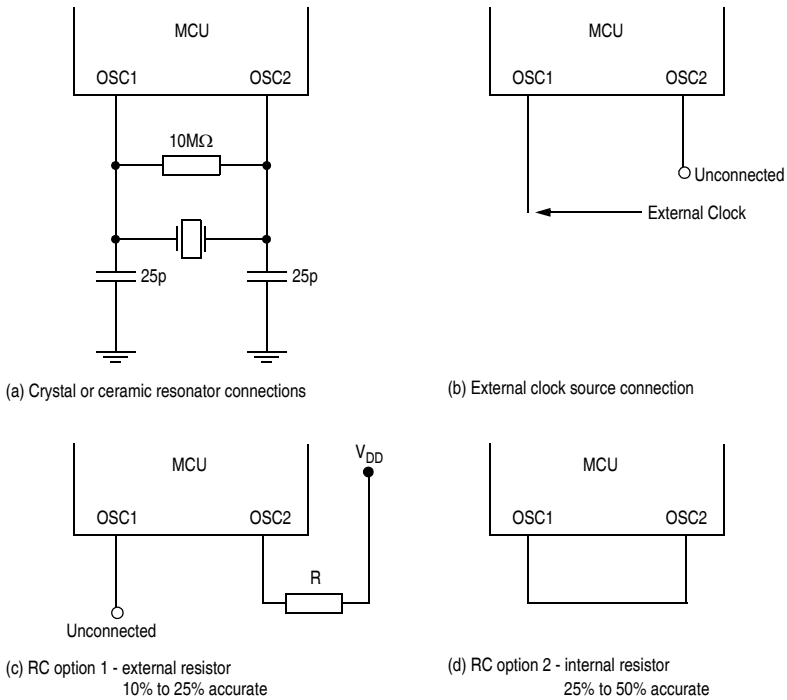

Figure 2-1 Oscillator Connections

2.2.1 Crystal Oscillator

The circuit in Figure 2-1(a) shows a typical oscillator circuit for an AT-cut, parallel resonant crystal. The crystal manufacturer's recommendations should be followed, as the crystal parameters determine the external component values required to provide maximum stability and reliable start-up. The load capacitance values used in the oscillator circuit design should include all stray capacitances. The crystal and components should be mounted as close as possible to the pins for start-up stabilization and to minimize output distortion. An external start-up resistor of approximately 10MΩ is needed between OSC1 and OSC2 for the crystal type oscillator.

2.2.2 External Clock

An external clock from another CMOS-compatible device can be connected to the OSC1 input, with the OSC2 input not connected, as shown in Figure 2-1(b).

2.2.3 RC Oscillator Option

This configuration is intended to be the lowest cost option in applications where oscillator accuracy is not important. An internal constant current source and a capacitor have been integrated on-chip, connected between the OSC2 pin and VSS. Thus by either connecting a resistor to VDD from OSC2 or by putting a wire strap between OSC1 and OSC2 self-oscillations at the frequency as shown in Figure 2-2 and Figure 2-3 can be induced.

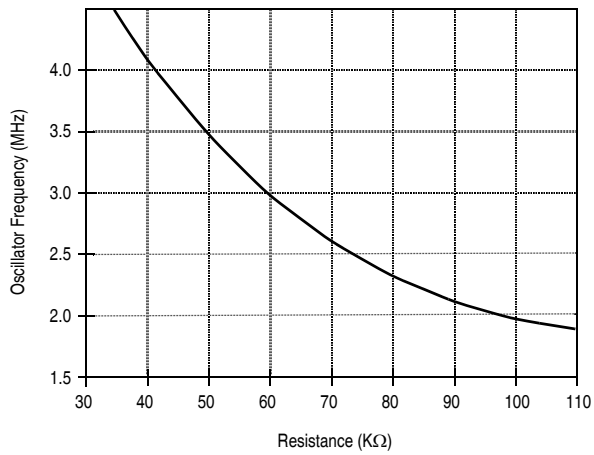

Figure 2-2 Typical Oscillator Frequency for Selected External Resistor

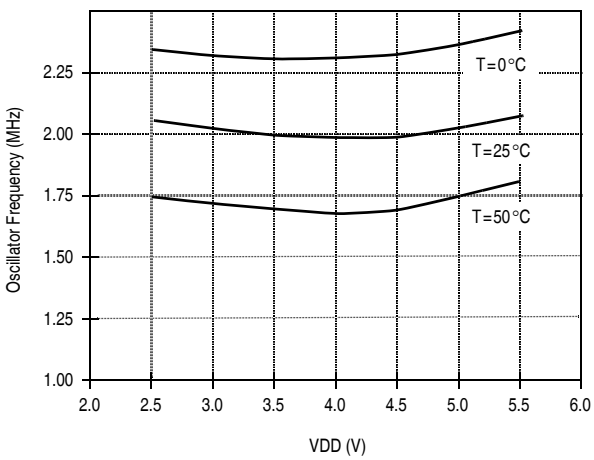

Figure 2-3 Typical Oscillator Frequency for Wire-Strap Connection

2.3 Pin Assignments

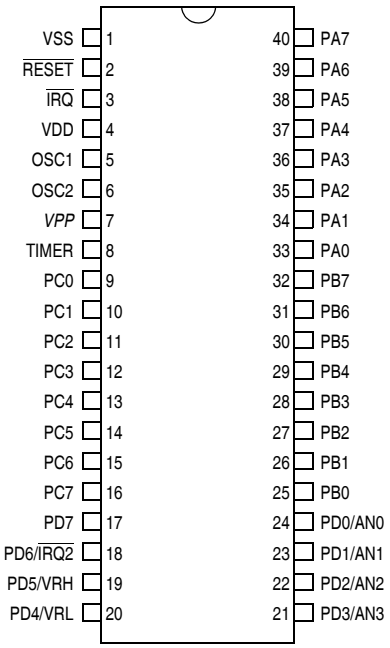

Figure 2-4 Pin Assignment for 40-pin PDIP