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MC68HC711D3
MC68HC11D3
MC68HC11D0
MC68L11D0

Data Sheet

HC11
Microcontrollers

MC68HC711D3
Rev. 2.1
07/2005

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MC68HC711D3

Data Sheet

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
September, 2003	2	Reformatted to current publications standards	N/A
		Removed references to PROG mode.	Throughout
		Corrected pin assignments for: Figure 1-2. Pin Assignments for 40-Pin Plastic DIP Figure 1-3. Pin Assignments for 44-Pin PLCC Added Figure 1-4. Pin Assignments for 44-Pin QFP	 4 5 6
		1.9 Interrupt Request (IRQ) — Reworked description for clarity.	7
		2.4 Programmable Read-Only Memory (PROM) — Updated with additional data.	13
		Section 10. Ordering Information and Mechanical Specifications — Added mechanical specifications for 44-pin plastic quad flat pack (QFP).	133
		Added the following appendices: Appendix A. MC68HC11D3 and MC68HC11D0 Appendix B. MC68L11D0	 137 143
July, 2005	2.1	Updated to meet Freescale identity guidelines.	Throughout

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Chapter 1
General Description

1.1 Introduction

This section depicts the general characteristics and features of the MC68HC711D3 high-density complementary metal-oxide semiconductor (HCMOS) microcontroller unit (MCU).

The MC68HC711D3 contains highly sophisticated on-chip peripheral functions. This high-speed, low-power programmable read-only memory (PROM) MCU has a nominal bus speed of 3 MHz. The fully static design allows operations at frequencies down to dc.

The MC68HC11D3 and MC68HC11D0 are read-only memory (ROM) based high-performance microcontrollers (MCU) based on the MC68HC11E9 design. The MC68L11D0 is an extended-voltage version of the MC68HC11D0 that can operate in applications that require supply voltages as low as 3.0 V. The information in this document pertains to all the devices with the exceptions noted in Appendix A MC68HC11D3 and MC68HC11D0 and Appendix B MC68L11D0.

1.2 Features

Features of the MC68HC711D3 include:

- Expanded 16-bit timer system with four-stage programmable prescaler
- Non-return-to-zero (NRZ) serial communications interface (SCI)
- Power-saving stop and wait modes
- 64 Kbytes memory addressability
- Multiplexed address/data bus
- Serial peripheral interface (SPI)
- 4 Kbytes of one-time programmable read-only memory (OTPROM)
- 8-bit pulse accumulator circuit
- 192 bytes of static random-access memory (RAM) (all saved during standby)
- Real-time interrupt (RTI) circuit
- Computer operating properly (COP) watchdog system
- Available in these packages:
  - 40-pin plastic dual in-line package (DIP)
  - 44-pin plastic leaded chip carrier (PLCC)
  - 44-pin plastic quad flat pack (QFP)

1.3 Structure

Refer to Figure 1-1, which shows the structure of the MC68HC711D3 MCU.

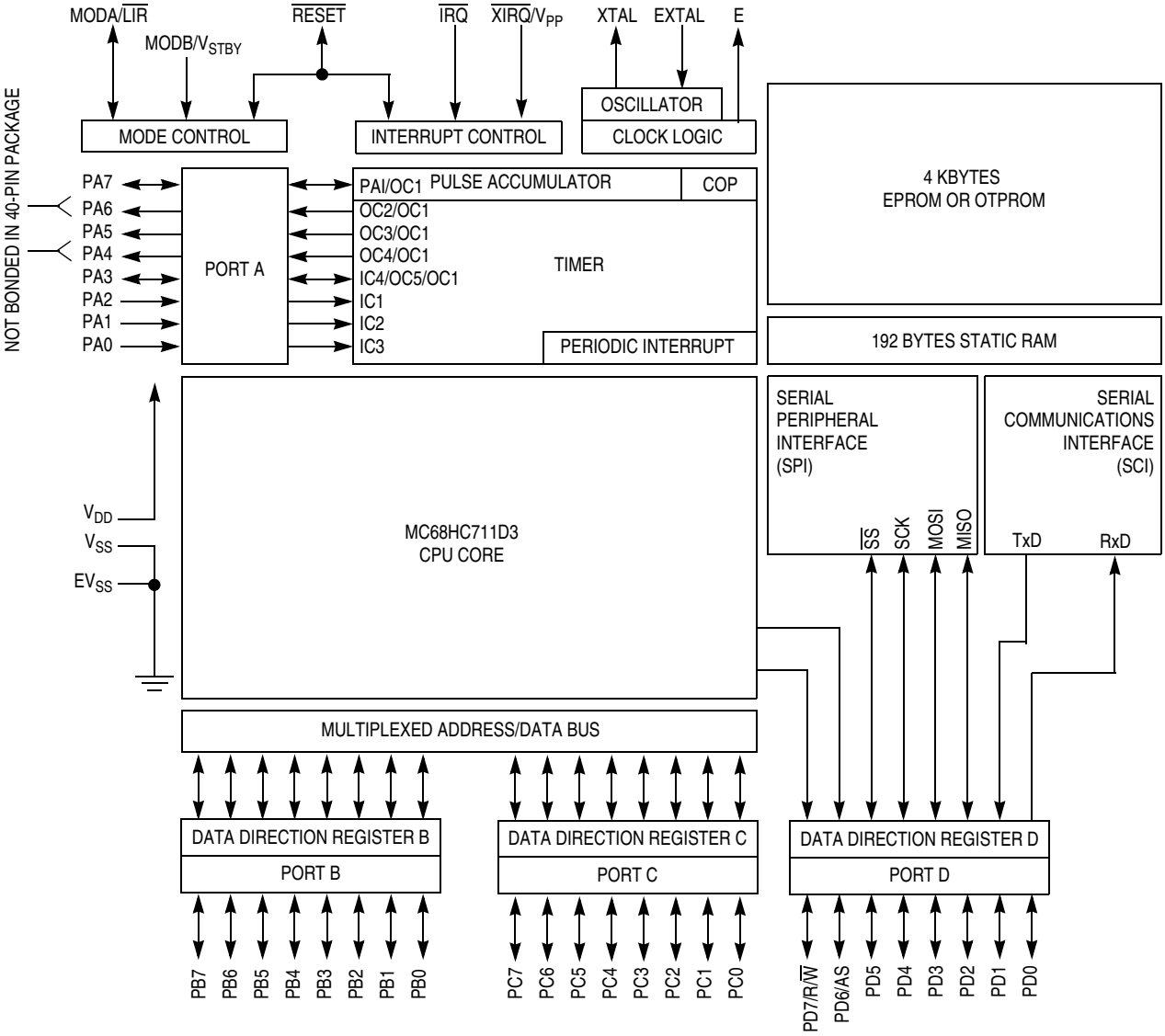


Figure 1-1. MC68HC711D3 Block Diagram

1.4 Pin Descriptions

Refer to Figure 1-2, Figure 1-3, and Figure 1-4 for pin assignments.

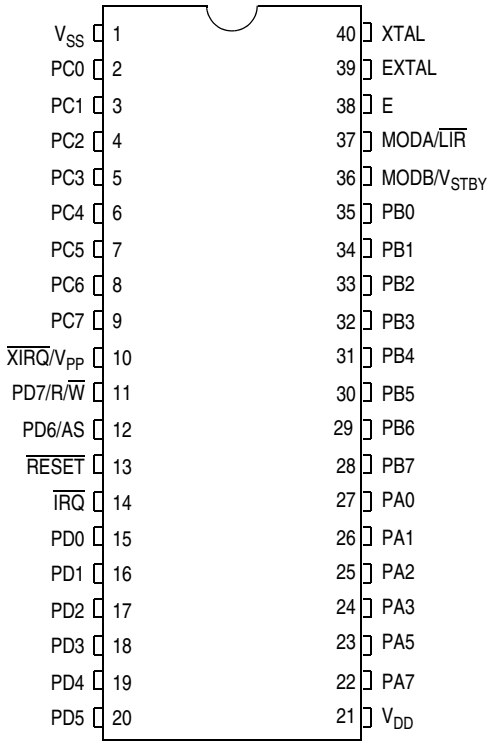


Figure 1-2. Pin Assignments for 40-Pin Plastic DIP

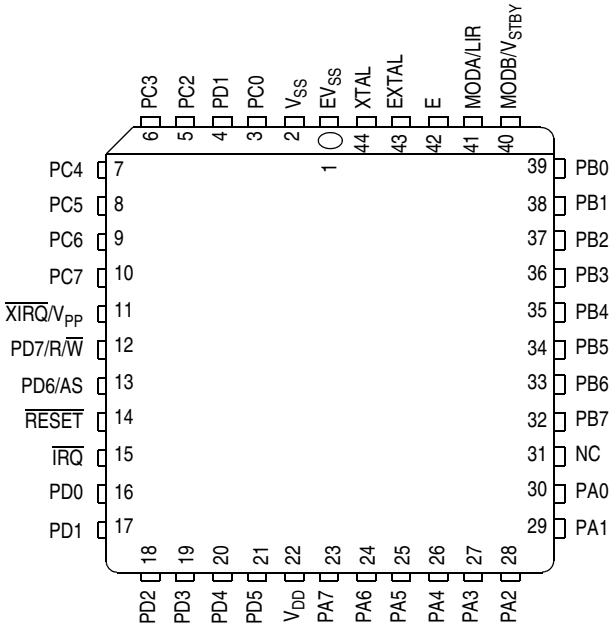


Figure 1-3. Pin Assignments for 44-Pin PLCC

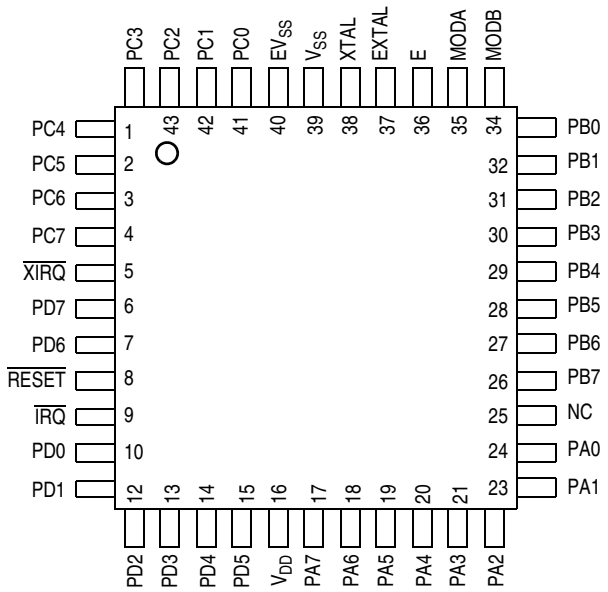


Figure 1-4. Pin Assignments for 44-Pin QFP

1.5 Power Supply (V_{DD}, V_{SS}, and EV_{SS})

Power is supplied to the MCU through V_{DD} and V_{SS}. V_{DD} is the power supply (+5 V ±10%) and V_{SS} is ground (0 V). EV_{SS}, available on the 44-pin PLCC and QFP, is an additional ground pin.

1.6 Reset ($\overline{\text{RESET}}$)

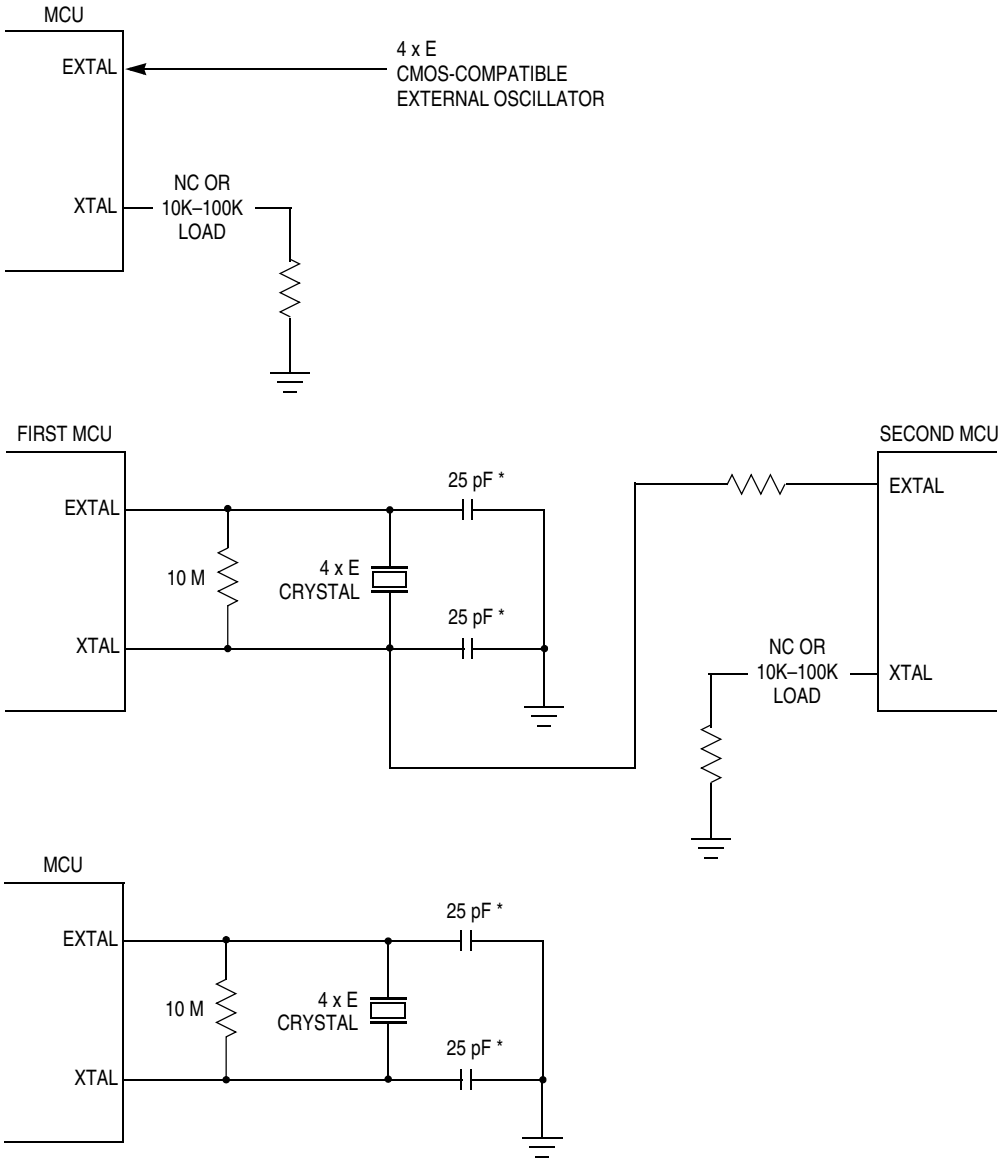
An active low bidirectional control signal, $\overline{\text{RESET}}$, acts as an input to initialize the MCU to a known startup state. It also acts as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or computer operating properly (COP) watchdog circuit. In addition, the state of this pin is one of the factors governing the selection of BOOT mode.

1.7 Crystal Driver and External Clock Input (XTAL and EXTAL)

These two pins provide the interface for either a crystal or a CMOS compatible clock to control the internal clock generator circuitry. The frequency applied to these pins is four times higher than the desired E-clock rate. Refer to Figure 1-5 for crystal and clock connections.

1.8 E-Clock Output (E)

E is the output connection for the internally generated E clock. The signal from E is used as a timing reference. The frequency of the E-clock output is one fourth that of the input frequency at the XTAL and EXTAL pins. The E clock can be turned off in single-chip mode for greater noise immunity if desired. See 4.3.6 Highest Priority I Interrupt and Miscellaneous Register (HPRIO) for details.



* Values includes all stray capacitances.

Figure 1-5. Oscillator Connections

1.9 Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ input provides a means of applying asynchronous interrupt requests to the microcontroller unit (MCU). Either negative edge-sensitive triggering or level-sensitive triggering is program selectable by using the IRQE bit of the OPTION register. $\overline{IRQ}$ is always configured to level-sensitive triggering at reset.

While the programmable read-only memory (PROM) is being programmed, this pin provides the chip enable ($\overline{CE}$) signal. To prevent accidental programming of the PROM during reset, an external resistor is required on $\overline{IRQ}$ to pull the pin to V_{DD}.

1.10 Non-Maskable Interrupt/Programming Voltage ($\overline{XIRQ}/V_{PP}$)

The $\overline{XIRQ}$ input provides the capability for asynchronously applying non-maskable interrupts to the MCU after a power-on reset (POR). During reset, the X bit in the condition code register (CCR) is set masking any interrupt until enabled by software. This level-sensitive input requires an external pullup resistor to V_{DD}.

In the programming configuration of the bootstrap mode, this pin is used to supply one-time programmable read-only memory (OTPROM) programming voltage, V_{PP}, to the MCU. To avoid programming accidents during reset, this pin should be equal to V_{DD} during normal operation unless $\overline{XIRQ}$ is active.

1.11 MODA and MODB (MODA/$\overline{LIR}$ and MODB/V_{STBY})

As reset transitions, these pins are used to latch the part into one of the four central processor unit (CPU) controlled modes of operation. The $\overline{LIR}$ output can be used as an aid to debugging once reset is completed. The open-drain $\overline{LIR}$ pin goes to an active low during the first E-clock cycle of each instruction and remains low for the duration of that cycle. The V_{STBY} input is used to retain random-access memory (RAM) contents during power down.

1.12 Read/Write (R/$\overline{W}$)

This pin performs either of two separate functions, depending on the operating mode.

- In single-chip and bootstrap modes, R/$\overline{W}$ functions as input/output port D bit 7. Refer to Chapter 5 Input/Output (I/O) Ports for further information.
- In expanded multiplexed and test modes, R/$\overline{W}$ performs a read/write function. R/$\overline{W}$ controls the direction of transfers on the external data bus.

1.13 Port D Bit 6/Address Strobe (PD6/AS)

This pin performs either of two separate functions, depending on the operating mode.

- In single-chip and bootstrap modes, the pin functions as input/output port D bit 6.
- In the expanded multiplexed and test modes, it provides an address strobe (AS) function. AS is used to demultiplex the address and data signals at port C.

Refer to Chapter 2 Operating Modes and Memory for further information.

1.14 Input/Output Lines (PA7–PA0, PB7–PB0, PC7–PC0, and PD7–PD0)

In the 44-pin PLCC package, 32 input/output lines are arranged into four 8-bit ports: A, B, C, and D. The lines of ports B, C, and D are fully bidirectional. Port A has two bidirectional, three input-only, and three output-only lines in the 44-pin PLCC packaging. In the 40-pin DIP, two of the output-only lines are not bonded.

Each of these four ports serves a purpose other than input/output (I/O), depending on the operating mode or peripheral functions selected.

NOTE

Ports B, C, and two bits of port D are available for I/O functions only in single-chip and bootstrap modes.

Refer to Table 1-1 for details about the functions of the 32 port signals within different operating modes.

Table 1-1. Port Signal Functions

Port/Bit	Single-Chip and Bootstrap Mode	Expanded Multiplexed and Special Test Mode
PA0	PA0/IC3	
PA1	PA1/IC2	
PA2	PA2/IC1	
PA3	PA3/OC5/IC4/and-or OC1	
PA4[1]	PA4/OC4/and-or OC1	
PA5	PA5/OC3/and-or OC1	
PA6[1]	PA6/OC2/and-or OC1	
PA7	PA7/PAI/and-or OC1	
PB0	PB0	A8
PB1	PB1	A9
PB2	PB2	A10
PB3	PB3	A11
PB4	PB4	A12
PB5	PB5	A13
PB6	PB6	A14
PB7	PB7	A15
PC0	PC0	A0/D0
PC1	PC1	A1/D1
PC2	PC2	A2/D2
PC3	PC3	A3/D3
PC4	PC4	A4/D4
PC5	PC5	A5/D5
PC6	PC6	A6/D6
PC7	PC7	A7/D7
PD0	PD0/RxD	
PD1	PD1/TxD	
PD2	PD2/MISO	
PD3	PD3/MOSI	
PD4	PD4/SCK	
PD5	PD5/$\overline{SS}$	
PD6	PD6	AS
PD7	PD7	R/$\overline{W}$

1. In the 40-pin package, pins PA4 and PA6 are not bonded. Their associated I/O and output compare functions are not available externally. They can still be used as internal software timers, however.

Chapter 2
Operating Modes and Memory

2.1 Introduction

This section contains information about:

- The modes that define MC68HC711D3 operating conditions
- The on-chip memory that allows the microcontroller unit (MCU) to be configured for various applications
- The 4-Kbytes of programmable read-only memory (PROM)

2.2 Operating Modes

The MC68HC711D3 uses two dedicated pins, MODA and MODB, to select one of two normal operating modes or one of two special operating modes. A value reflecting the microcontroller unit (MCU) status or mode selected is latched on bits SMOD and MDA of the highest priority I-bit interrupt and miscellaneous register (HPRIO) on the rising edge of reset. The normal operating modes are the single-chip and expanded-multiplexed modes. The special operating modes are the bootstrap and test modes. Table 2-1 shows mode selection according to the values encoded on the MODA and MODB pins, and the value latched in the SMOD and MDA bits.

Table 2-1. Mode Selection

RESET	MODA	MODB	Mode Selected	SMOD	MDA
1	0	1	Normal — single chip	0	0
1	1	1	Normal — expanded multiplexed	0	1
1	0	0	Special — bootstrap (BOOT)	1	0
1	1	0	Special — test	1	1
0	0	0	Reserved	X	X

2.2.1 Single-Chip Mode

In single-chip mode, the MCU functions as a self-contained microcontroller and has no external address or data bus. The 4-Kbyte erasable programmable read-only memory (EPROM) would contain all program code and is located at $F000–$FFFF. This mode provides maximum use of the pins for on-chip peripheral functions, and all the address and data activity occurs within the MCU.

2.2.2 Expanded Multiplexed Mode

In the expanded-multiplexed mode, the MCU can address up to 64 Kbytes of address space. High-order address bits are output on the port B pins. Low-order address bits and the bidirectional data bus are multiplexed on port C. The AS pin provides the control output used in demultiplexing the low-order address. The R/$\overline{W}$ pin is used to control the direction of data transfer on the port C bus.

If this mode is entered out of reset, the EPROM is located at $7000–$7FFF and vector accesses are from external memory. To be in expanded-multiplexed mode with EPROM located at $F000–$FFFF, it is necessary to start in single-chip mode, executing out of EPROM, and then set the MDA bit of the HPRIO register to switch mode.

NOTE

R/$\overline{W}$, AS, and the high-order address bus (port B) are inputs in single-chip mode. These inputs may need to be pulled up so that off-chip accesses cannot occur while the MCU is in single-chip mode.

2.2.3 Special Bootstrap Mode (BOOT)

This special mode is similar to single-chip mode. The resident bootloader program contains a 256-byte program in a special on-chip read-only memory (ROM). The user downloads a small program into on-board RAM using the SCI port. Program control is passed to RAM when an idle line of at least four characters occurs. In this mode, all interrupt vectors are mapped to RAM (see Table 2-2), so that the user can set up a jump table, if desired.

Bootstrap mode (BOOT) is entered out of reset if the voltage level on both MODA and MODB is low. The programming aspect of bootstrap mode, used to program the one-time programmable ROM (OTPROM) through the MCU, is entered automatically if $\overline{IRQ}$ is low and programming voltage is available on the V_{PP} pin. $\overline{IRQ}$ should be pulled up while in reset with MODA and MODB configured for bootstrap mode to prevent unintentional programming of the EPROM.

This versatile mode (BOOT) can be used for test and diagnostic functions on completed modules and for programming the on-board PROM. The serial receive logic is initialized by software in the bootloader ROM, which provides program control for the SCI baud rate and word format. Mode switching to other modes can occur under program control by writing to the SMOD and MDA bits of the HPRIO register. Two special bootloader functions allow either an immediate jump-to-RAM at memory address $0000 or an immediate jump-to-EPROM at $F000.

Table 2-2. Bootstrap Mode Jump Vectors

Address	Vector
00C4	SCI
00C7	SPI
00CA	Pulse accumulator input edge
00CD	Pulse accumulator overflow
00D0	Timer overflow
00D3	Timer output compare 5/input capture 4
00D6	Timer output compare 4
00D9	Timer output compare 3
00DC	Timer output compare 2
00DF	Timer output compare 1
00E3	Timer input capture 3
00E5	Timer input capture 2
00E8	Timer input capture 1

Table 2-2. Bootstrap Mode Jump Vectors (Continued)

Address	Vector
00EB	Real-time interrupt
00EE	IRQ
00F1	XIRQ
00F4	SWI
00F7	Illegal opcode
00FA	COP fail
00FD	Clock monitor
BF00 (Boot)	Reset

2.2.4 Special Test Mode

This special expanded mode is primarily intended or production testing. The user can access a number of special test control bits in this mode. Reset and interrupt vectors are fetched externally from locations $BFC0–$BFFF. A switch can be made from this mode to other modes under program control.

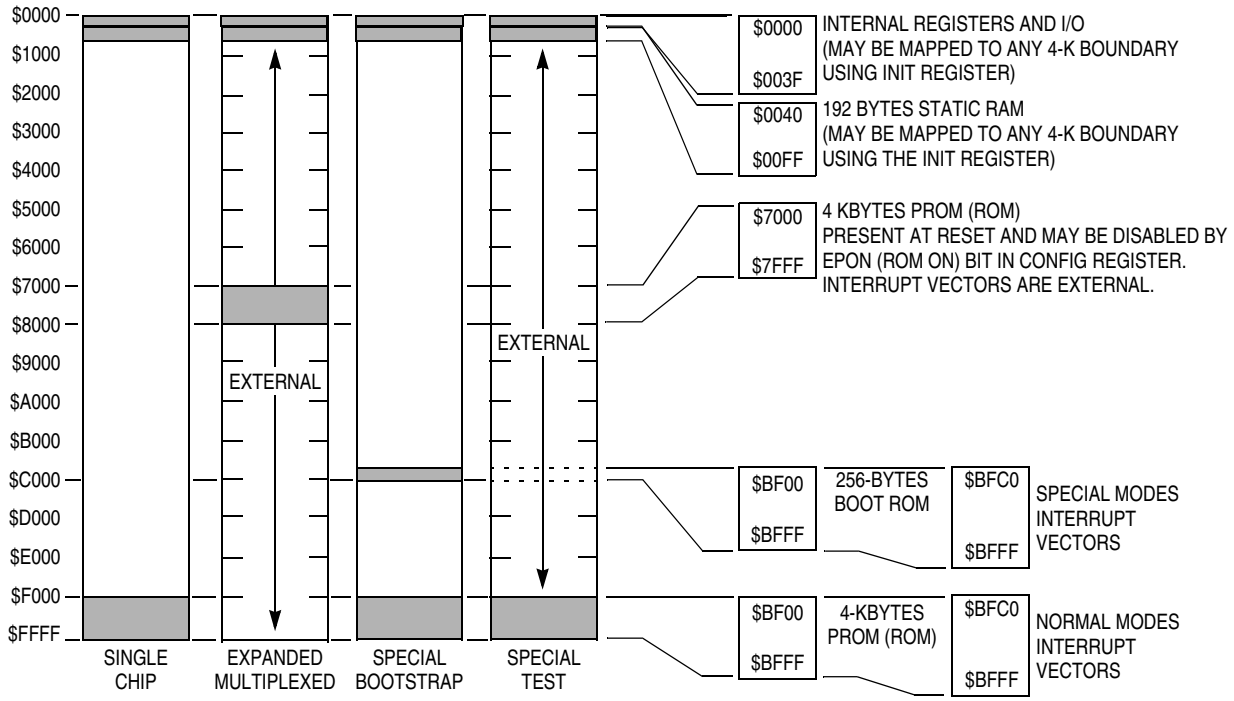
2.3 Memory Map

Figure 2-1 illustrates the memory map for both normal modes of operation (single-chip and expanded-multiplexed), as well as for both special modes of operation (bootstrap and test).

- In the single-chip mode, the MCU does not generate external addresses. The internal memory locations are shown in the shaded areas, and the contents of these shaded areas are explained on the right side of the diagram.
- In expanded-multiplexed mode, the memory locations are basically the same as in the single-chip mode except that the memory locations between shaded areas are for externally addressed memory and I/O.
- The special bootstrap mode is similar to the single-chip mode, except that the bootstrap program ROM is located at memory locations $BF00–$BFFF, vectors included.
- The special test mode is similar to the expanded-multiplexed mode except the interrupt vectors are at external memory locations.

2.3.1 Control and Status Registers

Figure 2-2 is a representation of all 64 bytes of control and status registers, I/O and data registers, and reserved locations that make up the internal register block. This block may be mapped to any 4-K boundary in memory, but reset locates it at $0000–$003F. This mappability factor and the default starting addresses are indicated by the use of a bold **0** as the starting character of a register's address.



MODB	MODA	Mode Selected
1	0	Single-chip (mode 0)
1	1	Expanded multiplexed (mode 1)
0	0	Special bootstrap
0	1	Special test

Figure 2-1. MC68HC711D3 Memory Map

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PORTA) See page 61.	Read: Write:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		Reset:	Hi-Z	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
$0001	Reserved		R	R	R	R	R	R	R	R
$0002	Port C Control Register (PIOC) See page 63.	Read: Write:	0	0	CWOM	0	0	0	0	0
		Reset:	0	0	0	0	0	0	0	0
$0003	Port C Data Register (PORTC) See page 63.	Read: Write:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Reset:	Reset configures pins as Hi-Z inputs							
$0004	Port B Data Register (PORTB) See page 62.	Read: Write:	PB7	PB6	PB5	PB4	PB3	BP2	BP1	PB0
		Reset:	Reset configures pins as Hi-Z inputs							
$0005	Reserved		R	R	R	R	R	R	R	R
$0006	Data Direction Register for Port B (DDRB) See page 62.	Read: Write:	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0
		Reset:	0	0	0	0	0	0	0	0
$0007	Data Direction Register for Port C (DDRC) See page 63.	Read: Write:	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
		Reset:	0	0	0	0	0	0	0	0
$0008	Port D Data Register (PORTD) See page 64.	Read: Write:	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
		Reset:	0	0	0	0	0	0	0	0
$0009	Data Direction Register for Port D (DDRD) See page 64.	Read: Write:	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
		Reset:	0	0	0	0	0	0	0	0
$000A	Reserved		R	R	R	R	R	R	R	R
$000B	Timer Compare Force Register (CFORC) See page 93.	Read: Write:	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0
		Reset:	0	0	0	0	0	0	0	0
$000C	Output Compare 1 Mask Register (OC1M) See page 93.	Read: Write:	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0
		Reset:	0	0	0	0	0	0	0	0
$000D	Output Compare 1 Data Register (OC1D) See page 94.	Read: Write:	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Figure 2-2. Register and Control Bit Assignments (Sheet 1 of 5)