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M68HC11 Microcontrollers

MC68HC11P2
MC68HC711P2

Technical Data

MC68HC11P2/D
Rev. 1, 4/2002

freescale semiconductor

MC68HC11P2
MC68HC711P2

Technical Data — Rev 1.0

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Section 1. General Description

1.1 Contents

1.2 Introduction

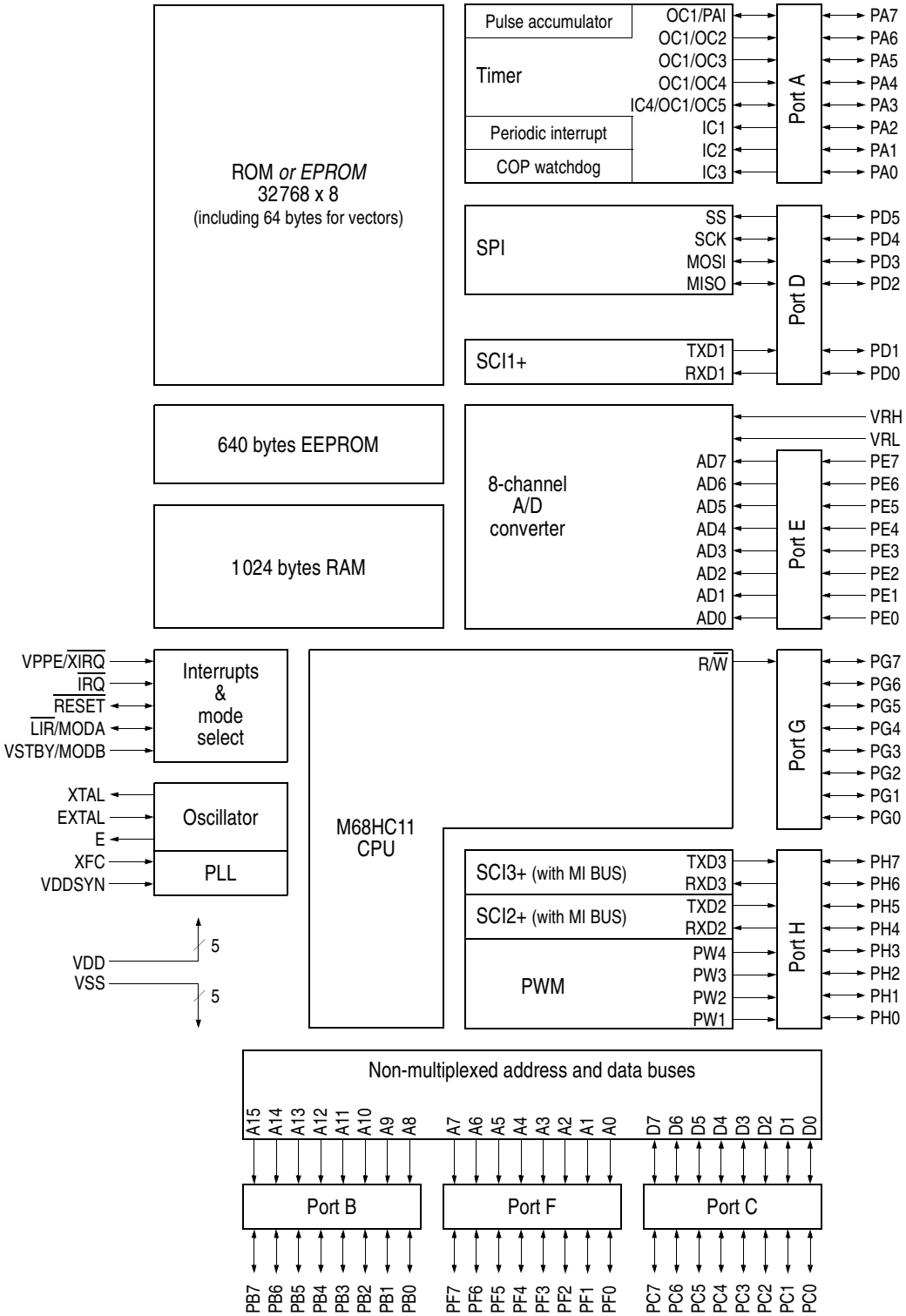
The MC68HC11P2 8-bit microcomputer is a member of the M68HC11 family of HCMOS microcomputers. In addition to 32kbytes of ROM, the MC68HC11P2 contains 1kbyte of RAM and 640 bytes of EEPROM. With its advanced timer and communication features (including MI BUS[1]) the MC68HC11P2 is especially suitable for mobile communications and automotive applications.

The MC68HC711P2 is an EPROM version of the MC68HC11P2, with the User ROM replaced by a similar amount of EPROM. All references to the MC68HC11P2 apply equally to the MC68HC711P2, unless otherwise noted. *References specific to the MC68HC711P2 are italicised in the text.*

1. The Motorola interconnect bus (MI BUS) is a serial communications protocol which supports distributed real-time control efficiently and with a high degree of noise immunity. It allows data

1.3 Features

- Low power, high performance M68HC11 CPU core, with 4MHz bus capability
- Power saving PLL clock circuit, with automatic disable during WAIT mode
- 32kbytes of User ROM (MC68HC11P2); *32kbytes User EPROM (MC68HC711P2)*
- 1kbyte of RAM
- 640 bytes of byte-erasable User EEPROM, with on-chip charge pump
- Up to 50 general purpose I/O lines, plus up to 12 input-only lines
- Non-multiplexed address and data buses, permitting direct access to the full 64k address map
- 16-bit timer with 3/4 input captures and 4/5 output compares; pulse accumulator and COP watchdog timer
- Three 8- or 9-bit SCI subsystems, two with MI BUS† capability
- SPI subsystem, with software selectable MSB/LSB first option
- 8-channel, 8-bit analog-to-digital (A/D) converter
- Four 8-bit PWM timer channels (may be concatenated to form one, or two, 16-bit channels)
- Available in 84-pin PLCC *or 84-pin CERQUAD* packages



General Description

Section 2. Pin Descriptions

2.1 Contents

2.2 Introduction

The MC68HC11P2 is available in an 84-pin plastic-leaded chip carrier (PLCC); *the MC68HC711P2 is also available in an 84-pin windowed cerquad package, to allow full use of the EPROM.* Most pins on this MCU serve two or more functions, as described in the following paragraphs. Refer to **Figure 2-1** which shows the pin assignments for both 84-pin packages.

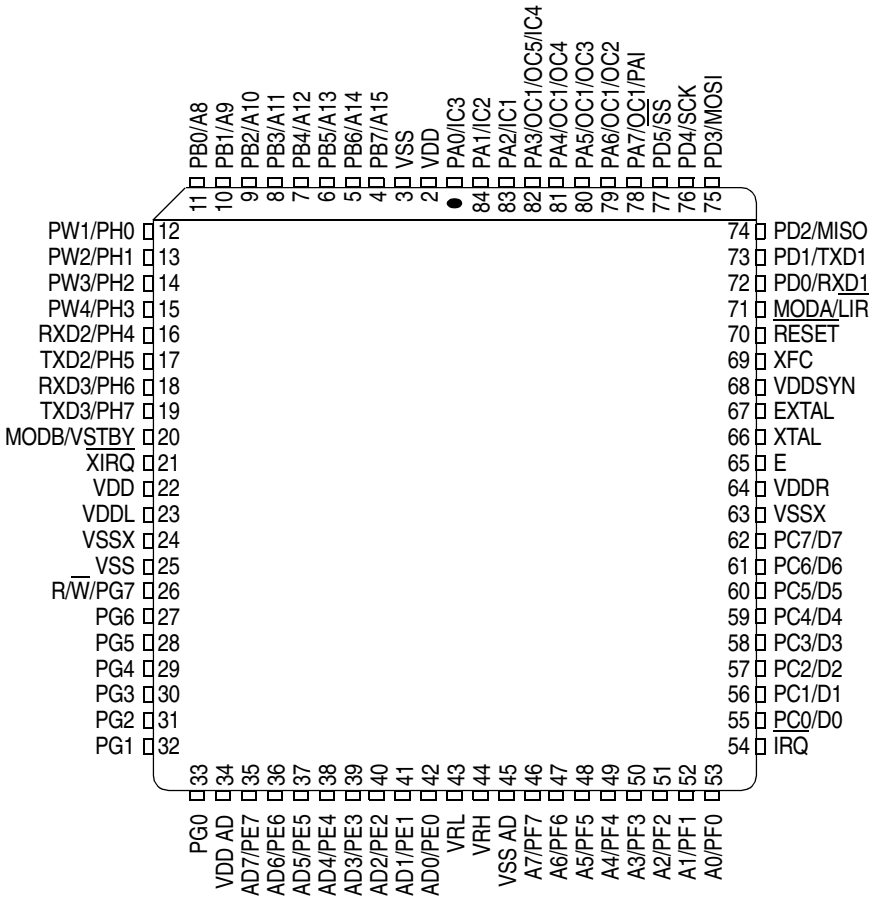


Figure 2-1. 84-pin PLCC/*CERQUAD* pinout

2.3 VDD and VSS

Power is supplied to the microcontroller via these pins. VDD is the positive supply and VSS is ground. The MCU operates from a single 5V (nominal) power supply.

It is in the nature of CMOS designs that very fast signal transitions occur on the MCU pins. These short rise and fall times place very high short-duration current demands on the power supply. To prevent noise problems, special care must be taken to provide good power supply bypassing at the MCU. Bypass capacitors should have good high-

Bypassing requirements vary, depending on how heavily the MCU pins are loaded.

The MC68HC11P2 MCU has five VDD pins and five VSS pins. One pair of these pins is reserved for supplying power to the analog-to-digital converter (VDD AD, VSS AD); two pairs are used for the internal logic (VDD, VSS); the remaining two pairs supply power for the port logic on either half of the chip (VDDL, VSSX and VDDR, VSSX). This arrangement minimizes the injection of noise into the digital circuitry on the chip.

2.4 $\overline{\text{RESET}}$

An active low bidirectional control signal, $\overline{\text{RESET}}$, acts as an input to initialize the MCU to a known start-up state. It also acts as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or the COP watchdog circuit. The CPU distinguishes between internal and external reset conditions by sensing whether the reset pin rises to a logic one in less than six E clock cycles after a reset has occurred. It is therefore not advisable to connect an external resistor-capacitor (RC) power-up delay circuit to the reset pin of M68HC11 devices because the circuit charge time constant can cause the device to misinterpret the type of reset that occurred. Refer to **Resets and Interrupts** for further information.

Figure 2-2 illustrates a typical reset circuit that includes an external switch together with a low voltage inhibit circuit, to prevent power transitions, or RAM or EEPROM corruption.

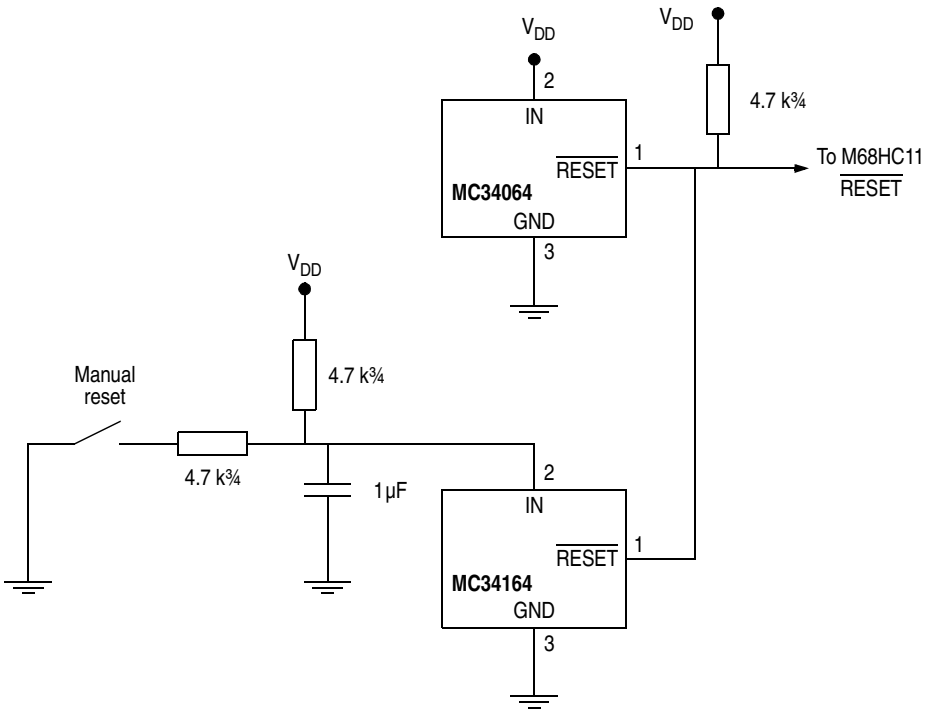


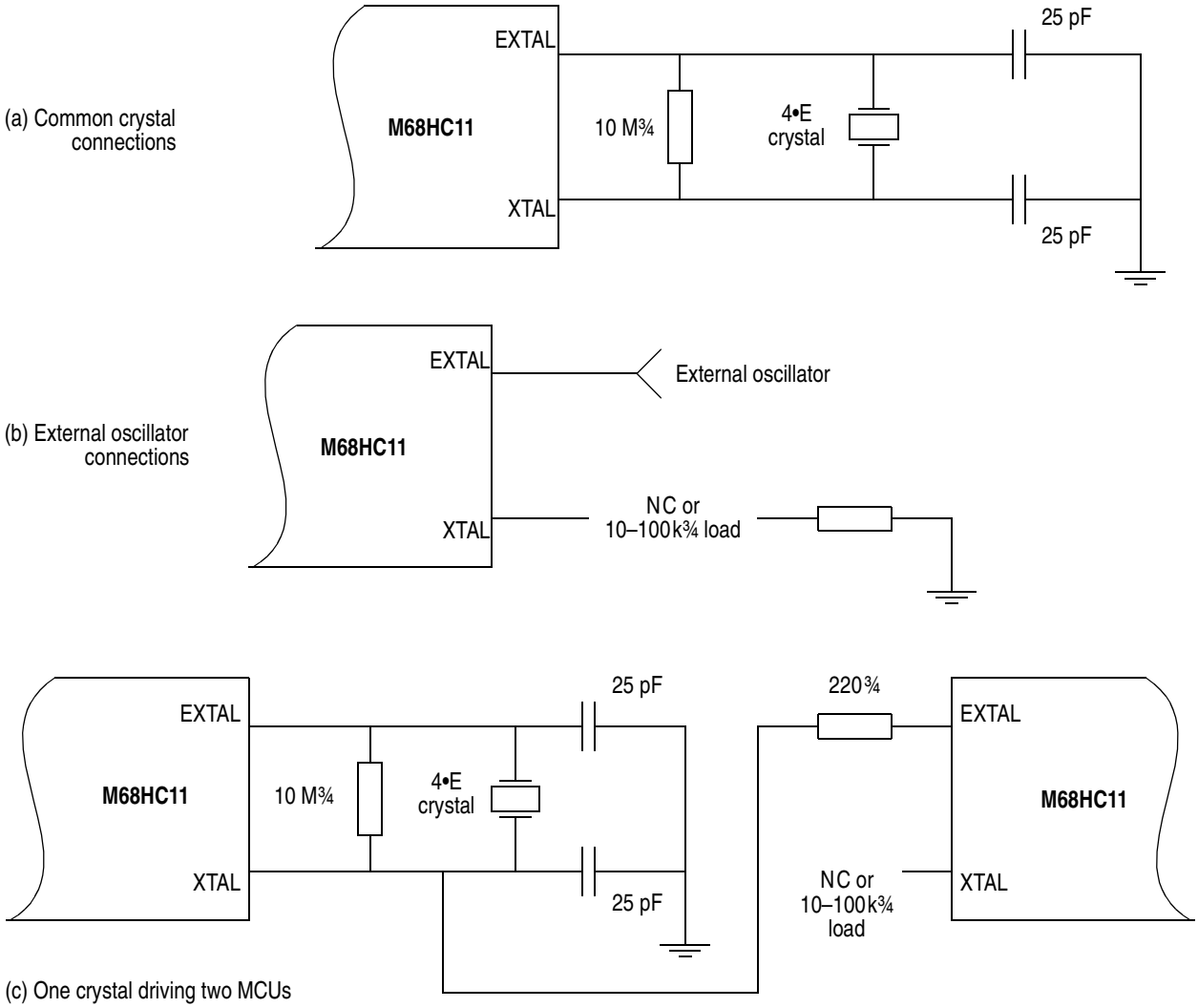
Figure 2-2. External reset circuitry

2.5 Crystal driver and external clock input (XTAL, EXTAL)

These two pins provide the interface for either a crystal or a CMOS compatible clock to control the internal clock generator circuitry. The frequency applied to these pins must be four times higher than the desired E clock rate (unless the PLL circuit is used to provide the E clock).

The XTAL pin is normally left unconnected when an external CMOS compatible clock input is connected to the EXTAL pin. However, a 10 k¾ to 100 k¾ load resistor connected from XTAL to ground can be used to reduce RFI noise emission. The XTAL output is normally intended to drive only a crystal. The XTAL output can be buffered with a high-impedance buffer, or it can be used to drive the EXTAL input of another M68HC11 family device.

In all cases, use caution when designing circuitry associated with the oscillator pins. Load capacitances shown in the oscillator circuits include all stray layout capacitances. See **Figure 2-3**.



Note: capacitor values include all stray capacitance.

Figure 2-3. Oscillator connections