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# MC68HC908GZ60
# MC68HC908GZ48
# MC68HC908GZ32

Data Sheet

***M68HC08***
***Microcontrollers***

MC68HC908GZ60
Rev. 6.0
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# MC68HC908GZ60
# MC68HC908GZ48
# MC68HC908GZ32

**Data Sheet**

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

# Revision History

| Date | Revision Level | Description | Page Number(s) |
|---|---|---|---|
| April, 2004 | N/A | Initial release | N/A |
| May, 2004 | 1.0 | 9.7.3 Keyboard Interrupt Polarity Register — Corrected the bit description of the KBIP7–KBIP0 bits. | 119 |
| | | 14.8.8 ESCI Prescaler Register — Reworked note under PDS2–PDS0 description for clarity. | 212 |
| | | Table 22-1. MC Order Numbers — Corrected order numbers. | 329 |
| | | Figure 22-1. Device Numbering System — Reworked diagram to reflect correct order numbers. | 329 |
| | | Table A-1. MC Order Numbers — Corrected order numbers. | 342 |
| | | Figure A-3. Device Numbering System — Reworked diagram to reflect correct order numbers. | 342 |
| | | B.4 Ordering Information — Corrected order numbers. | 346 |
| | | Figure B-3. Device Numbering System — Reworked diagram to reflect correct order numbers. | 346 |
| June, 2005 | 2.0 | Reformatted to Freescale publication standards | Throughout |
| | | Table 14-6. ESCI LIN Control Bits — Corrected Functionality entries | 211 |
| | | 14.9.1 ESCI Arbiter Control Register — Corrected bit ACLK bit description | 215 |
| | | 14.9.3 Bit Time Measurement — Corrected definition for ACLK bit | 216 |
| March, 2006 | 3.0 | 10.5 Clock Generator Module (CGM) — Updated description to remove erroneous information. | 122 |
| July, 2006 | 4.0 | Added section 1.5.15 Unused Pin Termination | 31 |
| | | Chapter 13 Input/Output (I/O) Ports — Replaced note | 169 |
| | | Table 14-6. ESCI LIN Control Bits — Updated functionality column. | 213 |
| | | 18.6 TIM1 During Break Interrupts — Updated first paragraph for clarity. | 270 |
| | | 19.6 TIM2 During Break Interrupts — Updated first paragraph for clarity. | 290 |
| | | 20.2.1.2 TIM During Break Interrupts — Updated first paragraph for clarity. | 302 |
| | | Figure 20-10. Normal Monitor Mode Circuit and Figure 20-11. Forced Monitor Mode — Changed capacitor values | 307 |
| | | 21.5 5.0-Vdc Electrical Characteristics — Updated minimum value for low-voltage inhibit, trip rising voltage (VTRIPR). | 317 |
| | | 21.9.2 CGM Component Information — Updated values for feedback bias resistor | 322 |

## Revision History (Continued)

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| October, 2006 | 5.0 | 12.2 Features — Corrected timer link connection from TIM2 channel 0 to TIM1 channel 0. | 135 |
| | | 12.9 Timer Link — Corrected timer link connection from TIM2 channel 0 to TIM1 channel 0. | 147 |
| | | 21.5 5.0-Vdc Electrical Characteristics and<br>21.6 3.3-Vdc Electrical Characteristics — Updated DC injection current specification. | 317<br>319 |
| April, 2007 | 6.0 | Figure 2-2. Control, Status, and Data Registers — Changed TBMCLKSEL to TMBCLKSEL to be compatible with development tool nomenclature | 37 |
| | | Chapter 5 Configuration Register (CONFIG) — Changed COPCLK to CGMXCLK and TBMCLKSEL to TMBCLKSEL to be compatible with development tool nomenclature | 91<br>92<br>93 |
| | | 10.6.2 Stop Mode — Changed COPCLK to CGMXCLK | 125 |
| | | Figure 14-3. ESCI Module Block Diagram — Changed BUS_CLK to BUS CLOCK and removed reference to 4xBUSCLK | 192 |
| | | 14.4.2 Transmitter — Changed ESCIBDSRC to SCIBDSRC | 194 |
| | | 14.9.1 ESCI Arbiter Control Register and 14.9.3 Bit Time Measurement — Replaced one quarter with one half in the definition for ACLK = 1 | 217<br>218 |
| | | Figure 17-1. Timebase Block Diagram, 17.5 TBM Interrupt Rate, and Table 17-1. Timebase Divider Selection — Changed TBMCLKSEL to TMBCLKSEL to be compatible with development tool nomenclature | 260<br>261 |
| | | 21.9 Clock Generation Module (CGM) Characteristics — Updated section to include the following:<br>21.9.1 CGM Operating Conditions<br>21.9.2 CGM Component Information<br>21.9.3 CGM Acquisition/Lock Time Information | <br>322<br>322<br>323 |

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**Appendix A**
**MC68HC908GZ48**



**Appendix B**
**MC68HC908GZ32**

# Chapter 1
# General Description

## 1.1 Introduction

The MC68HC908GZ60, MC68HC908GZ48, and MC68HC908GZ32 are members of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

The information contained in this document pertains to all three devices with the exceptions noted in Appendix A MC68HC908GZ48 and Appendix B MC68HC908GZ32.

## 1.2 Features

For convenience, features have been organized to reflect:

- Standard features
- Features of the CPU08

### 1.2.1 Standard Features

Features of the MC68HC908GZ60 include:

- High-performance M68HC08 architecture optimized for C-compilers
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- 8-MHz internal bus frequency
- Clock generation module supporting 1-MHz to 8-MHz crystals
- MSCAN08 (scalable controller area network) controller (implementing 2.0b protocol as defined in BOSCH specification dated September 1991)
- FLASH program memory security[1]
- On-chip programming firmware for use with host personal computer which does not require high voltage for entry
- In-system programming (ISP)
- System protection features:
  - Optional computer operating properly (COP) reset
  - Low-voltage detection with optional reset and selectable trip points for 3.3-V and 5.0-V operation
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- Low-power design; fully static with stop and wait modes

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

- Standard low-power modes of operation:
  - Wait mode
  - Stop mode
- Master reset pin and power-on reset (POR)
- On-chip FLASH memory:
  - MC68HC908GZ60 — 60 Kbytes
  - MC68HC908GZ48 — 48 Kbytes
  - MC68HC908GZ32 — 32 Kbytes
- Random-access memory (RAM):
  - MC68HC908GZ60 — 2048 bytes
  - MC68HC908GZ48 — 1536 bytes
  - MC68HC908GZ32 — 1536 bytes
- Serial peripheral interface (SPI) module
- Enhanced serial communications interface (ESCI) module
- One 16-bit, 2-channel timer interface module (TIM1) with selectable input capture, output compare, and pulse-width modulation (PWM) capability on each channel
- One 16-bit, 6-channel timer interface module (TIM2) with selectable input capture, output compare, and pulse-width modulation (PWM) capability on each channel
- Timebase module with clock prescaler circuitry for eight user selectable periodic real-time interrupts with optional active clock source during stop mode for periodic wakeup from stop using an external crystal
- 24-channel, 10-bit successive approximation analog-to-digital converter (ADC)
- 8-bit keyboard wakeup port with software selectable rising or falling edge detect, as well as high or low level detection
- Up to 53 general-purpose input/output (I/O) pins, including:
  - 40 shared-function I/O pins, depending on package choice
  - Up to 13 dedicated I/O pins, depending on package choice
- Selectable pullups on inputs only on ports A, C, and D. Selection is on an individual port bit basis. During output mode, pullups are disengaged.
- Internal pullups on $\overline{\text{IRQ}}$ and $\overline{\text{RST}}$ to reduce customer system cost
- High current 10-mA sink/source capability on all port pins
- Higher current 20-mA sink/source capability on PTC0–PTC4 and PTF0–PTF3
- User selectable clockout feature with divide by 1, 2, and 4 of the bus or crystal frequency
- User selection of having the oscillator enabled or disabled during stop mode
- BREAK module (BRK) to allow single breakpoint setting during in-circuit debugging
- Available packages:
  - 32-pin low-profile quad flat pack (LQFP)
  - 48-pin low-profile quad flat pack (LQFP)
  - 64-pin quad flat pack (QFP)
- Specific features in 32-pin LQFP are:
  - Port A is only 4 bits: PTA0–PTA3; shared with ADC and KBI modules
  - Port B is only 6 bits: PTB0–PTB5; shared with ADC module
  - Port C is only 2 bits: PTC0–PTC1; shared with MSCAN module
  - Port D is only 7 bits: PTD0–PTD6; shared with SPI, TIM1 and TIM2 modules
  - Port E is only 2 bits: PTE0–PTE1; shared with ESCI module

- Specific features in 48-pin LQFP are:
  - Port A is 8 bits: PTA0–PTA7; shared with ADC and KBI modules
  - Port B is 8 bits: PTB0–PTB7; shared with ADC module
  - Port C is only 7 bits: PTC0–PTC6; shared with MSCAN module
  - Port D is 8 bits: PTD0–PTD7; shared with SPI, TIM1, and TIM2 modules
  - Port E is only 6 bits: PTE0–PTE5; shared with ESCI module
- Specific features in 64-pin QFP are:
  - Port A is 8 bits: PTA0–PTA7; shared with ADC and KBI modules
  - Port B is 8 bits: PTB0–PTB7; shared with ADC module
  - Port C is only 7 bits: PTC0–PTC6; shared with MSCAN module
  - Port D is 8 bits: PTD0–PTD7; shared with SPI, TIM1, andTIM2 modules
  - Port E is only 6 bits: PTE0–PTE5; shared with ESCI module
  - Port F is 8 bits: PTF0–PTF7; shared with TIM2 module
  - Port G is 8 bits; PTG0–PTG7; shared with ADC module

### 1.2.2 Features of the CPU08

Features of the CPU08 include:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8 × 8 multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Efficient C language support

## 1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908GZ60. Refer to Appendix A MC68HC908GZ48 and Appendix B MC68HC908GZ32.

## 1.4 Pin Assignments

Figure 1-2, Figure 1-3, and Figure 1-4 illustrate the pin assignments for the 32-pin LQFP, 48-pin LQFP, and 64-pin QFP respectively.