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Freescale Semiconductor
Data Sheet Addendum

Document Number: MC68HC908KX8
Rev. 3
10/2014

Addendum for MC68HC908KX8 Data Sheet, Rev. 2.1

1 New information added to the MC68HC908KX8 data sheet

Please replace the last row of the table in Section 17.5 with the two last rows of the table below.

17.5 5.0-Vdc DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Pullup resistor PTA0–PTA4	R_{PU}	24	—	48	kΩ
Pullup resistor $\overline{IRQ1}$	R_{PU}	19	—	43	kΩ

1. V_{DD} = 5.5 Vdc to 4.5 Vdc, V_{SS} = 0 Vdc, T_A = –40°C to +125°C, unless otherwise noted
2. Typical values reflect average measurements at midpoint of voltage range, 25°C only.

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Addendum to rev. 2.1
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MC68HC908KX8
MC68HC908KX2
MC68HC08KX8

Data Sheet

M68HC08
Microcontrollers

MC68HC908KX8
Rev. 2.1
07/2005

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Data Sheet

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
April, 2001	0.1	Label for pin 9 corrected in Figure 1-1 and Figure 1-2	19, 20
		$FF is the erase state of the FLASH, not $00.	82, 252, 255
		First bulleted paragraph under the subsection 15.5 Interrupts reworded for clarity	177
		Revision to the description of the CHxMAX bit and the note that follows that description	183
		Forced monitor mode information added to Table 16-1.	192
		In Figure 16-10. Monitor Data Format, resistor value for connection between VTST and IRQ1 changed from 10 kΩ to 1 kΩ.	194
February, 2002	1.0	7.2 Features — Corrected third bullet	71
		7.7.3 ICG Trim Register — Corrected description of the TRIM7:TRIM0 bits	97
		14.2 Features — Corrected divide by factors in first bullet	165
		Figure 14-1. Timebase Block Diagram — Corrected divide-by-2 blocks	166
		Table 14-1. Timebase Divider Selection — Corrected last divider tap entry	167
		Section 15. Timer Interface Module (TIM) — Timer discrepancies corrected throughout this section	169
		17.4 Thermal Characteristics — Corrected SOIC thermal resistance and maximum junction temperature	202
		17.5 5.0-Vdc DC Electrical Characteristics and — Corrected footnote for VDD supply current in stop mode	203 and 204
		Appendix B. MC68HC08KX8 — Added to supply exception information for the MC68HC08KX8	215
March, 2004	2.0	Reformatted to current publication standards	Throughout
		2.7 FLASH Page Erase Operation — Updated procedure	33
		2.8 FLASH Mass Erase Operation — Updated procedure	33
		2.9 FLASH Program/Read Operation — Updated procedure	34
		Figure 5-1. COP Block Diagram — Updated figure	53
		Table 6-1. Instruction Set Summary — Added WAIT instruction	69
		Section 7. Internal Clock Generator Module (ICG) — Updated with new information	71 through 98
		14.2 Features — Corrected values given in the first bullet	165
		Table 15-3. Mode, Edge, and Level Selection — Reworked for clarity	182
		17.11 Memory Characteristics — Updated table with new information	210
July, 2005	2.1	Updated to meet Freescale identity guidelines.	Throughout

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MC68HC908KX2

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Chapter 1
General Description

1.1 Introduction

The MC68HC908KX8 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCU). The M68HC08 Family is based on the customer-specified integrated circuit (CSIC) design strategy. All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

The information contained is this document pertains to the MC68HC908KX2 and the MC68HC08KX8 with the exceptions found in:

- Appendix A MC68HC908KX2
- Appendix B MC68HC08KX8

1.2 Features

Features include:

- High-performance M68HC08 architecture
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- Maximum internal bus frequencies of:
  - 8 MHz at 5.0 V
  - 4 MHz at 3.0 V
- Internal oscillator requiring no external components:
  - Software selectable bus frequencies
  - 25 percent accuracy with trim capability to 2 percent
  - Clock monitor
  - Option to allow use of external clock source or external crystal/ceramic resonator
- Eight Kbytes of on-chip, in-circuit programmable FLASH memory
- FLASH program memory security[1]
- On-chip programming firmware for use with host personal computer which does not require high voltage for entry
- 192 bytes of on-chip random-access memory (RAM)
- 16-bit, 2-channel timer interface (TIM) module
- 4-channel, 8-bit, analog-to-digital converter (ADC) with high-voltage reference (V_{REFH}) double bonded to V_{DD} pin

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

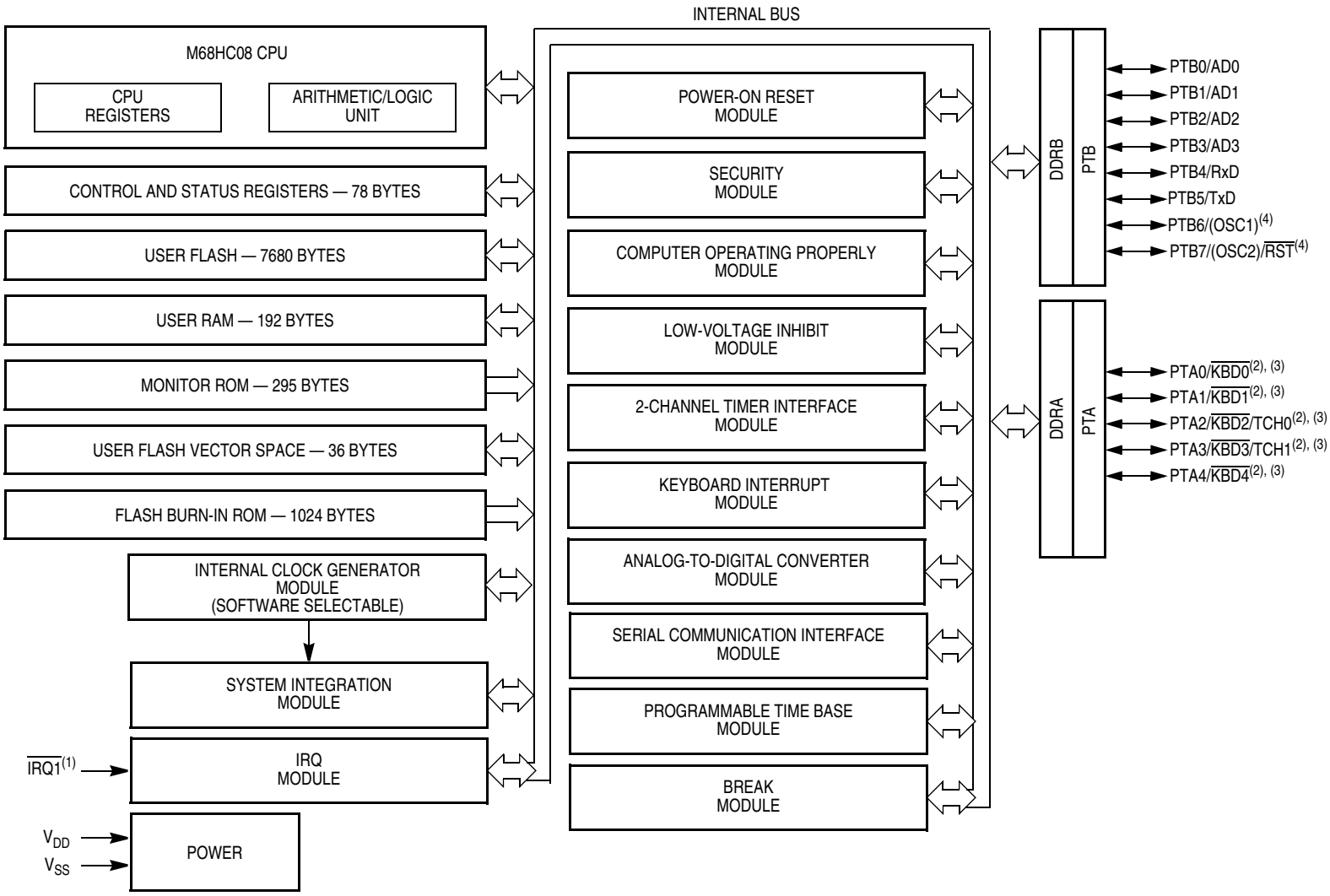
- Serial communications interface (SCI) module
- 5-bit keyboard interrupt (KBI) with wakeup feature
- 13 general-purpose input/output (I/O) ports:
  - Five shared with KBI and TIM, with 15-mA source/15-mA sink capabilities and with programmable pullups on general- purpose input ports
  - Four shared with ADC
  - Two shared with SCI
- Low-voltage inhibit (LVI) module with software selectable trip points, 2.6-V or 4.3-V trip point
- Timebase module (TBM) with
  - Clock prescaler for eight user-selectable, periodic real-time interrupts
  - Active clock source in stop mode for periodic wakeup from stop using external crystal or internal oscillator
- External asynchronous interrupt pin with internal pullup ($\overline{\text{IRQ1}}$)
- System protection features:
  - Computer operating properly (COP) reset
  - Low-voltage detection with reset
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- 16-pin plastic dual in-line (PDIP) or small outline (SOIC) package
- Low-power design fully static with stop and wait modes
- Internal power-up reset circuit requiring no external pins
- –40°C to +125°C operation

Features of the CPU08 include:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes, eight more than the M68HC05
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8 × 8 multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Third party C language support

1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908KX8.



Notes:
1. Pin contains integrated pullup resistor
2. High-current source/sink pin
3. Pin contains software selectable pullup resistor if general function I/O pin is configured as input.

Figure 1-1. MC68HC908KX8 MCU Block Diagram

1.4 Pin Assignments

Figure 1-2 shows the pin assignments for MC68HC908KX8.

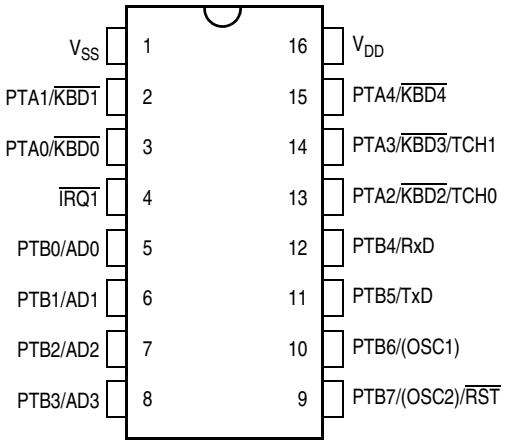
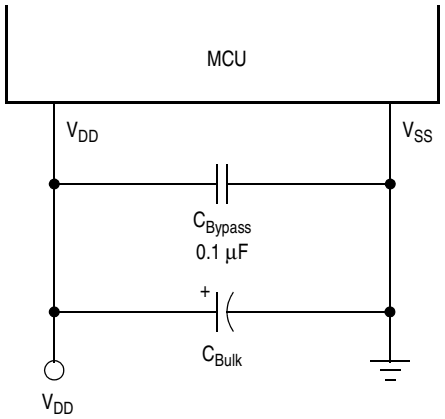


Figure 1-2. PDIP and SOIC Pin Assignments

1.4.1 Supply Pins (V_{DD} and V_{SS})

V_{DD} and V_{SS} are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU as shown in Figure 1-3. Place the bypass capacitors as close to the MCU power pins as possible. Use high-frequency response ceramic capacitors for C_{Bypass}. C_{Bulk} are optional bulk current bypass capacitors for use in applications that require the port pins to source high-current levels.



Note: Component values shown represent typical applications.

Figure 1-3. Power Supply Bypassing

1.4.2 Oscillator Pins (OSC1 and OSC2)

The OSC1 and OSC2 pins are available through programming options in the configuration register. These pins then become the connections to an external clock source or crystal/ceramic resonator. PTB7 and PTB6 are not available for the crystal/ceramic resonator option and PTB6 is unavailable for the external clock source option.

1.4.3 External Interrupt Pin ($\overline{\text{IRQ1}}$)

$\overline{\text{IRQ1}}$ is an asynchronous external interrupt pin with an internal pullup resistor. See Chapter 8 External Interrupt (IRQ).

1.4.4 Port A Input/Output (I/O) Pins (PTA4/$\overline{\text{KBD4}}$–PTA0/$\overline{\text{KBD0}}$)

PTA4/$\overline{\text{KBD4}}$–PTA0/$\overline{\text{KBD0}}$ is a 5-bit special-function port that shares its pins with the keyboard interrupt (KBI) module and the 2-channel timer module (TIM).

- Any or all of the port A pins can be programmed to serve as keyboard interrupt pins. The respective pin utilizes an internal pullup resistor when enabled. See Chapter 9 Keyboard Interrupt Module (KBI).
- Each port A pin contains a software selectable internal pullup resistor when the general-function I/O port is configured as an input. See Chapter 11 Input/Output (I/O) Ports (PORTS). The pullup resistor is automatically disabled once a TIM special function is enabled for that pin.
- All port A pins are high-current source/sink pins.

NOTE

Any unused inputs and I/O ports should be tied to an appropriate logic level (either V_{DD} or V_{SS}). Although the I/O ports of the MC68HC908KX8 do not require termination, termination is recommended to reduce the possibility of static damage.

1.4.5 Analog Reference Pin (V_{REFH})

The V_{REFH} pin is the analog reference voltage for the analog-to-digital converter (ADC) module. The voltage is supplied through a double-bond to the V_{DD} pin. See Chapter 17 Electrical Specifications for ADC parameters.

1.4.6 Port B Input/Output (I/O) Pins (PTB7/(OSC2)/$\overline{\text{RST}}$–PTB0/AD0)

PTB7/(OSC2)/$\overline{\text{RST}}$–PTB0/AD0 are general-purpose bidirectional I/O port pins, all sharing special functions.

- PTB7 and PTB6 share with the on-chip oscillator circuit through configuration options. See 7.3.3 External Clock Generator.
- PTB5 and PTB4 share with the SCI module. See Chapter 12 Serial Communications Interface Module (SCI).
- PTB3–PTB0 share with the ADC module. See Chapter 3 Analog-to-Digital Converter (ADC).

Chapter 2
Memory

2.1 Introduction

The central processor unit (CPU08) can address 64 Kbytes of memory space.

The memory map, shown in Figure 2-1, includes:

- 7680 bytes of FLASH memory
- 192 bytes of random-access memory (RAM)
- 36 bytes of user-defined vectors
- 295 bytes of monitor read-only memory (ROM)

2.2 I/O Registers

Most of the control, status, and data registers are in the zero-page area of $0000–$003F. Additional input/output (I/O) registers have the following addresses:

- $FE01 — SIM reset status register, SRSR
- $FE04 — Interrupt status register 1, INT1
- $FE05 — Interrupt status register 2, INT2
- $FE06 — Interrupt status register 3, INT3
- $FE08 — FLASH control register, FLCR
- $FE09 — Break address register high, BRKH
- $FE0A — Break address register low, BRKL
- $FE0B — Break status and control register, BRKSCR
- $FE0C — LVI status register, LVISR
- $FF7E — FLASH block protect register, FLBPR
  in non-volatile FLASH memory
- $FFFF — COP control register, COPCTL

A summary of the available registers is provided in Figure 2-2. Table 2-1 is a list of vector locations.

2.3 Monitor ROM

The 295 bytes at addresses $FE20–$FF46 are reserved ROM addresses that contain the instructions for the monitor functions.