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MC68HC908LB8

Data Sheet

M68HC08
Microcontrollers

MC68HC908LB8
Rev. 1
8/2005

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MC68HC908LB8

Data Sheet

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
1/2005	0	First release	N/A
8/2005	1	Section 4.7 Application Information added. Minor changes to the second and third paragraphs in the note in Section 10.4.9 Deadtime Insertion.	56 101

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Chapter 1
General Description

1.1 Introduction

The MC68HC908LB8 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes, memory types, and package types. The MC68HC908LB8 has peripherals dedicated to high resolution PWM and power factor correction (PFC).

1.2 Features

For convenience, features have been organized to reflect:

- Standard features of the MC68HC908LB8
- Features of the CPU08

1.2.1 Standard Features of the MC68HC908LB8

Features of the MC68HC908LB8 include:

- 8-MHz internal bus frequency
- Trimmable internal oscillator:
  - 4.0 MHz internal bus operation
  - 8-bit trim capability
  - 25% untrimmed
  - 5% trimmed
- 8 Kbytes of 10 K write/erase cycle typical on-chip in application programmable FLASH memory with security option[1]
- 128 bytes of on-chip random-access memory (RAM)
- Dual channel high resolution PWM with dead time insertion and shutdown input. The outputs use frequency dithering to achieve a 4 ns output resolution.
- Dual channel pulse-width modulator (PWM) module to provide power factor correction capability
- Seven channel, 8-bit successive approximation analog-to-digital converter (ADC)
- Op amp/comparator for power factor correction capability or general purpose use
- 7-bit keyboard interrupt
- One 16-bit, 2-channel timer interface module with one output available on port pin (PTA6) for input capture and PWM
- 17 general-purpose input/output (I/O) pins and one input only pin
  - Three shared with high resolution PWM (HRP)
  - Three shared with PWM module

1. No security feature is absolutely secure. However, Freescale Semiconductor's strategy is to make reading or copying the FLASH difficult for unauthorized users.

  - Three shared with op amp/comparator
  - Seven shared with ADC module (AD[0:6])
  - One shared with timer channel 0
  - Two shared with OSC1 and OSC2
  - One shared with reset
  - Seven shared with keyboard interrupt
  - One input-only pin shared with external interrupt (IRQ)
- Available packages:
  - 20-pin small outline integrated chip (SOIC) package
  - 20-pin plastic dual in-line package (PDIP)
- On-chip programming firmware for use with host personal computer which does not require high voltage for entry
- System protection features:
  - Optional computer operating properly (COP) reset
  - Low-voltage reset
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- Low-power design; fully static with stop and wait modes
- Standard low-power modes of operation:
  - Wait mode
  - Stop mode
- Master reset pin and power-on reset (POR)
- 674 bytes of FLASH programming routines read-only memory (ROM)
- Break module (BRK) to allow single breakpoint setting during in-circuit debugging
- Internal pullup on $\overline{\text{RST}}$ pin to reduce customer system cost

- Selectable pullups on ports A and C
  - Selection on an individual port bit basis
  - During output mode, pullups are disengaged
- High current 8-mA sink / 10-mA source capability on all port pins

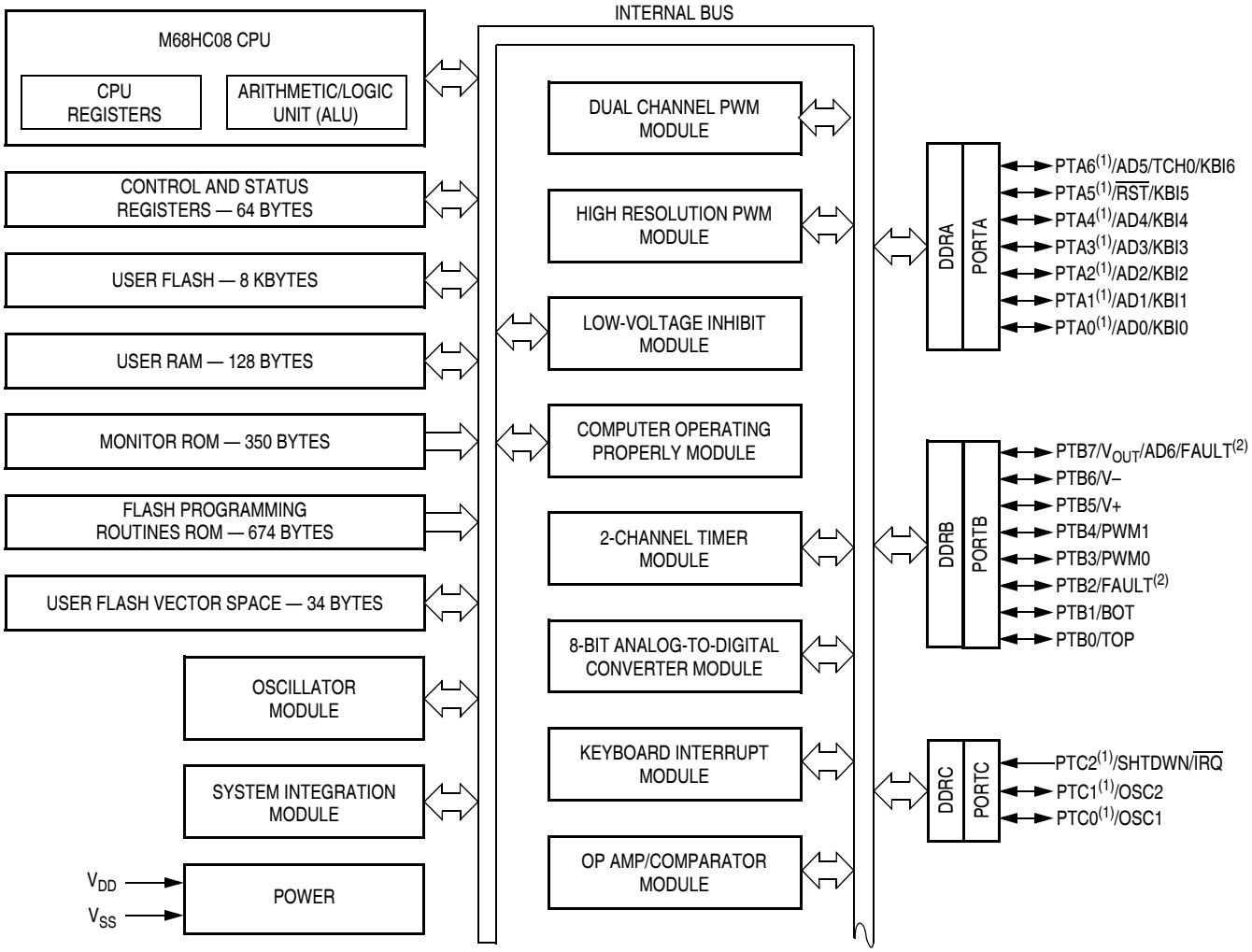
1.2.2 Features of the CPU08

Features of the CPU08 include:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8 × 8 multiply instruction
- Fast 16/8 divide instruction
- Binary coded decimal (BCD) instructions
- Optimization for controller applications
- Efficient C language support

1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908LB8.



Notes:
1. Pin contains integrated pullup device.
2. Fault function switchable between pins PTB2 and PTB7.

Figure 1-1. MCU Block Diagram

1.4 Pin Assignments

Figure 1-2 illustrates the pin assignments for the 20-pin SOIC package.

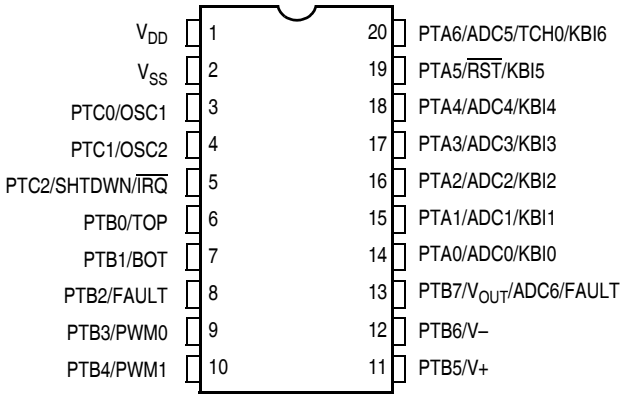


Figure 1-2. 20-Pin SOIC and PDIP Pin Assignments

1.5 Pin Functions

Table 1-1 provides a description of the pin functions.

Table 1-1. Pin Functions

Pin Name	Description	Input/Output
V_{DD}	Power supply	Power
V_{SS}	Power supply ground	Power
PTA0	PTA0 — General purpose I/O port	Input/Output
	KBI0 — Keyboard interrupt input 0	Input
	ADC0 — A/D channel 0 input	Input
PTA1	PTA1 — General purpose I/O port	Input/Output
	KBI1 — Keyboard interrupt input 1	Input
	ADC1 — A/D channel 1 input	Input
PTA2	PTA2 — General purpose I/O port	Input/Output
	KBI2 — Keyboard interrupt input 2	Input
	ADC2 — A/D channel 2 input	Input
PTA3	PTA3 — General purpose I/O port	Input/Output
	KBI3 — Keyboard interrupt input 3	Input
	ADC3 — A/D channel 3 input	Input
PTA4	PTA4 — General purpose I/O port	Input/Output
	KBI4 — Keyboard interrupt input 4	Input
	ADC4 — A/D channel 4 input	Input
PTA5	PTA5 — General purpose I/O port	Input/Output
	$\overline{RST}$ — Reset input, active low with internal pullup and Schmitt trigger	Input
	KBI5 — Keyboard interrupt input 5	Input

Table 1-1. Pin Functions (Continued)

Pin Name	Description	Input/Output
PTA6	PTA6 — General purpose I/O port	Input/Output
	KBI6 — Keyboard interrupt input 6	Input
	TCH0 — Timer Channel 0 I/O	Input/Output
	ADC5 — A/D channel 5 input	Input
PTB0	PTB0 — General purpose I/O port	Input/Output
	TOP — High resolution PWM output	Output
PTB1	PTB1 — General purpose I/O port	Input/Output
	BOT — High resolution PWM output	Output
PTB2	PTB2 — General purpose I/O port	Input/Output
	FAULT — High resolution PWM fault input (switchable between PTB2 and PTB7)	Input
PTB3	PTB3 — General purpose I/O port	Input/Output
	PWM0 — Pulse-width modulator output 0	Output
PTB4	PTB4 — General purpose I/O port	Input/Output
	PWM1 — Pulse-width modulator output 1	Output
PTB5	PTB5 — General purpose I/O port	Input/Output
	V+ — Op amp/comparator input	Input
PTB6	PTB6 — General purpose I/O port	Input/Output
	V– — Op amp/comparator input	Input
PTB7	PTB7 — General purpose I/O port	Input/Output
	V_{OUT} — Op amp/comparator output	Output
	ADC6 — A/D channel 6 input	Input
	FAULT — High resolution PWM fault input (switchable between PTB2 and PTB7)	Input
PTC0	PTC0 — General purpose I/O port	Input/Output
	OSC1 — XTAL, RC, or external oscillator input	Input
PTC1	PTC1 — General purpose I/O port	Input/Output
	OSC2 — XTAL oscillator output (XTAL option only) RC or internal oscillator output (OSC2EN = 1 in PTAPUE register)	Output Output
PTC2	PTC2 — General purpose input port	Input
	SHTDWN — High resolution PWM input	Input
	$\overline{IRQ}$ — External interrupt with programmable pullup and Schmitt trigger	Input

1.6 Pin Function Priority

Table 1-2 is meant to resolve the priority if multiple functions are enabled on a single pin.

NOTE

Upon reset all pins come up as input ports regardless of the priority table.

Table 1-2. Function Priority in Shared Pins

Pin Name	Highest-to-Lowest Priority Sequence
PTA0	ADC0 → KBI0 → PTA0
PTA1	ADC1 → KBI1 → PTA1
PTA2	ADC2 → KBI2 → PTA2
PTA3	ADC3 → KBI3 → PTA3
PTA4	ADC4 → KBI4 → PTA4
PTA5	$\overline{\text{RST}}$ → KBI5 → PTA5
PTA6	ADC5 → TCH0 → KBI6 → PTA6
PTB0	TOP → PTB0
PTB1	BOT → PTB1
PTB2	FAULT(1) → PTB2
PTB3	PWM0 → PTB3
PTB4	PWM1 → PTB4
PTB5	V+ → PTB5
PTB6	V– → PTB6
PTB7	V_{OUT} / ADC6 / FAULT(1)(2) → PTB7
PTC0	OSC1 → PTC0
PTC1	OSC2 → PTC1
PTC2	SHTDWN → $\overline{\text{IRQ}}$ → PTC2

NOTES:
1. Fault function is switchable between pins PTB2 and PTB7.
2. V_{OUT}, ADC6, and FAULT functions all share equal priority. All of these functions can be used simultaneously on this pin.

NOTE

Any unused inputs and I/O ports should be tied to an appropriate logic level (either V_{DD} or V_{SS}). Although the I/O ports of the MC68HC908LB8 do not require termination, termination is recommended to reduce the possibility of static damage.

1.7 System Clock Distribution

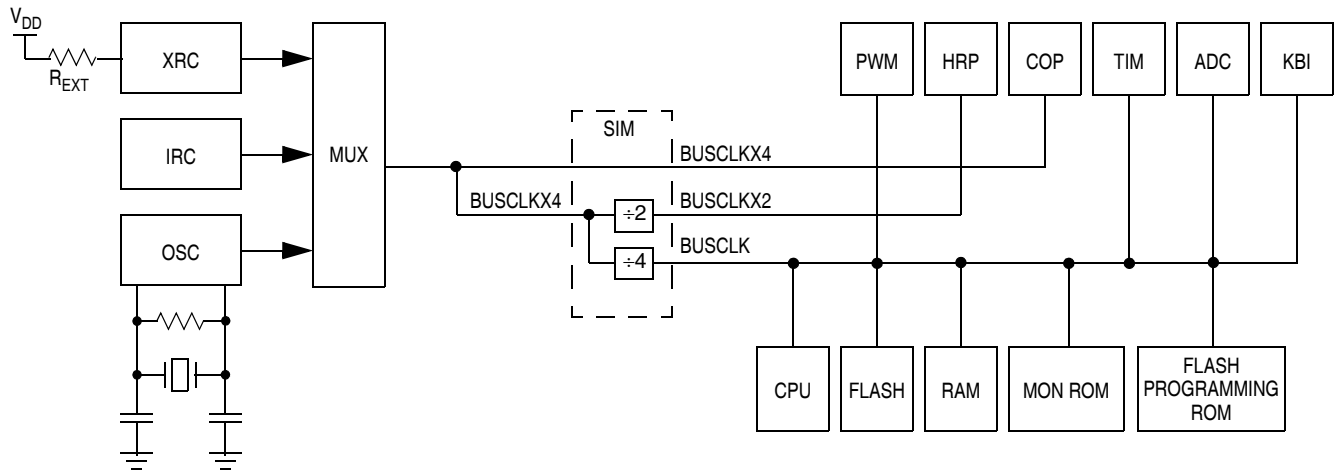


Figure 1-3. System Clock Distribution Diagram

Some of the modules inside the MCU use different clock sources. Figure 1-3 shows a simplified clock connection diagram. The OSC supplies the clock sources:

- BUSCLKX4 is the basic reference clock of the device. It is either:
  - The external crystal oscillator
  - An external clock source
  - An external RC oscillator
  - The internal oscillator

Chapter 2
Memory

2.1 Introduction

The CPU08 can address 64 Kbytes of memory space. The memory map, shown in Figure 2-1, includes:

- System registers
- 8192 bytes of user FLASH memory
- 128 bytes of random-access memory (RAM)
- 674 bytes of FLASH programming routines read-only memory (ROM)
- 34 bytes of user-defined vectors

2.2 Unimplemented Memory Locations

Accessing an unimplemented location can cause an illegal address reset. In the memory map (Figure 2-1) and in register figures in this document, unimplemented locations are shaded.

2.3 Reserved Memory Locations

Accessing a reserved location can have unpredictable effects on microcontroller (MCU) operation. In the Figure 2-1 and in register figures in this document, reserved locations are marked with the word Reserved or with the letter R.

2.4 Register Section

Most of the control, status, and data registers are in the zero page area of $0000–$0058. Additional I/O registers have these addresses:

- $FE00; break status register, BSR
- $FE01; SIM reset status register, SRSR
- $FE02; break auxiliary register, BRKAR
- $FE03; break flag control register, BFCR
- $FE04; interrupt status register 1, INT1
- $FE05; interrupt status register 2, INT2
- $FE06; reserved
- $FE07; reserved
- $FE08; FLASH control register, FLCR
- $FE09; break address register high, BRKH
- $FE0A; break address register low, BRKL
- $FE0B; break status and control register, BRKSCR
- $FE0C; LVI status register, LVISR
- $FF7E; FLASH block protect register, FLBPR