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M68060 User's Manual

**Including the
MC68060,
MC68LC060,
and
MC68EC060**

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PREFACE

The complete documentation package for the MC68060, MC68LC060, and MC68EC060 (collectively called M68060) consists of the M68060UM/AD, *M68060 User's Manual*, and the M68000PM/AD, *M68000 Family Programmer's Reference Manual*. The *M68060 User's Manual* describes the capabilities, operation, and programming of the M68060 superscalar 32-bit microprocessors. The *M68000 Family Programmer's Reference Manual* contains the complete instruction set for the M68000 family.

The introduction of this manual includes general information concerning the MC68060 and summarizes the differences among the M68060 family devices. Additionally, appendices provide detailed information on how these M68060 derivatives operate differently from the MC68060.

When reading this manual, disregard information concerning the floating-point unit in reference to the MC68LC060, and disregard information concerning the floating-point unit and memory management unit in reference to the MC68EC060.

The organization of this manual is as follows:

Section 1	Introduction
Section 2	Signal Description
Section 3	Integer Unit
Section 4	Memory Management Unit
Section 5	Caches
Section 6	Floating-Point Unit
Section 7	Bus Operation
Section 8	Exception Processing
Section 9	IEEE 1149.1 Test (JTAG) and Debug Pipe Control Modes
Section 10	Instruction Timings
Section 11	Applications
Section 12	Electrical and Thermal Characteristics
Section 13	Ordering Information and Mechanical Data
Appendix A	MC68LC060
Appendix B	MC68EC060
Appendix C	MC68060 Software Package
Appendix D	M68060 Instructions

MC68060 ACRONYM LIST

AGU—address generation unit
ALU—arithmetic logic unit
ATC—address translation cache
BUSCR—bus control register
CACR—cache control register
CCR—condition code register
CM—cache mode
CPU—central processing unit
DFC—destination function code
DTTx—data transparent translation register
DRAM—dynamic random access memory
FPIAR—floating-point instruction address register
FPCR—floating-point control register
FPSP—floating-point software package
FPSR—floating-point status register
FPU—floating-point unit
FP7–FP0—floating-point data registers 7–0
FSLW—fault status long word
IEE—integer execute unit
IFP—instruction fetch pipeline
IFU—instruction fetch unit
IPU—instruction pipe unit
ISP—interrupt stack pointer
ITTR—instruction transparent translation register
IU—integer unit
JTAG—Joint Test Action Group
MMU—memory management unit



MC68060 Acronym List

MMUSR—memory management unit status register

M68060SP—M68060 software package

NANs—not-a-numbers

NOP—no operation

OEP—operand execution pipeline

OPU—operand pipe unit

PC—program counter

PCR—processor configuration register

PGI—page index field

PI—pointer index field

PLL—phase-locked loop

pOEP—primary operand execution pipeline

RI—root index field

SFC—source function code

SNAN—signaling not-a-number

sOEP—secondary operand execution pipeline

SP—stack pointer

SR—status register

SRP—supervisor root pointer register

SSP—supervisor stack pointer

TAP—test access port

TCR—translation control register

TTL—transistor-transistor logic

TTR—transparent translation register

UPA—user page attribute

URP—user root pointer register

USP—user stack pointer

VBR—vector base register

VLSI—very large-scale integration

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SECTION 1 INTRODUCTION

The superscalar MC68060 represents a new line of Motorola microprocessor products. The first generation of the M68060 product line consists of the MC68060, MC68LC060, and MC68EC060. All three microprocessors offer superscalar integer performance of over 100 MIPS at 66 MHz. The MC68060 comes fully equipped with both a floating-point unit (FPU) and a memory management unit (MMU) for high-performance embedded control and desktop applications. For cost-sensitive embedded control and desktop applications where an MMU is required, but the additional cost of a FPU is not justified, the MC68LC060 offers high-performance at a low cost. Specifically designed for low-cost embedded control applications, the MC68EC060 eliminates both the FPU and MMU, permitting designers to leverage MC68060 performance while avoiding the cost of unnecessary features. Throughout this product brief, all references to the MC68060 also refer to the MC68LC060 and the MC68EC060, unless otherwise noted.

Leveraging many of the same performance enhancements used by RISC designs as well as providing innovative architectural techniques, the MC68060 harnesses new levels of performance for the M68000 family. Incorporating 2.5 million transistors on a single piece of silicon, the MC68060 employs a deep pipeline, dual issue superscalar execution, a branch cache, a high-performance floating-point unit (MC68060 only), eight Kbytes each of on-chip instruction and data caches, and dual on-chip demand paging MMUs (MC68060 and MC68LC060 only). The MC68060 allows simultaneous execution of two integer instructions (or an integer and a float instruction) and one branch instruction during each clock.

The MC68060 features a full internal Harvard architecture. The instruction and data caches are designed to support concurrent instruction fetch, operand read and operand write references on every clock. Separate 8-Kbyte instruction and 8-Kbyte data caches can be frozen to prevent allocation over time-critical code or data. The independent nature of the caches allows instruction stream fetches, data-stream fetches, and external accesses to occur simultaneously with instruction execution. The operand data cache is four-way banked to permit simultaneous read and write access each clock.

A very high bandwidth internal memory system coupled with the compact nature of the M68000 family code allows the MC68060 to achieve extremely high levels of performance, even when operating from low-cost memory such as a 32-bit wide dynamic random access memory system.

Instructions are fetched from the internal cache or external memory by a four-stage instruction fetch pipeline. The MC68060 variable-length instruction system is internally decoded into a fixed-length representation and channeled into an instruction buffer. The instruction buffer acts as a FIFO which provides a decoupling mechanism between the instruction fetch